



# 3.3V/5V 1.25Gbps PECL LOW-POWER LIMITING POST AMPLIFIER w/TTL SIGNAL DETECT

**SY88933V**  
Final

## FEATURES

- Single 3.3V or 5V power supply
- DC to 1.25Gbps operation
- Low noise PECL data outputs
- Chatter-free OC-TTL signal detect (SD) output with internal 6.75k $\Omega$  pull-up resistor
- TTL EN input
- Programmable SD level set ( $SD_{LVL}$ )
- Available in a tiny 10-pin MSOP (3mm) package

## APPLICATIONS

- 1.25Gbps Ethernet
- 1.55Mbps and 622Mbps SONET/SDH
- High-gain line driver and line receiver
- 531Mbps and 1062Mbps Fibre Channel
- Gigabit interface converter

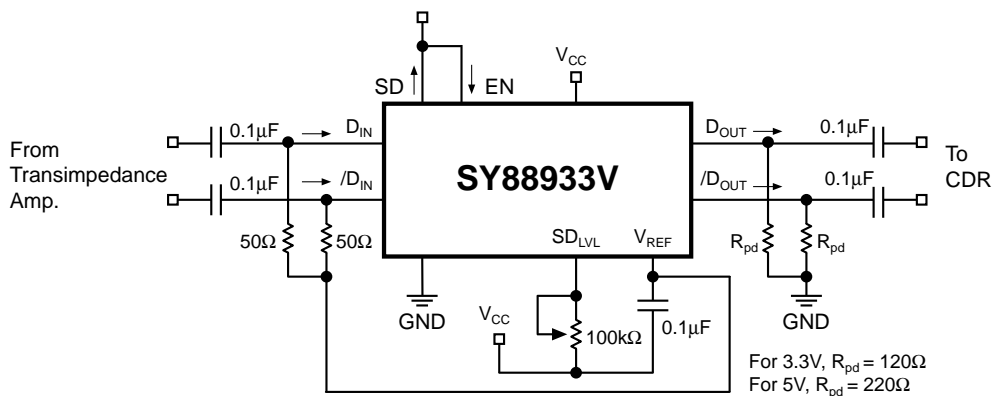
## DESCRIPTION

The SY88933V low-power limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88933V quantizes these signals and outputs PECL level waveforms.

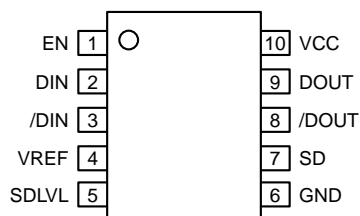
The SY88933V operates from a single +3.3V or +5V power supply, over temperatures ranging from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . With its wide bandwidth and high gain, signals with data rates up to 1.25Gbps and as small as 5mVp-p can be amplified to drive devices with PECL inputs.

The SY88933V generates a TTL SD output. A programmable signal-detect level set pin ( $SD_{LVL}$ ) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by  $SD_{LVL}$  and deasserts low otherwise. EN deasserts the true output signal without removing the input signal. Typically 4.6dB SD hysteresis is provided to prevent chattering.

## TYPICAL APPLICATIONS CIRCUIT



## PACKAGE/ORDERING INFORMATION



**10-Pin MSOP (K10-1)**

## Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY88933VKC	K10-1	Commercial	933V
SY88933VKCTR <sup>(Note 1)</sup>	K10-1	Commercial	933V
SY88933VKI	K10-1	Industrial	933V
SY88933VKITR <sup>(Note 1)</sup>	K10-1	Industrial	933V

**Note 1.** Tape and Reel.

## PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1	EN	TTL Input: Default is high.	Enable: Deasserts true data output when high.
2	DIN	Data Input	True data input.
3	/DIN	Data Input	Complementary data input.
4	VREF		Reference voltage: capacitor here to $V_{CC}$ helps stabilize $SD_{LVL}$ .
5	SDLVL	Input	Signal-Detect Level Set: a resistor from this pin to $V_{CC}$ sets the threshold for the data input amplitude at which SD will be asserted.
6	GND	Ground	Device ground.
7	SD	Open-collector TTL output w/ internal 6.75k $\Omega$ pull-up resistor	Signal-Detect: asserts high when the data input amplitude rises above the threshold set by $SD_{LVL}$ .
8	/DOUT	PECL Output	Complementary data output.
9	DOUT	PECL Output	True data output.
10	VCC	Power Supply	Positive power supply.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	0V to +7.0V
Input Voltage ( $D_{IN}$ , $\overline{D}_{IN}$ )	0 to $V_{CC}$
Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
EN Voltage	0 to $V_{CC}$
$V_{REF}$ Current	-800 $\mu$ A to +500 $\mu$ A
$SD_{LVL}$ Voltage	$V_{REF}$ to $V_{CC}$
Storage Temperature ( $T_S$ )	-55°C to +125°C

**Operating Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ )	+3.0V to +3.6V or +4.5V to +5.5V
Ambient Temperature ( $T_A$ ), <b>Note 3</b>	-40°C to +85°C
Junction Temperature ( $T_J$ ), <b>Note 3</b>	-40°C to +120°C
Package Thermal Resistance	
MSOP	
( $\theta_{JA}$ ) Still-Air	113°C/W

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Commercial devices are guaranteed from 0°C to +85°C ambient temperature.

**DC ELECTRICAL CHARACTERISTICS**

$V_{CC} = 3.0V$  to  $3.6V$  or  $4.5V$  to  $5.5V$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC}$	Power Supply Current	No output load		22	42	mA
$SD_{LVL}$	$SD_{LVL}$ Voltage		$V_{REF}$		$V_{CC}$	V
$V_{IH}$	EN Input HIGH Voltage		2.0			V
$V_{IL}$	EN Input LOW Voltage				0.8	V
$I_{IH}$	EN Input HIGH Current	$V_{IN} = 2.7V$ $V_{IN} = V_{CC}$			20 100	$\mu A$ $\mu A$
$I_{IL}$	EN Input LOW Current	$V_{IN} = 0.5V$	-0.3			mA
$V_{OH}$	SD Output HIGH Level	$V_{CC} \geq 3.3V$ $V_{CC} < 3.3V$	2.4 2.0			V V
$V_{OL}$	SD Output LOW Level	$I_{OL} = +2mA$			0.5	V
$V_{OH}$	PECL Output HIGH Voltage	$50\Omega$ to $V_{CC}-2V$ output load	$V_{CC}-1.085$	$V_{CC}-0.955$	$V_{CC}-0.880$	V
$V_{OL}$	PECL Output LOW Voltage	$50\Omega$ to $V_{CC}-2V$ output load	$V_{CC}-1.830$	$V_{CC}-1.705$	$V_{CC}-1.555$	V
$V_{OFFSET}$	Differential Output Offset				$\pm 100$	mV
$V_{IHCMR}$	Common Mode Range	<b>Note 1</b>	GND +2.0		$V_{CC}$	V
$V_{REF}$	Reference Voltage	<b>Note 2</b>	$V_{CC}-1.38$	$V_{CC}-1.32$	$V_{CC}-1.26$	V

**Note 1.** The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

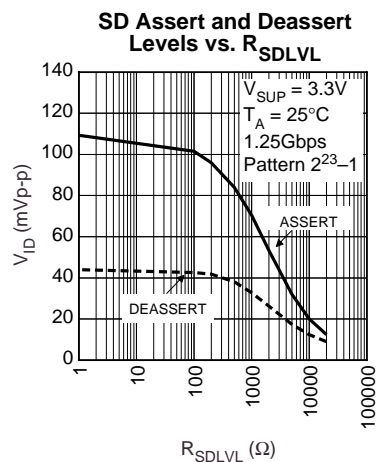
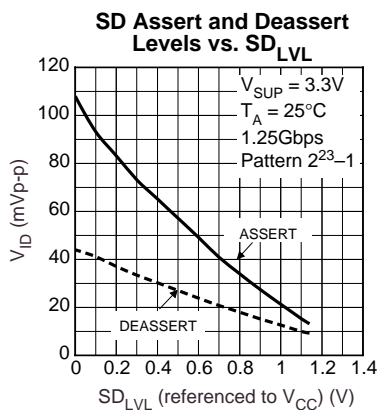
**Note 2.** The current provided into or from  $V_{REF}$  must be limited to 800 $\mu A$  source and 500 $\mu A$  sink.

## AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.0V$  to  $3.6V$  or  $4.5V$  to  $5.5V$ ;  $R_{LOAD} = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; typical values at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Min	Typ	Max	Units
HYS	SD Hysteresis	electrical signal	2	4.6	8	dB
$t_{OFF}$	SD Release Time			0.1	0.5	$\mu s$
$t_{ON}$	SD Assert Time			0.2	0.5	$\mu s$
$V_{ID}$	Differential Input Voltage Swing		5		1800	mVp-p
$V_{OD}$	Differential Output Voltage Swing	$V_{ID} \geq 18mVp-p$ $V_{ID} = 5mVp-p$		1500 400		mVp-p mVp-p
$V_{SR}$	SD Sensitivity Range		5		50	mVp-p
$A_{V(Diff)}$	Differential Voltage Gain			38		dB
$B_{-3dB}$	3dB Bandwidth		1			GHz
$S_{21}$	Single-Ended Small-Signal Gain		26	32		dB
$t_r, t_f$	Differential Output Rise/Fall Time (20% to 80%)	$V_{ID} > 100mVp-p$ and $50\Omega$ to $V_{CC} - 2V$ load			260	ps

## TYPICAL OPERATING CHARACTERISTICS



## DETAILED DESCRIPTION

The SY88933V low-power limiting post amplifier operates from a single +3.3V or +5V power supply, over temperatures from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Signals with data rates up to 1.25Gbps and as small as 5mVp-p can be amplified. Figure 1 shows the allowed input voltage swing. The SY88933V generates an SD output.  $\text{SD}_{\text{LVL}}$  sets the sensitivity of the input amplitude detection.

### Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88933V's input stage. The high-sensitivity of the input amplifier allows signals as small as 5mVp-p to be detected and amplified. The input amplifier allows input signals as large as 1800mVp-p. Input signals are linearly amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88933V outputs typically 1500mVp-p voltage-limited waveforms for input signals that are greater than 18mVp-p. Applications requiring the SY88933V to operate with high-gain should have the upstream TIA placed as close as possible to the SY88933V's input pins to ensure the best performance of the device.

### Output Buffer

The SY88933V's PECL output buffer is designed to drive 50 $\Omega$  lines. The output buffer requires appropriate termination for proper operation. An external 50 $\Omega$  resistor to  $V_{\text{CC}}-2\text{V}$  for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method.

### Signal-Detect

The SY88933V generates a chatter-free SD open-collector TTL output with internal 6.75k $\Omega$  pullup resistor as shown in Figure 4. SD is used to determine that the input amplitude is large enough to be considered a valid input. SD asserts high if the input amplitude rises above the threshold set by

$\text{SD}_{\text{LVL}}$  and deasserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a loss of signal condition. EN deasserts the true output signal without removing the input signals. Typically 4.6dB SD hysteresis is provided to prevent chattering.

### Signal-Detect Level Set

A programmable SD level set pin ( $\text{SD}_{\text{LVL}}$ ) sets the threshold of the input amplitude detection. Connecting an external resistor between  $V_{\text{CC}}$  and  $\text{SD}_{\text{LVL}}$  sets the voltage at  $\text{SD}_{\text{LVL}}$ . This voltage ranges from  $V_{\text{CC}}$  to  $V_{\text{REF}}$ . The external resistor creates a voltage divider between  $V_{\text{CC}}$  and  $V_{\text{REF}}$  as shown in Figure 5. If desired, an appropriate external voltage may be applied rather than using a resistor. The smaller the external resistor, implying a smaller voltage difference from  $\text{SD}_{\text{LVL}}$  to  $V_{\text{CC}}$ , the smaller the SD sensitivity. Hence, larger input amplitude is required to assert SD. "Typical Operating Characteristics" shows the relationship between the input amplitude detection sensitivity and the  $\text{SD}_{\text{LVL}}$  voltage.

### Hysteresis

The SY88933V provides typically 4.6dB SD electrical hysteresis. By definition, a power ratio measured in dB is  $10\log(\text{power ratio})$ . Power is calculated as  $V_{\text{IN}}^2/R$  for an electrical signal. Hence the same ratio can be stated as  $20\log(\text{voltage ratio})$ . While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88933V provides typically 2.3dB SD optical hysteresis. As the SY88933V is an electrical device, this datasheet refers to hysteresis in electrical terms. With 6dB SD hysteresis, a voltage factor of two is required to assert or deassert SD.

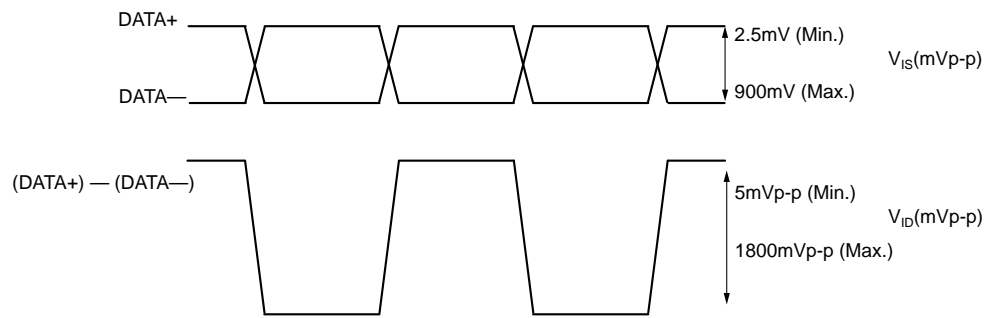
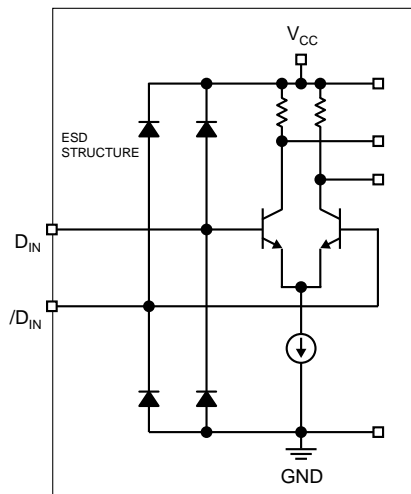
Figure 1.  $V_{IS}$  and  $V_{ID}$  Definitions

Figure 2. Input Structure

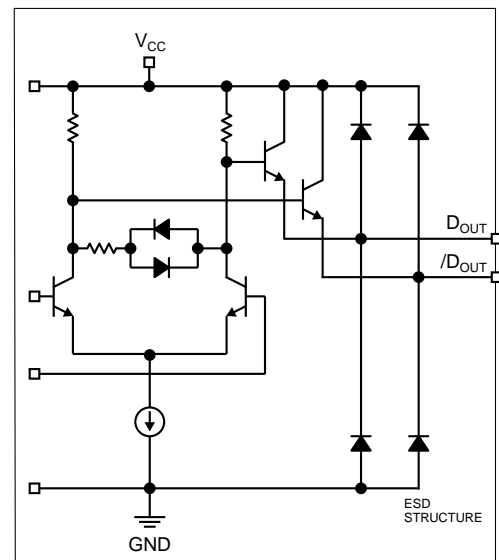


Figure 3. Output Structure

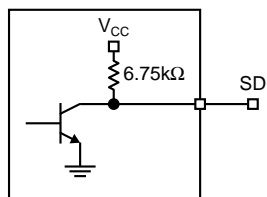
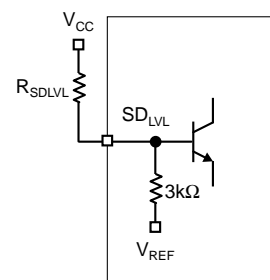
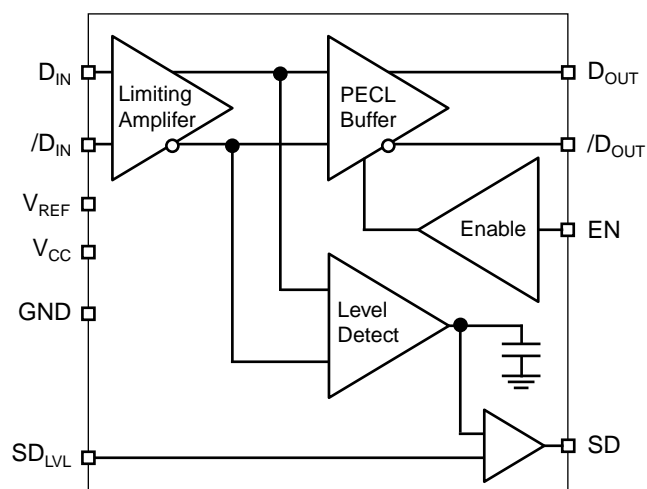


Figure 4. SD Output Structure

Figure 5.  $SD_{LVL}$  Setting Circuit

## FUNCTIONAL BLOCK DIAGRAM



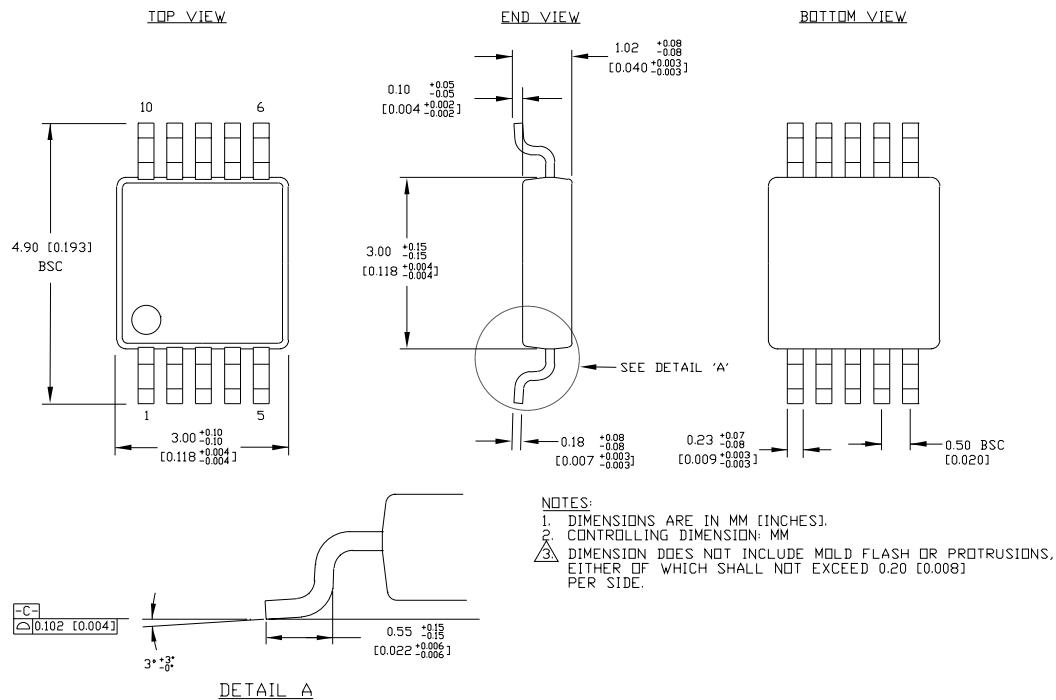
## DESIGN PROCEDURE

### Layout and PCB Design

Since the SY88933V is a high-frequency component, performance can be largely determined by the board layout and design. A common problem with high-gain amplifiers is the feedback from the large swing outputs to the input via the power supply.

The SY88933V's ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

# 10 LEAD MSOP (K10-1)



Rev. 00

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