

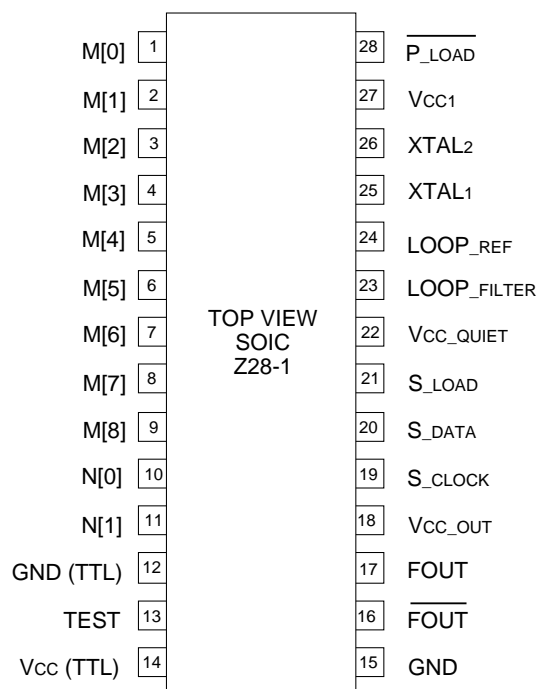
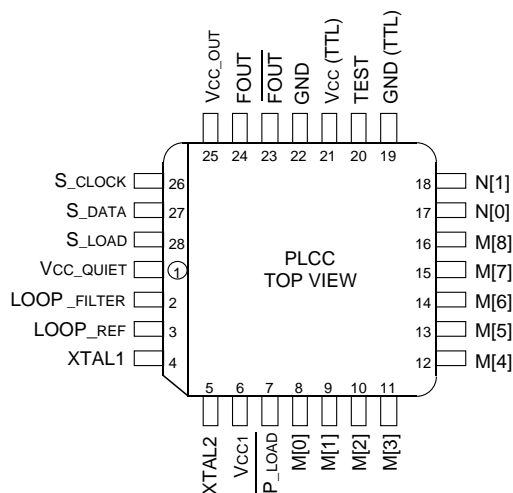
## FEATURES

- 5V and 3.3V power supply options
- 50MHz to 950MHz differential PECL outputs
- $\pm 25$ ps peak-to-peak output jitter
- Minimal frequency over-shoot
- Synthesized architecture
- Serial 3 wire interface
- Parallel interface for power-on
- Internal quartz reference oscillator driven by quartz crystal
- External loop filter optimizes performance/cost
- Applications note (AN-07) for ease of design-ins
- Available in 28-pin PLCC and SOIC packages

## DESCRIPTION

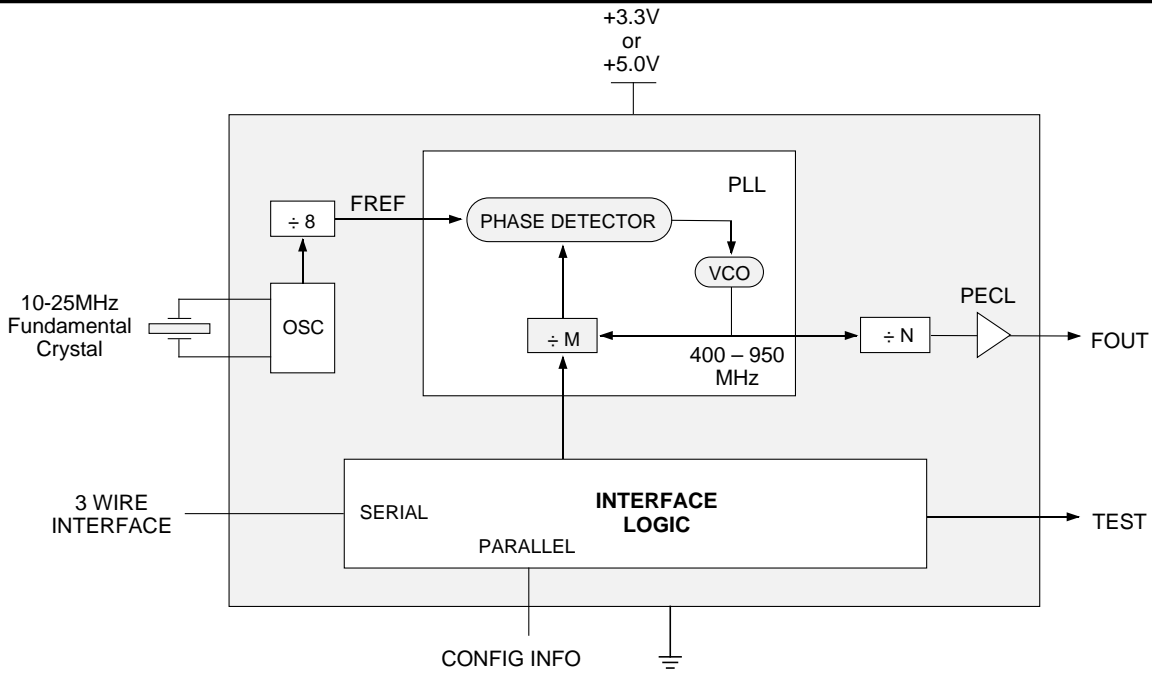
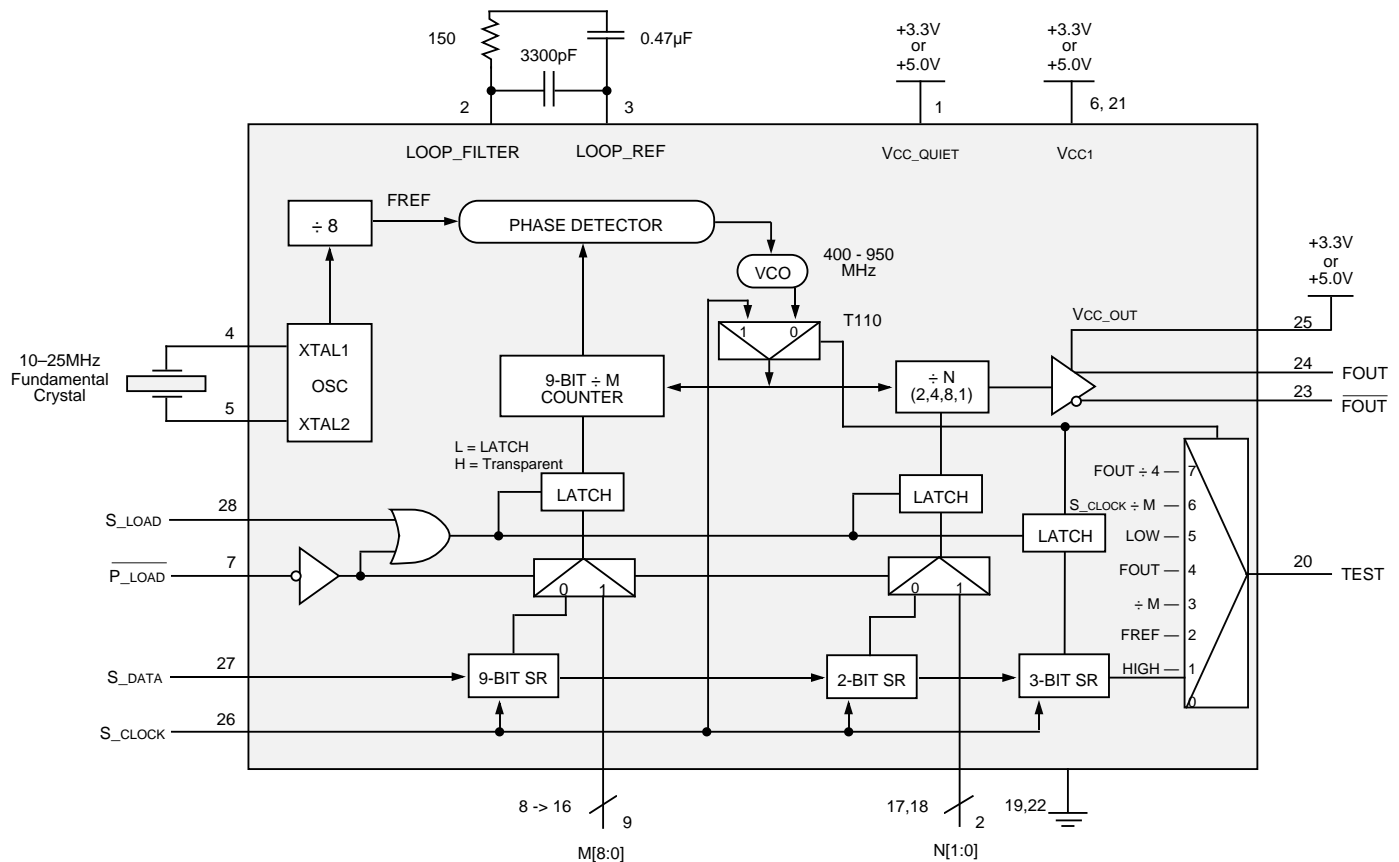
The SY89430V is a general purpose, synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal VCO will operate over a range of frequencies from 400MHz to 950MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4 or 8. With the output configured to divide the VCO frequency by 2, and with a 16MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps.

## PIN CONFIGURATION



## APPLICATIONS

- Workstations
- Advanced communications
- High end consumer
- High-performance computing
- RISC CPU clock
- Graphics pixel clock
- Test equipment
- Other high-performance processor-based applications

**BLOCK DIAGRAM****DETAILED BLOCK DIAGRAM****NOTE:**

Pin numbers reference PLCC pinout.

## PIN DESCRIPTIONS

### INPUTS

#### XTAL1, XTAL2

These pins form an oscillator when connected to an external crystal. The crystal is series resonant.

#### S\_LOAD

This TTL pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH; thus, the register data must be stable on the HIGH-to-LOW transition of S\_LOAD for proper operation.

#### S\_DATA

This TTL pin is the input to the serial configuration shift registers.

#### S\_CLOCK

This TTL pin clocks the serial configuration shift registers. On the rising edge of this signal, data from S\_DATA is sampled.

#### P\_LOAD

This TTL pin loads the configuration latches with the contents of the parallel inputs. The latches will be transparent when this signal is LOW; thus, the parallel data must be stable on the LOW-to-HIGH transition of P\_LOAD for proper operation.

#### M[8:0]

These TTL pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of P\_LOAD. M[8] is the MSB, M[0] is the LSB. The binary count on the M pins equates to the divide-by value for the PLL.

#### N[1:0]

These TTL pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of P\_LOAD.

N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

### OUTPUTS

#### FOUT, FOUT

These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.

#### TEST

The function of this TTL output is determined by the serial configuration bits T[2:0].

### POWER

#### VCC1

This is the positive supply for the chip and is normally connected to +3.3V or +5.0V.

#### VCC\_OUT

This is the positive reference for the PECL outputs, FOUT and FOUT. It is constrained to be less than or equal to VCC1.

#### VCC\_QUIET

This is the positive supply for the PLL and should be as noise-free as possible for low-jitter operation.

#### GND

These pins are the negative supply for the chip and are normally all connected to ground.

### OTHER

#### LOOP\_FILTER

This is an analog I/O pin that provides the loop filter for the PLL.

#### LOOP\_REF

This is an analog I/O pin that provides a reference voltage for the PLL.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
VCC	Power Supply Voltage	−0.5 to +7.0	V
VI	Input Voltage	−0.5 to +7.0	V
IOUT	Output Source Continuous Surge	50 100	mA
T <sub>store</sub>	Storage Temperature	−65 to +150	°C
T <sub>A</sub>	Operating Temperature	−0 to +75	°C

#### NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**WITH 16MHZ INPUT**

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
400	200	0	1	1	0	0	1	0	0	0
402	201	0	1	1	0	0	1	0	0	1
404	202	0	1	1	0	0	1	0	1	0
406	203	0	1	1	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
944	472	1	1	1	0	1	1	0	0	0
946	473	1	1	1	0	1	1	0	0	1
948	474	1	1	1	0	1	1	0	1	0
950	475	1	1	1	0	1	1	0	1	1

**FUNCTIONAL DESCRIPTION**

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by eight before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 2MHz.

The VCO within the PLL operates over a range of 400–950MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock. External loop filter components are utilized to allow for optimal phase jitter performance.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. The output divider is configured through either the serial or the parallel interfaces and can provide one of four divider ratios (1, 2, 4 or 8). This divider extends the performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω to VCC –2volts. The positive reference for the output driver is provided by a dedicated power pin (VCC\_OUT) to reduce noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally upon system reset, the P\_LOAD input is held LOW until sometime after power becomes valid. With S\_LOAD held LOW, on the LOW-to-HIGH transition of P\_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pull-up resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count.

The serial interface logic is implemented with a 14-bit shift register scheme. The register shifts once per rising edge of the S\_CLOCK input. The serial input S\_DATA must meet set-up and hold timing as specified in the AC parameters section of this data sheet. With P\_LOAD held HIGH, the configuration latches will capture the value in the shift register on the HIGH-to-LOW edge of the S\_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

## PROGRAMMING INTERFACE

Programming the device is accomplished by properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can be represented by this formula:

$$F_{OUT} = \left( \frac{F_{XTAL}}{8} \right) \times \frac{M}{N}$$

Where  $F_{XTAL}$  is the crystal frequency,  $M$  is the loop divider modulus, and  $N$  is the output divider modulus. Note that it is possible to select values of  $M$  such that the PLL is unable to achieve loop lock. To avoid this, always make sure that  $M$  is selected to be  $200 \leq M \leq 510$  for a 16MHz input reference.

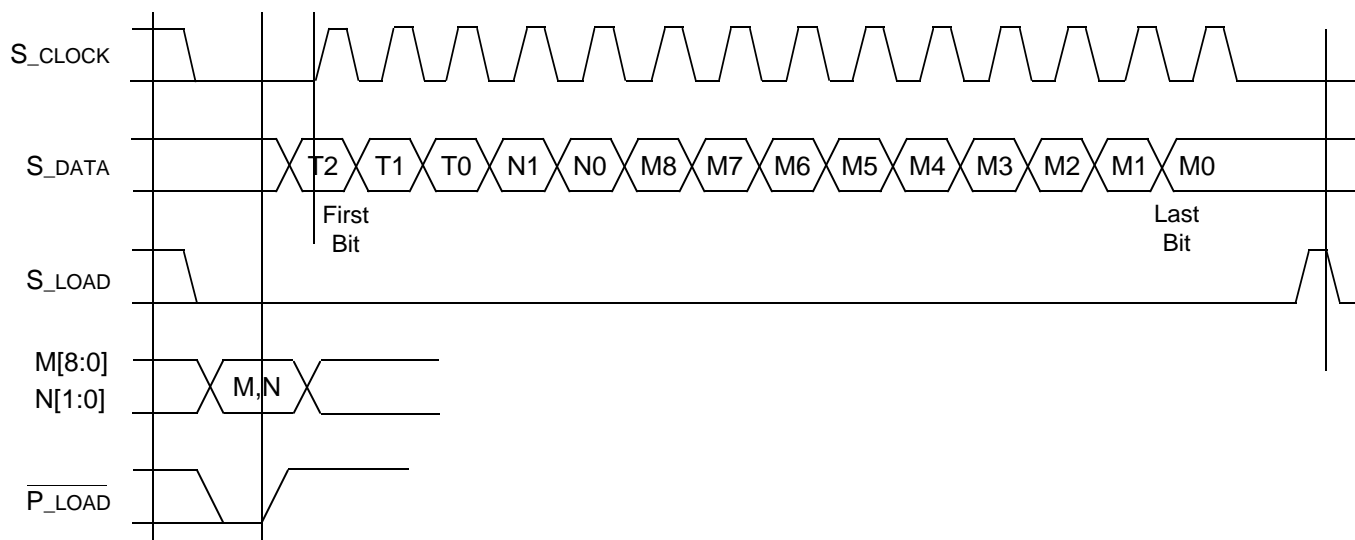
$M[8:0]$  and  $N[1:0]$  are normally specified once at power-on, through the parallel interface, and then possibly again through the serial interface. This approach allows the designer to bring up the application at one frequency and then change or fine-tune the clock, as the ability to control the serial interface becomes available. To minimize transients in the frequency domain, the output should be varied in the smallest step size possible.

T2	T1	T0	TEST	FOUT / FOUT
0	0	0	Data Out – Last Bit SR	FVCO ÷ N
0	0	1	HIGH	FVCO ÷ N
0	1	0	FREF	FVCO ÷ N
0	1	1	M Counter Output	FVCO ÷ N
1	0	0	FOUT	FVCO ÷ N
1	0	1	LOW	FVCO ÷ N
1	1	0	S_CLOCK ÷ M	S_CLOCK ÷ N
1	1	1	FOUT ÷ 4	FVCO ÷ N

The TEST output provides visibility for one of several internal nodes (as determined by the  $T[1:0]$  bits in the serial configuration stream). It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the TTL output may not be able to toggle fast enough for some of the higher output frequencies. The  $T_2$ ,  $T_1$ ,  $T_0$  configuration latches are preset to 000 when  $P\_LOAD$  is low, so that the FOUT outputs are as jitter-free as possible. The serial configuration port can be used to select one of the alternate functions for this pin.

The Test register is loaded with the first three bits, the  $N$  register with the next two and the  $M$  register with the final eight bits of the data stream on the  $S\_DATA$  input. For each register the most significant bit is loaded first ( $T_2$ ,  $N_1$  and  $M_8$ ).

When  $T[2:0]$  is set to 100 the SY89430V is placed in PLL bypass mode. In this mode the  $S\_CLOCK$  input is fed directly into the  $M$  and  $N$  dividers. The  $N$  divider drives the FOUT differential pair and the  $M$  counter drives the TEST output pin. In this mode the  $S\_CLOCK$  input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree (See detailed Block Diagram). Because the  $S\_CLOCK$  is a TTL level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the  $S\_CLOCK$  is 125MHz as the minimum divide ratio of the  $N$  counter is 2. Note that the  $M$  counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.



**100H ECL DC ELECTRICAL CHARACTERISTICS**

VCC1 = VCC\_QUIET = VCC\_TTL = VCC\_OUT = +3.3V to +5.0V ±5%; TA = 0°C to +75°C

Symbol	Parameter	Min.	Max.	Unit	Condition
VOH	Output HIGH Voltage	VCC_OUT -1.075	VCC_OUT -0.830	V	50Ω to VCC_OUT -2V
VOL	Output LOW Voltage	VCC_OUT -1.860	VCC_OUT -1.570	V	50Ω to VCC_OUT -2V

**TTL DC ELECTRICAL CHARACTERISTICS**

VCC1 = VCC\_QUIET = VCC\_TTL = VCC\_OUT = +3.3V to +5.0V ±5%; TA = 0°C to +75°C

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
VIH	Input HIGH Voltage	2.0	—	2.0	—	2.0	—	V	—
VIL	Input LOW Voltage	—	0.8	—	0.8	—	0.8	V	—
IiH	Input HIGH Current	—	50	—	50	—	50	μA	VIN = 2.7V
IiL	Input LOW Current	—	-0.6	—	-0.6	—	-0.6	mA	VIN = 0.5V
VIK	Input Clamp Voltage	—	-1.2	—	-1.2	—	-1.2	V	IIN = -12mA
VOH	Output HIGH Voltage	—	2.0	—	2.0	—	2.0	V	IOH = -2.0mA
VOL	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	IOL = 8mA
Ios	Output Short Circuit Current	-100 (Typ.)		-100 (Typ.)		-100 (Typ.)		mA	VOUT = 0V
Icc1	Supply Current	—	220	—	220	—	220	mA	5.0V ±5%
		0.91X of 5V Val.		0.91X of 5V Val.		0.91X of 5V Val.		mA	3.3V ±5%
	Typical % of Icc1	VCC1		33%		33%			
		VCC_OUT		9%		9%			
		VCC_QUIET		14%		14%			
		VCC_TTL		44%		44%			

**AC ELECTRICAL CHARACTERISTICS**

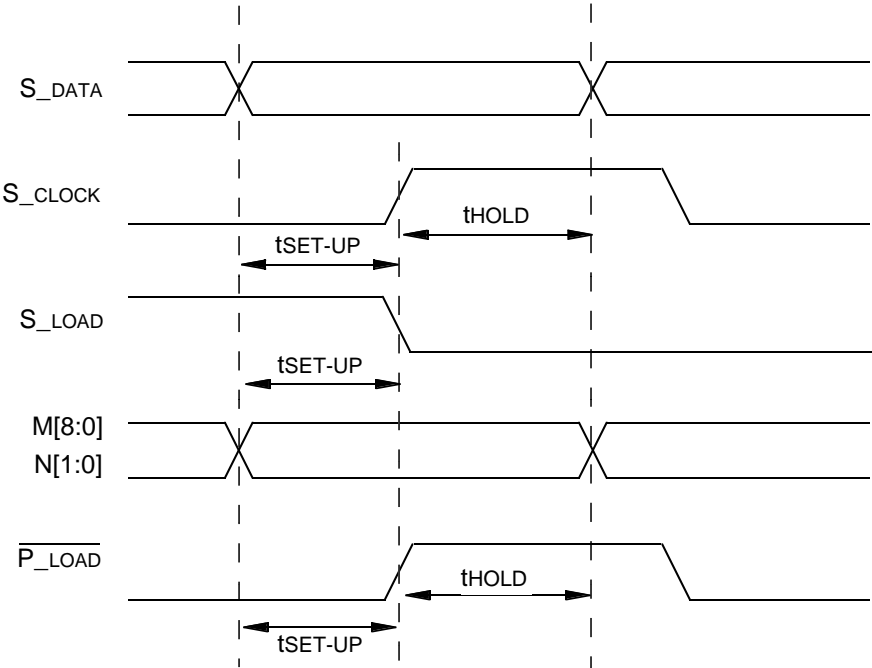
VCC1 = VCC\_QUIET = VCC\_TTL = VCC\_OUT = +3.3V to +5.0V ±5%; TA = 0°C to +75°C

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +75°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
fMAXI	Maximum Input Frequency <sup>(1)</sup> S_CLOCK Xtal Oscillator	— 10	10 25	— 10	10 25	— 10	10 25	MHz	Fundamental Cyrstal
fMAXO	Maximum Output Frequency VCO (Internal) FOUT	400 50	950 950	400 50	950 950	400 50	950 950	MHz	
tLOCK	Maximum PLL Lock Time	—	10	—	10	—	10	ms	
tjitter	Cycle-to-Cycle Jitter (Peak-to-Peak)	—	±25	—	±25	—	±25	ps	Test output static
ts	Setup Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20	—	20	—	20	—	ns	
		20	—	20	—	20	—		
		20	—	20	—	20	—		
th	Hold Time S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20	—	20	—	20	—	ns	
		20	—	20	—	20	—		
		20	—	20	—	20	—		
tpw(MIN)	Minimum Pulse Width S_LOAD P_LOAD	50	—	50	—	50	—	ns	
		50	—	50	—	50	—		
tDC	FOUT Duty Cycle	45	55	45	55	45	55	%	
tr tf	Output Rise/Fall 20% to 80% FO	100	500	100	500	100	500	ps	

**NOTE:**

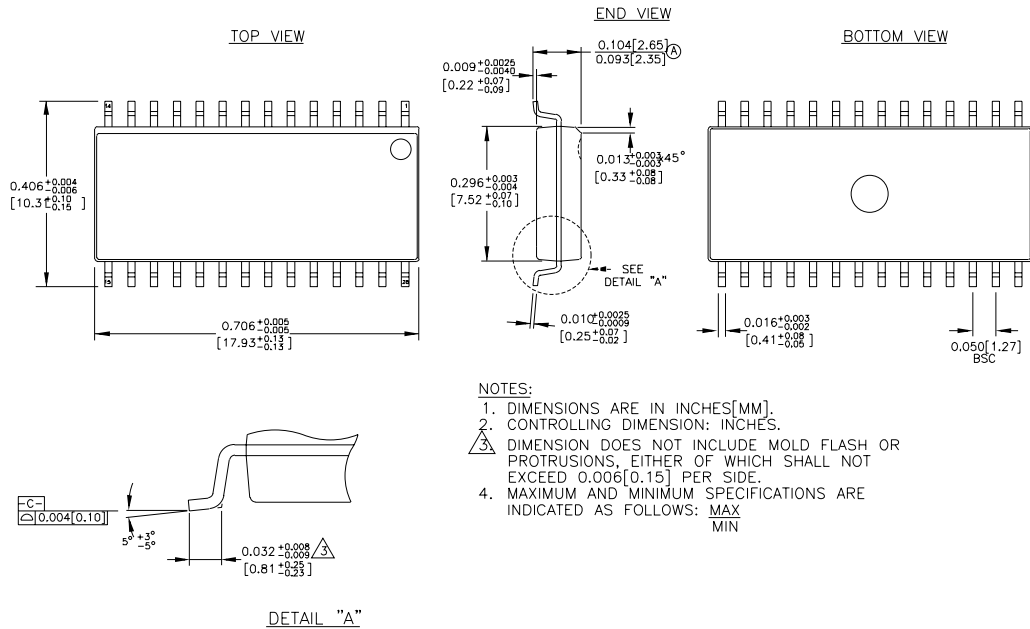
1. 10MHz is the maximum frequency to load the feedback divide registers. S\_CLOCK can be switched at high frequencies when used as a test clock in TEST\_MODE 6.

**TIMING DIAGRAM**

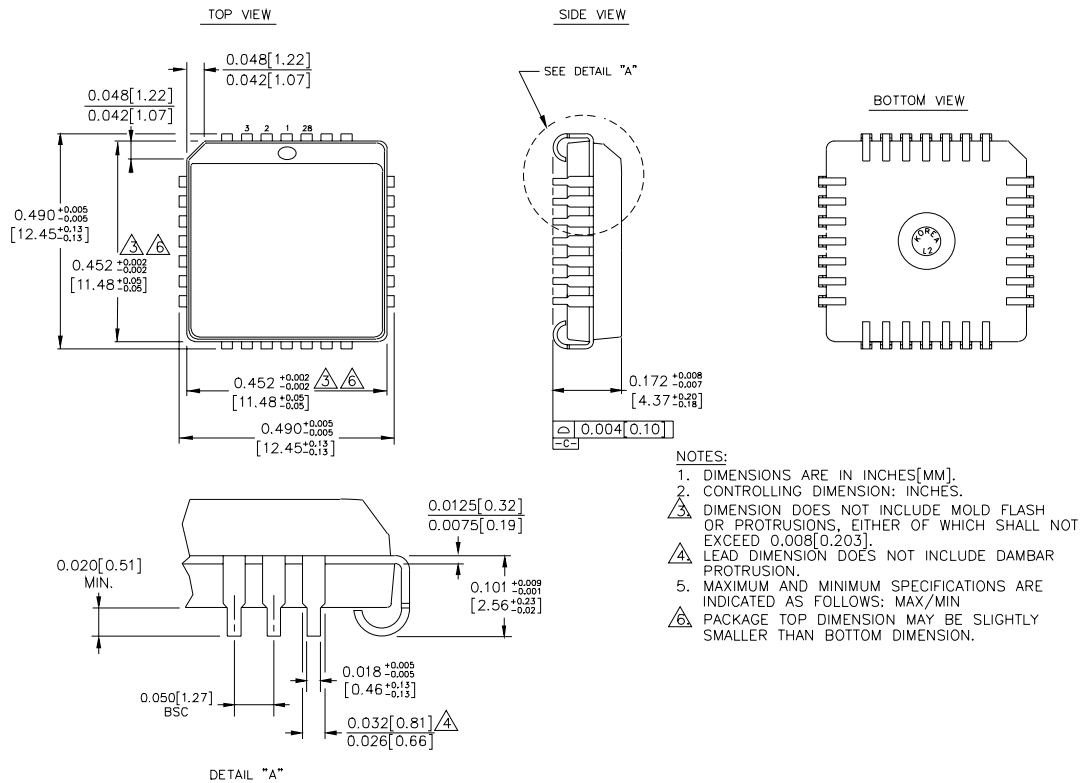


**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY89430VJC	J28-1	Commercial
SY89430VJCTR	J28-1	Commercial
SY89430VZC	Z28-1	Commercial
SY89430VZCTR	Z28-1	Commercial

**28 LEAD SOIC .300" WIDE (Z28-1)**

Rev. 02

**28 LEAD PLCC (J28-1)**

Rev. 03

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