

FEATURES

- High-performance dual 1:10, 1GHz LVDS fanout buffer/translator
- Two banks of 10 differential LVDS outputs
- Guaranteed AC parameters over temperature and voltage:
 - > 1GHz f_{MAX}
 - < 50ps within device skew
 - < 400ps t_r , t_f time
- Each bank includes a 2:1 input mux
- 2:1 mux input accepts LVDS and LVPECL
- Low jitter performance
 - < 1ps (rms) cycle-to-cycle jitter
 - < 1ps (pk-pk) total jitter
- 3.3V supply voltage
- Output enable function
- LVDS input includes internal 100Ω termination
- Available in a 64-Pin EPAD-TQFP



Precision Edge™

DESCRIPTION

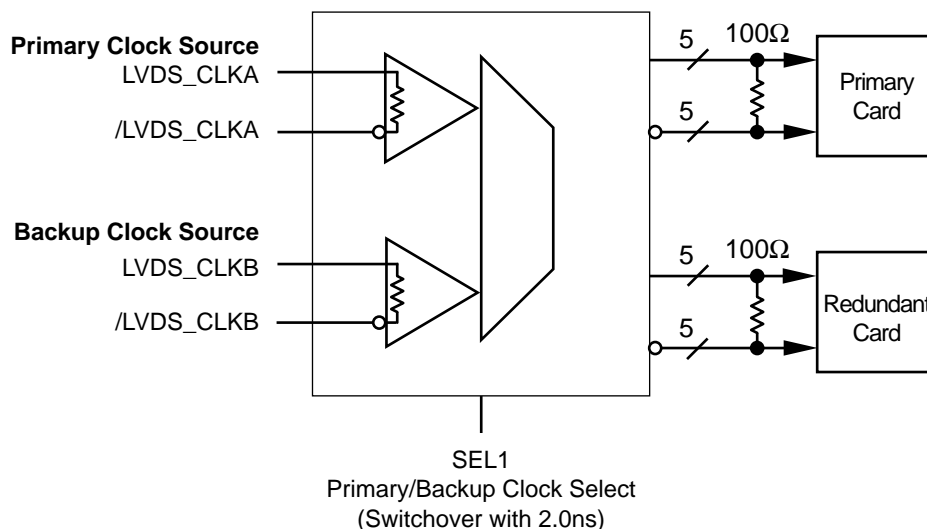
The SY89828L is a precision fanout buffer with 20 differential LVDS (Low Voltage Differential Swing) output pairs. The part is designed for use in low voltage 3.3V applications that require a large number of outputs to drive precisely aligned, ultra low-skew signals to their destination. The input is multiplexed from either LVDS or LVPECL (Low Voltage Positive Emitter Coupled Logic) by the CLK_SEL1 and CLK_SEL2 pins. The Output Enables (OE1 and OE2) are synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89828L features a low pin-to-pin skew of less than 50ps—performance previously unachievable in a standard product having such a high number of outputs. The SY89828L is available in a single space saving package, enabling a lower overall cost solution.

APPLICATIONS

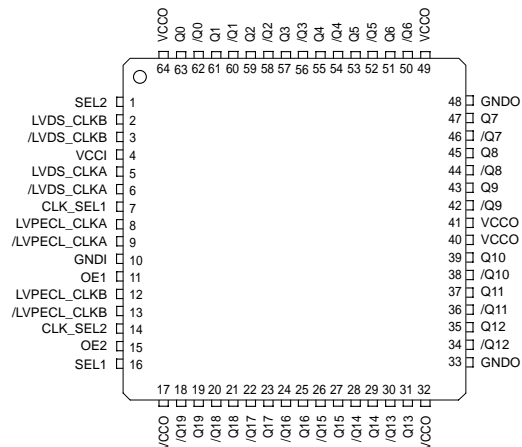
- Enterprise networking
- High-end servers
- Communications

TYPICAL APPLICATION CIRCUIT



System using SY89828L as a switchover circuit from a Primary Clock to a Redundant backup Clock in a fail-safe application. LVPECL inputs not shown in this application.

PACKAGE/ORDERING INFORMATION

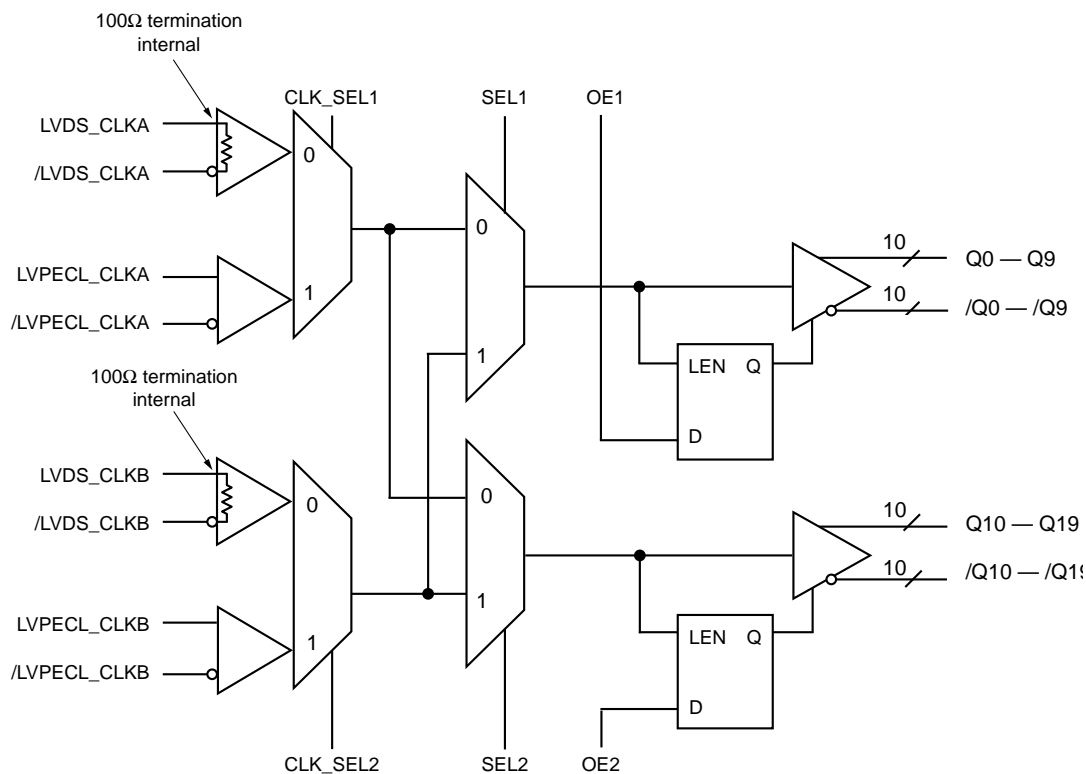


64-Pin TQFP (H64-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking
SY89828LHI	H64-1	Industrial	SY89828L

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin Number	Pin Name	I/O	Type	Internal P/U	Pin Function
5, 6	LVDS_CLKA /LVDS_CLKA	Input	LVDS	3.5kΩ Pull-up See Fig. 2	Differential clock input selected by CLK_SEL1, SEL1 and SEL2. Can be left floating if not selected. Floating input, if selected produces an indeterminate output. Has internal 100Ω termination.
2, 3	LVDS_CLKB /LVDS_CLKB	Input	LVDS	3.5kΩ Pull-up See Fig. 2	Differential clock input selected by CLK_SEL1, SEL1 and SEL2. Can be left floating if not selected. Floating input, if selected produces an indeterminate output. Has internal 100Ω termination.
8, 9	LVPECL_CLKA /LVPECL_CLKA	Input	LVPECL	75kΩ pull-down See Fig. 1	Differential clock input selected by CLK_SEL1, SEL1 and SEL2. Can be left floating. Floating input, if selected produces a LOW at output. Requires external termination.
12, 13	LVPECL_CLKB /LVPECL_CLKB	Input	LVPECL	75kΩ pull-down See Fig. 1	Differential clock input selected by CLK_SEL2, SEL1 and SEL2. Requires external termination.
7	CLK_SEL1	Input	LVTTTL/ CMOS	11kΩ Pull-up	Selects LVDS_CLKA input when LOW and LVPECL_CLKA input when HIGH.
14	CLK_SEL2	Input	LVTTTL/ CMOS	11kΩ Pull-up	Selects LVDS_CLKB input when LOW and LVPECL_CLKB input when HIGH.
16	SEL1	Input	LVTTTL/ CMOS	11kΩ Pull-up	Selects input source CLKA when LOW and CLKB when HIGH for outputs Q0 – Q9 and /Q0 – /Q9.
1	SEL2	Input	LVTTTL/ CMOS	11kΩ Pull-up	Selects input source CLKA when LOW and CLKB when HIGH for outputs Q10 – Q19 and /Q10 – /Q19.
11	OE1	Input	LVTTTL/ CMOS	11kΩ Pull-up	Enable input synchronized internally to prevent output glitches or runt pulses.
15	OE2	Input	LVTTTL/ CMOS	11kΩ Pull-up	Enable input synchronized internally to prevent output glitches or runt pulses.
4	VCCI	Power			Core VCC connected to 3.3V supply. Not connected to VCCO internally. Connected to VCCO on PCB. Bypass with 0.1μF in parallel with 0.01μF low ESR capacitors as close to VCC pins as possible.
17, 32, 40, 41, 49, 64	VCCO	Power			Output buffer VCC connected to 3.3V supply. Not connected to VCCI internally. Connected to VCCI on PCB. Bypass with 0.1μF in parallel with 0.01μF low ESR capacitors as close to VCC pins as possible.
10	GNDI	Power			Core ground not connected to GNDO internally. To be connected to GNDO on PCB.
33, 48	GNDO	Power			Output buffer ground not connected to GNDI internally. To be connected to GNDI on PCB.
63, 61, 59, 57, 55 53, 51, 47, 45, 43	Q0 – Q9	Output	LVDS		Differential clock outputs from CLKA when SEL1 = LOW and from CLKB when SEL1 = HIGH. Q outputs are static when OE1 = LOW. Unused output pair must be terminated with 100Ω to maintain low jitter and skew.
62, 60, 58, 56, 54 52, 50, 46, 44, 42	/Q0 – /Q9	Output	LVDS		Differential clock outputs (complement) from CLKA when SEL1 = LOW and from CLKB when SEL1 = HIGH. /Q outputs are static HIGH when OE1 = LOW. Unused output pairs must be externally terminated with 100Ω to maintain low jitter and skew.
39, 37, 35, 31, 29 27, 25, 23, 21, 19	Q10 – Q19	Output	LVDS		Differential outputs from CLKA when SEL2 = LOW and from CLKB when SEL2 = HIGH. Q outputs are static LOW when OE2 = LOW. Unused output pairs must be externally terminated with 100Ω to maintain low jitter and skew.

Pin Number	Pin Name	I/O	Type	Internal P/U	Pin Function
38, 36, 34, 30, 28 26, 24, 22, 20, 18	/Q10 – /Q19	Output	LVDS		Differential outputs (complement) from CLKA when SEL2 = LOW and from CLKB when SEL2 = HIGH. /Q outputs are static HIGH when OE2 = LOW. Unused output pairs must be externally terminated with 100Ω to maintain low jitter and skew.

TRUTH TABLE

OE1 ⁽¹⁾	OE2 ⁽¹⁾	SEL1 ⁽¹⁾	SEL2 ⁽¹⁾	CLK_SEL1 ⁽¹⁾	CLK_SEL2 ⁽¹⁾	Q0 – Q9	/Q0 – /Q9	Q10 – Q19	/Q10 – /Q19
1	1	0	0	0	X	LVDS_CLKA	/LVDS_CLKA	LVDS_CLKA	/LVDS_CLKA
1	1	0	0	1	X	LVPECL_CLKA	/LVPECL_CLKA	LVPECL_CLKA	/LVPECL_CLKA
1	1	0	1	0	0	LVDS_CLKA	/LVDS_CLKA	LVDS_CLKB	/LVDS_CLKB
1	1	0	1	0	1	LVDS_CLKA	/LVDS_CLKA	LVPECL_CLKB	/LVPECL_CLKB
1	1	0	1	1	0	LVPECL_CLKA	/LVPECL_CLKA	LVDS_CLKB	/LVDS_CLKB
1	1	0	1	1	1	LVPECL_CLKA	/LVPECL_CLKA	LVPECL_CLKB	/LVPECL_CLKB
1	1	1	0	0	0	LVDS_CLKB	/LVDS_CLKB	LVDS_CLKA	/LVDS_CLKA
1	1	1	0	0	1	LVPECL_CLKB	/LVPECL_CLKB	LVDS_CLKA	/LVDS_CLKA
1	1	1	0	1	0	LVDS_CLKB	/LVDS_CLKB	LVPECL_CLKA	/LVPECL_CLKA
1	1	1	0	1	1	LVPECL_CLKB	/LVPECL_CLKB	LVPECL_CLKA	/LVPECL_CLKA
1	1	1	1	X	0	LVDS_CLKB	/LVDS_CLKB	LVDS_CLKB	/LVDS_CLKB
1	1	1	1	X	1	LVPECL_CLKB	/LVPECL_CLKB	LVPECL_CLKB	/LVPECL_CLKB
0	1	X	0	0	X	LOW	HIGH	LVDS_CLKA	/LVDS_CLKA
0	1	X	0	1	X	LOW	HIGH	LVPECL_CLKA	/LVPECL_CLKA
0	1	X	1	X	0	LOW	HIGH	LVDS_CLKB	/LVDS_CLKB
0	1	X	1	X	1	LOW	HIGH	LVPECL_CLKB	/LVPECL_CLKB
1	0	0	X	0	X	LVDS_CLKA	/LVDS_CLKA	LOW	HIGH
1	0	0	X	1	X	LVPECL_CLKA	/LVPECL_CLKA	LOW	HIGH
1	0	1	X	X	0	LVDS_CLKB	/LVDS_CLKB	LOW	HIGH
1	0	1	X	X	1	LVPECL_CLKB	/LVPECL_CLKB	LOW	HIGH
0	0	X	X	X	X	LOW	HIGH	LOW	HIGH

NOTE:

1. Input has internal pull-up so floating input = 1.

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{CCI} , V_{CCO}) -0.5 to +4.0V
Input Voltage (V_{IN}) -0.5 to V_{CCI}
Output Current (I_{OUT}) ± 10 mA
Storage Temperature (T_S) -65 to +150°C
ESD Rating, Note 3 1kV

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Devices are ESD sensitive. Handling precautions recommended.

Operating Ratings(Note 2)

Supply Voltage +3V to +3.6V
Ambient Temperature (T_A) -40°C to +85°C
Package Thermal Resistance	
TQFP (θ_{JA})	
<i>Exposed pad soldered to GND</i>	
Still-Air (multi-layer PCB) 23°C/W
-200lfpm (multi-layer PCB) 18°C/W
-500lfpm (multi-layer PCB) 15°C/W
<i>Exposed pad <u>NOT</u> soldered to GND (not recommended)</i>	
Still-Air (multi-layer PCB) 44°C/W
-200lfpm (multi-layer PCB) 36°C/W
-500lfpm (multi-layer PCB) 30°C/W
TQFP (θ_{JC}) 4.4°C/W

DC ELECTRICAL CHARACTERISTICS

Power Supply: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCI} , V_{CCO}	V_{CC} Core, V_{CC} Output	Note 4	3.0	3.3	3.6	V
I_{CCI}	I_{CC} Core	Max. V_{CC}		45	70	mA
I_{CCO}	I_{CC} Output	No Load, Max. V_{CC}		160	260	mA

Note 4. V_{CCI} and V_{CCO} must be connected together on the PCB such that they remain at the same potential. V_{CCI} and V_{CCO} are not internally connected on the die.

LVDS Input: $V_{CC} = 3.3\text{V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		0		2.4	V
V_{ID}	Differential Input Swing		100			mV
I_{IL}	Input LOW Current		-1.25			mA
R_{IN}	LVDS Differential Input Resistance (LVDS_CLK to /LVDS_CLK)		80	100	120	Ω

DC ELECTRICAL CHARACTERISTICS**LVPECL Input:** $V_{CC} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage (Single-Ended)		$V_{CC} - 1.165$		$V_{CC} - 0.880$	V
V_{IL}	Input LOW Voltage		$V_{CC} - 1.945$		$V_{CC} - 1.625$	V
V_{PP}	Minimum Input Swing (LVPECL_CLK)	Note 5	300			mV
V_{CMR}	Common Mode Range (LVPECL_CLK)	Note 6	GNDI + 1.8		$V_{CCI} - 0.4$	V
I_{IH}	Input HIGH Current				150	μA
I_{IL}	Input LOW Current		0.5			μA

Note 5. The V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.**Note 6.** V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI} . The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.). CMR range varies 1:1 with V_{CCI} . V_{CMR} (min) is fixed at GNDI + 1.8V.**CMOS/LVTTL:** $V_{CC} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{CC}$			150	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.5V$	-600			μA

LVDS Output: $V_{CC} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	Note 7, 8	250	350	400	mV
V_{OH}	Output HIGH Voltage	Note 7			1.474	V
V_{OL}	Output LOW Voltage	Note 7	0.925			V
V_{OCM}	Output Common Mode Voltage	Note 8	1.125		1.375	V
ΔV_{OCM}	Change in Commom Mode Voltage		-50		50	mV

Note 7. Measured as per Figure 3, 100Ω across Q and /Q outputs.**Note 8.** Measured as per Figure 4.

AC ELECTRICAL CHARACTERISTICS(NOTE 1)

$V_{CC} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Toggle Frequency	Note 2	1.0			GHz
t_{PHL} t_{PLH}	Differential Propagation Delay Note 3	LVPECL Input: 150mV LVPECL Input: 800mV	0.950 0.80	1.15 1.0	1.45 1.3	ns ns
		LVDS Input: 100mV LVDS Input: 400mV	1.10 0.950	1.35 1.20	1.60 1.450	ns ns
$t_{SWITCHOVER}$	Clock Input Switchover	CLK_SEL to Valid Output		1.55	1.85	ns
$t_{S(OE)}$	Output Enable Set-Up Time	Note 4	1.0			ns
$t_{H(OE)}$	Output Enable Hold Time	Note 4	0.5			ns
t_{SKEW}	Within Device Skew	Note 5 $0^\circ C$ to $+85^\circ C$ $-40^\circ C$		25 35	50 75	ps ps
	Part-to-Part Skew	Note 6			400	ps
t_{JITTER}	Cycle-to-Cycle Total Jitter	Note 7 Note 8		<1	<1 2	ps(rms) ps(pk-pk)
t_r, t_f	Output Rise/Fall Times (20% to 80%)		200	290	400	ps

Note 1. 100Ω termination between Q and /Q outputs. Airflow ≥ 300 lfpm, or exposed pad soldered to ground plane.

Note 2. f_{MAX} is defined as the maximum toggle frequency, measured with a 750mV LVPECL input or 350mV LVDS input. Outut swing is > 200mV.

Note 3. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.

Note 4. Set-up and hold time applies to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold time does not apply. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.

Note 5. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device identical input transition, operating at the same voltage and temperature.

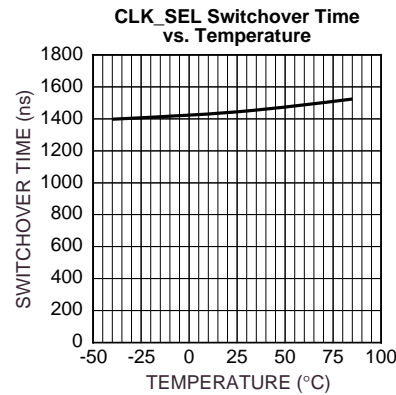
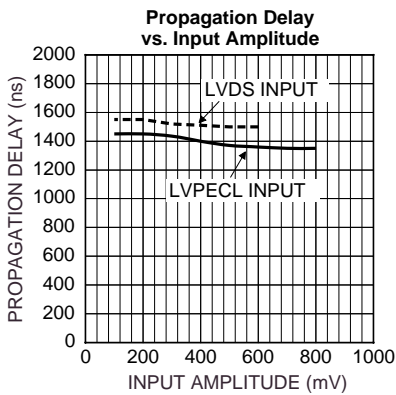
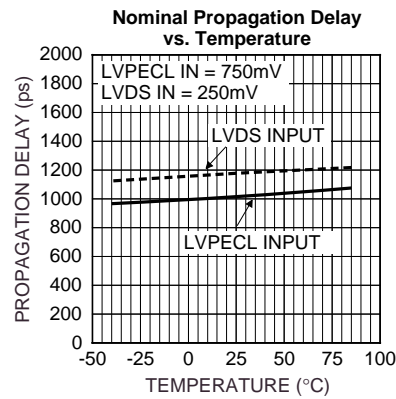
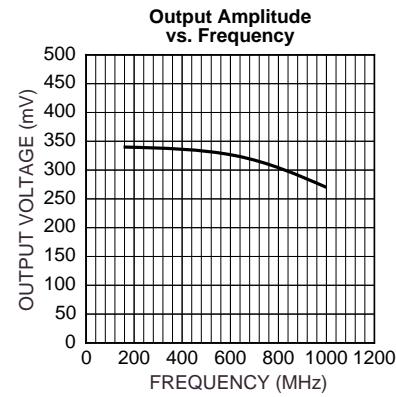
Note 6. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature. Part-to-part skew is the total skew difference; pin-to-pin skew + part-to-part skew.

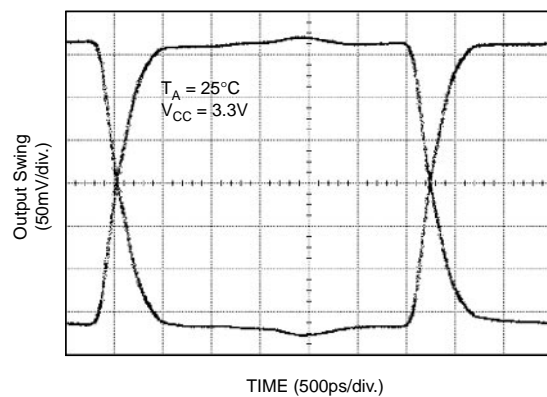
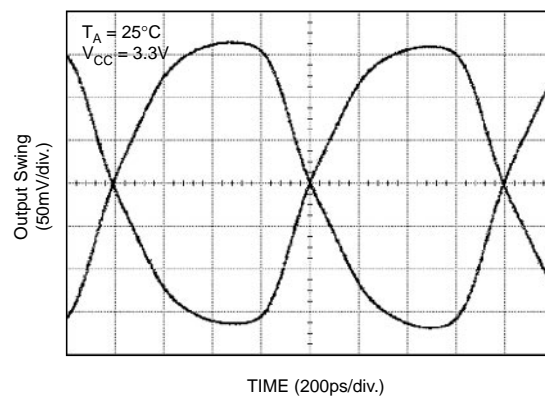
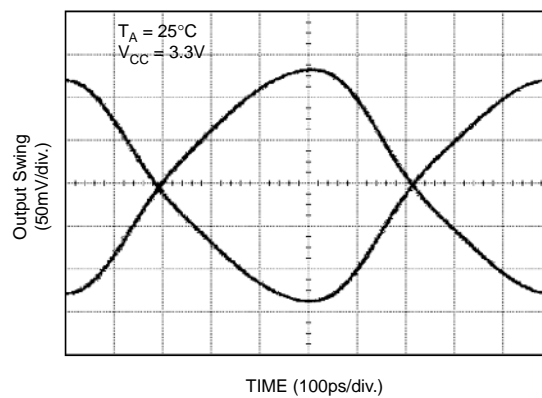
Note 7. Cycle-to-cycle jitter definition: The variation period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER_CC} = T_n - T_{n+1}$ where T is the time between rising edges of the output signal.

Note 8. Total jitter definition: with an ideal clock input, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TYPICAL OPERATING CHARACTERISTICS

(Conditions: $V_{CC} = 3.3V$, $T_A = 25^{\circ}C$, unless otherwise stated)



FUNCTIONAL CHARACTERISTICS**155MHz Output****622MHz Output****1GHz Output**

LVPECL/LVDS INPUTS

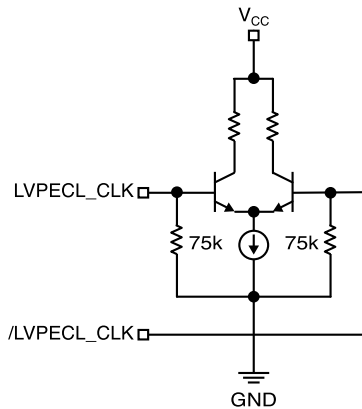


Figure 1. Simplified LVPECL Input Stage

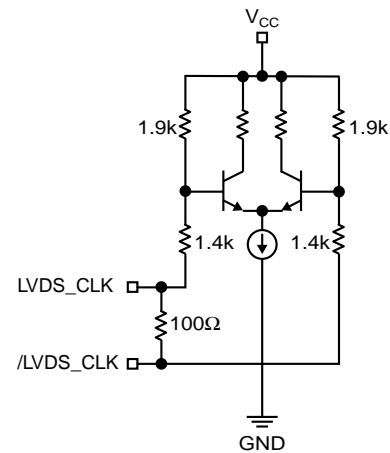


Figure 2. Simplified LVDS Input Stage

LVDS OUTPUTS

LVDS stands for Low Voltage Differential Swing. LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground

between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is also kept tight, to keep EMI low.

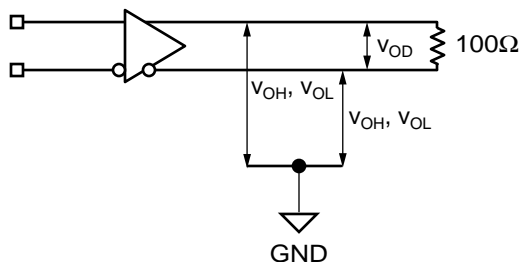


Figure 3. LVDS Differential Measurement

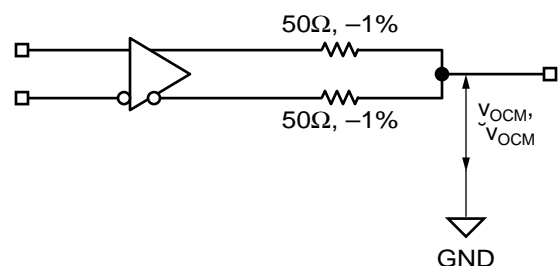


Figure 4. LVDS Common Mode Measurement

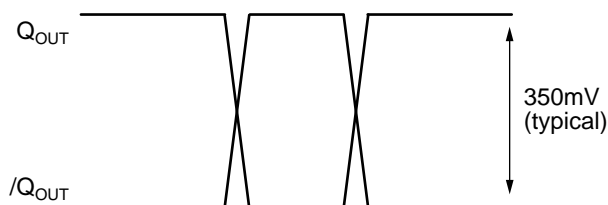


Figure 5. Output Driver Signal Levels (Single-Ended)

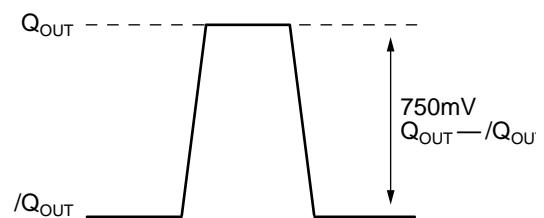


Figure 6. Output Driver Signal Levels (Differential)

DETAILED DESCRIPTION

The SY89828L is a precision dual 1:10 fanout buffer. It allows either LVPECL or LVDS inputs, selectable by an input muxes, and outputs 2 sets of 10 LVDS output pairs. The device features 2 synchronous output enables. The SY89828L provides extremely low skew across its outputs.

LVPECL_CLKA, LVPECL_CLKB

The SY89828L allows two inputs with standard LVPECL voltage swings. These inputs may be adjusted per the data sheet characteristics regarding the CMR and minimum input swing. As the SY89828L contains no appropriate internal termination, upstream devices need to be properly terminated to provide the proper LVPECL input swing. If not being used (CLK_SEL1 and CLK_SEL2 are LOW), these input pairs may be left floating, as they are internally terminated to ground via 75kΩ pull-down resistors.

LVDS_CLKA, LVDS_CLKB

The SY89828L allows two inputs with standard LVDS voltage swings. The SY89828L provides an appropriate internal 100Ω termination resistor. Hence, upstream LVDS devices do not require external termination to drive the SY89828L. If not being used (CLK_SEL1 and CLK_SEL2 are HIGH), these inputs pair may be left floating.

SEL1, SEL2 TTL Inputs

The SEL1 Input is used to select either CLKA (SEL1 is LOW) or CLKB (SEL1 is HIGH) for the Q0-Q9 differential output pairs. In a similar manner, The SEL2 Input is used to select either CLKA (SEL2 is LOW) or CLKB (SEL2 is HIGH) for the Q10-Q19 differential output pairs.

CLK_SEL1, CLK_SEL2 TTL Inputs

The CLK_SEL1 Input is used to select either LVDS_CLKA (CLK_SEL1 is LOW) or LVPECL_CLKA (CLK_SEL1 is HIGH). In a similar manner, The CLK_SEL2 Input is used to select either LVDS_CLKB (CLK_SEL2 is LOW) or LVPECL_CLKB (CLK_SEL2 is HIGH).

OE1, OE2 TTL Inputs

The SY89828L's output enable functions are designed to disable the outputs only when the outputs are LOW. The OE1 TTL Input controls the Q0-Q9 outputs and OE2 controls the Q10-Q19 outputs. This avoids the possibility of generating runt pulses. The OE1 and OE2 inputs are asynchronous inputs, but operate as synchronous enables. For synchronous operation, please adhere to the specific setup and hold times. When disabled, the Q outputs are LOW and the /Q outputs are HIGH.

Q0-Q9, Q10-Q19 LVDS Outputs

The SY89828L's LVDS outputs swing typically 350mV around a 1.25V common mode voltage above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input is kept tight to keep EMI low. Each of the SY89828L's LVDS outputs should be terminated with a 100Ω termination resistor including any unused output pairs. This ensures the best jitter and skew performance of the device. In a similar manner, The SEL2 Input is used to select either CLKA (SEL2 is LOW) or CLKB (SEL2 is HIGH) for the Q10-Q19 differential output pairs.

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY55855V	Dual CML/PECL/LVPECL-to-LVDS Translator	www.micrel.com/product-info/products/sy55855v.shtml
SY89825U	2.5/3.3V 1:22 High-Performance, Low-Voltage PECL Bus Clock Driver & Translator w/Internal Termination	www.micrel.com/product-info/products/sy89825u.shtml
SY89826U	3.3V 1GHz Precision 1:22 LVDS Fanout Buffer with 2:1 Input Mux	www.micrel.com/product-info/products/sy89826u.shtml
SY89829U	2.5/3.3V High-Performance, Dual 1:10 LVPECL Clock Driver w/Internal Termination & Redundant Switchover	www.micrel.com/product-info/products/sy89829u.shtml
M-0317	HBW Solutions	www.micrel.com/product-info/products/solutions.shtml
Exposed pad	Amkor Exposed Pad Application Note	www.amkor.com/products/notes_papers/ePad.pdf

12.00 [0.472] BSC SQ.

10.00 [0.394] BSC SQ.

5.00 $\begin{smallmatrix} +0.05 \\ -0.05 \\ [0.197 \pm 0.012] \end{smallmatrix}$

64

49

1

48

5.00 $\begin{smallmatrix} +0.03 \\ -0.03 \\ [0.197 \pm 0.012] \end{smallmatrix}$

16

33

17

32

0.50 [0.020] BSC

SEE DETAIL "A"

1.20 [0.047] MAX.

0.01 [0.004]

0.22 $\begin{smallmatrix} +0.05 \\ -0.05 \\ [0.009 \pm 0.002] \end{smallmatrix}$

DETAIL "A"

0° MIN.

0.20 [0.008]

0.09 [0.004]

0.15 [0.006]

0.05 [0.002]

0-7°

0.60 $\begin{smallmatrix} +0.15 \\ -0.05 \\ [0.024 \pm 0.006] \end{smallmatrix}$

1.00 [0.039] REF.

NOTES:

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev.

Note 1. Package meets Level 3 qualifications.

Note 2. All parts are 100% baked and dry-packed before shipment.

Note 3. Exposed pad must be soldered to a ground for proper thermal management.

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