

**MMC 4070 MMC 4077**

# **QUAD EXCLUSIVE-OR GATE 4070** **QUAD EXCLUSIVE-NOR GATE 4077**

## GENERAL DESCRIPTION

The MMC 4070/4077 are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package.

The MMC 4070 contains four independent exclusive-OR gates.

The MMC 4077 contains four independent exclusive-NOR gates.

The MMC 4070 and MMC 4077 provide the system designer with a means for direct implementation of exclusive-OR and exclusive-NOR function, respectively.

## FEATURES

- Medium-speed operation  $t_{PHL} = t_{PLH} = 65$  ns (TYP.) at  $V_{DD} = 10$  V,  $C_L = 50$  pF
- 100% tested for quiescent current

## APPLICATIONS

- Logical comparators
- Adders/subtractors
- Parity generators and checkers

## ABSOLUTE MAXIMUM RATINGS

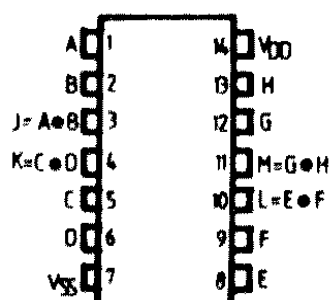
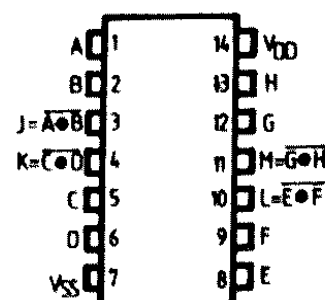
$V_{DD}^*$	Supply voltage: G and H types	-0.5 to 20	V
	E and F types	-0.5 to 18	V
$V_i$	Input voltage	-0.5 to $V_{DD}+0.5$	V
$I_i$	DC input current (any one input)	$\pm 10$	mA
$P_{tot}$	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for $T_A$ = full package-temperature range	100	mW
$T_A$	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C
$T_{stg}$	Storage temperature	-65 to 150	°C

\* All voltage values are referred to  $V_{SS}$  pin voltage

## RECOMMENDED OPERATING CONDITIONS

$V_{DD}^*$	Supply voltage: G and H types	3 to 18	V
	E and F types	3 to 15	V
$V_i$	Input voltage	0 to $V_{DD}$	V
$T_A$	Operating temperature: G and H types	-55 to 125	°C
	E and F types	-40 to 85	°C

## CONNECTION DIAGRAMS

**MMC 4070****MMC 4077**

**STATIC ELECTRICAL CHARACTERISTICS**

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNI
			V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   (μA)	V <sub>DD</sub> (V)	T <sub>LOW</sub>		25°C			T <sub>HIGH</sub>		
							min.	max.	min.	typ	max.	min.	max.	
I <sub>L</sub>	Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
	E, F types	0/ 5			5		4		0.02	4		30		
		0/10			10		8		0.02	8		60		
			0/15			15		16		0.02	16		120	
V <sub>OH</sub>	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V <sub>OL</sub>	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V <sub>IH</sub>	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V <sub>IL</sub>	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I <sub>OH</sub>	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
	E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1			
		0/ 5	4.6		5	-0.52		-0.44	-1		-0.36			
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9			
		0/15	13.5		15	-3.6		-3.0	-6.8		-2.4			
I <sub>OL</sub>	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36			
		0/10	0.5		10	1.3		1.1	2.6		0.9			
		0/15	1.5		15	3.6		3.0	6.8		2.4			
I <sub>IH</sub> I <sub>IL</sub>	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 <sup>-5</sup>	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10 <sup>-5</sup>	±0.3		±1	
C <sub>I</sub>	Input capacitance			Any input						5	7.5			pf

\* T<sub>LOW</sub> = -55°C for G, H devices; -40°C for E, F devices.\* T<sub>HIGH</sub> = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V<sub>DD</sub> = 5 V2 V min. with V<sub>DD</sub> = 10 V2.5 V min. with V<sub>DD</sub> = 15 V

**DYNAMIC ELECTRICAL CHARACTERISTICS**

$T = 25^{\circ}\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$ , typical temperature coefficient for all  $V_{DD}$  values is  $0.3\%/^{\circ}\text{C}$ , all input rise and fall times =  $20\text{ ns}$

PARAMETER	TEST CONDITIONS		VALUES			UNIT
		$V_{CC}(\text{V})$	MIN.	TYP.	MAX.	
$t_{PHL}$ Propagation delay time $t_{PLH}$		5		140	280	ns
		10		85	130	
		15		50	100	
$t_{HL}$ Transition time $t_{LH}$		5		100	200	ns
		10		50	100	
		15		40	80	

**TRUTH TABLE**

(of 4 gates)

4070

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

here 1 = High level  
0 = Low level  
 $J = A \oplus B$

4077

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

here 1 = High level  
0 = Low level  
 $J = A \ominus B$

**FUNCTIONAL DIAGRAM**