

# SYNCHRONOUS DRAM

**MT48LC8M16LFFF – 2 MEG x 16 x 4 BANKS**  
**MT48G8M16LFFF – 2 MEG x 16 x 4 BANKS**  
**MT48V8M16LFFF – 2 MEG x 16 x 4 BANKS**

*This data sheet is an addendum. The complete 128Mb Mobile SDRAM data sheet is at: <http://www.micron.com/products/datasheet.jsp?path=/DRAM/Mobile&fileID=581>*

## Features

- Temperature Compensated Self Refresh (TCSR)
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT auto precharge, and Auto Refresh Modes
- Self Refresh Mode; standard and low power
- 64ms, 4,096-cycle refresh
- LVTTTL-compatible inputs and outputs
- Low voltage power supply
- Partial Array Self Refresh power-saving mode
- Extended mode register (must be programmed)

## OPTIONS

- VDD/VDDQ  
3.3V  
3.0V  
2.5V/2.5V-1.8V
- Configurations  
8 Meg x 16 (2 Meg x 16 x 4 banks)
- Self Refresh  
Supported  
Not Supported
- Package/Ball out  
Plastic Package  
54-ball FBGA (8mm x 9mm)  
54-ball FBGA (8mm x 9mm)
- Timing (Cycle Time)  
8ns @ CL = 3 (125 MHz)  
10ns @ CL = 3 (100 MHz)
- Operating Temperature Range  
Mobile (-25°C to +75°C)  
Industrial (-40°C to +85°C)

## MARKING

LC  
G<sup>1</sup>  
V

8M16

LF  
LX

FF  
BF<sup>2</sup>

-8  
-10

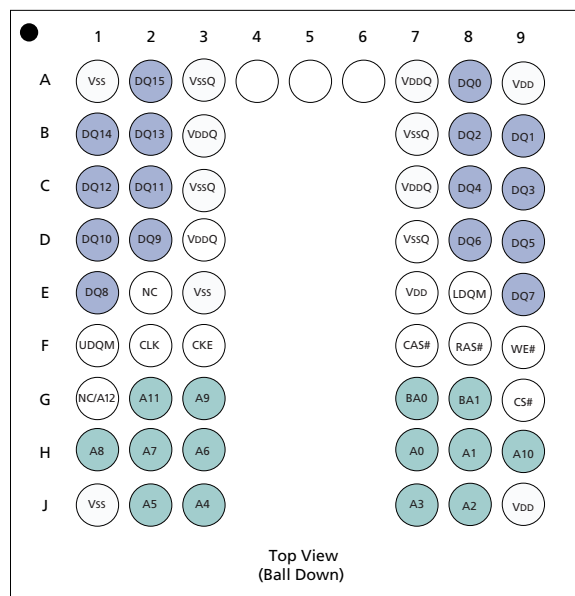
XT  
IT

NOTE: 1. IT supported only in LX version.  
2. Lead-free.

*Part Number Example:*

**MT48G8M16LFFF-8 XT**

**Figure 1: 54-Ball FBGA Pin Assignment (Top View)**



**Table 1: Address Table**

|                   | 8 MEG x16            |
|-------------------|----------------------|
| Configuration     | 2 Meg x 16 x 4 banks |
| Refresh Count     | 4K                   |
| Row Addressing    | 4K (A0–A11)          |
| Bank Addressing   | 4 (BA0, BA1)         |
| Column Addressing | 512 (A0–A8)          |

**Table 2: Key Timing Parameters**

Maximums, based on <sup>t</sup>CK; CL = CAS (READ) latency

| SPEED GRADE | CLOCK FREQUENCY | ACCESS TIME |        |        | <sup>t</sup> RCD | <sup>t</sup> RP |
|-------------|-----------------|-------------|--------|--------|------------------|-----------------|
|             |                 | CL = 1      | CL = 2 | CL = 3 |                  |                 |
| -8          | 125 MHz         | –           | –      | 6ns    | 20ns             | 20ns            |
| -10         | 100 MHz         | –           | –      | 6ns    | 20ns             | 20ns            |
| -8          | 100 MHz         | –           | 7ns    | –      | 20ns             | 20ns            |
| -10         | 83 MHz          | –           | 7ns    | –      | 20ns             | 20ns            |
| -8          | 50 MHz          | 18ns        | –      | –      | 20ns             | 20ns            |
| -10         | 40 MHz          | 18ns        | –      | –      | 20ns             | 20ns            |


**Table 3: 128Mb SDRAM Part Numbers**

| PART NUMBER       | V <sub>DD</sub> /V <sub>DDQ</sub> | ARCHITECTURE | PACKAGE                   |
|-------------------|-----------------------------------|--------------|---------------------------|
| MT48LC8M16LFFF-xx | 3.3V / 3.3V                       | 8 Meg x 16   | 54-BALL FBGA              |
| MT48LC8M16LFBF-xx | 3.3V / 3.3V                       | 8 Meg x 16   | 54-BALL FBGA <sup>1</sup> |
| MT48G8M16LFFF-xx  | 3.0V / 3.0V                       | 8 Meg x 16   | 54-BALL FBGA              |
| MT48G8M16LFBF-xx  | 3.0V / 3.0V                       | 8 Meg x 16   | 54-BALL FBGA <sup>1</sup> |
| MT48G8M16LXFF-xx  | 3.0V / 3.0V                       | 8 Meg x 16   | 54-BALL FBGA              |
| MT48G8M16LXBF-xx  | 3.0V / 3.0V                       | 8 Meg x 16   | 54-BALL FBGA <sup>1</sup> |
| MT48V8M16LFFF-xx  | 2.5V / 2.5V-1.8V                  | 8 Meg x 16   | 54-BALL FBGA              |
| MT48V8M16LFBF-xx  | 2.5V / 2.5V-1.8V                  | 8 Meg x 16   | 54-BALL FBGA <sup>1</sup> |

NOTE:

1. Lead-free package.

## General Description

The Micron® 128Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11(x16) select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 128Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 128Mb SDRAM is designed to operate in 3.3V or 3.0V or 2.5V low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

**Table 4: Ball Descriptions**

| 54-BALL FBGA   | SYMBOL           | TYPE   | DESCRIPTION   |
|--|------------------|--------|---|
| F2   | CLK              | Input  | Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.  |
| F3   | CKE              | Input  | Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH. |
| G9   | CS#              | Input  | Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.   |
| F7, F8, F9   | CAS#, RAS#, WE#  | Input  | Command Inputs: CAS#, RAS#, and WE# (along with CS#) define the command being entered.  |
| E8, F1   | LDQM, UDQM       | Input  | Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. LDQM corresponds to DQ0–DQ7, UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM.  |
| G7, G8   | BA0, BA1         | Input  | Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. These pins also provide the op-code during a LOAD MODE REGISTER command  |
| H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2                 | A0–A11           | Input  | Address Inputs: A0–A11 are sampled during the ACTIVE command (row- address A0–A11) and READ/WRITE command (column-address A0–A8; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.  |
| A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2 | DQ0–DQ15         | I/O    | Data Input/Output: Data bus   |
| E2, G1   | NC               | –      | No Connect: These pins should be left unconnected. G1 is a no connect for this part but may be used as A12 in future designs.   |
| A7, B3, C7, D3   | V <sub>DDQ</sub> | Supply | DQ Power: Provide isolated power to DQs for improved noise immunity.  |
| A3, B7, C3, D7,  | V <sub>SSQ</sub> | Supply | DQ Ground: Provide isolated ground to DQs for improved noise immunity.  |
| A9, E7, J9   | V <sub>DD</sub>  | Supply | Power Supply: Voltage dependant on option.  |
| A1, E3, J1   | V <sub>SS</sub>  | Supply | Ground.   |

**Absolute Maximum Ratings**

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the opera-

tional sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 5: Absolute Maximum Ratings Table**

| PARAMETER/CONDITION                                 |                                       | MIN  | MAX  | UNITS |
|---|---------------------------------------|------|------|-------|
| Voltage on V <sub>DD</sub> /V <sub>DDQ</sub> Supply | Relative to V <sub>SS</sub> (3.3V)    | -1   | +4.6 | V     |
|   | Relative to V <sub>SS</sub> (3.0V)    | -1   | +4.6 | V     |
|   | Relative to V <sub>SS</sub> (2.5V)    | -0.5 | +3.6 | V     |
| Voltage on Inputs, NC or I/O Pins                   | Relative to V <sub>SS</sub> (3.3V)    | -1   | +4.6 | V     |
|   | Relative to V <sub>SS</sub> (3.0V)    | -1   | +4.6 | V     |
|   | Relative to V <sub>SS</sub> (2.5V)    | -0.5 | +3.6 | V     |
| Operating Temperature                               | T <sub>A</sub> (Mobile; XT parts)     | -25  | +75  | °C    |
|   | T <sub>A</sub> (Industrial; IT parts) | -40  | +85  | °C    |
| Storage Temperature (plastic)                       | –                                     | -55  | +150 | °C    |
| Power Dissipation                                   | –                                     | –    | 1    | W     |

**Table 6: DC Electrical Characteristics and Operating Conditions – LC Version**

Notes appear on standard 128Mb Mobile SDRAM data sheet; V<sub>DD</sub>/V<sub>DDQ</sub> = +3.3V ±0.3V

| PARAMETER/CONDITION  | SYMBOL           | MIN  | MAX                   | UNITS | NOTES |
|--|------------------|------|-----------------------|-------|-------|
| Supply Voltage   | V <sub>DD</sub>  | 3    | 3.6                   | V     |       |
| I/O Supply Voltage   | V <sub>DDQ</sub> | 3    | 3.6                   | V     |       |
| Input High Voltage: Logic 1; All inputs  | V <sub>IH</sub>  | 2    | V <sub>DD</sub> + 0.3 | V     | 22    |
| Input Low Voltage: Logic 0; All inputs   | V <sub>IL</sub>  | -0.3 | 0.8                   | V     | 22    |
| Data Output High Voltage: Logic 1; All inputs  | V <sub>OH</sub>  | 2.4  | –                     | V     |       |
| Data Output LOW Voltage: LOGIC 0; All inputs   | V <sub>OL</sub>  | –    | 0.4                   | V     |       |
| Input Leakage Current: Any Input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> (All other pins not under test = 0V) | I <sub>I</sub>   | -5   | 5                     | μA    |       |
| Output Leakage Current: DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>                           | I <sub>OZ</sub>  | -5   | 5                     | μA    |       |

**Table 7: DC Electrical Characteristics and Operating Conditions – G Version**

Notes appear on standard 128Mb Mobile SDRAM data sheet; V<sub>DD</sub>/V<sub>DDQ</sub> = +3.0V ±0.4V

| PARAMETER/CONDITION  | SYMBOL           | MIN  | MAX                   | UNITS | NOTES |
|--|------------------|------|-----------------------|-------|-------|
| Supply Voltage   | V <sub>DD</sub>  | 2.6  | 3.4                   | V     |       |
| I/O Supply Voltage   | V <sub>DDQ</sub> | 2.6  | 3.4                   | V     |       |
| Input High Voltage: Logic 1; All inputs  | V <sub>IH</sub>  | 2.0  | V <sub>DD</sub> + 0.3 | V     | 22    |
| Input Low Voltage: Logic 0; All inputs   | V <sub>IL</sub>  | -0.3 | 0.8                   | V     | 22    |
| Data Output High Voltage: Logic 1; All inputs  | V <sub>OH</sub>  | 2.4  | –                     | V     |       |
| Data Output Low Voltage: LOGIC 0; All inputs   | V <sub>OL</sub>  | –    | 0.4                   | V     |       |
| Input Leakage Current: Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> (All other pins not under test = 0V) | I <sub>I</sub>   | -5   | 5                     | μA    |       |
| Output Leakage Current: DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>                           | I <sub>OZ</sub>  | -5   | 5                     | μA    |       |


**Table 8: DC Electrical Characteristics and Operating Conditions – V Version**

Notes appear on standard 128Mb Mobile SDRAM data sheet;  $V_{DD} = 2.5 \pm 0.2V$ ,  $V_{DDQ} = +2.5V \pm 0.2V$  or  $+1.8V \pm 0.15V$

| PARAMETER/CONDITION  | SYMBOL    | MIN             | MAX            | UNITS   | NOTES |
|--|-----------|-----------------|----------------|---------|-------|
| Supply Voltage   | $V_{DD}$  | 2.3             | 2.7            | V       |       |
| I/O Supply Voltage   | $V_{DDQ}$ | 1.65            | 2.7            | V       |       |
| Input High Voltage: Logic 1; All inputs  | $V_{IH}$  | 1.25            | $V_{DD} + 0.3$ | V       | 22    |
| Input Low Voltage: Logic 0; All inputs   | $V_{IL}$  | -0.3            | +0.55          | V       | 22    |
| Data Output High Voltage: Logic 1; All inputs  | $V_{OH}$  | $V_{DDQ} - 0.2$ | –              | V       |       |
| Data Output Low Voltage: LOGIC 0; All inputs   | $V_{OL}$  | –               | 0.2            | V       |       |
| Input Leakage Current: Any input $0V \leq V_{IN} \leq V_{DD}$ (All other pins not under test = 0V) | $I_{II}$  | -5              | 5              | $\mu A$ |       |
| Output Leakage Current: DQs are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$                           | $I_{OZ}$  | -5              | 5              | $\mu A$ |       |

**Table 9: AC Electrical Characteristics and Operating Conditions**

$V_{DD} = +3.3V \pm 0.3V$  or  $+3.0V \pm 0.4V$  or  $+2.5V \pm 0.2V$

| PARAMETER/CONDITION                     | SYMBOL   | MIN | MAX | UNITS | NOTES |
|---|----------|-----|-----|-------|-------|
| Input High Voltage: Logic 1; All inputs | $V_{IH}$ | 1.4 | –   | V     |       |
| Input Low Voltage: Logic 0; All inputs  | $V_{IL}$ | –   | 0.4 | V     |       |



**Table 10: Electrical Characteristics and Recommended AC Operating Conditions**

Notes appear on standard 128Mb Mobile SDRAM data sheet

| AC CHARACTERISTICS                     |                       |                | -8          |         | -10         |         | UNITS | NOTES |
|--|-----------------------|----------------|-------------|---------|-------------|---------|-------|-------|
| PARAMETER                              |                       | SYMBOL         | MIN         | MAX     | MIN         | MAX     |       |       |
| Access time from CLK (pos. edge)       | CL = 3                | $t_{AC}^{(3)}$ |             | 6       |             | 6       | ns    | 27    |
|  | CL = 2                | $t_{AC}^{(2)}$ |             | 7       |             | 7       | ns    |       |
|  | CL = 1                | $t_{AC}^{(1)}$ |             | 18      |             | 18      | ns    |       |
| Address hold time                      |                       | $t_{AH}$       | 1           |         | 1           |         | ns    |       |
| Address setup time                     |                       | $t_{AS}$       | 2.5         |         | 2.5         |         | ns    |       |
| CLK high-level width                   |                       | $t_{CH}$       | 3           |         | 3           |         | ns    |       |
| CLK low-level width                    |                       | $t_{CL}$       | 3           |         | 3           |         | ns    |       |
| Clock cycle time                       | CL = 3                | $t_{CK}^{(3)}$ | 8           |         | 10          |         | ns    | 23    |
|  | CL = 2                | $t_{CK}^{(2)}$ | 10          |         | 12          |         | ns    | 23    |
|  | CL = 1                | $t_{CK}^{(1)}$ | 20          |         | 25          |         | ns    | 23    |
| CKE hold time                          |                       | $t_{CKH}$      | 1           |         | 1           |         | ns    |       |
| CKE setup time                         |                       | $t_{CKS}$      | 2.5         |         | 2.5         |         | ns    |       |
| CS#, RAS#, CAS#, WE#, DQM hold time    |                       | $t_{CMH}$      | 1           |         | 1           |         | ns    |       |
| CS#, RAS#, CAS#, WE#, DQM setup time   |                       | $t_{CMS}$      | 2.5         |         | 2.5         |         | ns    |       |
| Data-in hold time                      |                       | $t_{DH}$       | 1           |         | 1           |         | ns    |       |
| Data-in setup time                     |                       | $t_{DS}$       | 2.5         |         | 2.5         |         | ns    |       |
| Data-out high-impedance time           | CL = 3                | $t_{HZ}^{(3)}$ |             | 6       |             | 6       | ns    | 10    |
|  | CL = 2                | $t_{HZ}^{(2)}$ |             | 8       |             | 8       | ns    | 10    |
|  | CL = 1                | $t_{HZ}^{(1)}$ |             | 18      |             | 18      | ns    | 10    |
| Data-out low-impedance time            |                       | $t_{LZ}$       | 1           |         | 1           |         | ns    |       |
| Data-out hold time (load)              |                       | $t_{OH}$       | 2.5         |         | 2.5         |         | ns    |       |
| Data-out hold time (no load)           |                       | $t_{OHN}$      | 1.8         |         | 1.8         |         | ns    | 28    |
| ACTIVE to PRECHARGE command            |                       | $t_{RAS}$      | 48          | 120,000 | 50          | 120,000 | ns    |       |
| ACTIVE to ACTIVE command period        |                       | $t_{RC}$       | 80          |         | 100         |         | ns    |       |
| ACTIVE to READ or WRITE delay          |                       | $t_{RCD}$      | 20          |         | 20          |         | ns    |       |
| Refresh period (4,096 rows)            |                       | $t_{REF}$      |             | 64      |             | 64      | ms    |       |
| AUTO REFRESH period                    |                       | $t_{RFC}$      | 80          |         | 100         |         | ns    |       |
| PRECHARGE command period               |                       | $t_{RP}$       | 20          |         | 20          |         | ns    |       |
| ACTIVE bank a to ACTIVE bank b command |                       | $t_{RRD}$      | 20          |         | 20          |         | ns    |       |
| Transition time                        |                       | $t_T$          | 0.5         | 1.2     | 0.5         | 1.2     | ns    | 7     |
| WRITE recovery time                    | Auto precharge mode   | $t_{WR}^{(a)}$ | 1 CLK + 7ns |         | 1 CLK + 5ns |         | –     | 24    |
|  | Manual precharge mode | $t_{WR}^{(m)}$ | 15          |         | 15          |         | ns    | 25    |
| Exit SELF REFRESH to ACTIVE command    |                       | $t_{XSR}$      | 80          |         | 100         |         | ns    | 20    |



**Table 11: AC Functional Characteristics**

Notes appear on standard 128Mb Mobile SDRAM data sheet

| PARAMETER   |        | SYMBOL       | -8 | -10 | UNITS    | NOTES  |
|---|--------|--------------|----|-----|----------|--------|
| READ/WRITE command to READ/WRITE command                |        | $t_{CCD}$    | 1  | 1   | $t_{CK}$ | 17     |
| CKE to clock disable or power-down entry mode           |        | $t_{CKED}$   | 1  | 1   | $t_{CK}$ | 14     |
| CKE to clock enable or power-down exit setup mode       |        | $t_{PED}$    | 1  | 1   | $t_{CK}$ | 14     |
| DQM to input data delay                                 |        | $t_{DQD}$    | 0  | 0   | $t_{CK}$ | 17     |
| DQM to data mask during WRITES                          |        | $t_{DQM}$    | 0  | 0   | $t_{CK}$ | 17     |
| DQM to data high-impedance during READs                 |        | $t_{DQZ}$    | 2  | 2   | $t_{CK}$ | 17     |
| WRITE command to input data delay                       |        | $t_{DWD}$    | 0  | 0   | $t_{CK}$ | 17     |
| Data-in to ACTIVE command                               |        | $t_{DAL}$    | 5  | 5   | $t_{CK}$ | 15, 21 |
| Data-in to PRECHARGE command                            |        | $t_{DPL}$    | 2  | 2   | $t_{CK}$ | 16, 21 |
| Last data-in to burst STOP command                      |        | $t_{BDL}$    | 1  | 1   | $t_{CK}$ | 17     |
| Last data-in to new READ/WRITE command                  |        | $t_{CDL}$    | 1  | 1   | $t_{CK}$ | 17     |
| Last data-in to PRECHARGE command                       |        | $t_{RDL}$    | 2  | 2   | $t_{CK}$ | 16, 21 |
| LOAD MODE REGISTER command to ACTIVE or REFRESH command |        | $t_{MRD}$    | 2  | 2   | $t_{CK}$ | 26     |
| Data-out to high-impedance from PRECHARGE command       | CL = 3 | $t_{ROH(3)}$ | 3  | 3   | $t_{CK}$ | 17     |
|   | CL = 2 | $t_{ROH(2)}$ | 2  | 2   | $t_{CK}$ | 17     |
|   | CL = 1 | $t_{ROH(1)}$ | 1  | 1   | $t_{CK}$ | 17     |

**Table 12: IDD Specifications and Conditions – x16**

Notes appear on standard 128Mb Mobile SDRAM data sheet;  $V_{DD} = +3.3V \pm 0.3V$  or  $+3.0V \pm 0.4V$  or  $+2.5V \pm 0.2V$

| PARAMETER/CONDITION   |                                 | SYMBOL    | -8  | -10 | UNITS         | NOTES                    |
|---|---------------------------------|-----------|-----|-----|---------------|--------------------------|
| Operating Current: Active Mode;<br>Burst = 2; READ or WRITE; $t_{RC} = t_{RC}(\text{MIN})$                                |                                 | $I_{DD1}$ | 130 | 100 | mA            | 3, 18,<br>19, 32         |
| Standby Current: Power-Down Mode;<br>All banks idle; CKE = LOW  |                                 | $I_{DD2}$ | 350 | 350 | $\mu\text{A}$ | 32                       |
| Standby Current: Active Mode;<br>CKE = HIGH; CS# = HIGH; All banks active after $t_{RCD}$ met;<br>No accesses in progress |                                 | $I_{DD3}$ | 35  | 30  | mA            | 3, 12,<br>19, 32         |
| Operating Current: Burst Mode; Continuous burst;<br>READ or WRITE; All banks active                                       |                                 | $I_{DD4}$ | 100 | 95  | mA            | 3, 18,<br>19, 32         |
| Auto Refresh Current<br>CKE = HIGH; CS# = HIGH  | $t_{RFC} = t_{RFC}(\text{MIN})$ | $I_{DD5}$ | 210 | 170 | mA            | 3, 12, 18, 19,<br>32, 33 |
|   | $t_{RFC} = 15.625\mu\text{s}$   | $I_{DD6}$ | 3   | 3   | mA            |                          |


**Table 13: I<sub>DD7</sub> – Self Refresh Current Options – x16 (IT Only)**

Notes appear on standard 128Mb Mobile SDRAM data sheet; V<sub>DD</sub> = +3.3V ±0.3V or +3.0V ±0.4V or +2.5V±0.2V

| TEMPERATURE COMPENSATED SELF REFRESH | MAX TEMPERATURE | -8 AND -10 | UNITS | NOTES |
|--------------------------------------|-----------------|------------|-------|-------|
| PARAMETER/CONDITION                  |                 |            |       |       |
| Self Refresh Current:<br>CKE < 0.2V  | 85°C            | 800        | μA    | 4     |
|                                      | 70°C            | 500        | μA    | 4     |
|                                      | 45°C            | 350        | μA    | 4     |
|                                      | 15°C            | 300        | μA    | 4     |

**Table 14: Capacitance**

Notes appear on standard 128Mb Mobile SDRAM data sheet

| PARAMETER                                    | SYMBOL          | MIN | MAX | UNITS | NOTES |
|--|-----------------|-----|-----|-------|-------|
| Input Capacitance: CLK                       | C <sub>I1</sub> | 2.0 | 4.0 | pF    | 29    |
| Input Capacitance: All other input-only pins | C <sub>I2</sub> | 2.0 | 5.0 | pF    | 30    |
| Input/Output Capacitance: DQs                | C <sub>IO</sub> | 3.5 | 6.0 | pF    | 31    |



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