



8 MEG x 36, 16 MEG x 18, 32 MEG x 9
2.5V V_{EXT}, 1.8V V_{DD}, HSTL, RLD RAM II

288Mb CIO REDUCED LATENCY (RLDRAM II)

MT49H8M36
MT49H16M18
MT49H32M9

FEATURES

- 288Mb
- 400 MHz DDR operation (800 Mb/s/pin data rate)
- Organization
 - 8 Meg x 36, 16 Meg x 18, 32 Meg x 9
 - 8 banks
- Cyclic bank switching for maximum bandwidth
- Reduced cycle time (20ns at 400 MHz)
- Nonmultiplexed addresses (address multiplexing option available)
- SRAM-type interface
- Programmable read latency (RL), row cycle time, and burst sequence length
- Balanced read and write latencies in order to optimize data bus utilization
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Differential input data clocks (DKx, DKx#)
- On-chip DLL generates CK edge-aligned data and output data clock signals
- Data valid signal (QVLD)
- 32ms refresh (8K refresh for each bank; 64k refresh command must be issued in total each 32ms)
- 144-ball FBGA package
- HSTL I/O (1.5V or 1.8V nominal)
- 25 ohm–60 ohm matched impedance outputs
- 2.5V V_{EXT}, 1.8V V_{DD}, 1.5V or 1.8V V_{DDQ} I/O
- On-die termination (ODT) R_{TT}

OPTIONS

- Clock Cycle Timing
 - 2.5ns (400 MHz)
 - 3.3ns (300 MHz)
 - 5ns (200 MHz)

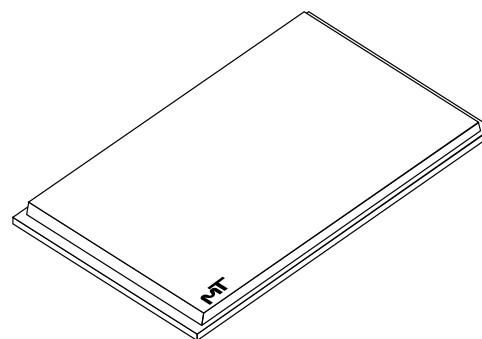
MARKING

MT49H8M36FM
MT49H16M18FM
MT49H32M9FM

- Package
 - 144-pin, 11mm x 18.5mm FBGA

FM

Figure 1
144-Ball FBGA



GENERAL DESCRIPTION

The Micron® 288Mb Reduced Latency DRAM (RLDRAM) is a high speed memory device designed for high bandwidth communication data storage. Applications include, but are not limited to, transmitting or receiving buffers in telecommunication systems and data or instruction cache applications requiring large amounts of memory. The chip's eight-bank architecture is optimized for high speed and achieves a peak bandwidth of 28.8 Gb/s, using a 36-bit interface and a maximum system clock of 400 MHz.

The double data rate (DDR) interface transfers two 36-, 18-, or 9-bit wide data word per clock cycle at the I/O pins. Output data is referenced to the free-running output data clock.

Commands, addresses, and control signals are registered at every positive edge of the differential input clock, while input data is registered at both positive and negative edges of the input data clock(s).

Read and write accesses to the RLD RAM are burst-oriented. The burst length is programmable from 2, 4, or 8¹ by setting the mode register.

The device is supplied with 2.5V and 1.8V for the core and 1.5V or 1.8V for the output drivers.

Bank-scheduled refresh is supported with row address generated internally.

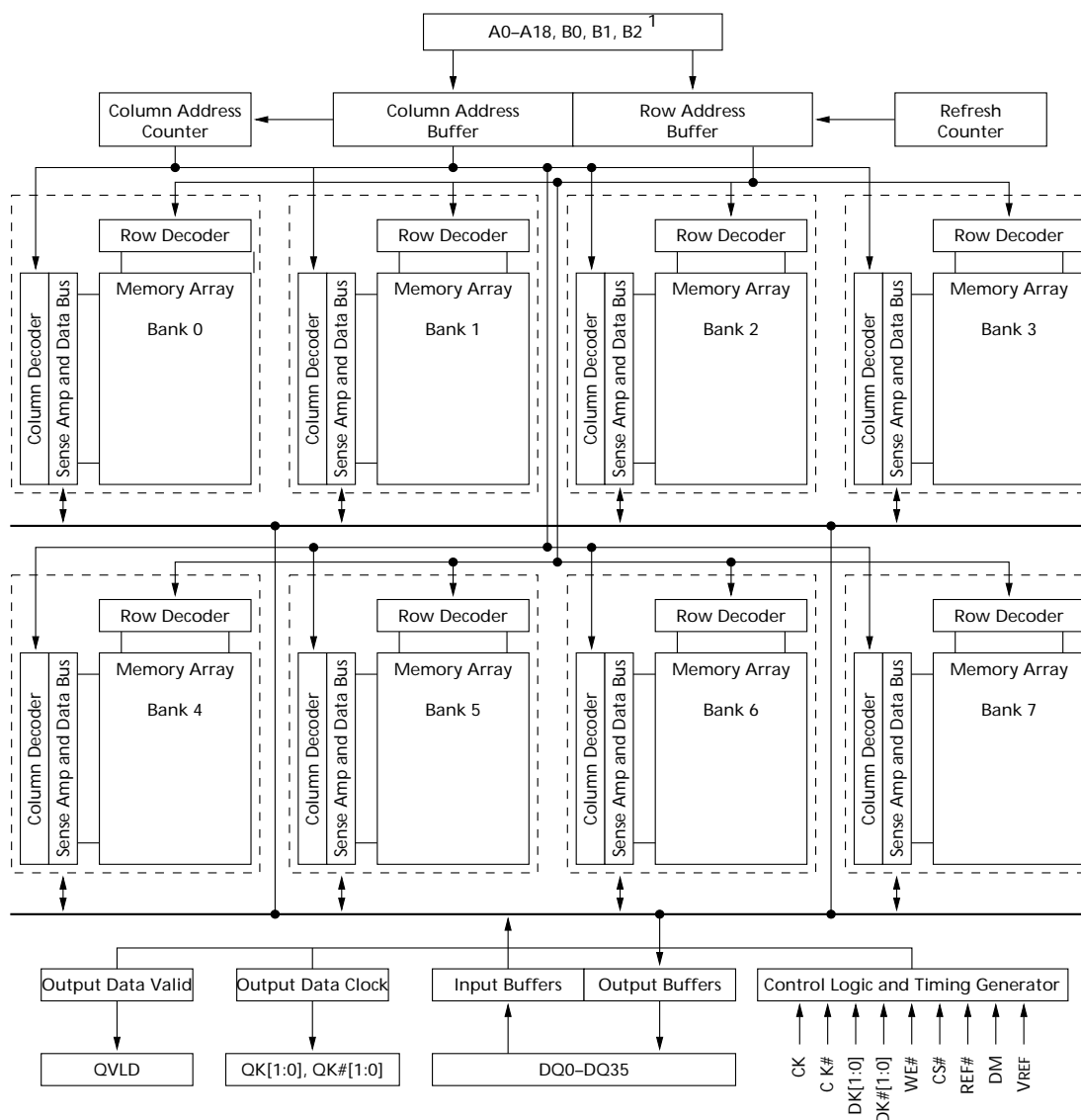
A standard FBGA 144-ball package is used to enable ultra high-speed data transfer rates and a simple upgrade path from former products.

NOTE: 1. Burst of 8 on x18 and x9 devices only.

Table 1: Valid Part Numbers

PART NUMBER	DESCRIPTION
MT49H8M36FM-xx	8 Meg x 36 RLD RAM II
MT49H16M18FM-xx	16 Meg x 18 RLD RAM II
MT49H32M9FM-xx	32 Meg x 9 RLD RAM II

Figure 2
Functional Block Diagram
8 Meg x 36



NOTE: 1. When the BL4 setting is used, A18 is a "Don't Care."



Figure 3
8 Meg x 36 Ball Assignment (Top View)
144-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V _{REF}	V _{SS}	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TMS	TCK
B	V _{DD}	DQ8	DQ9	V _{SSQ}					V _{SSQ}	DQ1	DQ0	V _{DD}
C	V _{TT}	DQ10	DQ11	V _{DDQ}					V _{DDQ}	DQ3	DQ2	V _{TT}
D	(A22) ¹	DQ12	DQ13	V _{SSQ}					V _{SSQ}	QK0#	QK0	V _{SS}
E	(A21) ²	DQ14	DQ15	V _{DDQ}					V _{DDQ}	DQ5	DQ4	(A20) ²
F	A5	DQ16	DQ17	V _{SSQ}					V _{SSQ}	DQ7	DQ6	QVLD
G	A8	A6	A7	V _{DD}					V _{DD}	A2	A1	A0
H	B2	A9	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A4	A3
J	DK0	DK0#	V _{DD}	V _{DD}					V _{DD}	V _{DD}	B0	CK
K	DK1	DK1#	V _{DD}	V _{DD}					V _{DD}	V _{DD}	B1	CK#
L	REF#	CS#	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A14	A13
M	WE#	A16	A17	V _{DD}					V _{DD}	A12	A11	A10
N	A18	DQ24	DQ25	V _{SSQ}					V _{SSQ}	DQ35	DQ34	(A19) ²
P	A15	DQ22	DQ23	V _{DDQ}					V _{DDQ}	DQ33	DQ32	DM
R	V _{SS}	QK1	QK1#	V _{SSQ}					V _{SSQ}	DQ31	DQ30	V _{SS}
T	V _{TT}	DQ20	DQ21	V _{DDQ}					V _{DDQ}	DQ29	DQ28	V _{TT}
U	V _{DD}	DQ18	DQ19	V _{SSQ}					V _{SSQ}	DQ27	DQ26	V _{DD}
V	V _{REF}	ZQ	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TDO	TDI

NOTE: 1. Reserved for future use. This may optionally be connected to GND.

2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.



Figure 4
16 Meg x 18 Ball Assignment (Top View)
144-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V _{REF}	V _{SS}	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TMS	TCK
B	V _{DD}	DNU ⁴	DQ4	V _{SSQ}					V _{SSQ}	DQ0	DNU ⁴	V _{DD}
C	V _{TT}	DNU ⁴	DQ5	V _{DDQ}					V _{DDQ}	DQ1	DNU ⁴	V _{TT}
D	(A22) ¹	DNU ⁴	DQ6	V _{SSQ}					V _{SSQ}	QK0#	QK0	V _{SS}
E	(A21) ²	DNU ⁴	DQ7	V _{DDQ}					V _{DDQ}	DQ2	DNU ⁴	(A20) ²
F	A5	DNU ⁴	DQ8	V _{SSQ}					V _{SSQ}	DQ3	DNU ⁴	QVLD
G	A8	A6	A7	V _{DD}					V _{DD}	A2	A1	A0
H	B2	A9	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A4	A3
J	NF ³	NF ³	V _{DD}	V _{DD}					V _{DD}	V _{DD}	B0	CK
K	DK	DK#	V _{DD}	V _{DD}					V _{DD}	V _{DD}	B1	CK#
L	REF#	CS#	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A14	A13
M	WE#	A16	A17	V _{DD}					V _{DD}	A12	A11	A10
N	A18	DNU ⁴	DQ14	V _{SSQ}					V _{SSQ}	DQ9	DNU ⁴	A19
P	A15	DNU ⁴	DQ15	V _{DDQ}					V _{DDQ}	DQ10	DNU ⁴	DM
R	V _{SS}	QK1	QK1#	V _{SSQ}					V _{SSQ}	DQ11	DNU ⁴	V _{SS}
T	V _{TT}	DNU ⁴	DQ16	V _{DDQ}					V _{DDQ}	DQ12	DNU ⁴	V _{TT}
U	V _{DD}	DNU ⁴	DQ17	V _{SSQ}					V _{SSQ}	DQ13	DNU ⁴	V _{DD}
V	V _{REF}	ZQ	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TDO	TDI

- NOTE:**
1. Reserved for future use. This may optionally be connected to GND.
 2. Reserved for future use. This signal is internally connected and has parasitic characteristics of an address input signal. This may optionally be connected to GND.
 3. No Function. This signal is internally connected and has parasitic characteristics of a clock input signal.
 4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND.



Figure 5
32 Meg x 9 Ball Assignment (Top View)
144-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	V _{REF}	V _{SS}	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TMS	TCK
B	V _{DD}	DNU ⁴	DNU ⁴	V _{SSQ}					V _{SSQ}	DQ0	DNU ⁴	V _{DD}
C	V _{TT}	DNU ⁴	DNU ⁴	V _{DDQ}					V _{DDQ}	DQ1	DNU ⁴	V _{TT}
D	(A22) ¹	DNU ⁴	DNU ⁴	V _{SSQ}					V _{SSQ}	QK0#	QK0	V _{SS}
E	(A21) ³	DNU ⁴	DNU ⁴	V _{DDQ}					V _{DDQ}	DQ2	DNU ⁴	A20
F	A5	DNU ⁴	DNU ⁴	V _{SSQ}					V _{SSQ}	DQ3	DNU ⁴	QVLD
G	A8	A6	A7	V _{DD}					V _{DD}	A2	A1	A0
H	B2	A9	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A4	A3
J	NF ²	NF ²	V _{DD}	V _{DD}					V _{DD}	V _{DD}	B0	CK
K	DK	DK#	V _{DD}	V _{DD}					V _{DD}	V _{DD}	B1	CK#
L	REF#	CS#	V _{SS}	V _{SS}					V _{SS}	V _{SS}	A14	A13
M	WE#	A16	A17	V _{DD}					V _{DD}	A12	A11	A10
N	A18	DNU ⁴	DNU ⁴	V _{SSQ}					V _{SSQ}	DQ4	DNU ⁴	A19
P	A15	DNU ⁴	DNU ⁴	V _{DDQ}					V _{DDQ}	DQ5	DNU ⁴	DM
R	V _{SS}	DNU ⁴	DNU ⁴	V _{SSQ}					V _{SSQ}	DQ6	DNU ⁴	V _{SS}
T	V _{TT}	DNU ⁴	DNU ⁴	V _{DDQ}					V _{DDQ}	DQ7	DNU ⁴	V _{TT}
U	V _{DD}	DNU ⁴	DNU ⁴	V _{SSQ}					V _{SSQ}	DQ8	DNU ⁴	V _{DD}
V	V _{REF}	ZQ	V _{EXT}	V _{SS}					V _{SS}	V _{EXT}	TDO	TDI

- NOTE:**
1. Reserved for future use. This signal is not connected.
 2. Reserved for future use. This signal is internally connected and has parasitic characteristics of a clock input signal.
 3. No Function. This signal is internally connected and has parasitic characteristics of a clock input signal.
 4. Do not use. This signal is internally connected and has parasitic characteristics of a I/O. This may optionally be connected to GND.


Table 2: Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
CK, CK#	Input	Input Clock: CK and CK# are differential clock inputs. Addresses and commands are latched on the rising edge of CK. CK# is ideally 180 degrees out of phase with CK.
CS#	Input	Chip Select: CS# enables the command decoder when low and disables it when high. When the command decoder is disabled, new commands are ignored, but internal operations continue.
WE#, REF#	Input	Command Inputs: Sampled at the positive edge of CK, WE#, and REF# define (together with CS#) the command to be executed.
A[0:20]	Input	Address Inputs: A[0:20] define the row and column addresses for READ and WRITE operations. During a MODE REGISTER SET, the address inputs define the register settings. They are sampled at the rising edge of CK. In the x36 configuration, A[20:19] are reserved for address expansion; in the x18 configuration, A[20] is reserved for address expansion. These expansion addresses can be treated as address inputs, but they do not affect the operation of the device.
A21	-	Reserved for future use. This signal is internally connected and can be treated as an address input.
A22	-	Reserved for future use. This signal is not connected and may be connected to ground.
BA[0:2]	Input	Bank Address Inputs: Select to which internal bank a command is being applied.
DQ0–DQ35	Input/ Output	Data Input/Output: The DQ signals form the 36-bit data bus. During READ commands, the data is referenced to both edges of QK. During WRITE commands, the data is sampled at both edges of DKx.
QKx, QKx#	Output	Output Data Clocks: QKx and QKx# are the opposite polarity output data clocks. During READs, they are transmitted by the RLD RAM and edge-aligned with data. QKx# is ideally 180 degrees out of phase with QKx. For the x36 device, QK0 and QK0# are aligned with DQ0–DQ17. QK1 and QK1# are aligned with DQ18–DQ35. For the x18 device, QK0 and QK0# are aligned with DQ0–DQ8. QK1 and QK1# are aligned with DQ9–DQ17. Consult the RLD RAM II design guide for more details.
DKx, DKx#	Input	Input Data Clock: DKx and DKx# are the differential input data clocks. All input data is referenced to both edges of DKx. DKx# is ideally 180 degrees out of phase with DKx. For the x36 device, DQ0–DQ17 are referenced to DK0 and DK0# and DQ18–DQ35 are referenced to DK1 and DK1#. For the x9 and x18 devices, all DQs are referenced to DK and DK#.
DM	Input	Input Data Mask: The DM signal is the input mask signal for WRITE data. Input data is masked when DM is sampled HIGH, along with the WRITE input data. DM is sampled on both edges of DK (DK1 for the x36 configuration).
QVLD	Output	Data Valid: The QVLD indicates valid output data. QVLD is edge-aligned with QKx and QKx#.
TMS TDI	Input	IEEE 1149.1 Test Inputs: JEDEC-standard 1.8V I/O levels. These pins may be left Not Connects if the JTAG function is not used in the circuit
TCK	Input	IEEE 1149.1 Clock Input: JEDEC-standard 1.8V I/O levels. This pin must be tied to V _{ss} if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 Test Output: JEDEC-standard 1.8V I/O level.
ZQ	Input/ Output	External Impedance [25–60Ω]: This signal is used to tune the device outputs to the system data bus impedance. DQ output impedance is set to 0.2 x RQ, where RQ is a resistor from this signal to ground. Connecting ZQ to GND invokes the minimum impedance mode. Connecting ZQ to V _{DD} invokes the maximum impedance mode. Refer to the Mode Register Bit Map to activate this function.


Table 2: Ball Descriptions (continued)

SYMBOL	TYPE	DESCRIPTION
V _{REF}	Input	Input Reference Voltage: Nominally V _{DDQ} /2. Provides a reference voltage for the input buffers.
V _{EXT}	Supply	Power Supply: 2.5V nominal. See DC Electrical Characteristics and Operating Conditions for range.
V _{DD}	Supply	Power Supply: 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range.
V _{DDQ}	Supply	Power Supply: Isolated Output Buffer Supply. Nominally, 1.5V or 1.8V. See DC Electrical Characteristics and Operating Conditions for range.
V _{SS}	Supply	Power Supply: GND.
V _{SSQ}	Supply	Power Supply: Isolated Output Buffer Supply. GND.
V _{TT}	Supply	Power Supply: Isolated Termination Supply. Nominally, V _{DDQ} /2. See DC Electrical Characteristics and Operating Conditions for range.
NF	–	No Function: These pins may be connected to ground.
DNU	–	Do Not Use: These pins may be connected to ground.



COMMANDS

According to the functional signal description, the following command sequences are possible. All input states or sequences not shown are illegal or reserved. All command and address inputs must meet setup and hold times around the rising edge of CK.

Table 3: Address Widths at Different Burst Lengths

BURST LENGTH	CONFIGURATION		
	x36	x18	x9
BL = 2	18:0	19:0	20:0
BL = 4	17:0	18:0	19:0
BL = 8	NA	17:0	18:0

Table 4: Command Table¹

OPERATION	CODE	CS#	WE#	REF#	A[20:0]	B[2:0]	NOTES
Device Deselect/No Operation	DESEL/NOP	H	X	X	X	X	
Mode Register Set	MRS	L	L	L	OPCODE	X	2
Read	READ	L	H	H	A	BA	3
Write	WRITE	L	L	H	A	BA	3
Auto Refresh	AREF	L	H	L	X	BA	

- NOTE:**
1. X represents a "Don't Care"; H represents a logic HIGH; L represents a logic LOW; A represents a valid address; and BA represents a valid bank address.
 2. Only A(17:0) are used for the MRS command.
 3. See above table; Address Widths at Different Burst Lengths.


Table 5: Description of Commands

COMMAND	DESCRIPTION
DESEL/NOP ¹	The NOP command is used to perform a no operation to the RLD RAM, which essentially deselects the chip. Use the NOP command to prevent unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. Output values depend on command history.
MRS	The mode register is set via the address inputs A(17:0). See the Mode Register Bit Map for further information. The MRS command can only be issued when all banks are idle and no bursts are in progress.
READ	The READ command is used to initiate a burst read access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(20:0) selects the data location within the bank.
WRITE	The WRITE command is used to initiate a burst write access to a bank. The value on the BA(2:0) inputs selects the bank, and the address provided on inputs A(20:0) selects the data location within the bank. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If the DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored (i.e., this part of the data word will not be written).
AREF	The AREF is used during normal operation of the RLD RAM to refresh the memory content of a bank. The command is nonpersistent, so it must be issued each time a refresh is required. The value on the BA(2:0) inputs selects the bank. The refresh address is generated by an internal refresh controller, effectively making each address bit a "Don't Care" during the AREF command. The RLD RAM requires 64K cycles at an average periodic interval of 0.49 μ s ² (MAX). To improve efficiency, eight AREF commands (one for each bank) can be posted to the RLD RAM at periodic intervals of 3.9 μ s ³ .

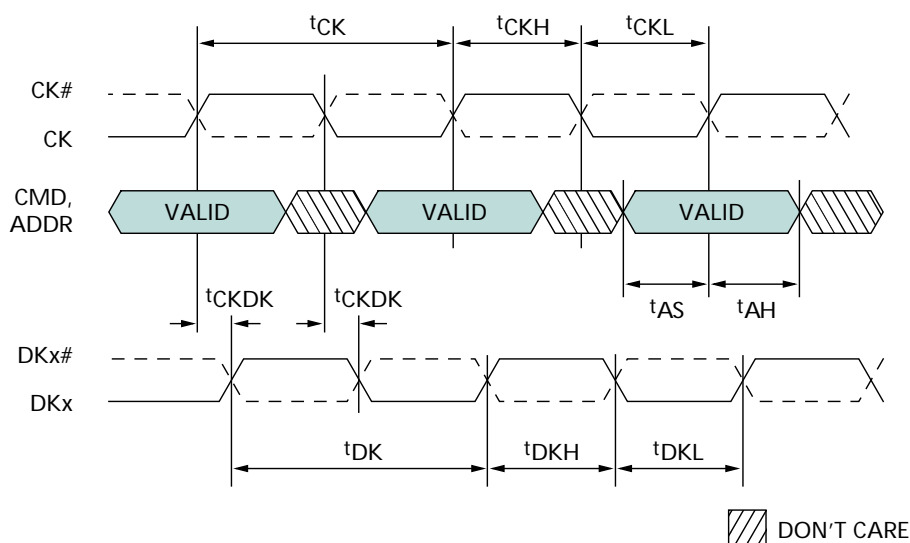
NOTE: 1. When the chip is deselected, internal NOP commands are generated and no commands are accepted.
2. Actual refresh is 32ms/8K/8 = 0.488 μ s.
3. Actual refresh is 32ms/8k = 3.90 μ s.

Table 6: AC Electrical Characteristics¹

DESCRIPTION	SYMBOL	-2.5		-3.3		-5		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock cycle time	^t CK, ^t DK	2.5	5.7	3.3	5.7	5.0	5.7	ns	
System frequency	^f CK, ^f DK	175	400	175	300	175	200	MHz	
Clock phase jitter	^t CKvar		0.30		0.30		0.30	ns	2
Clock HIGH time	^t CKH, ^t DKH	0.45	0.55	0.45	0.55	0.45	0.55	^t CK	
Clock LOW time	^t CKL, ^t DKL	0.45	0.55	0.45	0.55	0.45	0.55	^t CK	
Clock to input data clock	^t CKDK	-0.3	0.3	-0.3	0.3	-0.3	0.3	ns	
Mode register set cycle time to any command	^t MRSC	6		6		6		^t CK	
Setup Times									
Address/command and input setup time	^t AS/ ^t CS	0.4		0.5		0.8		ns	
Data-in and data mask to DK setup time	^t DS	0.25		0.3		0.4		ns	
Hold Times									
Address/command and input hold time	^t AH/ ^t CH	0.4		0.5		0.8		ns	
Data-in and data mask to DK hold time	^t DH	0.25		0.3		0.4		ns	
Data and Data Strobe									
Output data clock HIGH time	^t QKH	0.9	1.1	0.9	1.1	0.9	1.1	^t CKH	
Output data clock LOW time	^t QKL	0.9	1.1	0.9	1.1	0.9	1.1	^t CKL	
QK edge to clock edge skew	^t CKQK	-0.25	0.25	-0.3	0.3	-0.5	0.5	ns	
QK edge to output data edge	^t QKQ0, ^t QKQ1	-0.2	0.2	-0.25	0.25	-0.3	0.3	ns	3
QK edge to any output data edge	^t QKQ	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns	4
QK edge to data out High-Z	^t QKHZ		0.2		0.25		0.3	ns	
QK edge to QVLD	^t QKVLD	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns	

- NOTE:** 1. All timing parameters are measured relative to the crossing point of CK/CK#, DK/DK# and to the crossing point with V_{REF} of the command, address, and data signals.
2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
3. t_{QKQ0} is referenced to Q0-Q17 in x36 and Q0-Q8 in x18.
 t_{QKQ1} is referenced to Q18-Q35 in x36 and Q9-Q17 in x18.
4. t_{QKQ} takes into account the skew between any QKx and any Q.

FIGURE 6
Clock/Input Data Clock Command/Address Timings



INITIALIZATION

The RLD RAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operations or permanent damage to the device.

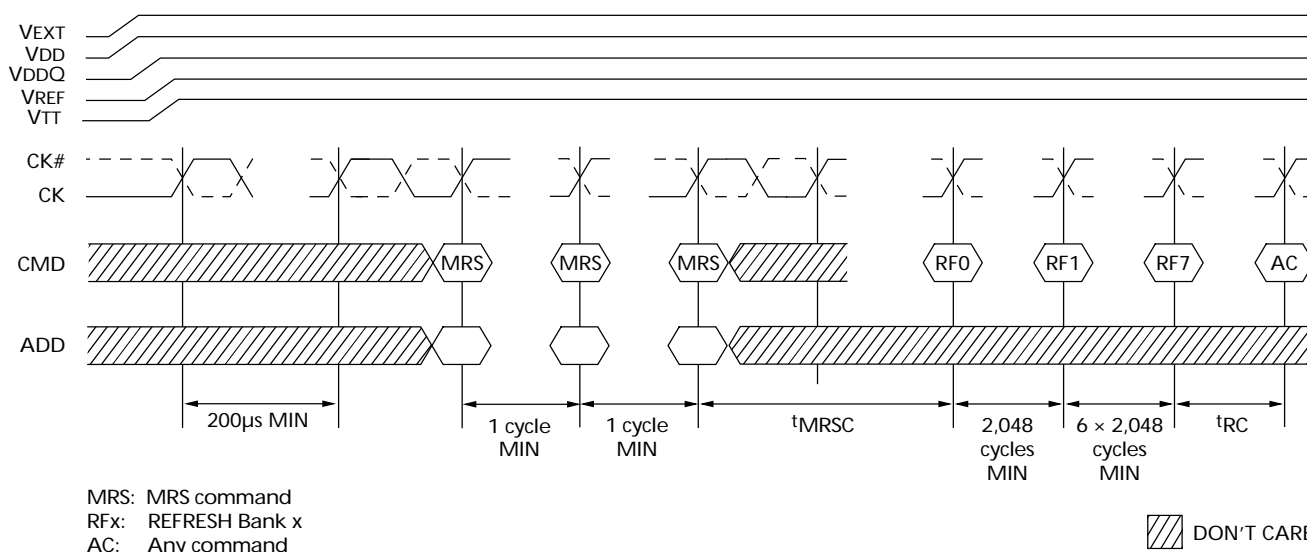
THE FOLLOWING SEQUENCE IS USED FOR POWER-UP:

1. Apply power (V_{EXT}, V_{DD}, V_{DDQ}, V_{REF}, V_{TT}) and start clock as soon as the supply voltages are stable.
Apply V_{DD} and V_{EXT} before or at the same time as V_{DDQ}. Apply V_{DDQ} before or at the same time as V_{REF} and V_{TT}. Although there is no timing relation

between V_{EXT} and V_{DD}, the chip starts the power-up sequence only after both voltages are at their nominal levels. The pad supply must not be applied before the core supplies. Maintain all remaining pins in NOP conditions.

2. Maintain stable conditions for 200μs (MIN).
3. Issue three MODE REGISTER Set commands: two dummies plus one valid MRS.
4. ^tMRSC after the valid MRS, issue eight AUTO REFRESH commands, one on each bank and separated by 2,048 cycles. Initial bank refresh order does not matter.
5. After ^tRC, the chip is ready for normal operation.

**Figure 7
Power-Up Sequence**



PROGRAMMABLE IMPEDANCE OUTPUT BUFFER

The RLD RAM II is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (R_Q) is connected between the ZQ pin and V_{ss}. The value of the resistor must be five times the desired impedance. For example, a 300Ω resistor is required for an output impedance of 60Ω. To ensure that output impedance is one fifth the value of R_Q (within 15 percent), the range of R_Q is 125Ω to 300Ω.

Output impedance updates may be required because, over time, variations may occur in supply voltage and

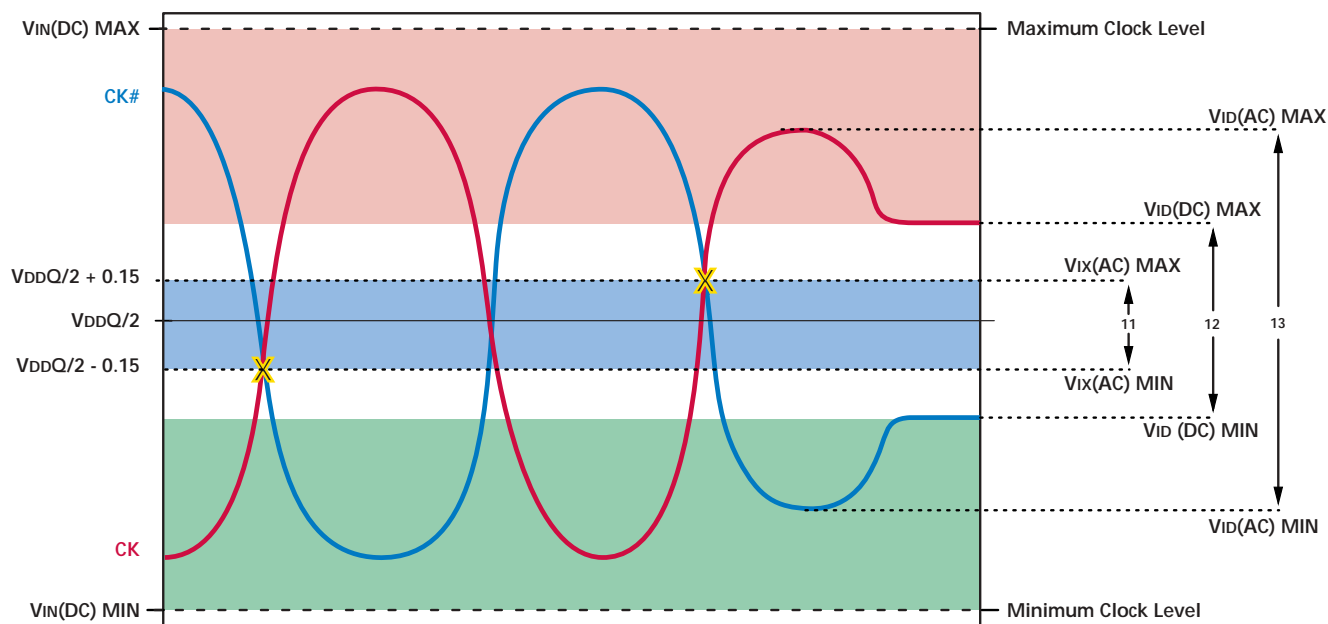
temperature. The device samples the value of R_Q. An impedance update is transparent to the system and does not affect device operation. All data sheet timing and current specifications are met during an update.

CLOCK CONSIDERATIONS

The RLD RAM II utilizes internal delay-locked loops for maximum output, data valid windows. It can be placed into a stopped-clock state to minimize power with a modest restart time of 1,024 cycles. Circuitry automatically resets the DLL when the absence of an input clock is detected.

Table 7: Clock Input Operating Conditions¹⁻⁸

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Clock Input Voltage Level; CK and CK#	V _{IN(DC)}	-0.3	V _{DDQ} + 0.3	V	
Clock Input Differential Voltage; CK and CK#	V _{ID(DC)}	0.2	V _{DDQ} + 0.6	V	9
Clock Input Differential Voltage; CK and CK#	V _{ID(AC)}	0.4	V _{DDQ} + 0.6	V	9
Clock Input Crossing Point Voltage; CK and CK#	V _{IX(AC)}	V _{DDQ} /2 - 0.15	V _{DDQ} /2 + 0.15	V	10

Figure 8
Clock Input


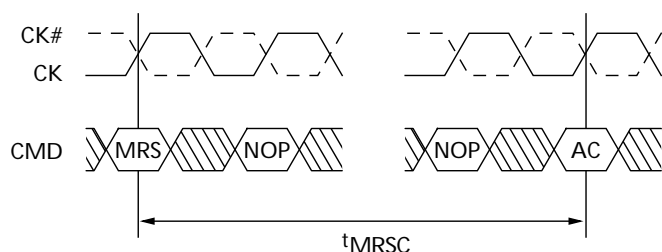
- NOTE:**
1. DKx and DKx# have the same requirements as CK and CK#.
 2. All voltages referenced to V_{ss}.
 3. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
 4. Outputs (except for I_{DD} measurements) measured with equivalent load.
 5. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between V_{IL(AC)} and V_{IH(AC)}.
 6. The AC and DC input level specifications are as defined in the HSTL Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
 7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is V_{REF}.
 8. CK and CK# input slew rate must be ≥ 2 V/ns (≥ 4 V/ns if measured differentially).
 9. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
 10. The value of V_{IX} is expected to equal V_{DDQ}/2 of the transmitting device and must track variations in the DC level of the same.
 11. CK and CK# must cross within this region.
 12. CK and CK# must meet at least V_{ID(DC)} MIN when static and centered around V_{DDQ}/2.
 13. Minimum peak-to-peak swing.



MODE REGISTER SET COMMAND (MRS)

The mode register stores the data for controlling the operating modes of the memory. It programs the RLD RAM configuration, burst length, test mode, and I/O options. During a MODE REGISTER SET command, the address inputs A(17:0) are sampled and stored in the mode register. ^tMRSC must be met before any command can be issued to the RLD RAM. The mode register may be set at any time during device operation. However, any pending operations are not guaranteed to successfully complete. See the RLD RAM II design guide for more details.

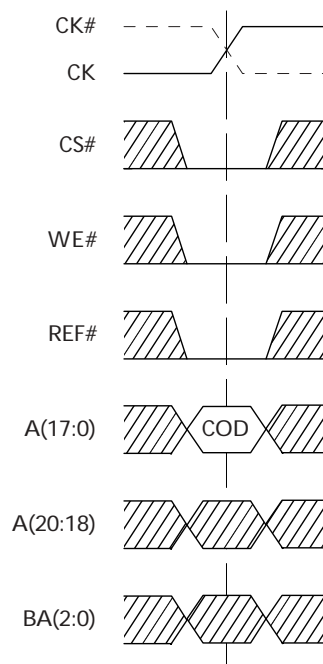
Figure 10
Mode Register Set Timing



Note: MRS: MRS command; AC: Any command

DON'T CARE

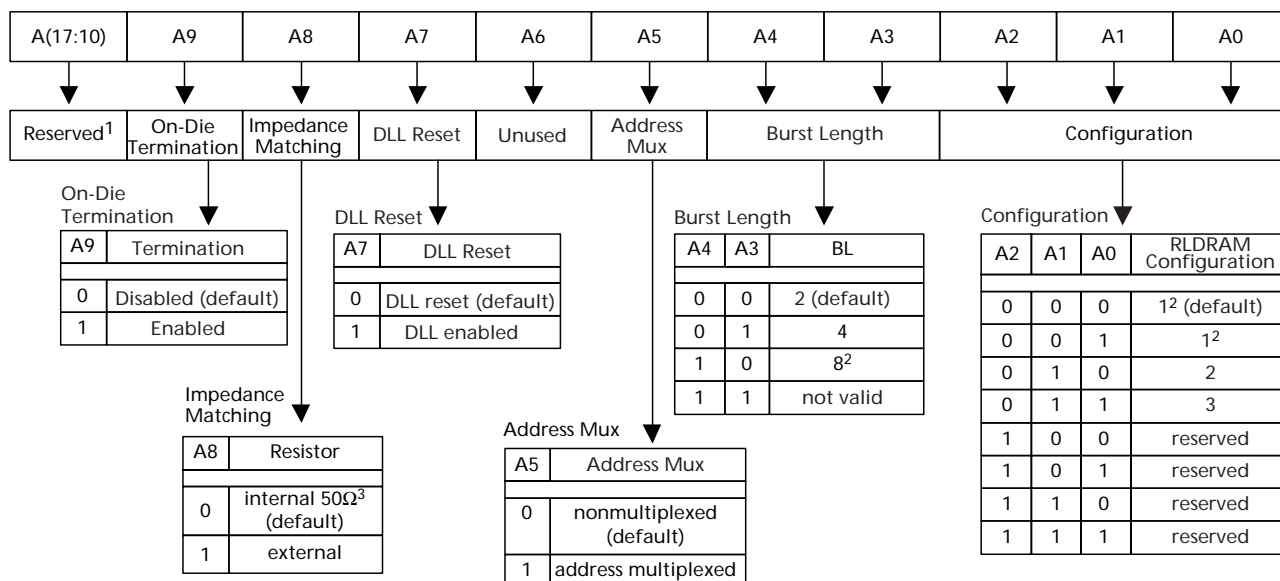
Figure 9
Mode Register Set



Note: COD: code to be loaded into the register

DON'T CARE

Figure 11
Mode Register Bit Map



NOTE: 1. Bits A(17:10) MUST be set to zero.

2. BL = 8 is not available for configuration 1.

3. ±15% temperature variation.



CONFIGURATION TABLE

Table 8 shows, for different operating frequencies, the different RLD RAM configurations that can be programmed into the mode register. The read and write latency (t_{RL} and t_{WL}) values along with the row cycle

times (t_{RC}) are shown in clock cycles as well as in nano-seconds.

The shaded areas correspond to configurations that are not allowed.

Table 8: RLD RAM Configuration Table

FREQUENCY	SYMBOL	CONFIGURATION			UNIT
		1 ¹	2	3	
	t_{RC}	4	6	8	cycles
	t_{RL}	4	6	8	cycles
	t_{WL}	5	7	9	cycles
400 MHz	t_{RC}			20.0	ns
	t_{RL}			20.0	ns
	t_{WL}			22.5	ns
300 MHz	t_{RC}		20.0	26.7	ns
	t_{RL}		20.0	26.7	ns
	t_{WL}		23.3	30.0	ns
200 MHz	t_{RC}	20.0	30.0	40.0	ns
	t_{RL}	20.0	30.0	40.0	ns
	t_{WL}	25.0	35.0	45.0	ns

NOTE: 1. BL = 8 is not available for configuration 1.



WRITE BASIC INFORMATION

Write accesses are initiated with a WRITE command, as shown in the WRITE Command figure on the right. Row and bank addresses are provided together with the WRITE command.

During WRITE commands, data will be registered at both edges of DK according to the programmed burst length (BL). A write latency (WL) one cycle longer than the programmed read latency (RL + 1) is present, with the first valid data registered at the first rising DK edge WL cycles after the WRITE command.

Any WRITE burst may be followed by a subsequent READ command. Figures 16 and 17 illustrate the timing requirements for a WRITE followed by a READ for bursts of two and four, respectively.

Setup and hold times for incoming DQ relative to the DK edges are specified as t_{DS} and t_{DH} . The input data is masked if the corresponding DM signal is HIGH. The setup and hold times for data mask are also t_{DS} and t_{DH} .

Figure 12
WRITE Command

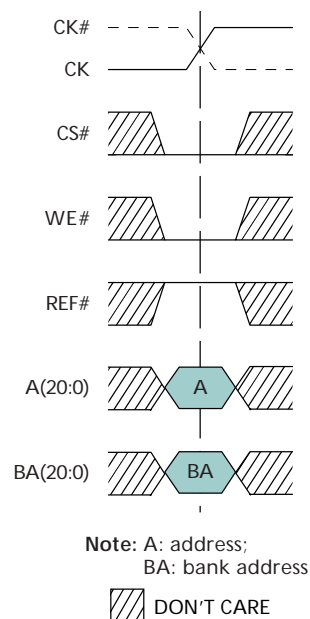


Figure 13
Basic WRITE Burst/DM Timing

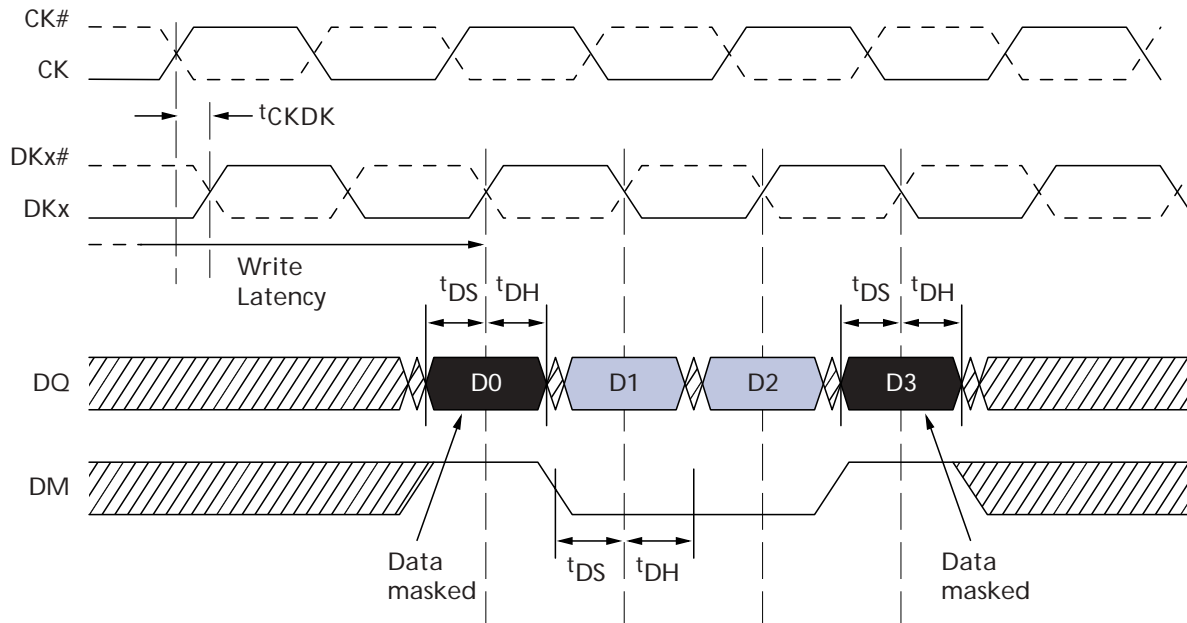


Table 9: Timing Parameters

SYMBOL	-2.5		-3.3		-5		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{DS}	0.25		0.3		0.4		ns
t_{DH}	0.25		0.3		0.4		ns
t_{CKDK}	-0.3	0.3	-0.3	0.3	-0.3	0.3	ns

Figure 14
WRITE Burst Basic Sequence: BL = 2, RL = 4, WL = 5, Configuration 1

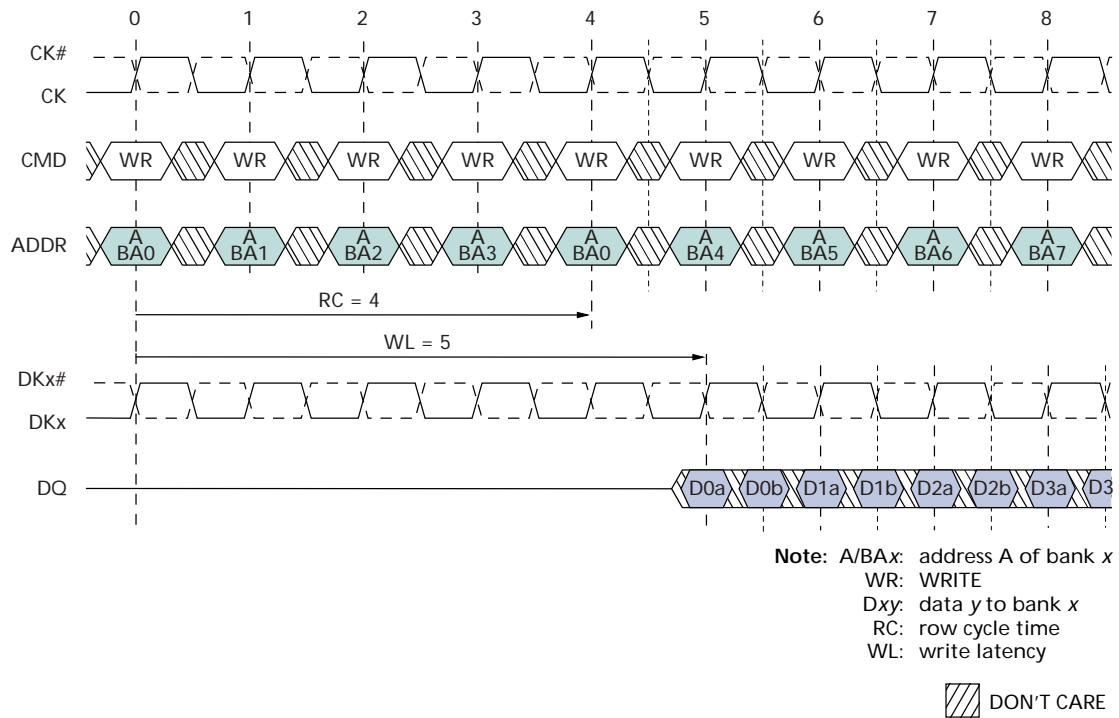
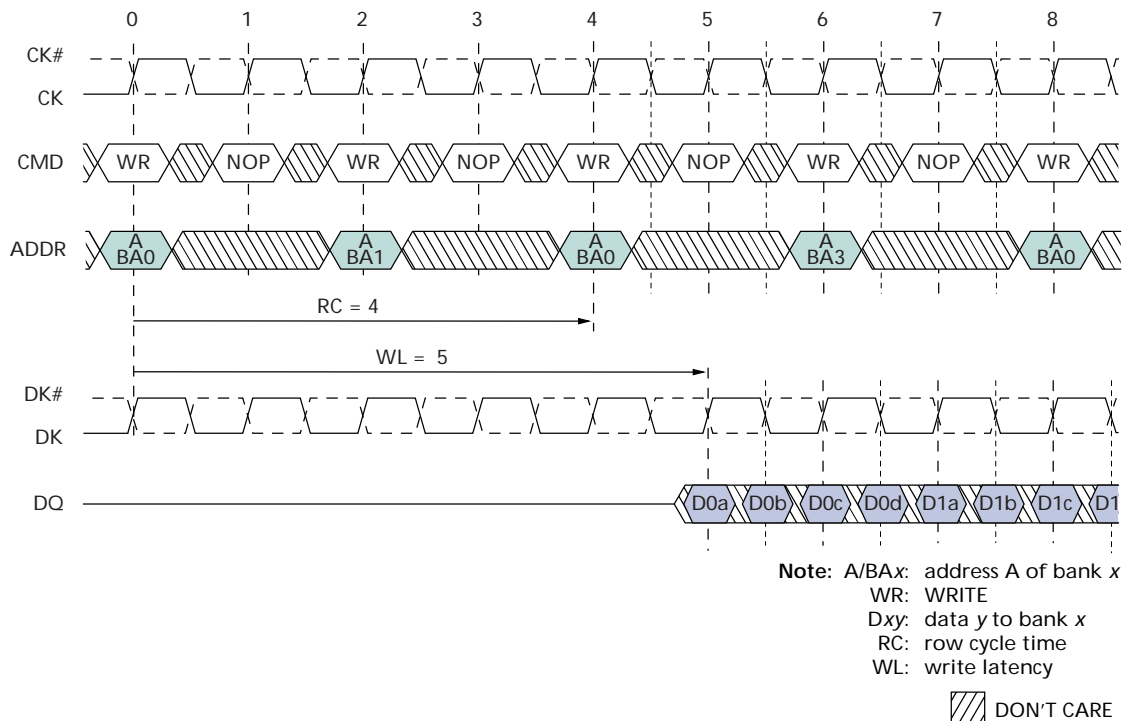


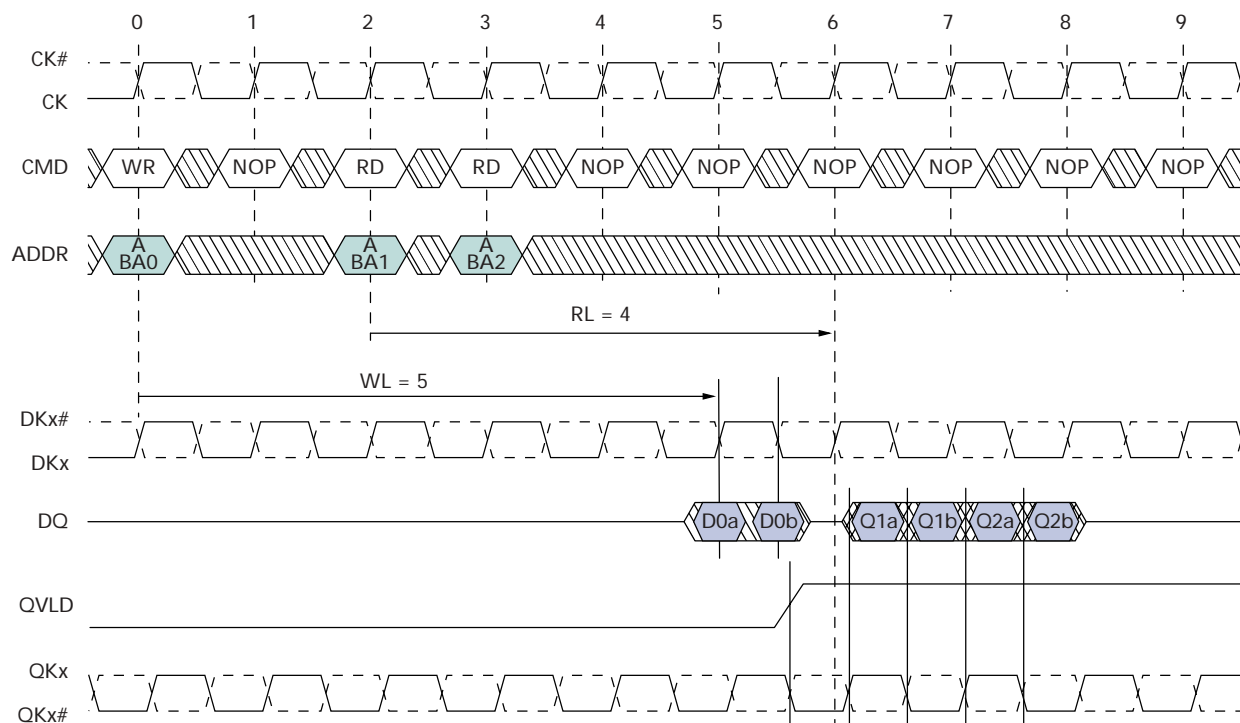
Figure 15
WRITE Burst Basic Sequence: BL = 4, RL = 4, WL = 5, Configuration 1



NOTE: Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.



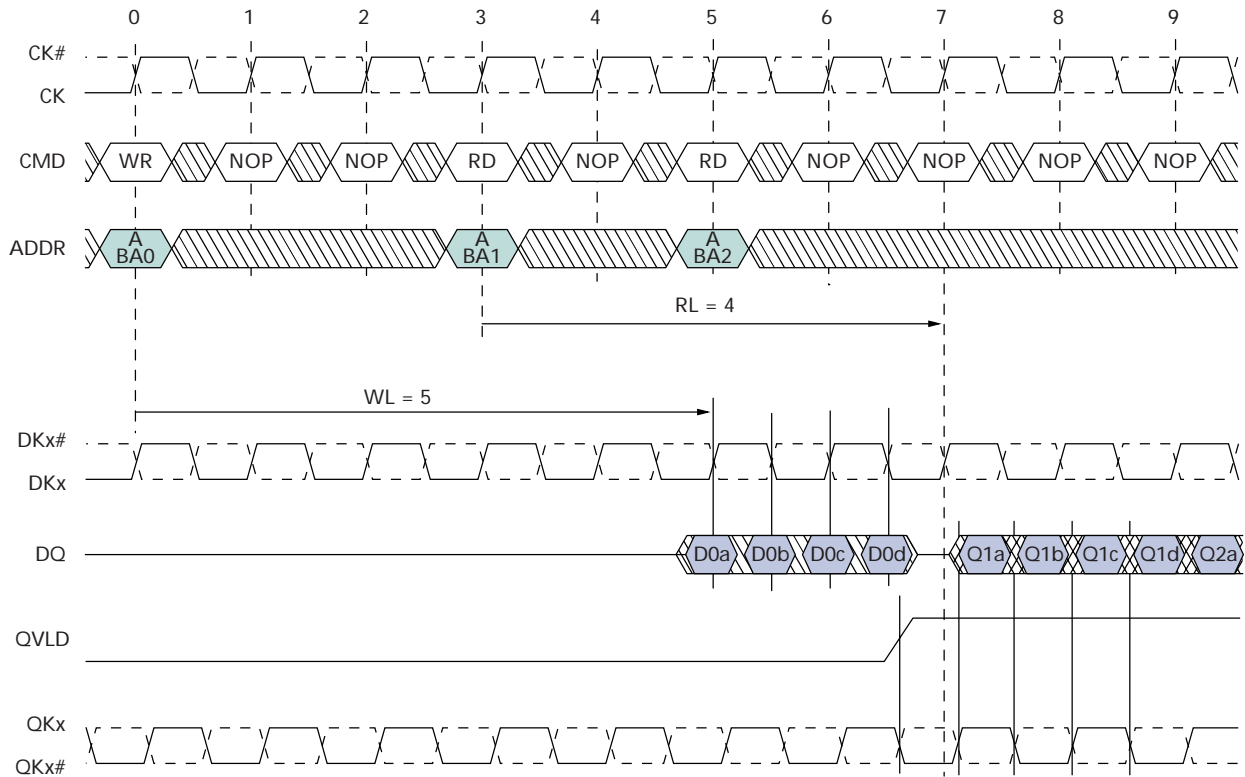
Figure 16
WRITE followed by READ: BL = 2, RL = 4, WL = 5, Configuration 1



Note: A/BAx: address A of bank x
 WR: WRITE
 Dxy: data y to bank x
 WL: write latency
 RD: READ
 Qxy: Data y from bank x
 RL: read latency

DON'T CARE
 UNDEFINED

Figure 17
WRITE followed by READ: BL = 4, RL = 4, WL = 5, Configuration 1



Note: A/BAx: address A of bank x
 WR: WRITE
 Dxy: data y to bank x
 WL: write latency
 RD: READ
 Qxy: Data y from bank x
 RL: read latency

DON'T CARE UNDEFINED

READ BASIC INFORMATION

Read accesses are initiated with a READ command, as shown in Figure 18. Row and bank addresses are provided with the READ command.

During READ bursts, the memory device drives the read data edge-aligned with the QK signal. After a programmable read latency, data is available at the outputs. The data valid signal indicates that valid data will be present in the next half clock cycle.

The skew between QK and the crossing point of CK is specified as t_{CKQK} . t_{QKQ0} is the skew between QK0 and the last valid data edge considered over all the data generated at the DQ signals. t_{QKQ1} is the skew between QK1 and the last valid data edge considered over all the data generated at the DQ signals. t_{QKQx} is derived at each QKx clock edge and is not cumulative over time. t_{QKQ} is the maximum of t_{QKQ0} and t_{QKQ1} .

After completion of a burst, assuming no other commands have been initiated, output data (DQ) will go High-Z. Back-to-back READ commands are possible, producing a continuous flow of output data.

The data valid window is derived from each QK transistion and is defined as: $\text{MIN}(t_{QKH}, t_{QKL}) - 2(t_{QKQ}(\text{MAX}))$.

Any READ burst may be followed by a subsequent WRITE command. Figures 22 and 23 illustrate the timing requirements for a READ followed by a WRITE. Depending on the programmed read latency, a READ-to-WRITE delay occurs in order to prevent bus contention. Some systems having long line lengths or severe skews may need additional idle cycles inserted. Refer to the RLD RAM II design guide for more details.

**Figure 18
READ Command**

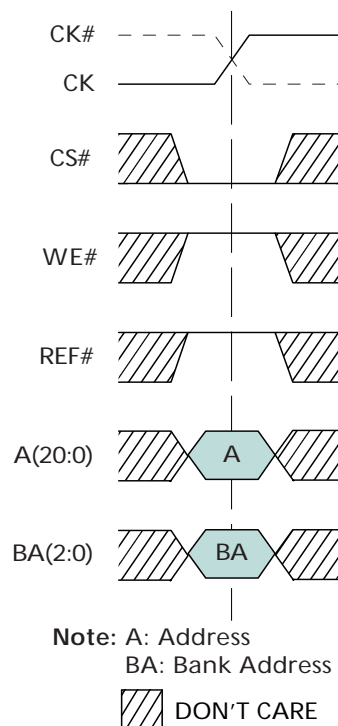
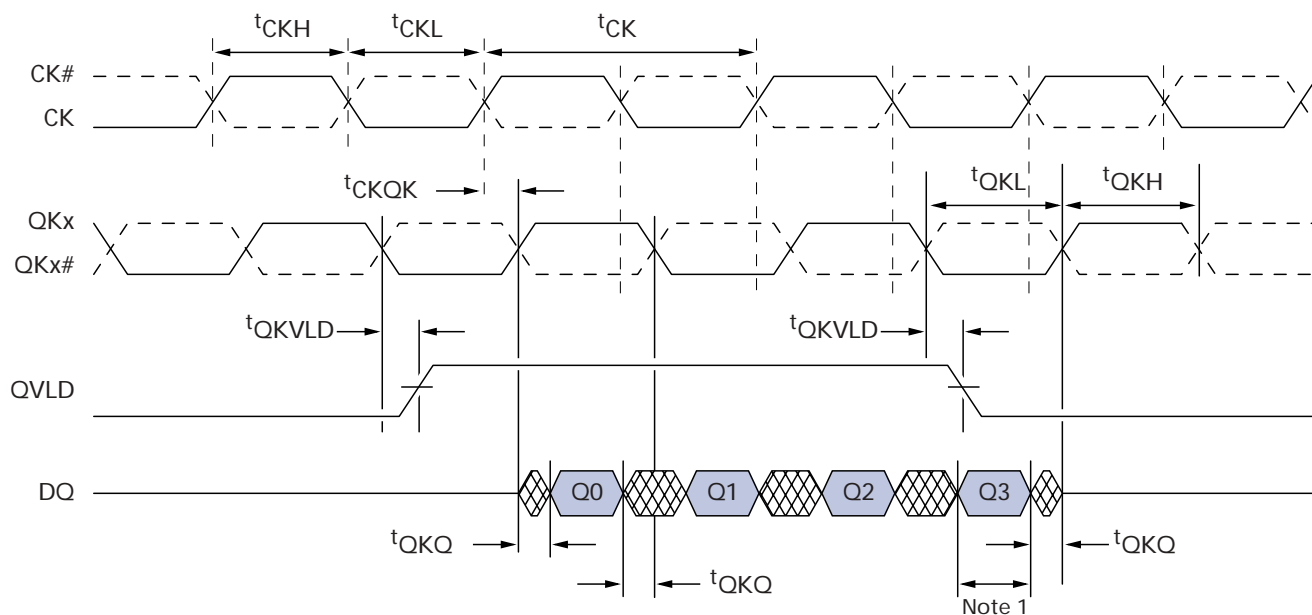


Figure 19
Basic READ Burst Timing



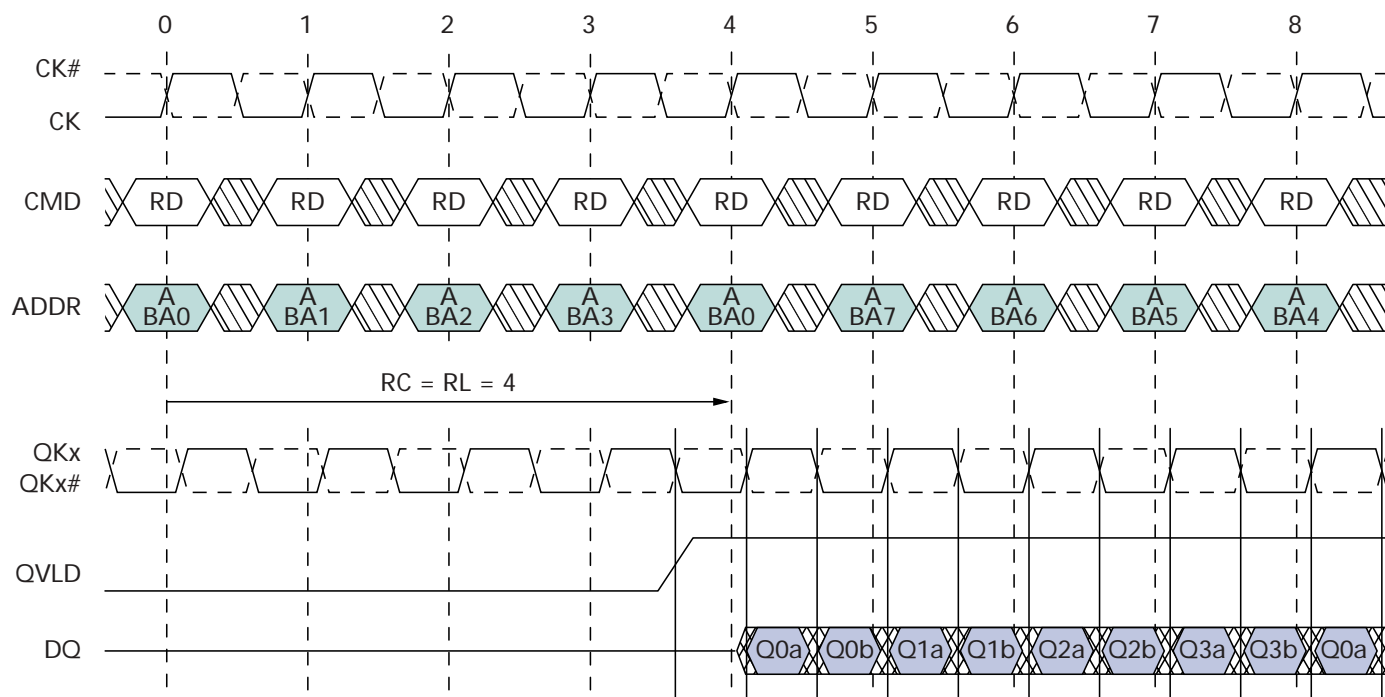
UNDEFINED

Table 10: Timing Parameters



SYMBOL	-2.5		-3.3		-5		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{CK}	2.5	5.7	3.3	5.7	5.0	5.7	ns
t _{CKH}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}
t _{CKL}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}
t _{CKQK}	-0.25	0.25	-0.3	0.3	-0.5	0.5	ns

SYMBOL	-2.5		-3.3		-5		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{QKQ}	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns
t _{QKQ0} , t _{QKQ1}	-0.2	0.2	-0.25	0.25	-0.3	0.3	ns
t _{QKVLD}	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns
t _{QKH}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CKH}
t _{QKL}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CKL}

- NOTE:**
1. Minimum data valid window can be expressed as MIN(t_{QKH}, t_{QKL}) - 2 x t_{QKQx}(MAX).
 2. t_{QKQ0} is referenced to DQ0–DQ17 in x36 and DQ0–DQ8 in x18.
t_{QKQ1} is referenced to DQ18–DQ35 in x36 and DQ9–DQ17 in x18.
 3. t_{QKQ} takes into account the skew between any QKx and any DQ.



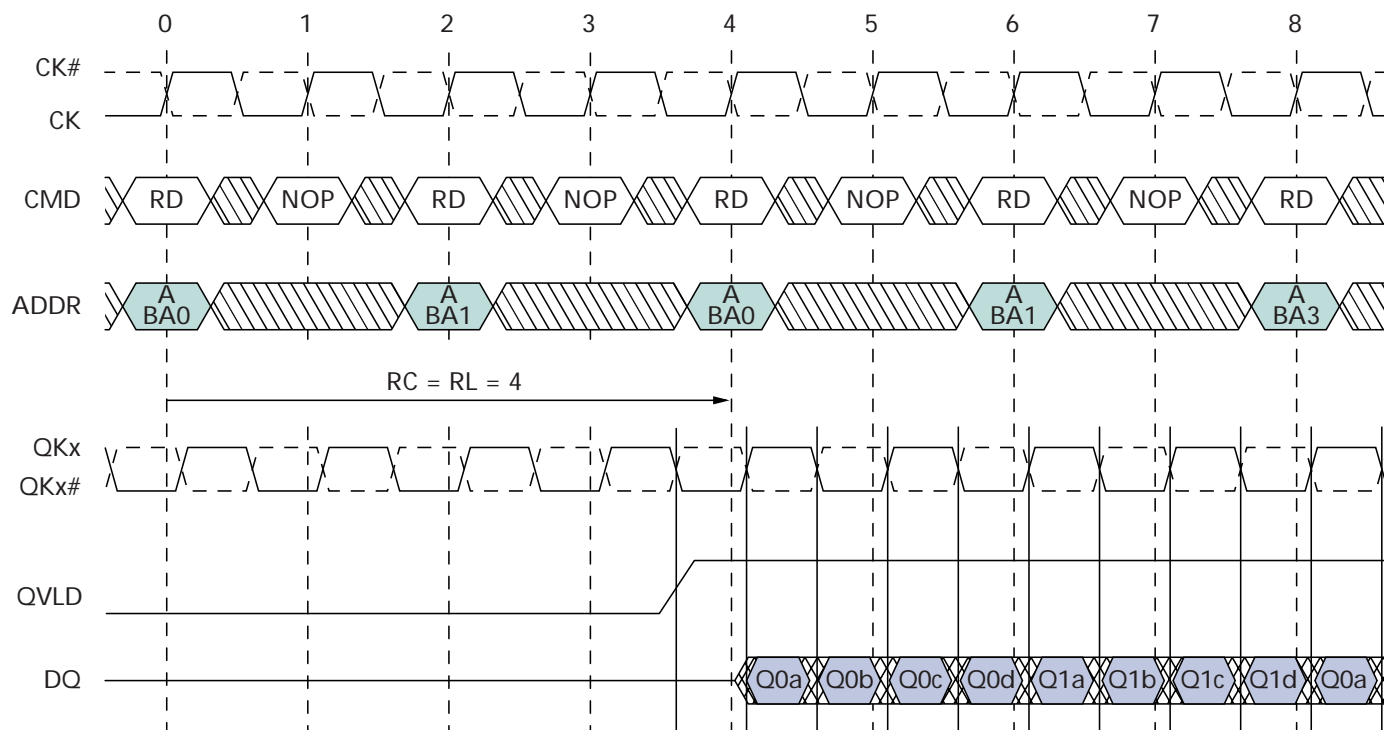
Note: A/BAx: address A of bank x
RD: READ
Dxy: data y to bank x
RC: row cycle time
RL: read latency

 DON'T CARE  UNDEFINED

NOTE: Any free bank may be used in any given CMD. The sequence shown is only one example of a bank sequence.



Figure 21
READ Burst: BL = 4, RL = 4, Configuration 1

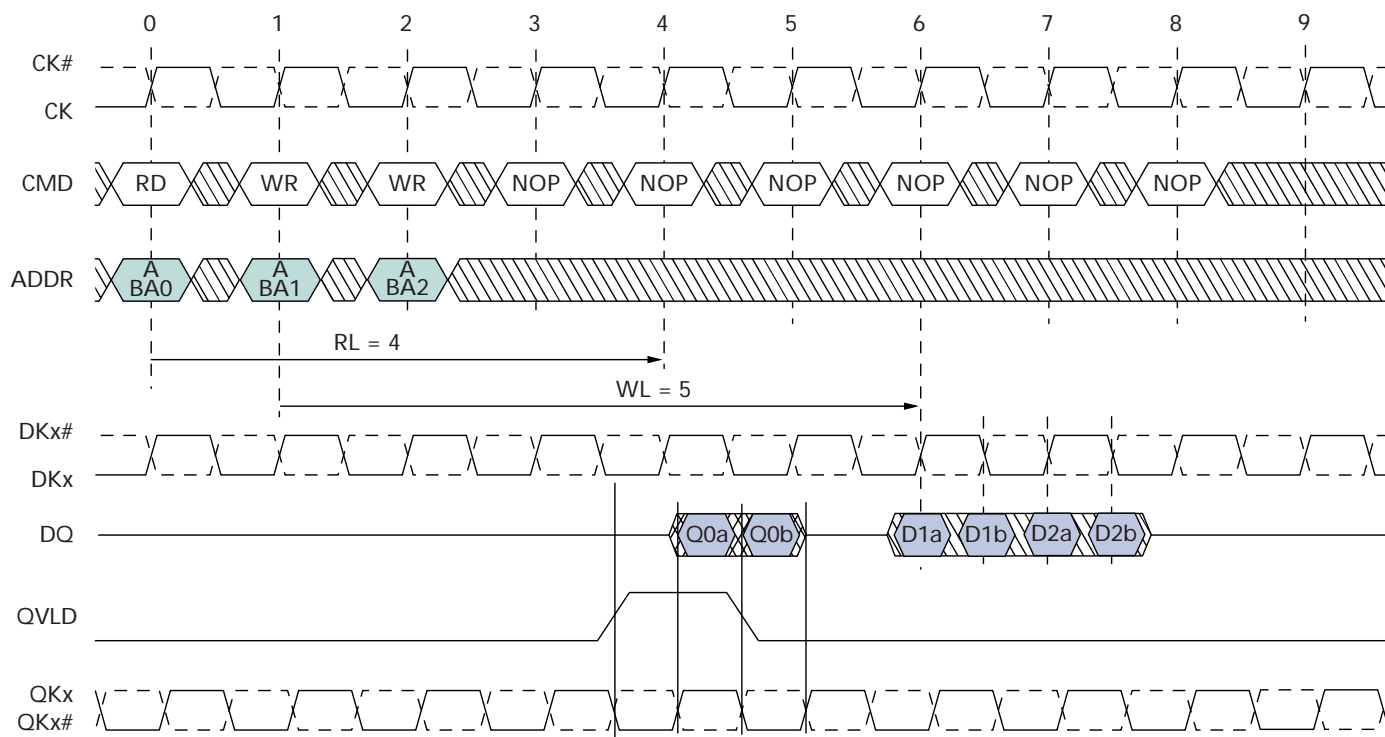


Note: A/BAx: address A of bank x
 RD: READ
 Dxy: data y to bank x
 RC: row cycle time
 RL: read latency

DON'T CARE UNDEFINED



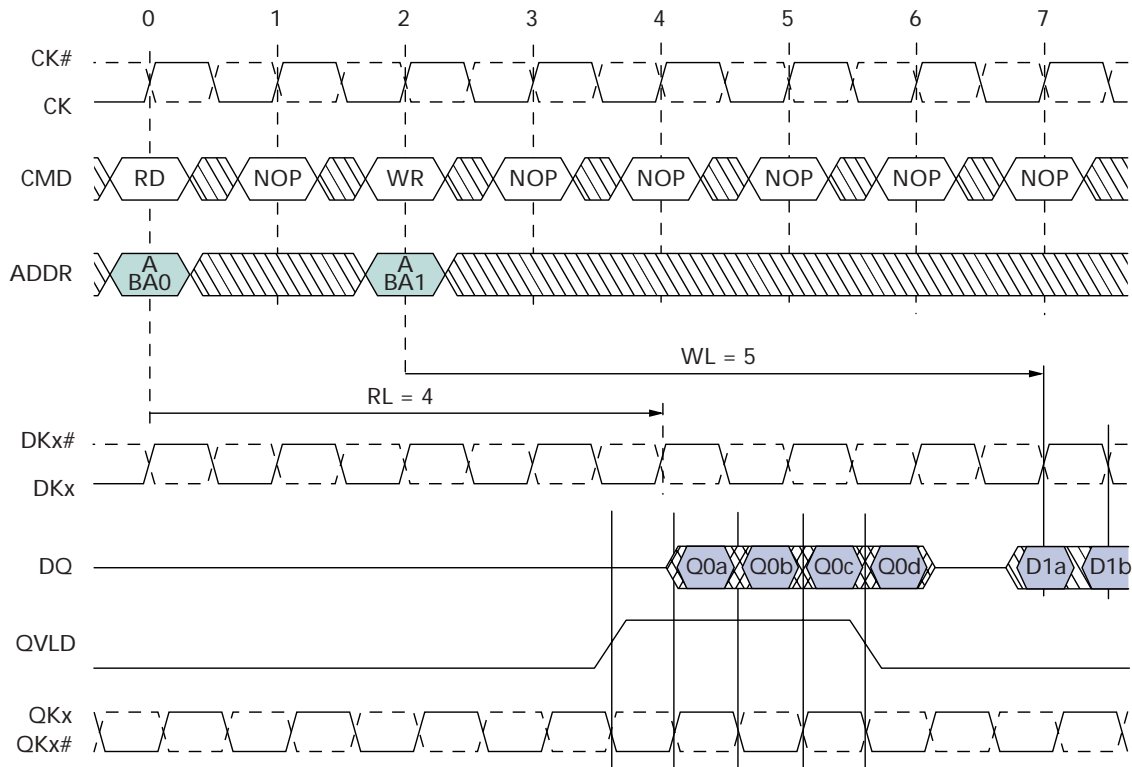
Figure 22
READ followed by WRITE, BL = 2, RL = 4, WL = 5, Configuration 1



Note: A/BAx: address A of bank x
 RD: READ
 Dxy: data y to bank x
 RL: read latency
 WL: write latency

DON'T CARE UNDEFINED

Figure 23
READ followed by WRITE, BL = 4, RL = 4, WL = 5, Configuration 1



Note: A/BA_x: address A of bank x
 WR: WRITE
 D_{xy}: data y to bank x
 WL: write latency
 RD: READ
 Q_{xy}: data y from bank x
 RL: read latency

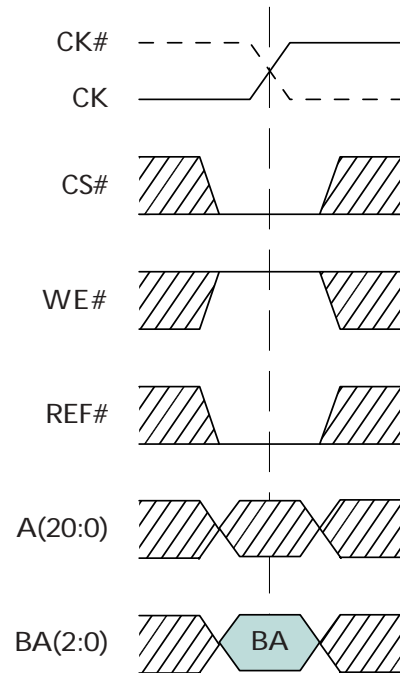
DON'T CARE UNDEFINED

AUTO REFRESH COMMAND (AREF)

AREF is used to perform a refresh cycle on one row in a specific bank. The row addresses are generated by an internal refresh counter for each bank; external address pins are "DON'T CARE." The delay between the AREF command and a subsequent command to the same bank must be at least t_{RC} .

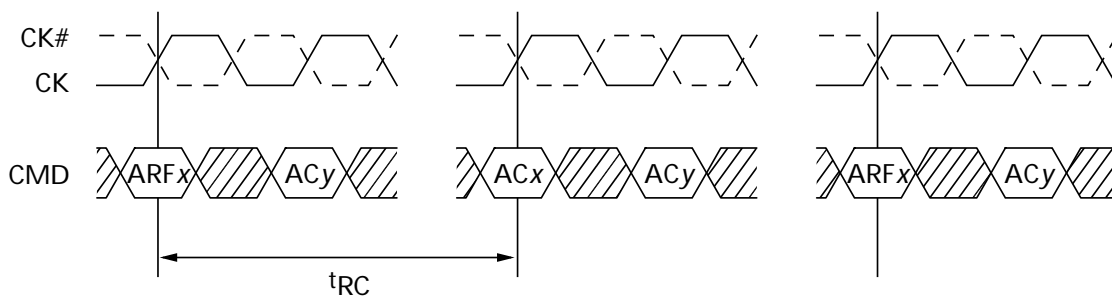
Within a period of 32ms (t_{REF}), the entire memory must be refreshed. Figure 25 illustrates an example of a continuous refresh sequence. Other refresh strategies, such as burst refresh, are also possible.

Figure 24
AUTO REFRESH Command



Note: BA: bank address

Figure 25
AUTO REFRESH Cycle



Note: ACx: Any command on bank x
 ARFx: Auto Refresh bank x
 ACy: Any command on different bank

DON'T CARE

NOTE: t_{RC} is configuration-dependent. Refer to Table 8: RLD RAM Configuration on page 14.



ON DIE TERMINATION

On-die Termination is enabled by setting A9 to one during a MODE REGISTER SET (MRS) command. With on-die termination on, all the DQs are terminated to V_{TT} with a resistance R_{TT}. The command, address, and clock signals are not terminated. Figure 26 below shows the equivalent circuit of a DQ receiver with on-die termina-

tion. On-die terminations are dynamically switched off during READ commands and are designed to be off prior to the RLD RAM driving the bus. Similarly, on-die terminations are designed to switch on after the RLD RAM has issued the last piece of data.

Table 11: On-Die Termination DC Parameters

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Termination Voltage		V _{TT}	0.95 x V _{REF}	1.05 x V _{REF}	V	1, 2
On-Die Termination		R _{TT}	135	165	Ω	3

- NOTE:**
1. All voltages referenced to V_{SS} (GND).
 2. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
 3. The R_{TT} value is measured at 70°C T_J.

Figure 26
On-Die Termination-Equivalent Circuit

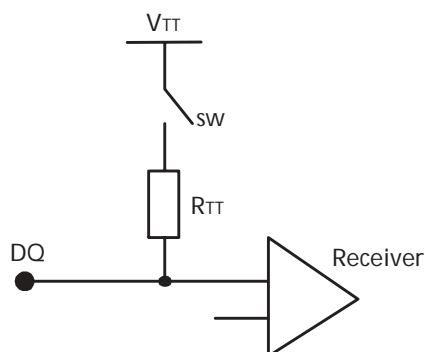
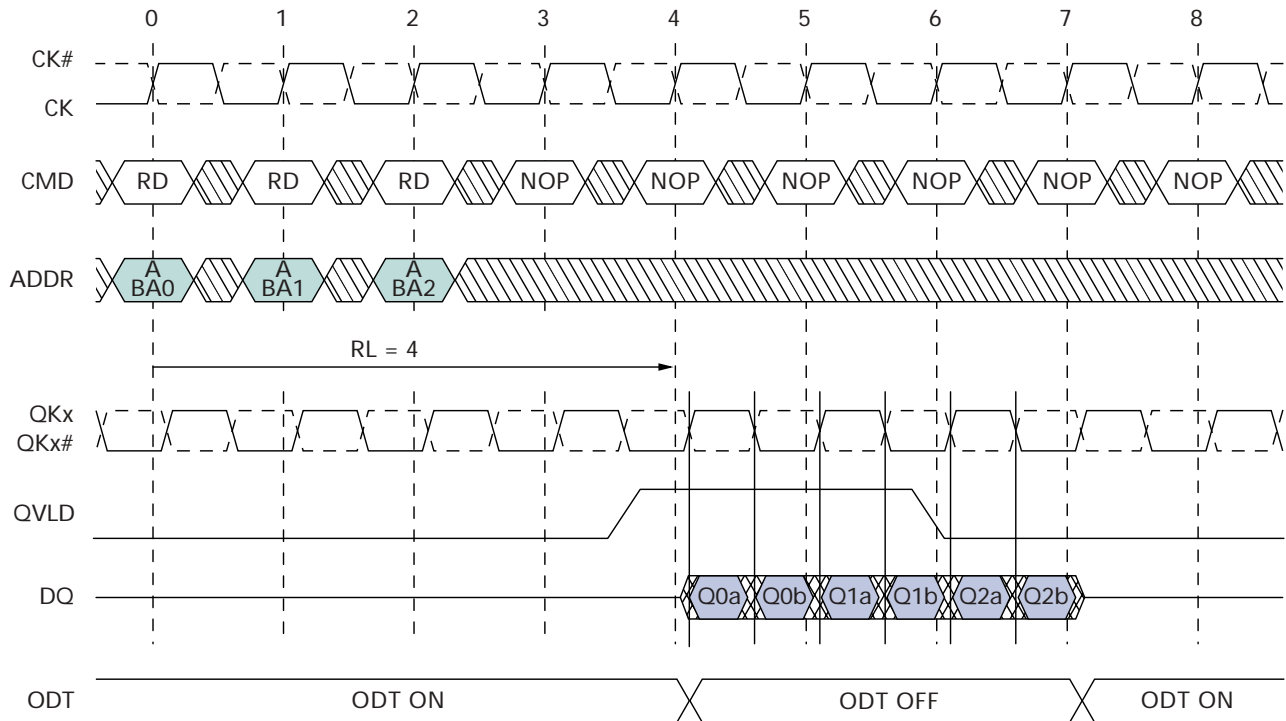


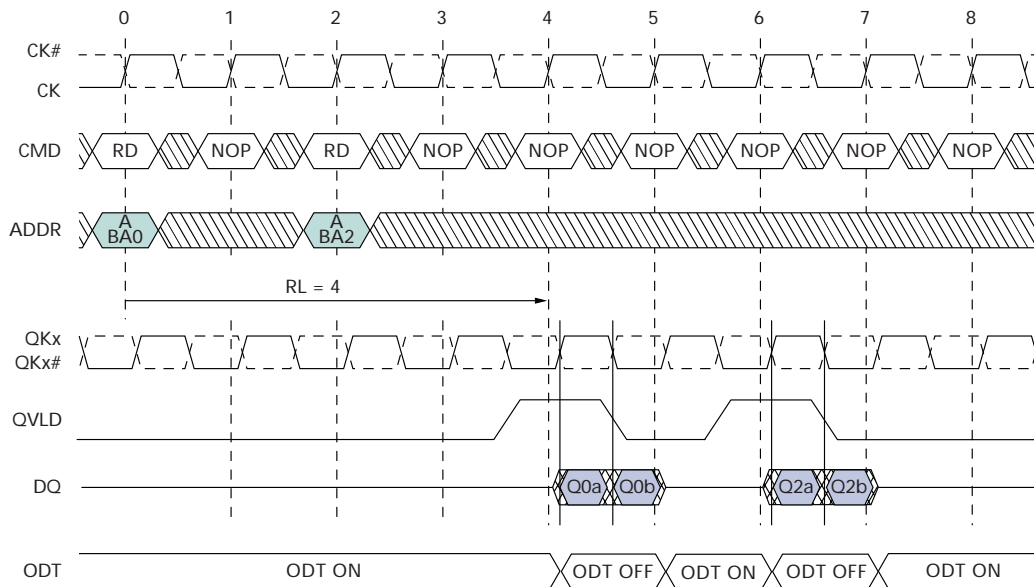
Figure 27
READ Burst with ODT: BL = 2, Configuration 1



Note: A/BAx: address A of bank x
RD: READ
Dxy: Data y to bank x
RL: read latency

DON'T CARE UNDEFINED

Figure 28
READ NOP READ with ODT: BL = 2, Configuration 1



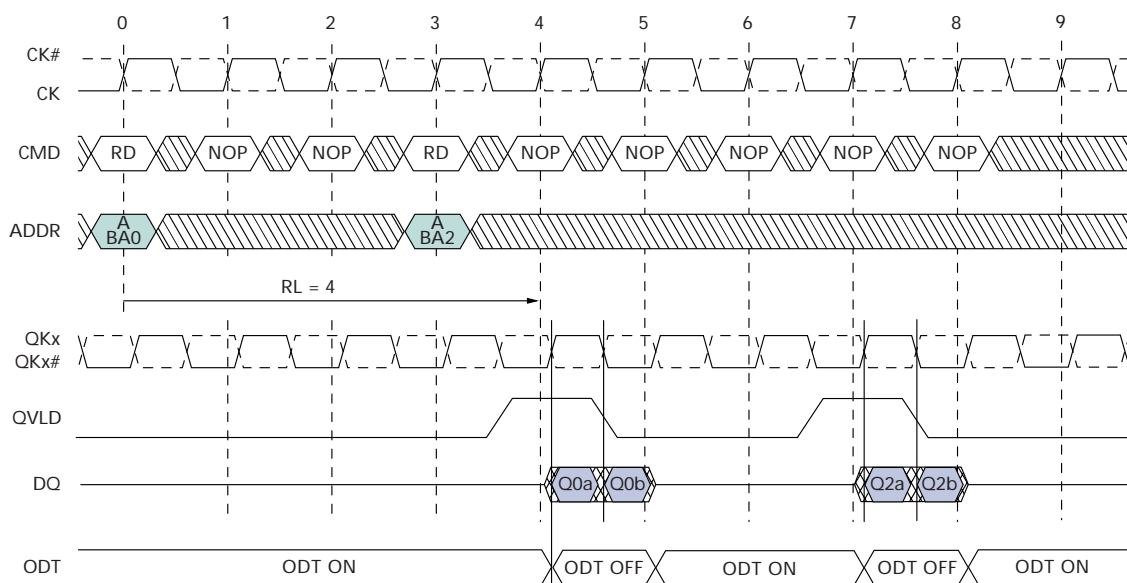
Note: A/BAx: address A of bank x
RD: READ

Dxy: data y to bank x

RL: read latency

DON'T CARE UNDEFINED

Figure 29
READ NOP NOP READ with ODT: BL = 2, Configuration 1



Note: A/BAx: address A of bank x
RD: READ

Dxy: data y to bank x

RL: read latency

DON'T CARE UNDEFINED

Figure 30
READ followed by WRITE with ODT: BL = 2, Configuration 1

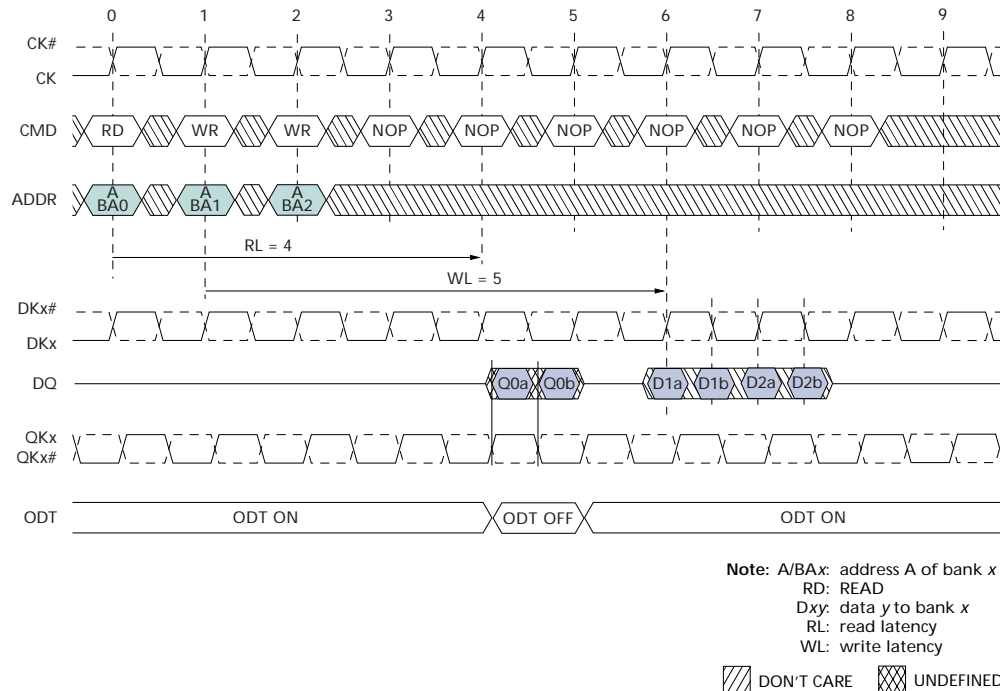
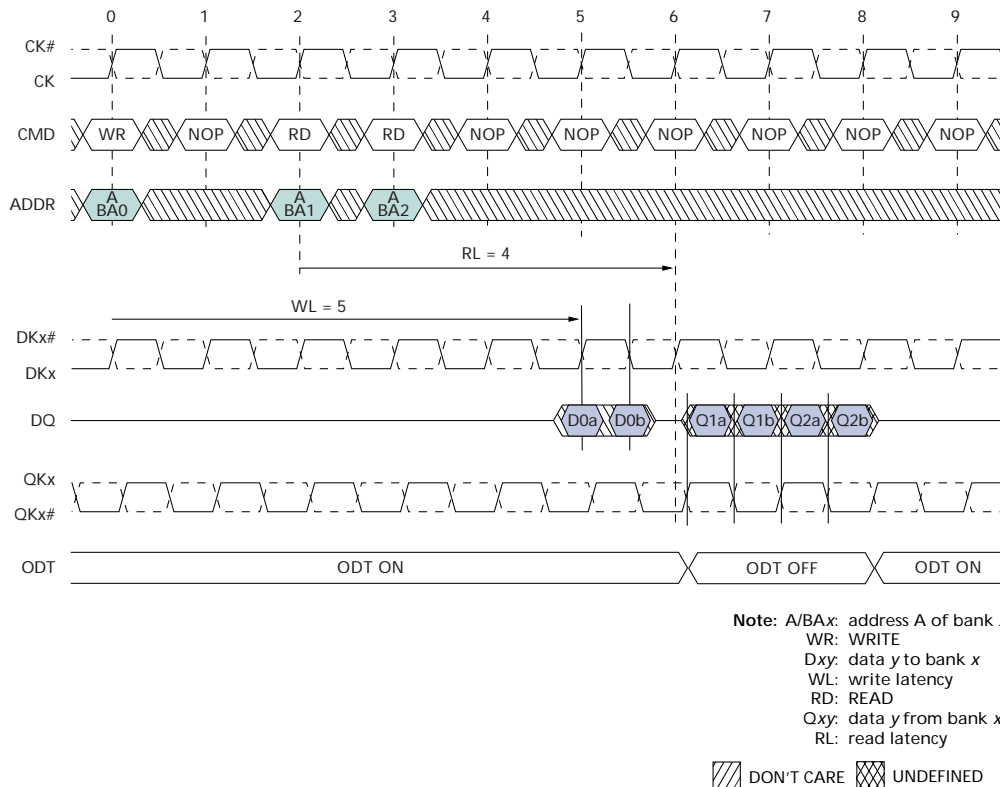


Figure 31
WRITE followed by READ with ODT: BL = 2, Configuration 1



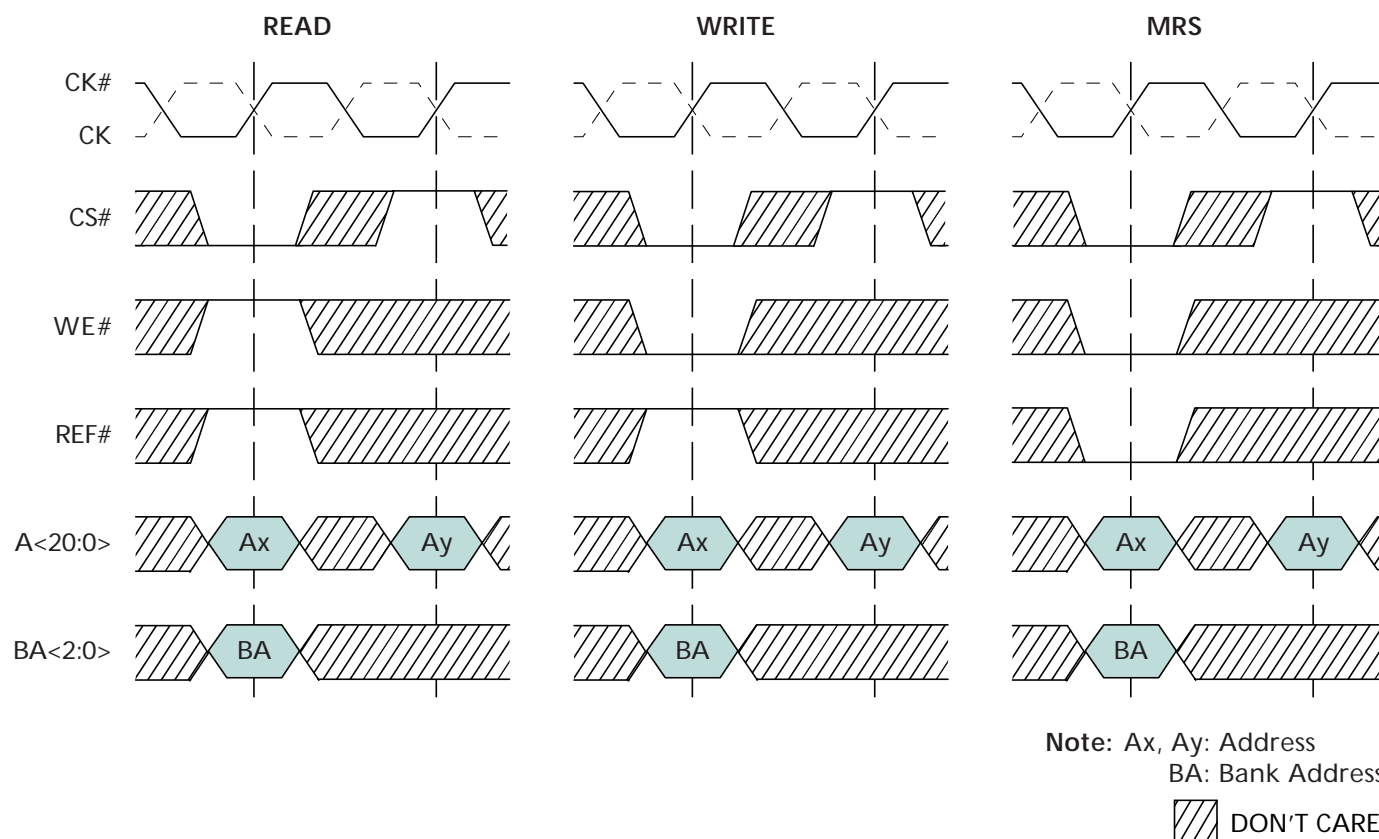


OPERATION WITH MULTIPLEXED ADDRESSES

In multiplexed address mode, the address can be provided to the RLD RAM in two parts that are latched into the memory with two consecutive rising clock edges. This provides the advantage that a maximum of 11 address pins are required to control the RLD RAM, reducing the number of pins on the controller side. The data bus efficiency in continuous burst mode is not affected for BL4 and BL8 since at least two clocks are required to read the data out of the memory. The bank addresses are delivered to the RLD RAM at the same time as the WRITE command and the first address part, Ax.

This option is available by setting bit A5 to '1' in the mode register. Once this bit is set, the READ, WRITE, and MRS commands follow the format described in Figure 32. See Figure 34 for the power-up sequence.

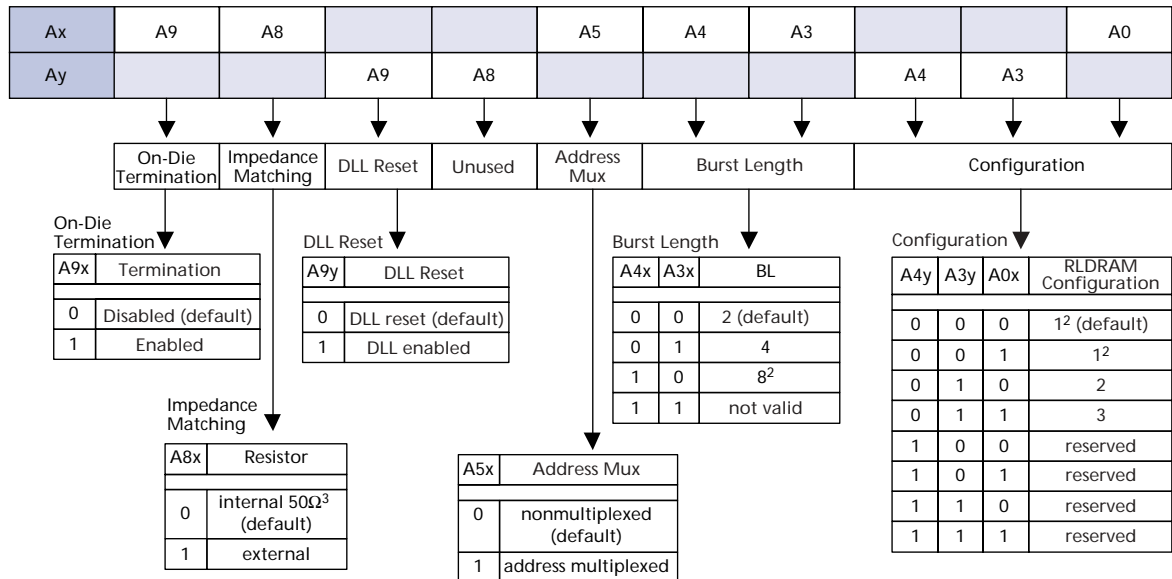
Figure 32
Command Description in Multiplexed Address Mode



NOTE: The minimum setup and hold times of the two address parts are defined t_{AS} and t_{AH} .

Figure 33
MODE REGISTER SET Command in Multiplexed Address Mode

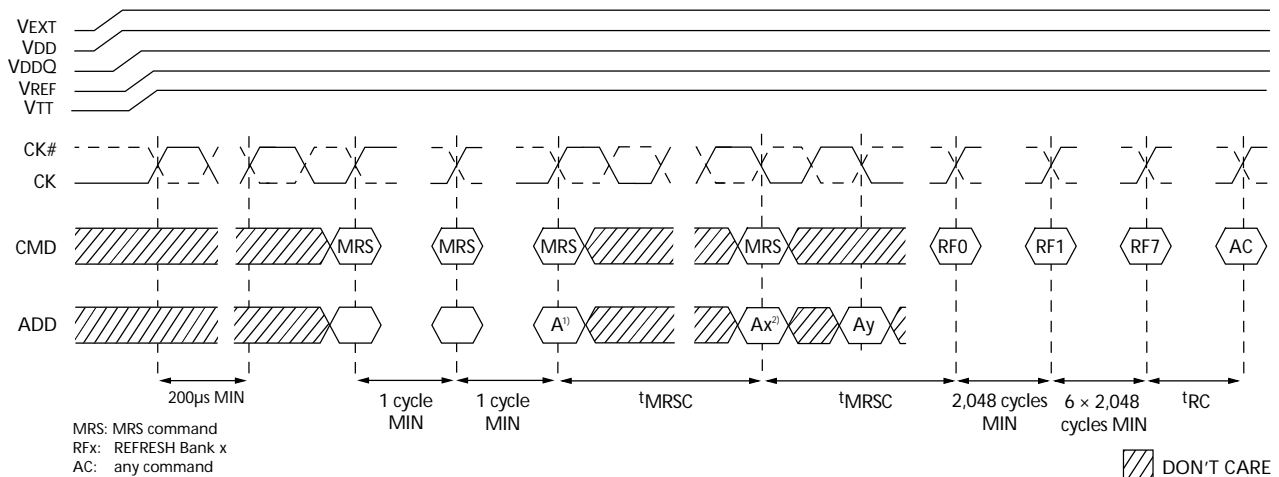
The addresses A0 to A6 must be set as follows in order to activate the mode register in the multiplexed address mode.



NOTE: 1. Bits A(17:11) MUST be set to zero.
2. BL = 8 is not available for configuration 1.
3. ±15% temperature variation.

Figure 34
Power-Up Sequence in Multiplexed Address Mode

The following sequence must be respected in order to power up the RLD RAM in the multiplexed address mode.



NOTE: 1. Address A5 must be set HIGH (muxed address mode setting when RLD RAM is in normal mode of operation).
2. Address A5 must be set HIGH (muxed address mode setting when RLD RAM is already in muxed address mode).



ADDRESS MAPPING

The address mapping is described in Table 12 as a function of data width and burst length.

Table 12: Address Mapping in Multiplexed Address Mode¹

DATA WIDTH	BURST LENGTH	PIN	ADDRESSES										
			A0 ²	A3	A4	A5 ³	A8	A9	A10	A13	A14	A17	A18
x36	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x18	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	X
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15
x9	BL = 2	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	A20	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 4	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	A19	A11	A12	A16	A15
	BL = 8	Ax	A0	A3	A4	A5	A8	A9	A10	A13	A14	A17	A18
		Ay	X	A1	A2	X	A6	A7	X	A11	A12	A16	A15

NOTE: 1. X means "Don't Care."
2. Reserved for A20 expansion in multiplexed mode.
3. Reserved for A21 expansion in multiplexed mode.



CONFIGURATION TABLE

In this mode, the read and write latencies are increased by one clock cycle. The RLD RAM cycle time remains the same, as described in Table 13.

Table 13: Configuration Table In Multiplexed Address Mode

CONFIGURATION					
FREQUENCY	SYMBOL	1 ¹	2	3	UNIT
	t _{RC}	4	6	8	cycles
	t _{RL}	5	7	9	cycles
	t _{WL}	6	8	10	cycles
400 MHz	t _{RC}			20.0	ns
	t _{RL}			22.5	ns
	t _{WL}			25.0	ns
300 MHz	t _{RC}		20.0	26.7	ns
	t _{RL}		23.3	30.0	ns
	t _{WL}		26.7	33.3	ns
200 MHz	t _{RC}	20.0	30.0	40.0	ns
	t _{RL}	25.0	35.0	45.0	ns
	t _{WL}	35.0	40.0	50.0	ns

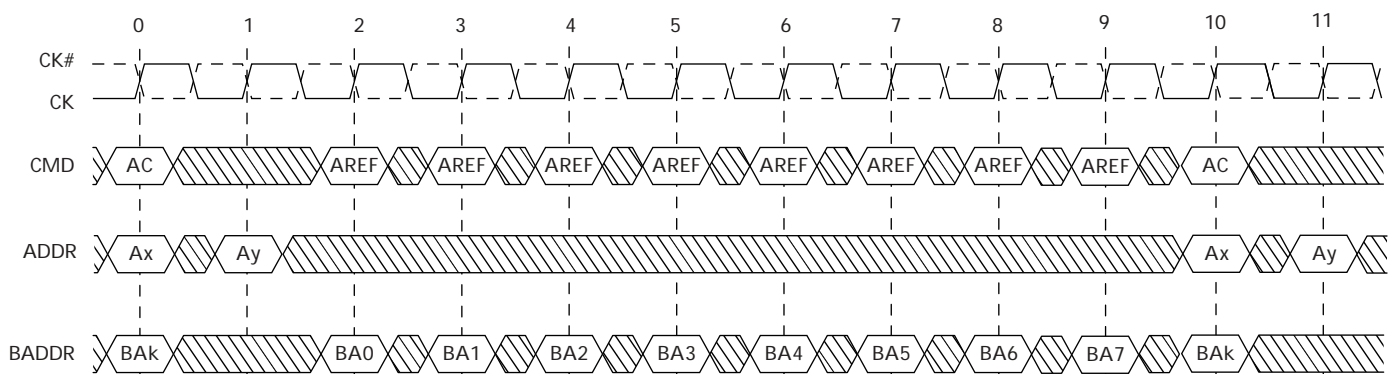
NOTE: 1. BL = 8 is not available for configuration 1.

REFRESH COMMAND IN MULTIPLEXED ADDRESS MODE

Similar to other commands, the refresh command is executed on the next rising clock edge when in the multiplexed address mode. However, since only bank address is required for AREF, the next command can be

applied on the following clock. The operation of the AREF command and any other command is represented in Figure 35.

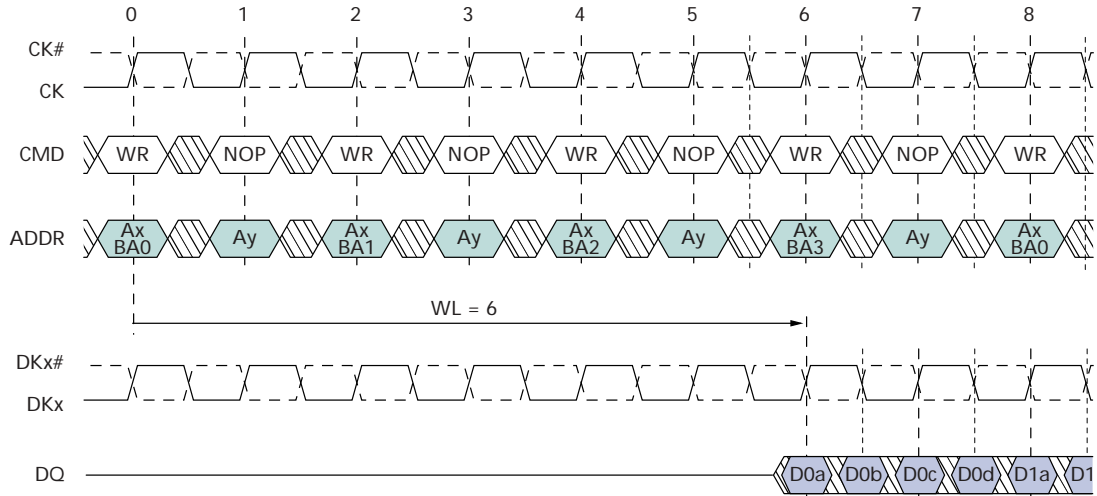
**Figure 35
Burst Refresh Operation**



Note: AREF: auto refresh
AC: any command
Ax: first part Ax of address
Ay: second part Ay of address
BAk: bank k; k is chosen so that t_{RC} is met

 DON'T CARE

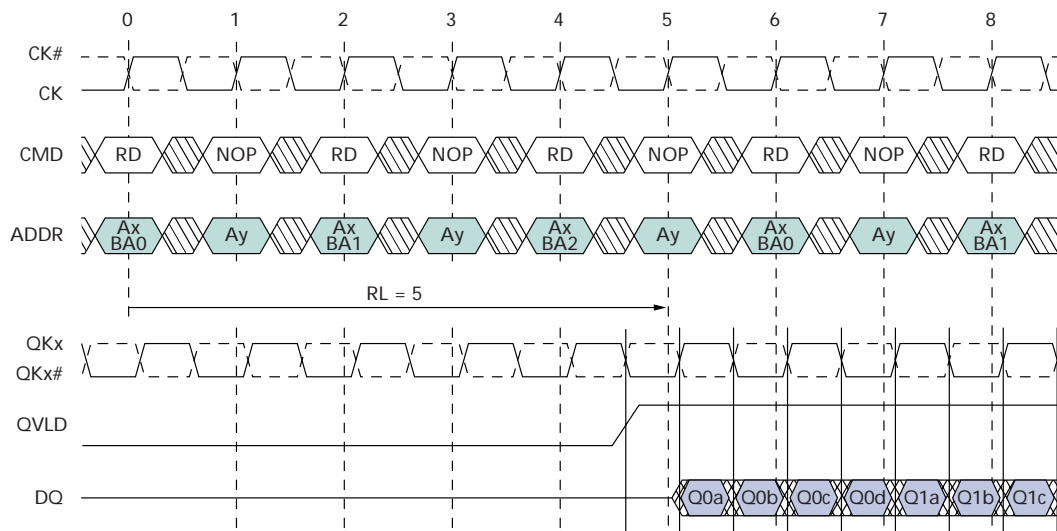
Figure 36
WRITE Burst Basic Sequence: BL = 4,
with Multiplexed Addresses, Configuration 1, WL = 6



Note: Ax/BAk: address Ax of bank k
Ay: address Ay of bank k
WR: WRITE
Djk: data k to bank j
WL: write latency

DON'T CARE

Figure 37
READ Burst Basic Sequence: BL = 4,
with Multiplexed Addresses, Configuration 1, RL = 5



Note: Ax/BAk: address Ax of bank k
Ay: address Ay of bank k
RD: READ
Qjk: data k to bank j
RL: read latency

DON'T CARE UNDEFINED

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

RLDRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-2001. The TAP operates using JEDEC-standard logic levels.

RLDRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

DISABLING THE JTAG FEATURE

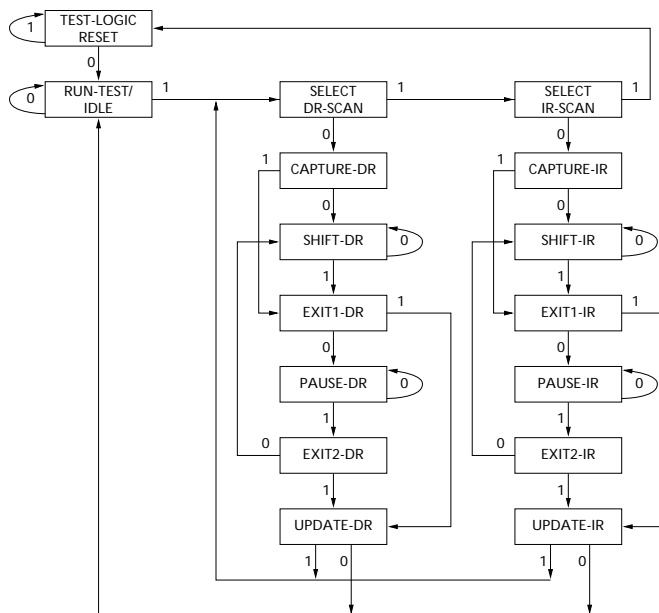
It is possible to operate RLDRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{ss}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state, which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Figure 38
TAP Controller State Diagram



Note: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 38. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register (see Figure 39).

TEST DATA-OUT (TDO)

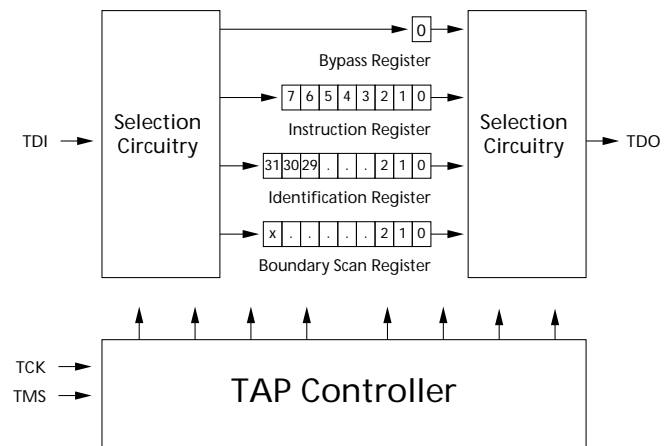
The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Figure 38). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see Figure 39).

PERFORMING A TAP RESET

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the RLDRAM and may be performed while the RLDRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

Figure 39
TAP Controller Block Diagram



Note: x = 112 for all configurations.



TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the RLD RAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

INSTRUCTION REGISTER

Eight-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 39. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins. This allows data to be shifted through the RLD RAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the RLD RAM. Several pins are also included in the scan register to reserved pins. The RLD RAM has a 113-bit register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the pins on the RLD RAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the RLD RAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET OVERVIEW

Many different instructions (2⁸) are possible with the eight-bit instruction register. All used combinations are listed in Table 18, Instruction Codes. These six instructions are described in detail below. The remaining instructions are reserved and should not be used.

The TAP controller used in this RLD RAM is fully compliant to the 1149.1 convention.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply a test vector, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output pins.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

HIGH Z

The HIGH Z instruction causes the boundary scan register to be connected between the TDI and TDO. This places all RLD RAM outputs into a High-Z state.

CLAMP

When the CLAMP instruction is loaded into the instruction register, the data driven by the output pins are determined from the values held in the boundary scan register.



SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the RLD RAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To ensure that the boundary scan register will capture the correct value of a signal, the RLD RAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}). The RLD RAM clock input might not be captured

correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 40
TAP Timing

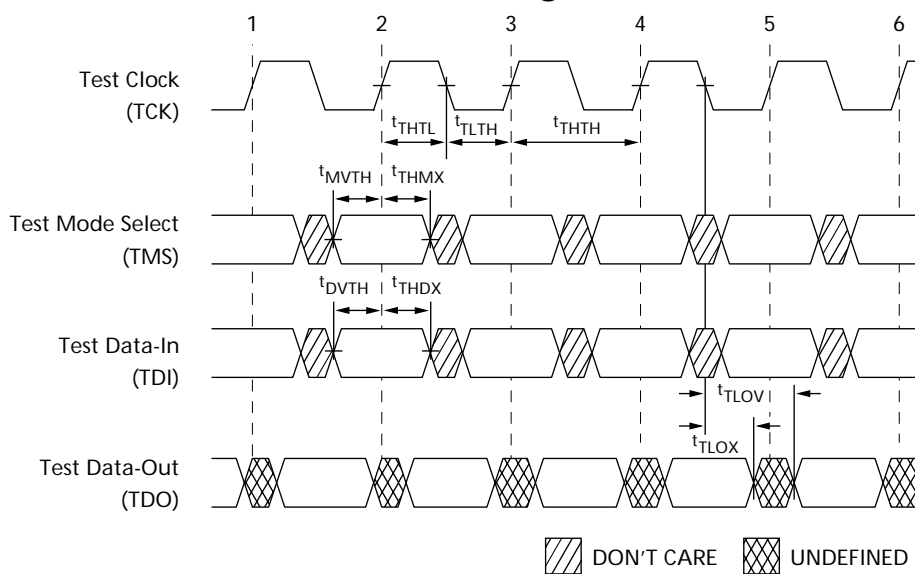


Table 14: TAP AC Electrical Characteristics¹

(+0°C ≤ T_J ≤ +100°C; +1.7V ≤ V_{DD} ≤ +1.9V)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	t_{THTH}	20		ns
Clock frequency	f_{TF}		50	MHz
Clock HIGH time	t_{THTL}	10		ns
Clock LOW time	t_{TLTH}	10		ns
Output Times				
TCK LOW to TDO unknown	t_{TLOX}	0		ns
TCK LOW to TDO valid	t_{TLOV}		10	ns
TDI valid to TCK HIGH	t_{DVTH}	5		ns
TCK HIGH to TDI invalid	t_{THDX}	5		ns
Setup Times				
TMS setup	t_{MVTH}	5		ns
Capture setup	t_{CS}	5		ns
Hold Times				
TMS hold	t_{THMX}	5		ns
Capture hold	t_{CH}	5		ns

NOTE: 1. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.


Table 15: TAP DC Electrical Characteristics and Operating Conditions

 (+0°C ≤ T_J ≤ 100°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	V _{REF} + 0.15	V _{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V _{IL}	V _{SSQ} - 0.3	V _{REF} - 0.15	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{DD}	I _{LI}	-5.0	5.0	μA	
Output Leakage Current	Output disabled, 0V ≤ V _{IN} ≤ V _{DDQ}	I _{LO}	-5.0	5.0	μA	
Output Low Voltage	I _{OLC} = 100μA	V _{OL1}		V _{REF} - tbd	V	1
Output Low Voltage	I _{OLT} = 2mA	V _{OL2}		V _{REF} - tbd	V	1
Output High Voltage	I _{OHC} = 100μA	V _{OH1}	V _{REF} + tbd		V	1
Output High Voltage	I _{OHT} = 2mA	V _{OH2}	V _{REF} + tbd		V	1

NOTE: 1. All voltages referenced to V_{SS} (GND).
 2. Overshoot: V_{IH}(AC) ≤ V_{DD} + 0.7V for t ≤ t_{CK}/2.
 Undershoot: V_{IL}(AC) ≥ -0.5V for t ≤ t_{CK}/2.
 During normal operation, V_{DDQ} must not exceed V_{DD}.

**Table 16: Identification Register Definitions**

INSTRUCTION FIELD	ALL DEVICES	DESCRIPTION
Revision Number (31:28)	abcd	ab = die revision cd = 10 for x36, 01 for x18, 00 for x9.
Device ID (27:12)	00jkidef10100111	def = 000 for 288M, 001 for 576M, 010 for 1G. i = 0 for common I/O, 1 for separate I/O. jk = 00 for RLD RAM, 01 for RLD RAM II.
Micron JEDEC ID Code (11:1)	00000101100	Allows unique identification of RLD RAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Table 17: Scan Register Sizes

REGISTER NAME	BIT SIZE
Instruction	8
Bypass	1
ID	32
Boundary Scan	113

Table 18: Instruction Codes

INSTRUCTION	CODE	DESCRIPTION
Extest	0000 0000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This operation does not affect RLD RAM operations.
ID Code	0010 0001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect RLD RAM operations.
Sample/Preload	0000 0101	Captures I/O ring contents. Places the boundary scan register between TDI and TDO.
Clamp	0000 0111	Selects the bypass register to be connected between TDI and TDO. Data driven by output pins are determined from values held in the boundary scan register.
High Z	0000 0011	Selects the bypass register to be connected between TDI and TDO. All outputs are forced into high impedance state.
Bypass	1111 1111	Places the bypass register between TDI and TDO. This operation does not affect RLD RAM operations.


Table 19: Boundary Scan (Exit) Order

BIT#	FBGA BALL
1	K1
2	K2
3	L2
4	L1
5	M1
6	M3
7	M2
8	N1
9	P1
10	N3
11	N3
12	N2
13	N2
14	P3
15	P3
16	P2
17	P2
18	R2
19	R3
20	T2
21	T2
22	T3
23	T3
24	U2
25	U2
26	U3
27	U3
28	V2
29	U10
30	U10
31	U11
32	U11
33	T10
34	T10
35	T11
36	T11
37	R10

BIT#	FBGA BALL
38	R10
39	R11
40	R11
41	P11
42	P11
43	P10
44	P10
45	N11
46	N11
47	N10
48	N10
49	P12
50	N12
51	M11
52	M10
53	M12
54	L12
55	L11
56	K11
57	K12
58	J12
59	J11
60	H11
61	H12
62	G12
63	G10
64	G11
65	E12
66	F12
67	F10
68	F10
69	F11
70	F11
71	E10
72	E10
73	E11
74	E11

BIT#	FBGA BALL
75	D11
76	D10
77	C11
78	C11
79	C10
80	C10
81	B11
82	B11
83	B10
84	B10
85	B3
86	B3
87	B2
88	B2
89	C3
90	C3
91	C2
92	C2
93	D3
94	D3
95	D2
96	D2
97	E2
98	E2
99	E3
100	E3
101	F2
102	F2
103	F3
104	F3
105	E1
106	F1
107	G2
108	G3
109	G1
110	H1
111	H2
112	J2
113	J1

NOTE: 1. Any unused pins that are in the order will read as the logic level applied to the ball site. If left floating, a value of '0' is returned.


ABSOLUTE MAXIMUM RATINGS*

Storage Temperature	-55°C to +150°C
I/O Voltage	-0.3V to V _{DDQ} + 0.3V
Voltage on V _{EXT} Supply	
Relative to V _{SS}	-0.3V to +2.8V
Voltage on V _{DD} Supply	
Relative to V _{SS}	-0.3V to +2.1V
Voltage on V _{DDQ} Supply	
Relative to V _{SS}	-0.3V to +2.1V
Junction Temperature**	110°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

Table 20: DC Electrical Characteristics and Operating Conditions

(+0°C ≤ T_J ≤ +100°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V _{EXT}	2.38	2.63	V	1
Supply Voltage		V _{DD}	1.7	1.9	V	1, 4
Isolated Output Buffer Supply		V _{DDQ}	1.4	V _{DD}	V	1, 4, 5
Reference Voltage		V _{REF}	0.49 x V _{DDQ}	0.51 x V _{DDQ}	V	1–3, 8
Termination Voltage		V _{TT}	0.95 x V _{REF}	1.05 x V _{REF}	V	9, 10
Input High (Logic 1) Voltage		V _{IH}	V _{REF} + 0.1	V _{DDQ} + 0.3	V	1, 4
Input Low (Logic 0) Voltage		V _{IL}	V _{SSQ} - 0.3	V _{REF} - 0.1	V	1, 4
Output High Current	V _{OH} = V _{DDQ} /2	I _{OH}	(V _{DDQ} /2) (1.15 x RQ/5)	(V _{DDQ} /2) (0.85 x RQ/5)	mA	6, 7, 11
Output Low Current	V _{OL} = V _{DDQ} /2	I _{OL}	(V _{DDQ} /2) (1.15 x RQ/5)	(V _{DDQ} /2) (0.85 x RQ/5)	mA	6, 7, 11
Clock Input Leakage Current	0V ≤ V _{IN} ≤ V _{DD}	I _{LC}	-5	5	μA	
Input Leakage Current	0V ≤ V _{IN} ≤ V _{DD}	I _{LI}	-5	5	μA	
Output Leakage Current	0V ≤ V _{IN} ≤ V _{DDQ}	I _{LO}	-5	5	μA	
Reference Voltage Current		I _{REF}	-5	5	μA	

- NOTE:**
1. All voltages referenced to V_{SS} (GND).
 2. Typically the value of V_{REF} is expect to be 0.5 x V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}.
 3. Peak-to-peak AC noise on V_{REF} must not exceed 2% V_{REF}(DC).
 4. Overshoot: V_{IH}(AC) ≤ V_{DD} + 0.7V for t ≤ t_{CK}/2.
Undershoot: V_{IL}(AC) ≥ -0.5V for t ≤ t_{CK}/2.
During normal operation, V_{DDQ} must not exceed V_{DD}.
Control input signals may not have pulse widths less than t_{CK}/2 or operate at frequencies exceeding t_{CK} (MAX).
 5. V_{DDQ} can be set to a nominal 1.5V ± 0.1V or 1.8V ± 0.1V supply
 6. I_{OH} and I_{OL} are defined as absolute values and are measured at V_{DDQ}/2. I_{OH} flows from the device, I_{OL} flows into the device.
 7. If MRS bit A8 is 0, use RQ = 250Ω in the equation in lieu of presence of an external impedance matched resistor.
 8. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2% of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±2%V_{DDQ}/2 for DC error and an additional ±2%V_{DDQ}/2 for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
 9. V_{TT} is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
 10. On-die termination may be selected using mode register bit 9 (see Mode Register Bit Map on page 10). A resistance R_{TT} from each data input signal to the nearest V_{TT} can be enabled. R_{TT} = 150Ω (± 10%) at 70°C T_J.
 11. For V_{OL} and V_{OH}, refer to the Spice Model fro the RLD RAM II Command Driver.

**Table 21: AC Electrical Characteristics and Operating Conditions**
 (+0°C ≤ T_J ≤ +100°C; +1.7V ≤ V_{DD} ≤ +1.9V, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Matched Impedance Mode	V _{IH}	V _{REF} + 0.2	V _{DDQ} + 0.2	V	
Input Low (Logic 0) Voltage	Matched Impedance Mode	V _{IL}	V _{SSQ} - 0.2	V _{REF} - 0.2	V	

Table 22: Capacitance

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Address/Control Input Capacitance	T _A = 25°C; f = 1 MHz	C _I	1.5	2.5	pF	
Input/Output Capacitance (DQ)		C _O	3.0	4.0	pF	
Clock Capacitance		C _{CK}	2.0	3.0	pF	

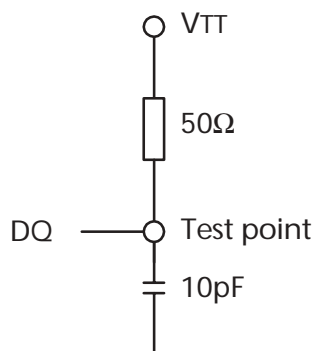
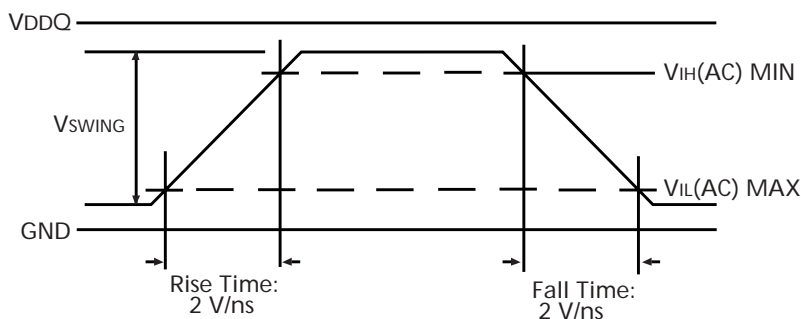
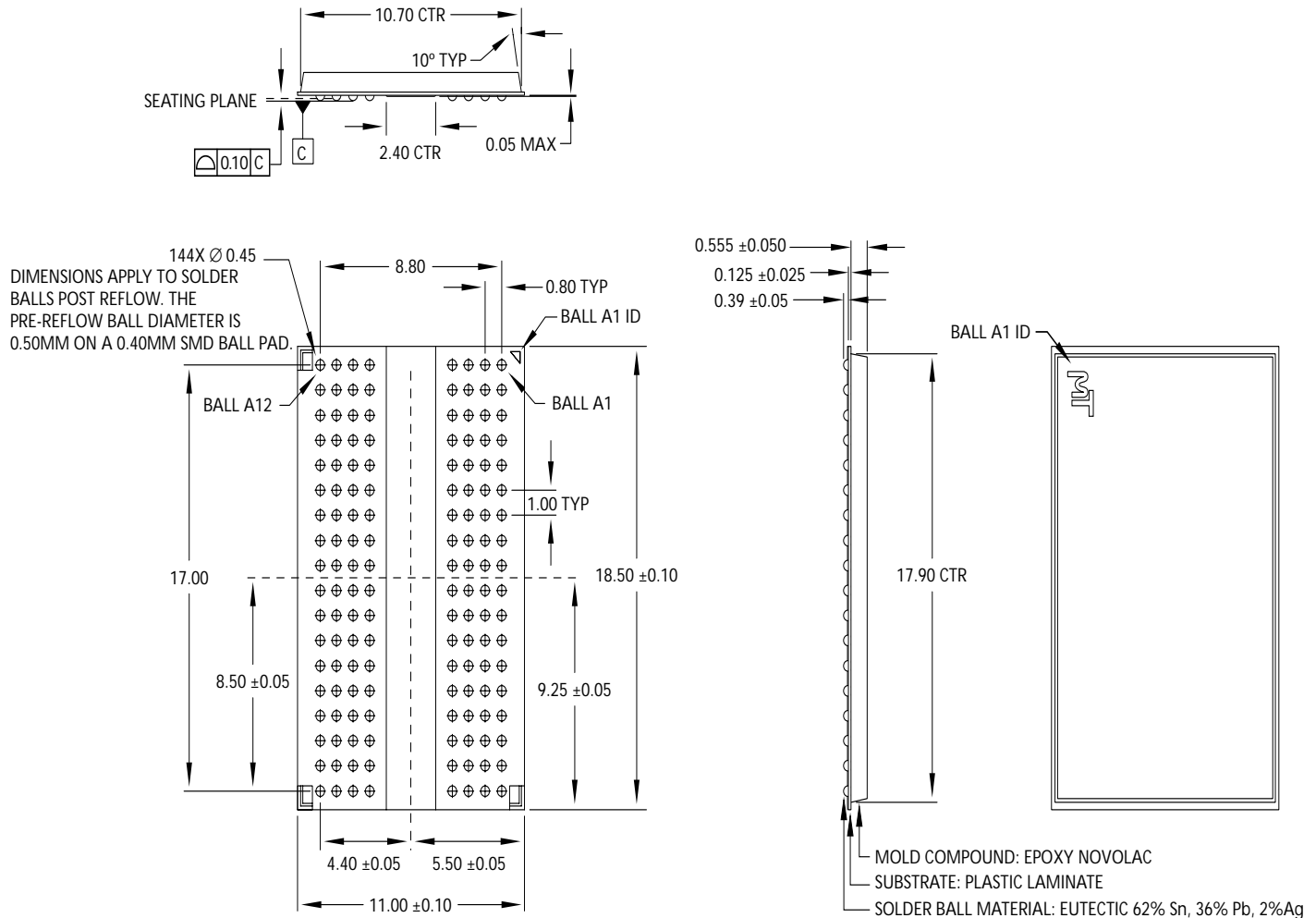
Figure 41
Output Test Conditions

Figure 42
Input Waveform



Table 13: I_{DD} Operating Conditions and Maximum Limits

(+0°C ≤ T_J ≤ +100°C; V_{DD} = MAX, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MAX			UNIT	NOTES
			-2.5	-3.3	-5		
Standby Current	^t CK = Idle All banks idle, no inputs toggling	I _{SB1} (V _{DD})	TBD	TBD	TBD	mA	
		I _{SB1} (V _{EXT})	TBD	TBD	TBD	mA	
Standby Current	^t CK = MIN, CS# = 1 No commands	I _{SB2} (V _{DD})	TBD	TBD	TBD	mA	
		I _{SB2} (V _{EXT})	TBD	TBD	TBD	mA	
Incremental Current	BL = 2, ^t CK = MIN, ^t RC = MIN, 1 bank active	I _{DD1} (V _{DD})	TBD	TBD	TBD	mA	
		I _{DD1} (V _{EXT})	TBD	TBD	TBD	mA	
Incremental Current	BL = 4, ^t CK = MIN, ^t RC = MIN, 1 bank active	I _{DD2} (V _{DD})	TBD	TBD	TBD	mA	
		I _{DD2} (V _{EXT})	TBD	TBD	TBD	mA	
Incremental Current	BL = 8, ^t CK = MIN, ^t RC = MIN, 1 bank active	I _{DD3} (V _{DD})	TBD	TBD	TBD	mA	
		I _{DD3} (V _{EXT})	TBD	TBD	TBD	mA	
Refresh Current	^t CK = MIN	I _{REF} (V _{DD})	TBD	TBD	TBD	mA	
		I _{REF} (V _{EXT})	TBD	TBD	TBD	mA	
Operating Supply Current Example	BL = 4, ^t CK = MIN, ^t RC = MIN, 4 banks interleave, address change up to 8 times during minimum ^t RC, continuous data	I _{DD4R} (V _{DD})	TBD	TBD	TBD	mA	
		I _{DD4R} (V _{EXT})	TBD	TBD	TBD	mA	

Figure 43
144-Ball FBGA



NOTE: 1. All dimensions in millimeters.

DATA SHEET DESIGNATION

Advance: This data sheet contains initial descriptions of products still under development.



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**REVISION HISTORY**

Rev. 4, Pub. 5/03	5/03
• JTAG numbering order has been reversed. (Page 42)	