FPM DRAM

MT4C1M16C3, MT4LC1M16C3

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/datasheets

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts, and packages
- High-performance, low-power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or 5V ±0.5V)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- Optional self refresh (S) for low-power data retention
- BYTE WRITE and BYTE READ access cycles
- 1,024-cycle refresh (10 row, 10 column addresses)
- FAST-PAGE-MODE (FPM) access

OPTIONS / MARKING

- Voltage[1]
  - 3.3V — LC
  - 5V — C
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Timing
  - 50ns access — -5
  - 60ns access — -6
- Refresh Rates
  - Standard Refresh (16ms period) — None
  - Self Refresh (128ms period) — S[2]
- Operating Temperature Range
  - Commercial (0°C to +70°C) — None
  - Extended (-20°C to +80°C) — ET[3]

Part Number Example:
MT4LC1M16C3DJ-5

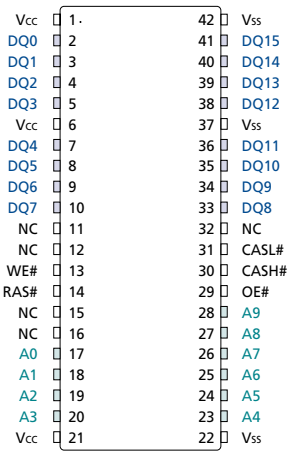
NOTE: 1. The third field distinguishes the low voltage offering: LC designates V_{CC} = 3.3V and C designates V_{CC} = 5V.
2. Contact factory for availability.
3. Available only on MT4C1M16C3 (5V)

KEY TIMING PARAMETERS

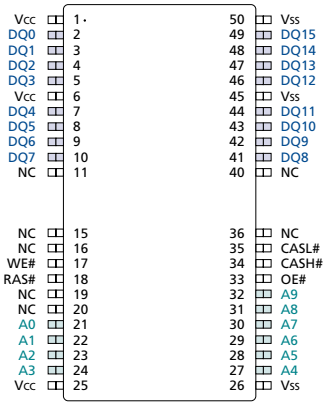
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-5	84ns	50ns	20ns	25ns	15ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Top View)

42-Pin SOJ



44/50-Pin TSOP



NOTE: The # symbol indicates signal is active LOW.

1 MEG x 16 FPM DRAM PART NUMBERS

PART NUMBER	SUPPLY	PACKAGE	REFRESH
MT4LC1M16C3DJ-6	3.3V	SOJ	Standard
MT4LC1M16C3DJ-6 S	3.3V	SOJ	Self
MT4LC1M16C3TG-6	3.3V	TSOP	Standard
MT4LC1M16C3TG-6 S	3.3V	TSOP	Self
MT4C1M16C3DJ-6	5V	SOJ	Standard
MT4C1M16C3TG-6	5V	TSOP	Standard

GENERAL DESCRIPTION

The 1 Meg x 16 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x16 configuration. The 1 Meg x 16 DRAM has both BYTE WRITE and WORD WRITE access cycles via two CAS# pins (CASL# and CASH#). These function identically to a single CAS# on other DRAMs in that either CASL# or CASH# will generate an internal CAS#.

The CAS# function and timing are determined by the first CAS# (CASL# or CASH#) to transition LOW and

GENERAL DESCRIPTION (continued)

the last CAS# to transition back HIGH. Use of only one of the two results in a BYTE access cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ0-DQ7), and CASH# transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15).

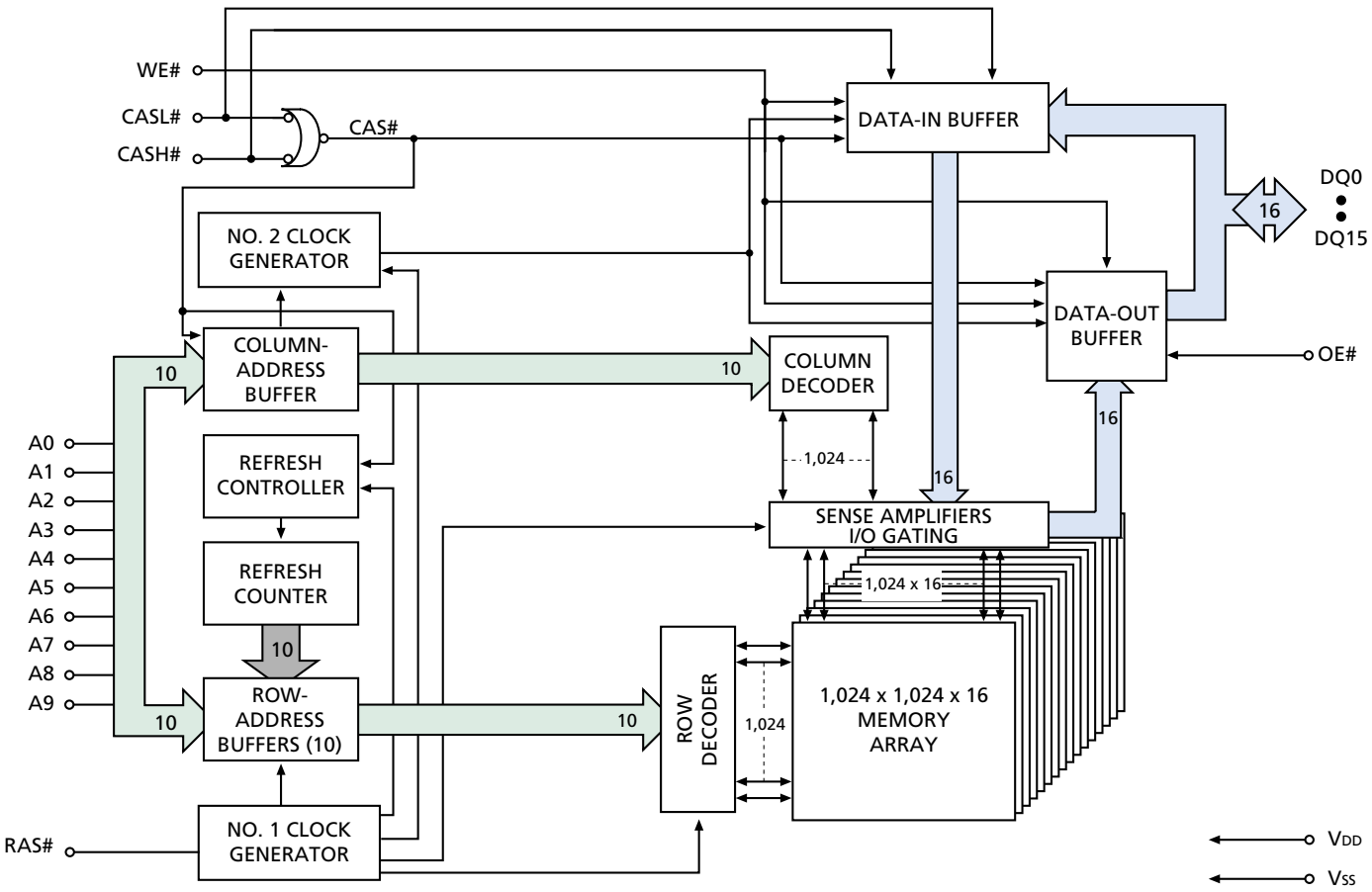
Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered ten bits (A0-A9) at a time. RAS# is used to latch the first ten bits and CAS# the latter ten bits. The CAS# function is determined by the first CAS# (CASL# or CASH#) to transition LOW and the last one to transition back HIGH. The CAS# function also determines whether the cycle will be a refresh cycle (RAS#-ONLY) or an active cycle (READ, WRITE, or READ-WRITE) once RAS# goes LOW.

The CASL# and CASH# inputs internally generate a CAS# signal that functions identically to a single CAS# input on other DRAMs. The key difference is that each CAS# input (CASL# and CASH#) controls its corresponding DQ tristate logic (in conjunction with OE# and WE#). CASL# controls DQ0-DQ7 and CASH# controls DQ8-DQ15. The two CAS# controls give the 1 Meg x 16 DRAM BYTE WRITE cycle capabilities.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS, whichever occurs last. Taking WE# LOW will initiate a WRITE cycle, selecting DQ0-DQ15. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle. If WE# goes LOW after CAS# goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS# and OE# remain LOW (regardless of WE# or RAS#). This late WE# pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE# and WE#.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION (continued)

The MT4LC1M16C3 must be refreshed periodically in order to retain stored data.

FAST PAGE MODE ACCESS

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standbylevel. The chip is also preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing anyRAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS# ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS# addresses (A0-A9) are executed at least every 16ms (128ms on the "S" version), regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of CASL# and CASH#. Enabling CASL# will select a lower byte access (DQ0-DQ7), while enabling CASH# will select an upper byte access (DQ0-DQ15). Enabling both CASL# and CASH# selects a WORD WRITE cycle.

The 1 Meg x 16 DRAM may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS# inputs. Figure 1 illustrates the BYTE WRITE and WORD WRITE cycles. Figure 2 illustrates BYTE READ and WORD READ cycles.

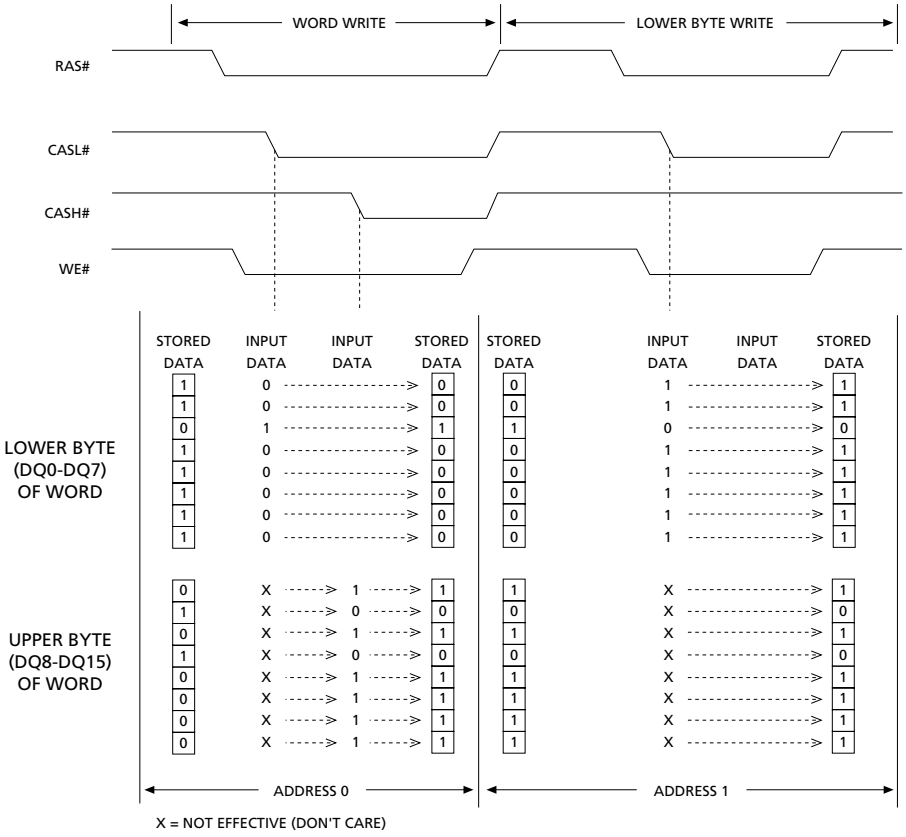


Figure 1
WORD and BYTE WRITE Example

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle. However, an EARLY WRITE on one byte and a LATE WRITE on the other byte, after a CAS# precharge has been satisfied, are permissible.

DRAM REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS# addresses are executed within ^{t}REF (MAX), regardless of sequence. The CBR and EXTENDED and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.

An optional self refresh mode is available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 125µs per row, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst CBR refresh sequence, all 1,024 rows must be refreshed using a minimum ^{t}RC refresh rate prior to resuming normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

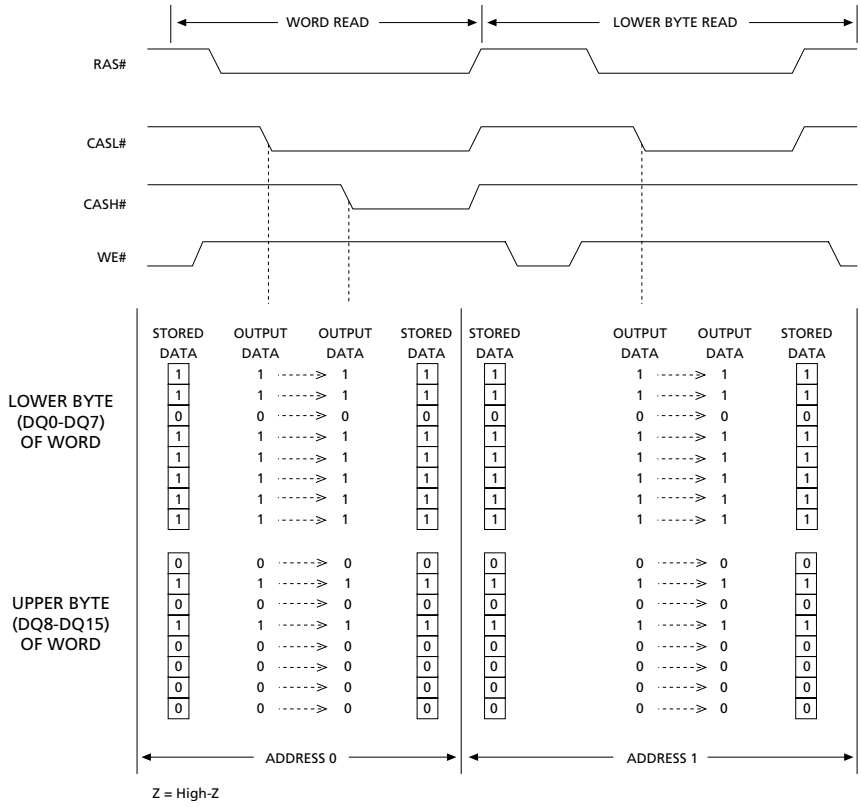


Figure 2
WORD and BYTE READ Example

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS}
- 3.3V ..... -1V to +4.6V
- 5V ..... -1V TO +7V

Voltage on NC, Inputs or I/O Pins Relative to V_{SS}
- 3.3V ..... -1V to +5.5V
- 5V ..... -1V TO +7V

Operating Temperature
- T_A (commercial) ..... 0°C to +70°C
- T_A (extended "ET") ..... -20°C to +80°C

Storage Temperature (plastic) ..... -55°C to +150°C

Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6; notes can be found on page 9); V_{CC} (MIN) ≤ V_{CC} ≤ V_{CC} (MAX)

		3.3V		5V			
PARAMETER/CONDITION	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{CC}	3	3.6	4.5	5.5	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2	5.5	2.4	V_{CC} + 1	V	
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-1.0	0.8	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: Any input at V_{IN} (0V ≤ V_{IN} ≤ V_{CC} + 0.3V); All other pins not under test = 0V	I_I	-2	2	-2	2	µA	
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA	V_{OH}	2.4	–	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA	V_{OL}	–	0.4	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V_{OUT} [0V ≤ V_{OUT} ≤ V_{CC} (MAX)]; DQ is disabled and in High-Z state	I_{OZ}	-5	5	-5	5	µA	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 6; notes can be found on page 9); V_{CC} (MIN) ≤ V_{CC} ≤ V_{CC} (MAX)

PARAMETER/CONDITION	SYMBOL	SPEED	3.3V	5V	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	ALL	1	2	mA	
STANDBY CURRENT: CMOS (non-"S" version only) (RAS# = CAS# = other inputs = V_{CC} - 0.2V)	I_{CC2}	ALL	500	500	µA	
STANDBY CURRENT: CMOS ("S" version only) (RAS# = CAS# = other inputs = V_{CC} - 0.2V)	I_{CC2}	ALL	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC3}	-5 -6	180 170	190 180	mA	23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{CC4}	-5 -6	110 90	120 110	mA	23
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{CC5}	-5 -6	180 170	190 180	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC6}	-5 -6	180 170	180 180	mA	4, 7
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^{t}RAS (MIN); WE# = V_{CC} - 0.2V; A0-A11, OE# and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC7}	ALL	300	300	µA	4, 7
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# $^{t}RASS$ (MIN) and CAS# held LOW; WE# = V_{CC} - 0.2V; A0-A11, OE# and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	ALL	300	300	µA	4, 7

CAPACITANCE

(Note: 2; notes can be found on page 9);

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: Addresses	C_{I1}	5	pF
Input Capacitance: RAS#, CASL#, CASH#, WE#, OE#	C_{I2}	7	pF
Input/Output Capacitance: DQ	C_{IO}	7	pF

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12; notes can be found on page 9); V_{CC} (MIN) ≤ V_{CC} ≤ V_{CC} (MAX)

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		25		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	27
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	42		49		ns	18
Access time from CAS	^tCAC		15		15	ns	29
Column-address hold time	^tCAH	8		10		ns	27
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	32, 35
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	4, 28
Last CAS# going LOW to first CAS# to return HIGH	^tCLCH	10		10		ns	30
CAS# to output in Low-Z	^tCLZ	0		0		ns	26, 29
CAS# precharge time	^tCP	8		5		ns	30
Access time from CAS# precharge	^tCPA		28		35	ns	28
CAS# to RAS# precharge time	^tCRP	5		5		ns	28
CAS# hold time	^tCSH	38		45		ns	28
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4, 27
CAS# to WE# delay time	^tCWD	28		35		ns	18, 27
WRITE command to CAS# lead time	^tCWL	8		10		ns	23, 29
Data-in hold time	^tDH	8		10		ns	19, 29
Data-in setup time	^tDS	0		0		ns	19, 29
Output disable	^tOD	0	12	0	15	ns	17, 26, 29
Output enable	^tOE		12		15	ns	22
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	20
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	11, 17, 23
OE# setup prior to RAS# during HIDDEN Refresh cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	31
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	47		56		ns	31
Access time from RAS#	^tRAC		50		60	ns	
RAS# to column-address delay time	^tRAD	9		12		ns	20
Row-address hold time	^tRAH	9		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
RAS# pulse width (Self Refresh)	^tRASS	100		100		µs	
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	11		14		ns	14, 27
READ command hold time (referenced to CAS)	^tRCH	0		0		ns	16, 28
READ command setup time	^tRCS	0		0		ns	27
Refresh period (1,024 cycles)	^tREF		16		16	ms	
Refresh period (1,024 cycles) "S" version	^tREF		128		128	ms	
RAS# precharge time	^tRP	30		40		ns	
RAS# to CAS# precharge time	^tRPC	5		5		ns	
RAS# precharge time (Self Refresh)	^tRPS	90		105		ns	
READ command hold time (referenced to RAS#)	^tRRH	0		0		ns	16
RAS# hold time	^tRSH	13		15		ns	36
READ-WRITE cycle time	^tRWC	116		140		ns	

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12; notes can be found on page 9); V_{CC} (MIN) ≤ V_{CC} ≤ V_{CC} (MAX)

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
RAS# to WE# delay time	^{t}RWD	67		79		ns	18
WRITE command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
WRITE command hold time	^{t}WCH	8		10		ns	36
WRITE command hold time (referenced to RAS#)	^{t}WCR	38		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	18, 27
WRITE command pulse width	^{t}WP	5		5		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	8		10		ns	

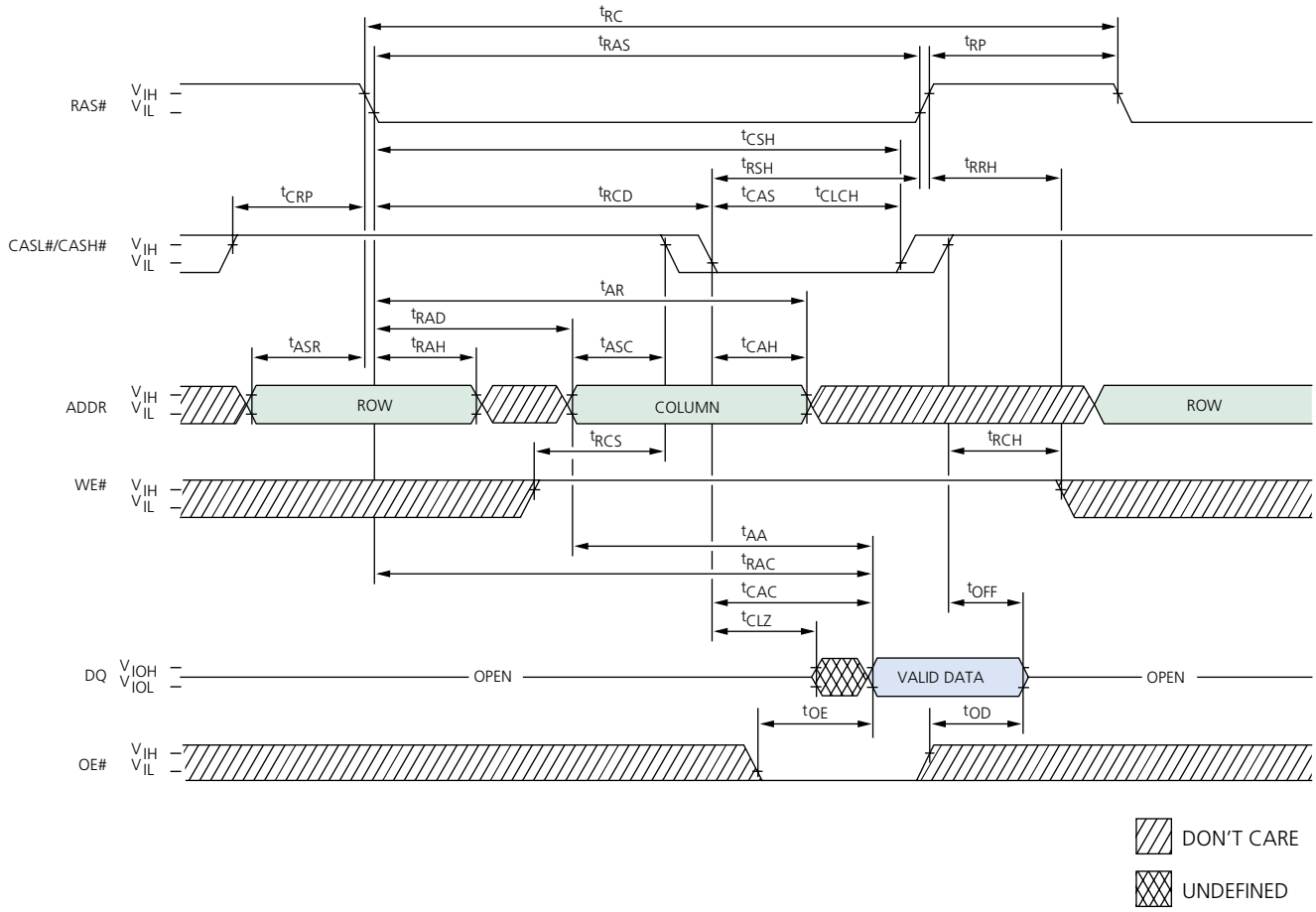
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V or 5.0V; f = 1 MHz.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the output open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) for commercial and (-20°C ≤ T_A ≤ 80°C) for extended "ET" is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC, and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
18. ^{t}WCS, ^{t}RWD, ^{t}AWD, and ^{t}CWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data out-put will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS# or OE# goes back to V_{IH}) is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. During a READ cycle, if OE# is LOW then taken HIGH before CAS# goes HIGH, Q goes open. If OE# is tied permanently LOW, LATE WRITE and READ-MODIFY-WRITE operations are not permissible and should not be attempted.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. All other inputs at 0.2V or V_{CC} - 0.2V.
23. Column address changed once each cycle.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^{t}OEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
25. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur.
26. The 3ns minimum is a parameter guaranteed by design.
27. The first CASx edge to transition LOW.
28. The last CASx edge to transition HIGH.
29. Output parameter (DQx) is referenced to corresponding CAS# input; DQ0-DQ7 by CASL# and DQ8-DQ15 by CASH#.
30. Last falling CASx edge to first rising CASx edge.
31. Last rising CASx edge to next cycle's last rising CASx edge.

NOTES (continued)

32. Last rising CASx edge to first falling CASx edge.
33. First DQs controlled by the first CASx to go LOW.
34. Last DQs controlled by the last CASx to go HIGH.
35. Each CASx must meet minimum pulse width.
36. Last CASx to go LOW.
37. All DQs controlled, regardless CASL# and CASH#.
38. If OE# is tied permanently LOW, LATE WRITE, or READ-MODIFY-WRITE operations are not permissible and should not be attempted.

READ CYCLE

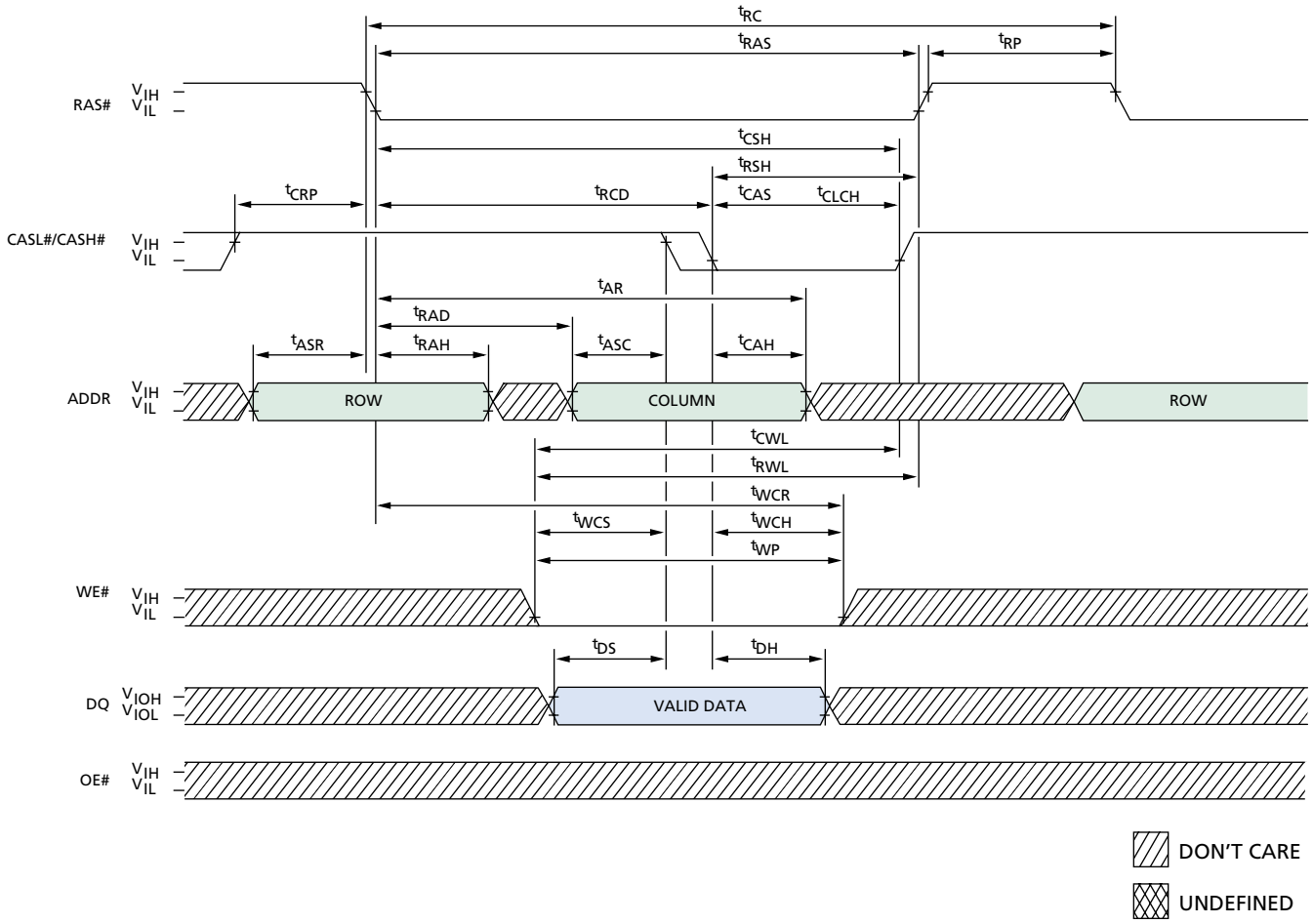


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	0	12	0	15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EARLY WRITE CYCLE

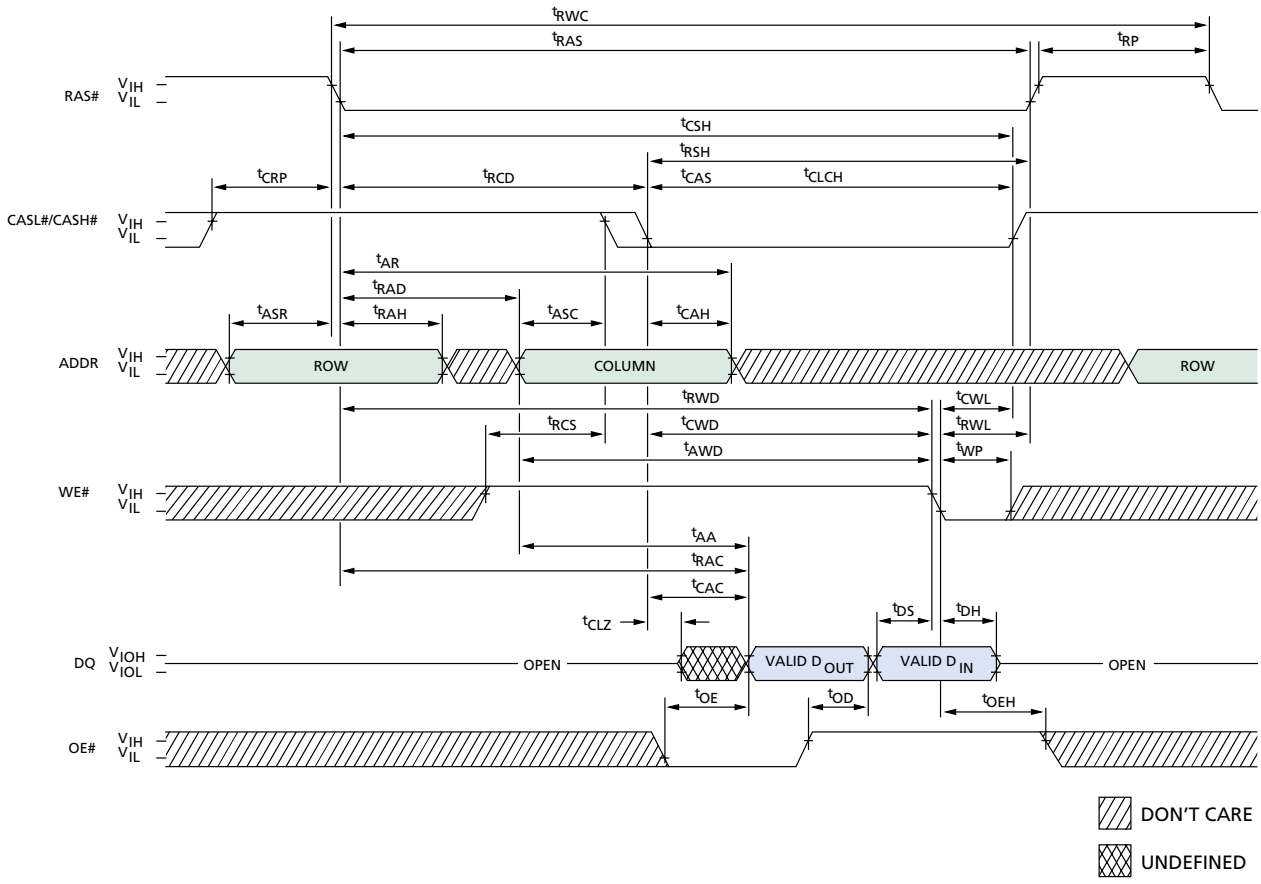


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	10		10		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD	9		12		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

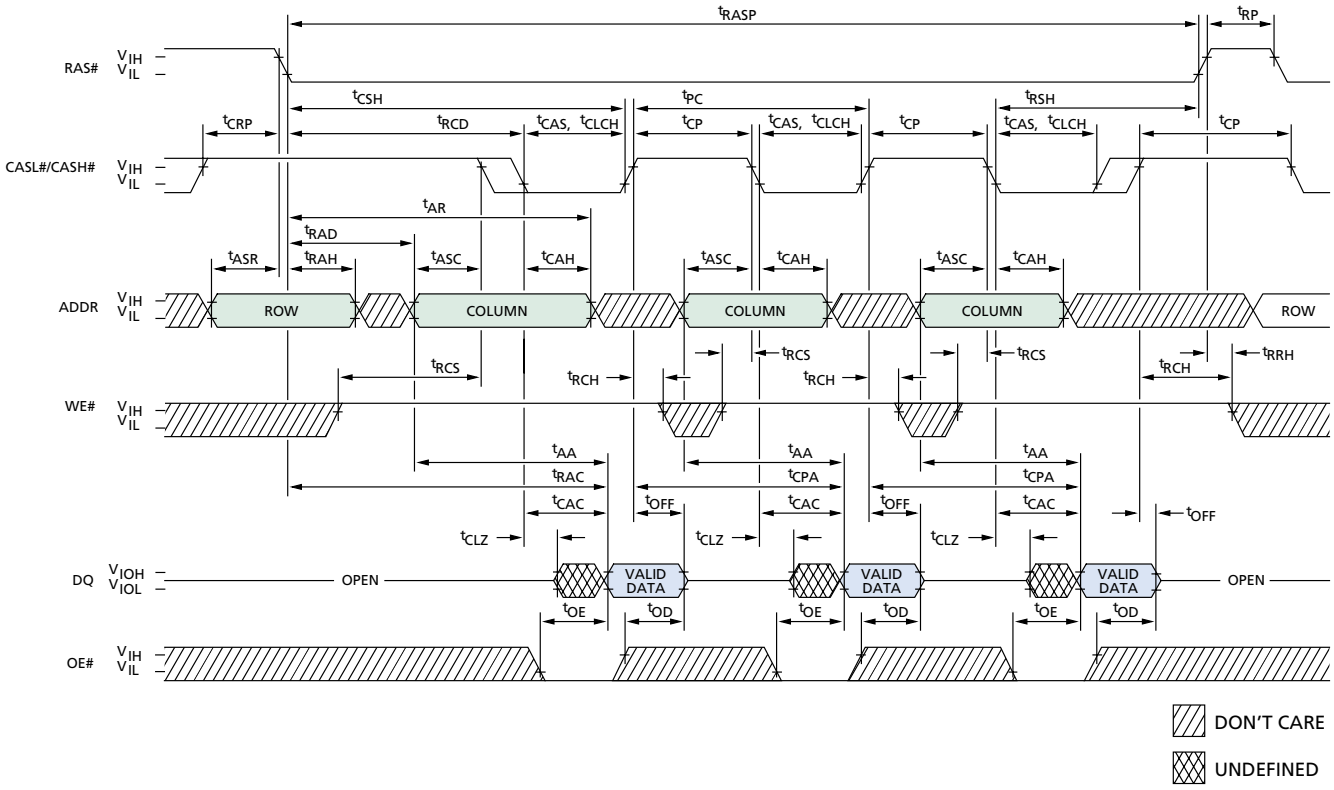


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		15		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	116		140		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

FAST-PAGE-MODE READ CYCLE

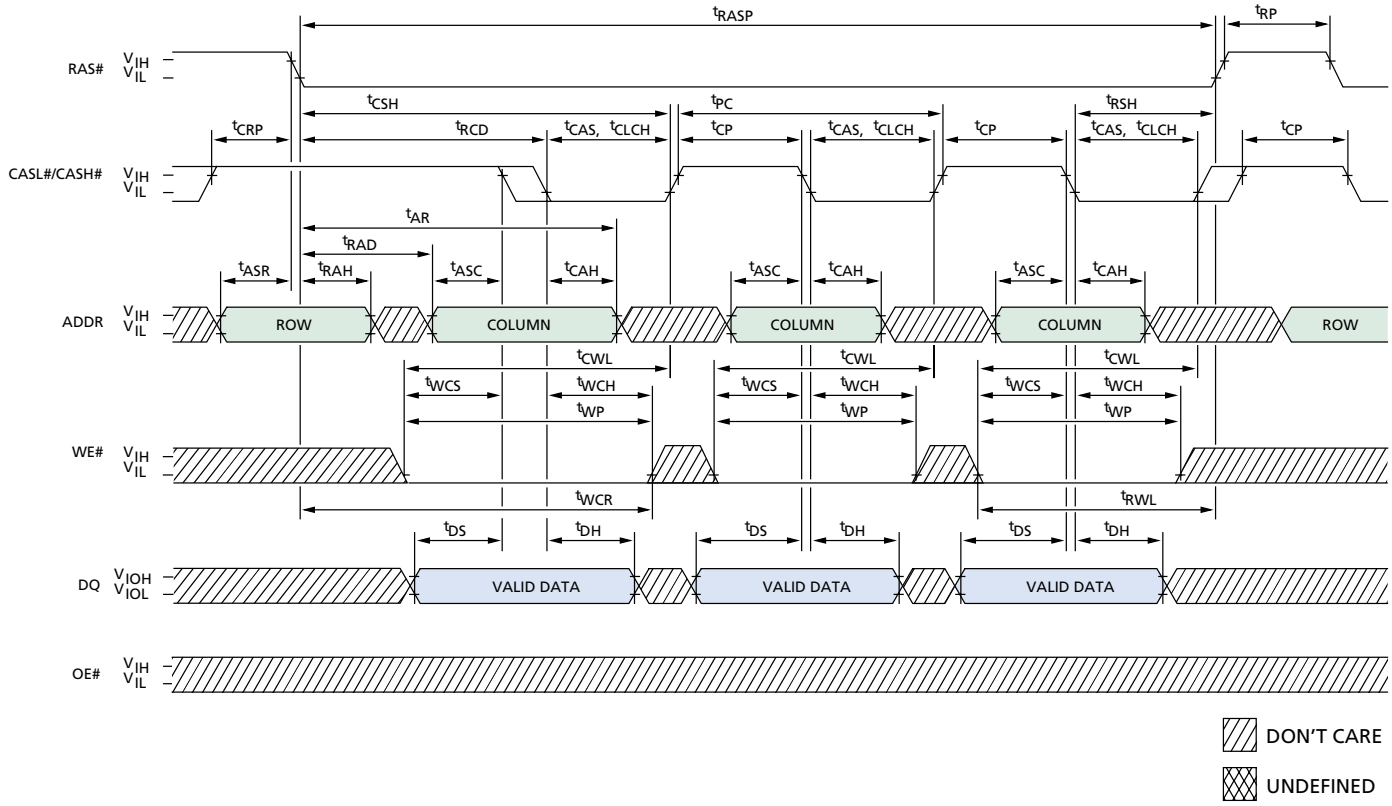


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCP	8		5		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

FAST-PAGE-MODE EARLY WRITE CYCLE



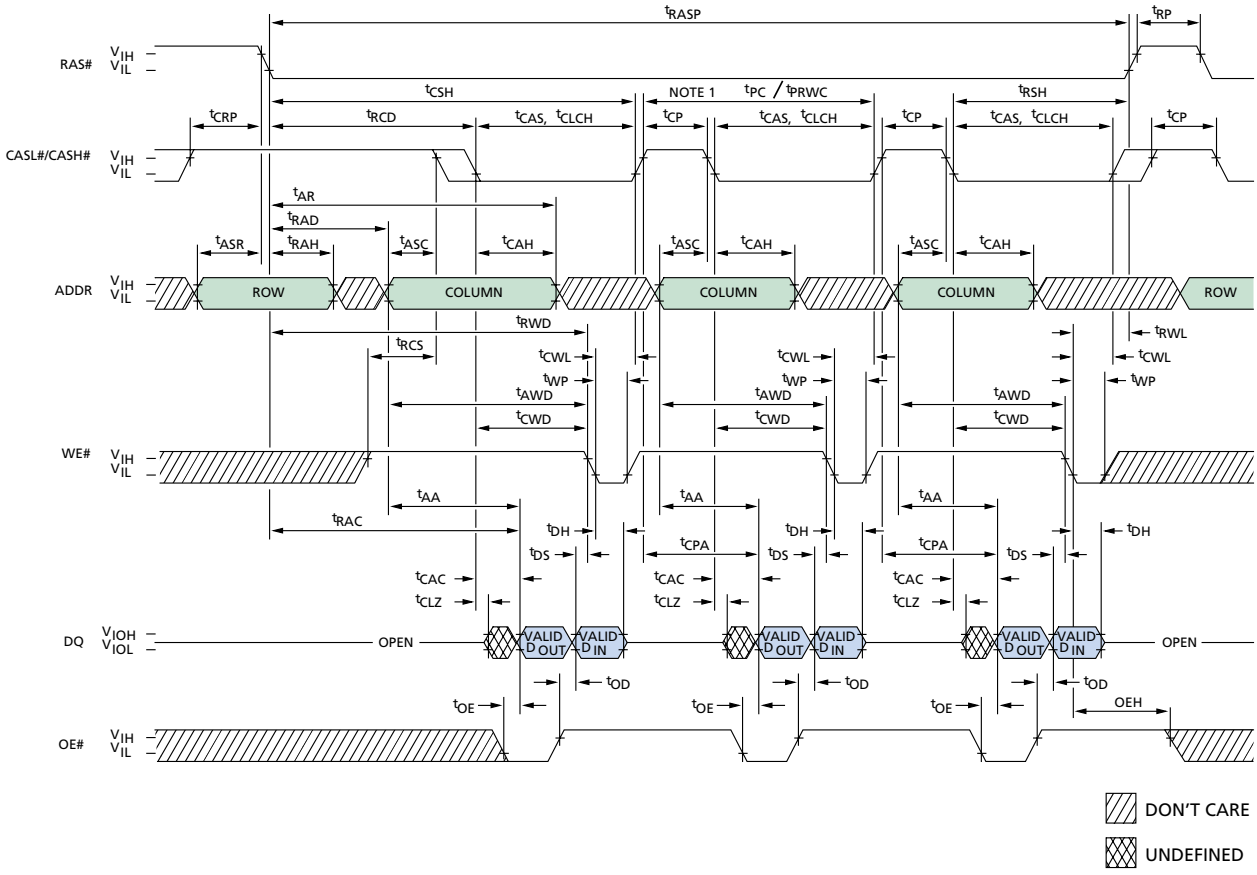
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	10		10		ns
tCP	8		5		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tPC	20		25		ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

FAST-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



TIMING PARAMETERS

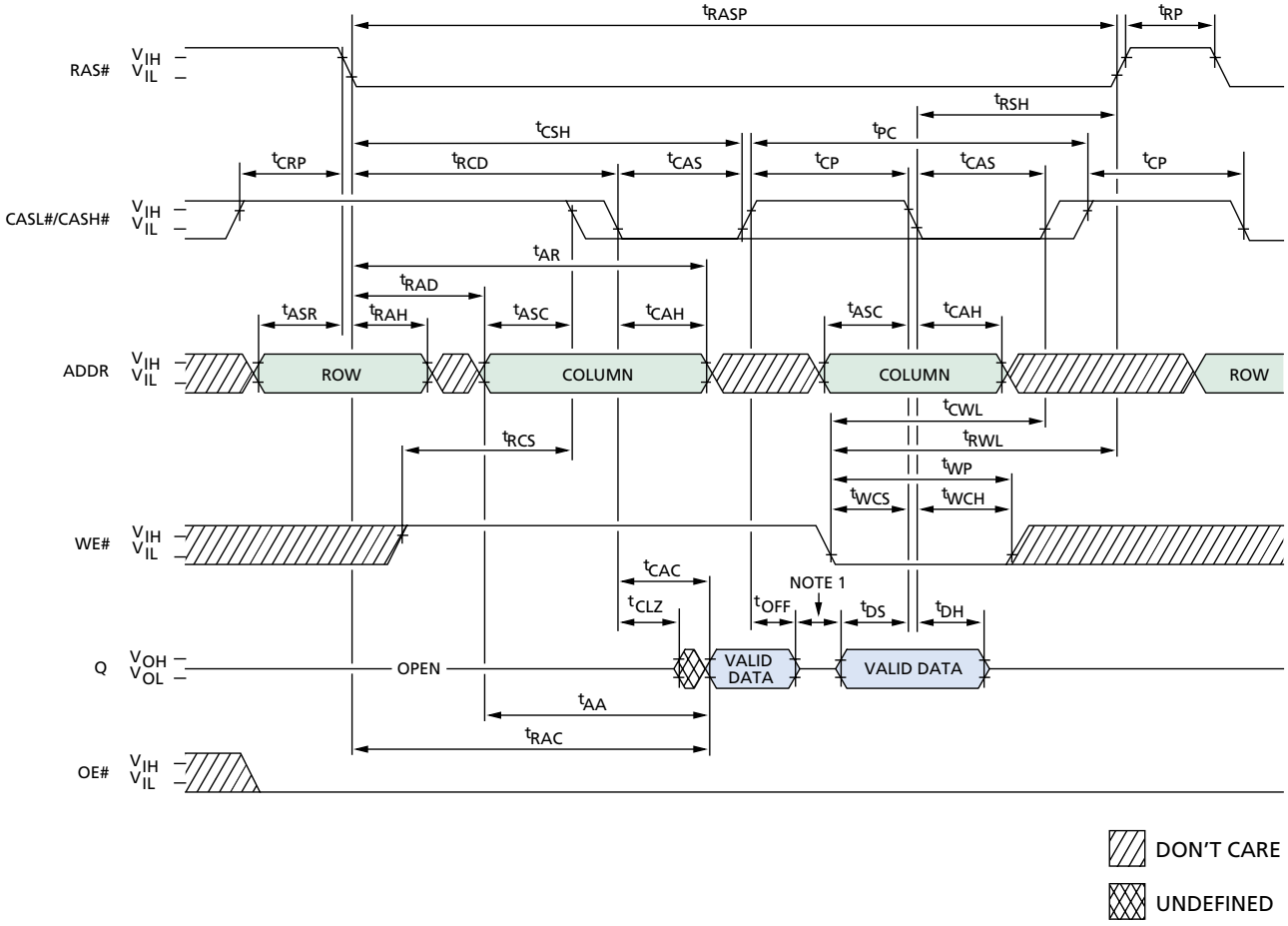
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		15		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	10		10		ns
tCLZ	0		0		ns
tCP	8		5		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tPC	20		25		ns
tPRWC	47		56		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

NOTE: 1. tPC is for LATE WRITE only.

FAST-PAGE-MODE READ EARLY WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)



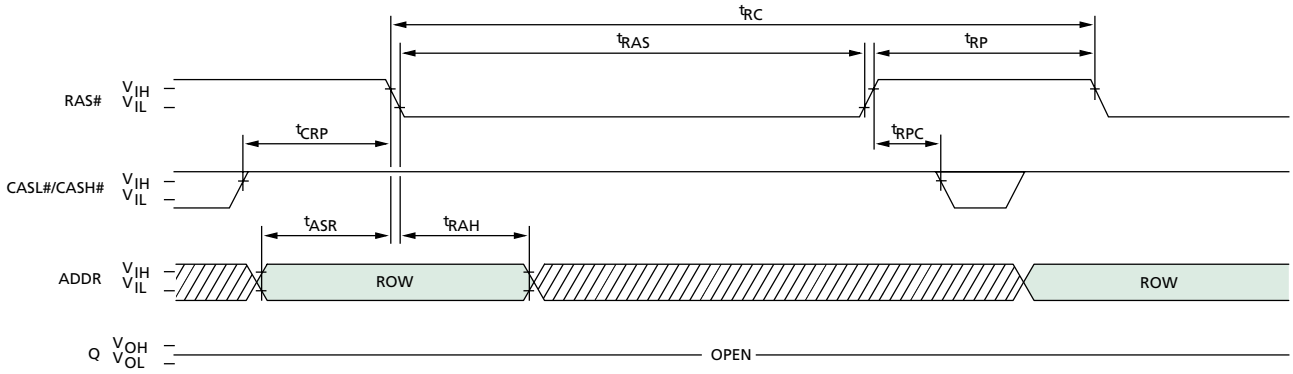
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		5		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

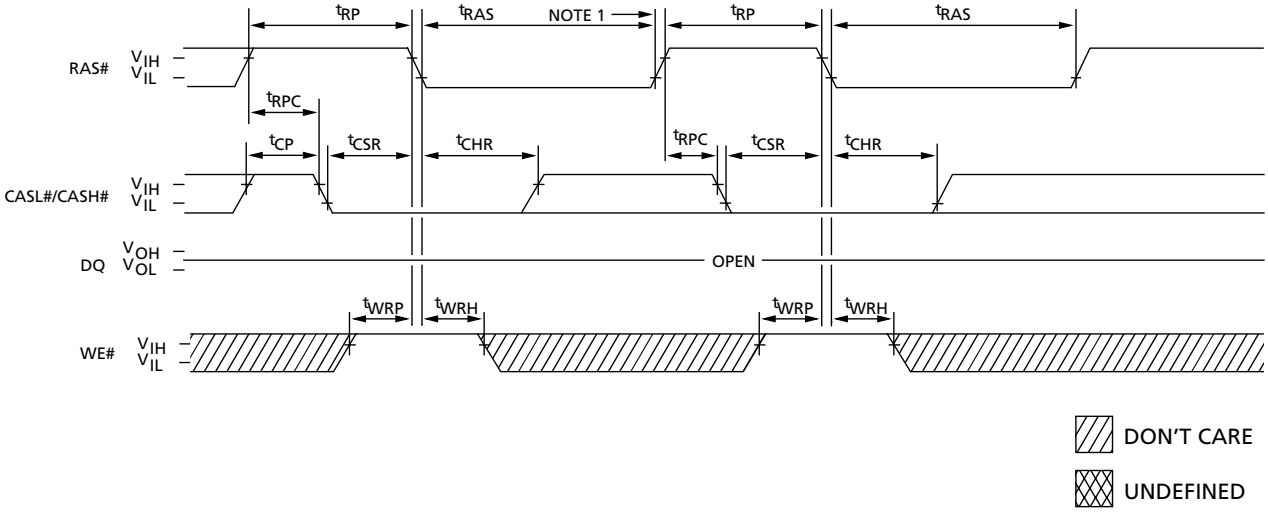
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWP	5		5		ns

NOTE: 1. tPC is for LATE WRITE only.

RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



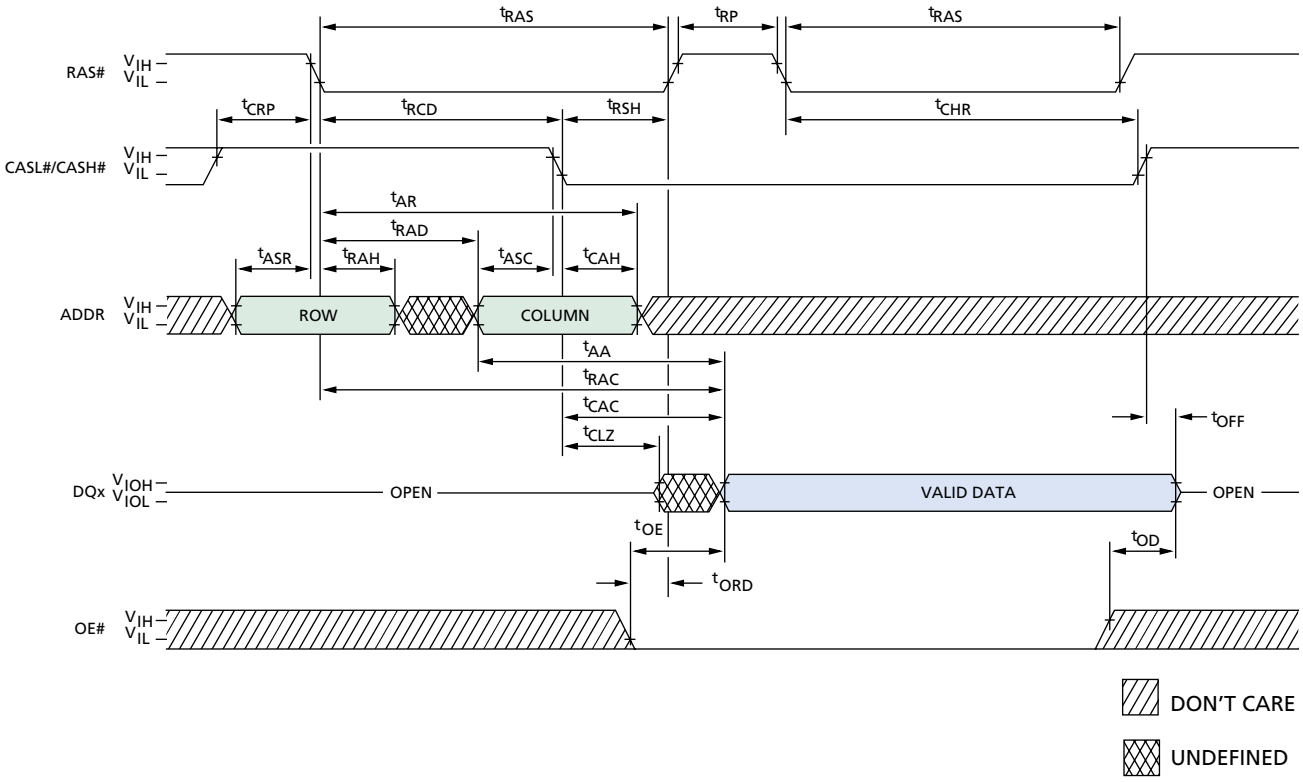
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR	8		10		ns
tCP	8		5		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	9		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAS	50		60	10,000	ns
tRC	84		104		ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTE: 1. End of CBR REFRESH cycle.

HIDDEN REFRESH CYCLE [1]
(WE# = HIGH; OE# = LOW)



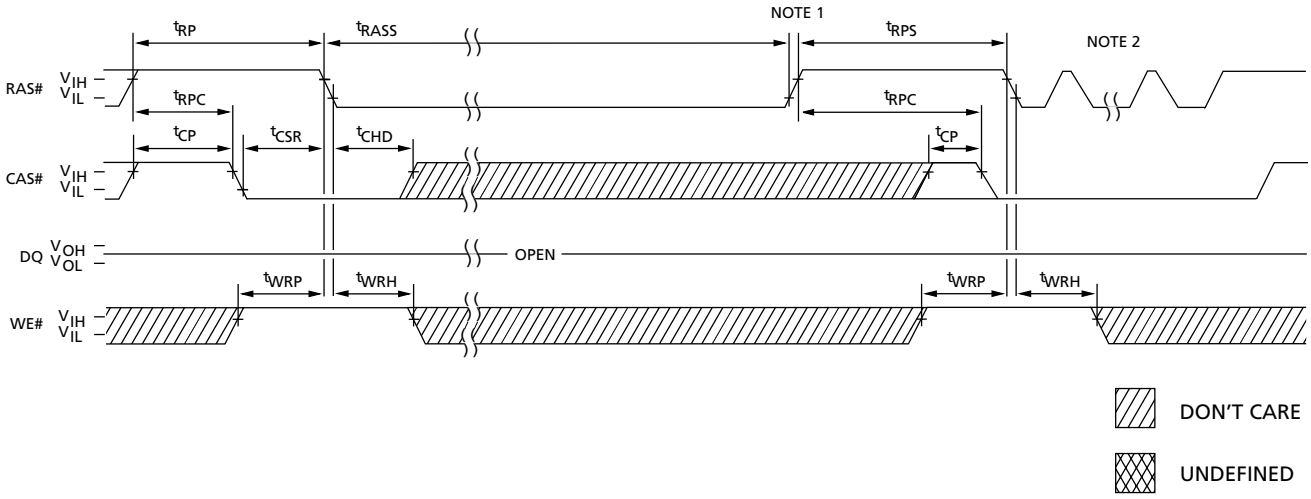
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



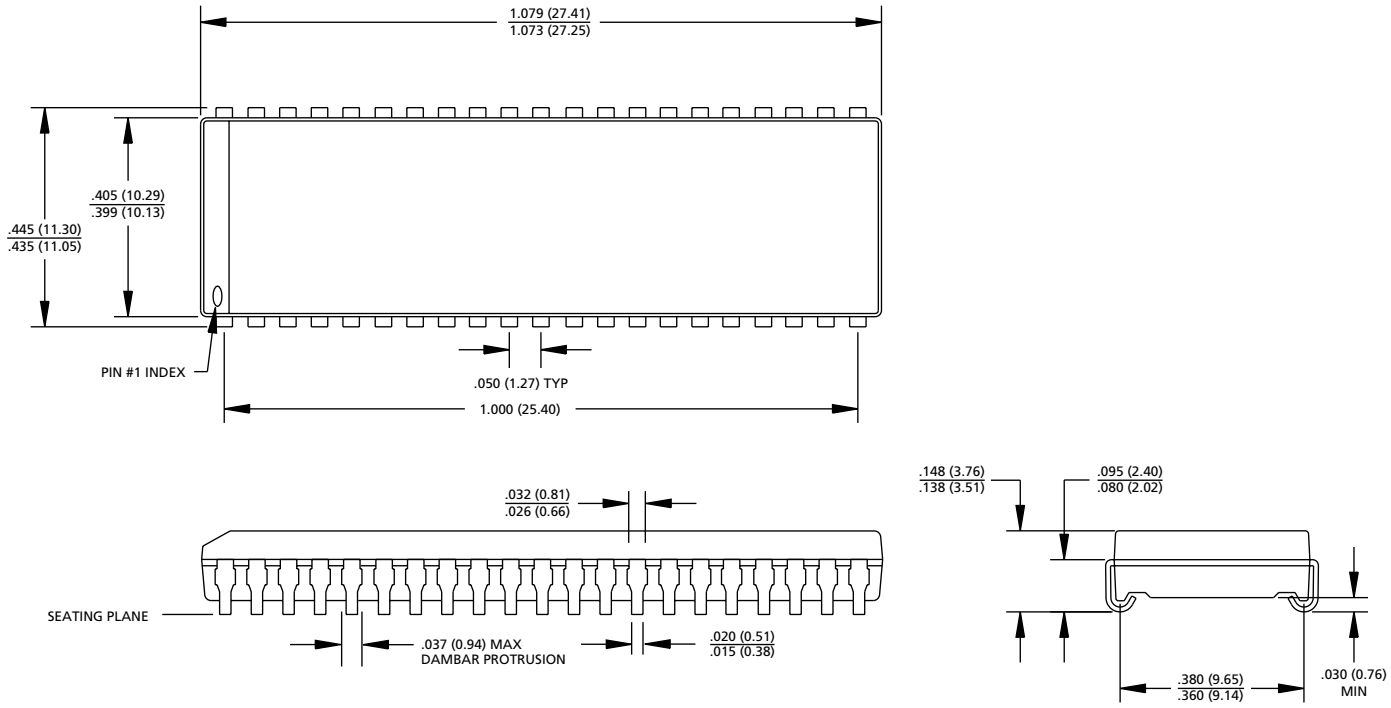
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCHD	15		15		ns
tCLCH	10		10		ns
tCP	8		5		ns
tCSR	5		5		ns
tRASS	100		100		µs

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRP	30		40		ns
tRPC	5		5		ns
tRPS	90		105		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed if RAS#-only or burst CBR refresh is used.

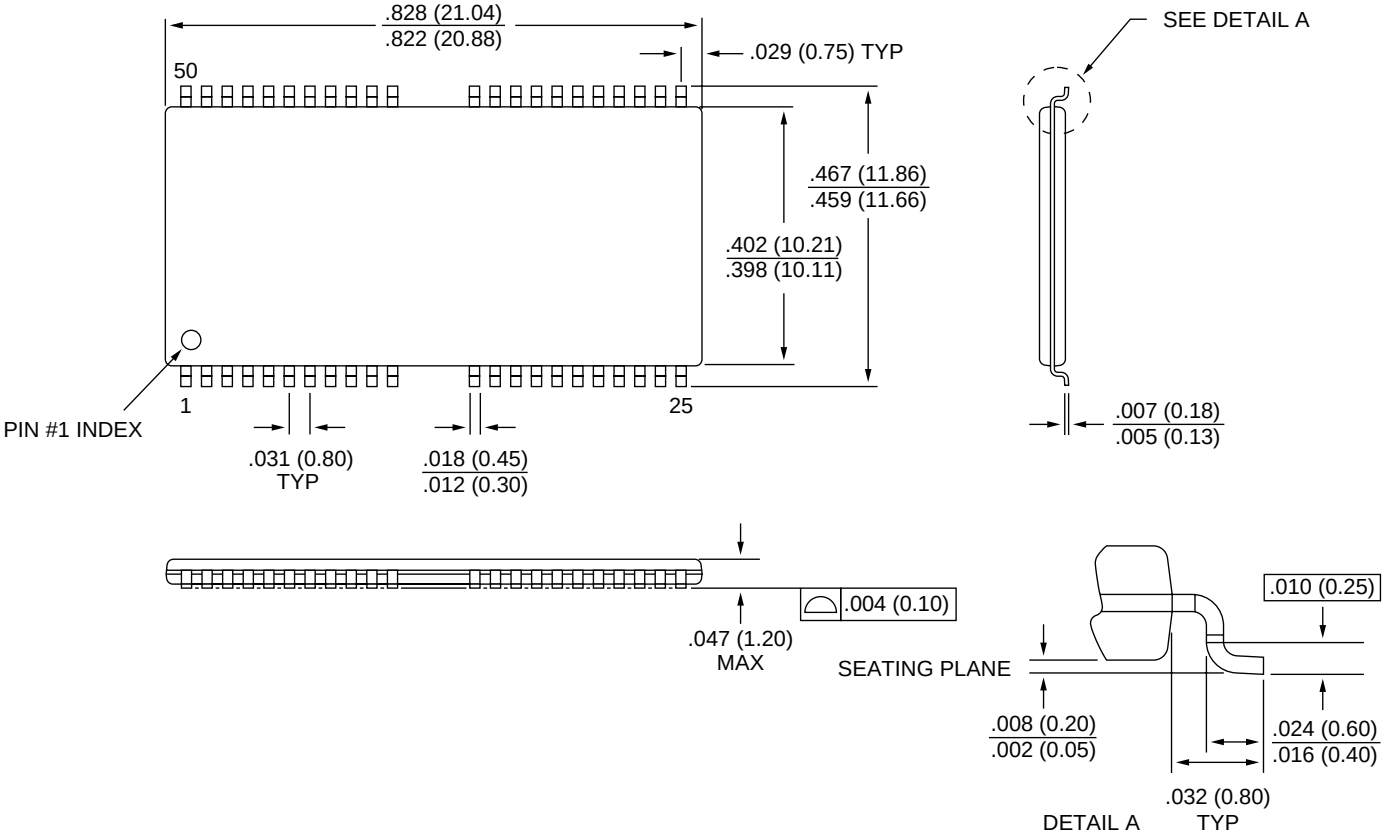
42-PIN PLASTIC SOJ (400 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

44/50-PIN PLASTIC TSOP (400 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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