

DRAM MODULE

1 MEG, 2 MEG x 32

4, 8 MEGABYTE, 5V, FAST PAGE
OR EDO PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process.
- Single +5V $\pm 10\%$ power supply
- All device pins are TTL-compatible
- Low power, 48mW standby; 1,824mW active, typical (8MB)
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ (CBR) and HIDDEN
- Multiple $\overline{\text{RAS}}$ lines allow x16 or x32 width
- 1,024-cycle refresh distributed across 16ms
- FAST PAGE MODE (FPM) operating mode or Extended Data-Out (EDO) PAGE MODE operating mode

OPTIONS

- Timing
 - 60ns access
 - 70ns access (FAST PAGE MODE only)

MARKING

- Packages
 - 72-pin SIMM M
 - 72-pin SIMM (gold) G
- Operating Modes
 - FAST PAGE MODE Blank
 - EDO PAGE MODE X

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-6	110ns	60ns	26ns	30ns	17ns	13ns

FPM Operating Mode

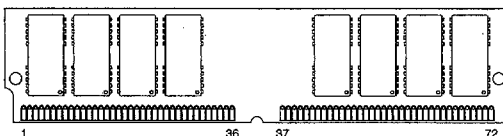
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)

72-Pin SIMM

(DD-3) 1 Meg x 32

(DD-4) 2 Meg x 32



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	V _{ss}	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	V _{ss}	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	V _{cc}
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	NC*/RAS1	63	DQ15
10	V _{cc}	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	WE	65	DQ16
12	A0	30	V _{cc}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	NC*/RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	V _{ss}

*4MB version only

DRAM SIMM

PART NUMBERS

EDO Operating Mode

PART NUMBER	DESCRIPTION
MT8D132G-xx X	1 Meg x 32, EDO, Gold
MT8D132M-xx X	1 Meg x 32, EDO, Tin/Lead
MT16D232G-xx X	2 Meg x 32, EDO, Gold
MT16D232M-xx X	2 Meg x 32, EDO, Tin/Lead

xx = speed

FPM Operating Mode

PART NUMBER	DESCRIPTION
MT8D132G-xx	1 Meg x 32, Gold
MT8D132M-xx	1 Meg x 32, Tin/Lead
MT16D232G-xx	2 Meg x 32, Gold
MT16D232M-xx	2 Meg x 32, Tin/Lead

xx = speed

GENERAL DESCRIPTION

The MT8D132(X) and MT16D232(X) are randomly accessed 4MB and 8MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits. A READ or WRITE cycle is selected with the \overline{WE} input. A logic HIGH on \overline{WE} dictates READ mode while a logic LOW on \overline{WE} dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last. EARLY WRITE occurs when \overline{WE} goes LOW prior to \overline{CAS} going LOW, the output pin(s) remain open (High-Z) until the next \overline{CAS} cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by \overline{RAS}

followed by a column-address strobed-in by \overline{CAS} . \overline{CAS} may be toggled-in by holding \overline{RAS} LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning \overline{RAS} HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after \overline{CAS} goes back HIGH. EDO provides for \overline{CAS} precharge time (t_{CP}) to occur without the output data going invalid. This elimination of \overline{CAS} output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of \overline{CAS} . EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after \overline{CAS} goes HIGH, as long as \overline{RAS} and \overline{OE} are held LOW and \overline{WE} is held HIGH (reference MT4C4007J DRAM data sheet for additional information on EDO functionality).

REFRESH

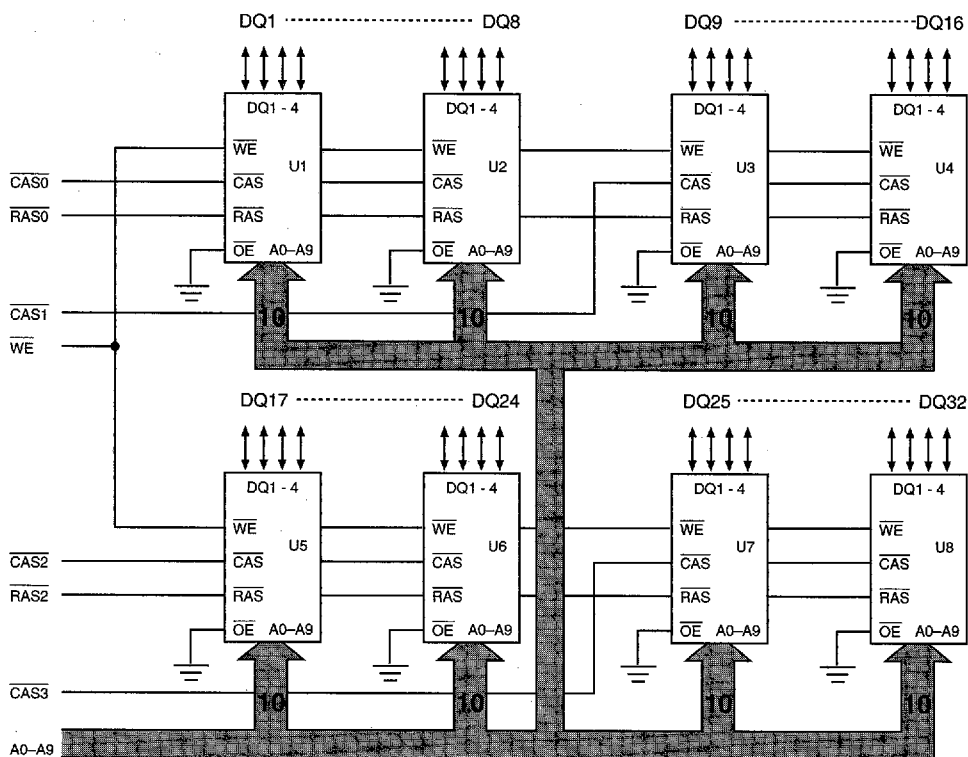
Returning \overline{RAS} and \overline{CAS} HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the \overline{RAS} HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE) or \overline{RAS} refresh cycle (\overline{RAS} ONLY, CBR or HIDDEN) so that all 1,024 combination of \overline{RAS} addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

x16 CONFIGURATION

For x16 applications, the corresponding DQ and \overline{CAS} pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and $\overline{CAS0}$ to $\overline{CAS2}$ and $\overline{CAS1}$ to $\overline{CAS3}$). Each \overline{RAS} is then a bank select for the x16 memory organization.

DRAM SIMM

FUNCTIONAL BLOCK DIAGRAM
MT8D132(X) (4MB)

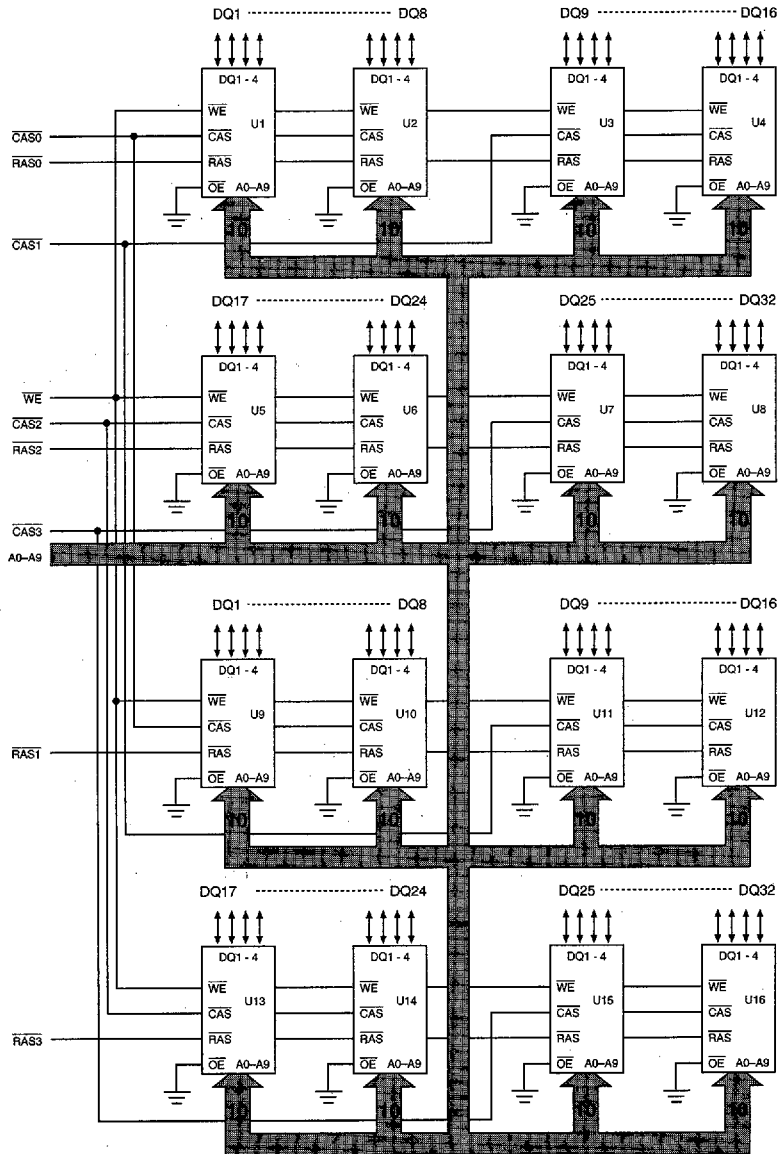


FAST PAGE MODE
U1-U8 = MT4C4001JDJ

EDO PAGE MODE
U1-U8 = MT4C4007JDJ

DRAM SIMM

FUNCTIONAL BLOCK DIAGRAM
MT16D232(X) (8MB)



FAST PAGE MODE
U1-U16 = MT4C4001J

EDO PAGE MODE
U1-U16 = MT4C4007JU

DRAM SIMM

TRUTH TABLE

FUNCTION		RAS	CAS		ADDRESSES		DATA-IN/OUT
				WE	lR	lC	DQ1-DQ32
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
	Any Cycle (X version)	L	L→H	H	n/a	n/a	Data-Out
EDO/FAST-PAGE-MODE EARLY WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

DRAM SIMM
**JEDEC DEFINED
PRESENCE-DETECT - MT8D132(X) (4MB)**

SYMBOL	PIN #	-6	-7
PRD1	67	V _{SS}	V _{SS}
PRD2	68	V _{SS}	V _{SS}
PRD3	69	NC	V _{SS}
PRD4	70	NC	NC

**JEDEC DEFINED
PRESENCE-DETECT - MT16D232(X) (8MB)**

SYMBOL	PIN #	-6	-7
PRD1	67	NC	NC
PRD2	68	NC	NC
PRD3	69	NC	V _{SS}
PRD4	70	NC	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} -1V to +7V
 Operating Temperature, T_A (ambient) 0°C to +70°C
 Storage Temperature (plastic) -55°C to +125°C
 Power Dissipation 8W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES	
Supply Voltage		V _{CC}	4.5	5.5	V		
Input High (Logic 1) Voltage, all inputs		V _{IH}	2.4	V _{CC} +1	V		
Input Low (Logic 0) Voltage, all inputs		V _{IL}	-1.0	0.8	V		
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ V _{CC} +1.0V (All other pins not under test = 0V)	CAS0-CAS3	I _{I1}	-8	8	μA		
	A0-A9, WE	I _{I2}	-32	32	μA	25	
	RAS0-RAS3	I _{I3}	-8	8	μA	25	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)		DQ1-DQ32	I _{OZ}	-20	20	μA	25
OUTPUT LEVELS High Voltage (I _{OUT} = -5mA) Low Voltage (I _{OUT} = 4.2mA)		V _{OH}	2.4		V		
		V _{OL}		0.4	V		

DRAM SIMM

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-6	-7		
STANDBY CURRENT: (TTL) (RAS = CAS = V _{IH})	I _{CC1}	4MB 8MB	16 32	16 32	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = other inputs = V _{CC} -0.2V)	I _{CC2}	4MB 8MB	8 16	8 16	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC3}	4MB 8MB	880 896	800 816	mA	2, 24
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS = V _{IL} , CAS, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC4}	4MB 8MB	640 656	560 576	mA	2, 24
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS = V _{IL} , CAS, address cycling: t _{PC} = t _{PC} [MIN])	I _{CC5} (X only)	4MB 8MB	640 656	— —	mA	2
REFRESH CURRENT: RAS ONLY Average power supply current (RAS cycling, CAS = V _{IH} : t _{RC} = t _{RC} [MIN])	I _{CC6}	4MB 8MB	880 896	800 816	mA	2, 24
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, address cycling: t _{RC} = t _{RC} [MIN])	I _{CC7}	4MB 8MB	880 896	800 816	mA	2, 19

CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		4MB	8MB		
Input Capacitance: A0-A9	C _{I1}	48	95	pF	17
Input Capacitance: WE	C _{I2}	64	127	pF	17
Input Capacitance: RAS0-RAS3	C _{I4}	32	32	pF	17
Input Capacitance: CAS0-CAS3	C _{I5}	16	32	pF	17
Input/Output Capacitance: DQ1-DQ32	C _{I0}	10	18	pF	17

FAST PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
Access time from column-address	t _{AA}		30		35	ns	
Column-address hold time (referenced to RAS)	t _{AR}	45		50		ns	
Column-address setup time	t _{ASC}	0		0		ns	
Row-address setup time	t _{ASR}	0		0		ns	
Access time from CAS	t _{CAC}		15		20	ns	9
Column-address hold time	t _{CAH}	10		15		ns	
CAS pulse width	t _{CAS}	15	10,000	20	10,000	ns	
CAS hold time (CBR REFRESH)	t _{CHR}	10		10		ns	19
CAS to output in Low-Z	t _{CLZ}	0		0		ns	
CAS precharge time	t _{CP}	10		10		ns	18
Access time from CAS precharge	t _{CPA}		35		40	ns	
CAS to RAS precharge time	t _{CRP}	10		10		ns	
CAS hold time	t _{CSH}	60		70		ns	
CAS setup time (CBR REFRESH)	t _{CSR}	10		10		ns	19
Write command to CAS lead time	t _{CWL}	15		20		ns	
Data-in hold time	t _{DH}	10		15		ns	15
Data-in hold time (referenced to RAS)	t _{DHR}	45		55		ns	
Data-in setup time	t _{DS}	0		0		ns	15
Output buffer turn-off delay	t _{OFF}	3	15	3	20	ns	12, 23, 26
FAST-PAGE-MODE READ or WRITE cycle time	t _{PC}	35		40		ns	
Access time from RAS	t _{RAC}		60		70	ns	8
RAS to column-address delay time	t _{RAD}	15	30	15	35	ns	22
Row-address hold time	t _{RAH}	10		10		ns	
Column-address to RAS lead time	t _{RAL}	30		35		ns	
RAS pulse width	t _{RAS}	60	10,000	70	10,000	ns	
RAS pulse width (FAST PAGE MODE)	t _{RASP}	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	t _{RC}	110		130		ns	
RAS to CAS delay time	t _{RCD}	20	45	20	50	ns	13
Read command hold time (referenced to CAS)	t _{RCH}	0		0		ns	14
Read command setup time	t _{RCS}	0		0		ns	
Refresh period (1,024 cycles)	t _{REF}		16		16	ms	

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($V_{cc} = +5V \pm 10\%$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX		
RAS precharge time	t_{RP}	40		50		ns	
RAS to CAS precharge time	t_{RPC}	0		0		ns	
Read command hold time	t_{RRH}	0		0		ns	14
RAS hold time	t_{RSH}	15		20		ns	
Write command to RAS lead time	t_{RWL}	15		20		ns	
Transition time (rise or fall)	t_T	3	50	3	50	ns	
Write command hold time	t_{WCH}	10		15		ns	
Write command hold time (referenced to RAS)	t_{WCR}	45		55		ns	
WE command setup time	t_{WCS}	0		0		ns	
Write command pulse width	t_{WP}	10		15		ns	
WE hold time (CBR REFRESH)	t_{WRH}	10		10		ns	
WE setup time (CBR REFRESH)	t_{WRP}	10		10		ns	

DRAM SIMM

EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
Access time from column-address	t_{AA}		30	ns	
Column-address setup to CAS precharge during WRITE	t_{ACH}	15		ns	
Column-address hold time (referenced to RAS)	t_{AR}	45		ns	
Column-address setup time	t_{ASC}	0		ns	
Row-address setup time	t_{ASR}	0		ns	
Access time from CAS	t_{CAC}		17	ns	9
Column-address hold time	t_{CAH}	10		ns	
CAS pulse width	t_{CAS}	13	10,000	ns	
CAS hold time (CBR REFRESH)	t_{CHR}	10		ns	19
CAS to output in Low-Z	t_{CLZ}	3		ns	23
Data output hold after CAS LOW	t_{COH}	5		ns	
CAS precharge time	t_{CP}	10		ns	18
Access time from CAS precharge	t_{CPA}		35	ns	
CAS to RAS precharge time	t_{CRP}	10		ns	
CAS hold time	t_{CSH}	50		ns	
CAS setup time (CBR REFRESH)	t_{CSR}	10		ns	19
Write command to CAS lead time	t_{CWL}	15		ns	
Data-in hold time	t_{DH}	9		ns	15
Data-in hold time (referenced to RAS)	t_{DHR}	45		ns	
Data-in setup time	t_{DS}	0		ns	15
Output buffer turn-off delay	t_{OFF}	3	15	ns	12, 23, 26
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	26		ns	
Access time from RAS	t_{RAC}		60	ns	8
RAS to column-address delay time	t_{RAD}	15	30	ns	22
Row-address hold time	t_{RAH}	10		ns	
Column-address to RAS lead time	t_{RAL}	30		ns	
RAS pulse width	t_{RAS}	60	10,000	ns	
RAS pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		ns	
RAS to CAS delay time	t_{RCD}	20	45	ns	13
Read command hold time (referenced to CAS)	t_{RCH}	0		ns	14
Read command setup time	t_{RCS}	0		ns	
Refresh period (1,024 cycles)	t_{REF}		16	ms	

DRAM SIMM

EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		UNITS	NOTES
PARAMETER	SYM	MIN	MAX		
RAS precharge time	t_{RP}	40		ns	
RAS to CAS precharge time	t_{RPC}	5		ns	
Read command hold time	t_{RRH}	0		ns	14
RAS hold time	t_{RSH}	15		ns	
Write command to RAS lead time	t_{RWL}	15		ns	
Transition time (rise or fall)	t_T	1.5	50	ns	4, 5
Write command hold time	t_{WCH}	10		ns	
Write command hold time (referenced to RAS)	t_{WCR}	45		ns	
\overline{WE} command setup time	t_{WCS}	0		ns	
Output disable delay from \overline{WE} (CAS HIGH)	t_{WHZ}	3	15	ns	
Write command pulse width	t_{WP}	10		ns	
\overline{WE} pulse width for output disable when CAS HIGH	t_{WPZ}	10		ns	
\overline{WE} hold time (CBR REFRESH)	t_{WRH}	10		ns	
\overline{WE} setup time (CBR REFRESH)	t_{WRP}	10		ns	

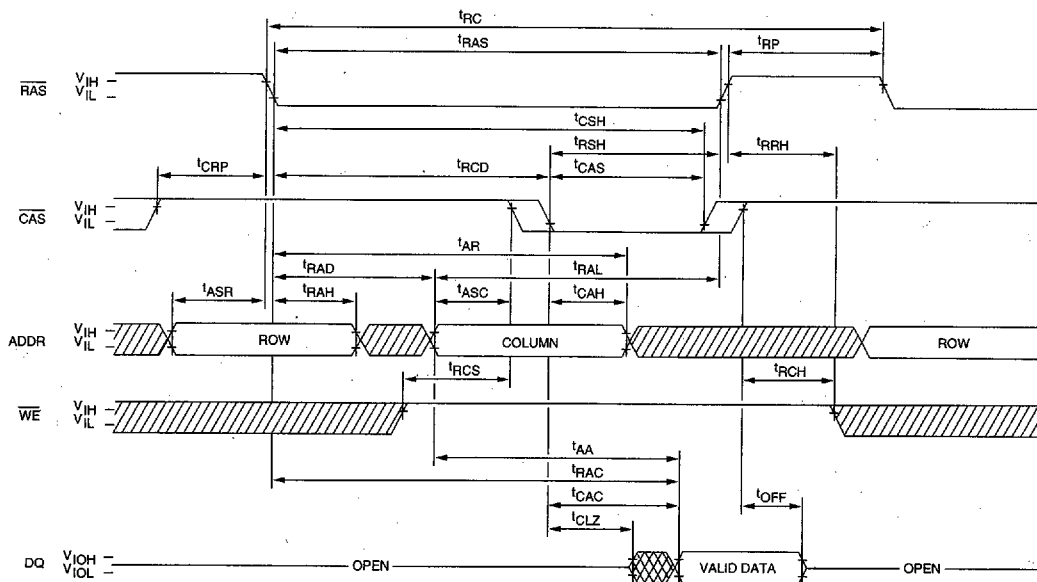
DRAM SIMM

NOTES

1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100 μ s is required after power-up followed by eight RAS refresh cycles (RAS ONLY or CBR with WE HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
4. AC characteristics assume tT = 5ns for FAST PAGE MODE and tT = 1.5ns for EDO PAGE MODE.
5. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C \leq TA \leq 70°C) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
9. Assumes that tRCD \geq tRCD (MAX).
10. If CAS and RAS = VIH, data output is High-Z.
11. If CAS = VIL, data output may contain data from the last valid READ cycle.
12. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
13. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
14. Either tRCH or tRRH must be satisfied for a READ cycle.
15. These parameters are referenced to CAS leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, VCC = 4.5V, DC bias = 2.4V at 15mV RMS).
18. If CAS is LOW at the falling edge of RAS, data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS must be pulsed HIGH for tCP.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to OE being grounded on U1-U8/U16.
22. Operation within the tRAD (MAX) limit ensures that tRCD (MAX) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, then access time is controlled exclusively by tAA.
23. The 3ns minimum is a parameter guaranteed by design.
24. Column-address changed once each cycle.
25. 4MB module values will be half of those shown.
26. For FAST PAGE MODE option, tOFF is determined by the first RAS or CAS signal to transition HIGH. In comparison, tOFF on an EDO option is determined by the latter of the RAS and CAS signal to transition HIGH.
27. Applies to both EDO and FAST PAGE MODES.

DRAM SIMM

READ CYCLE **(FAST PAGE MODE Module)**



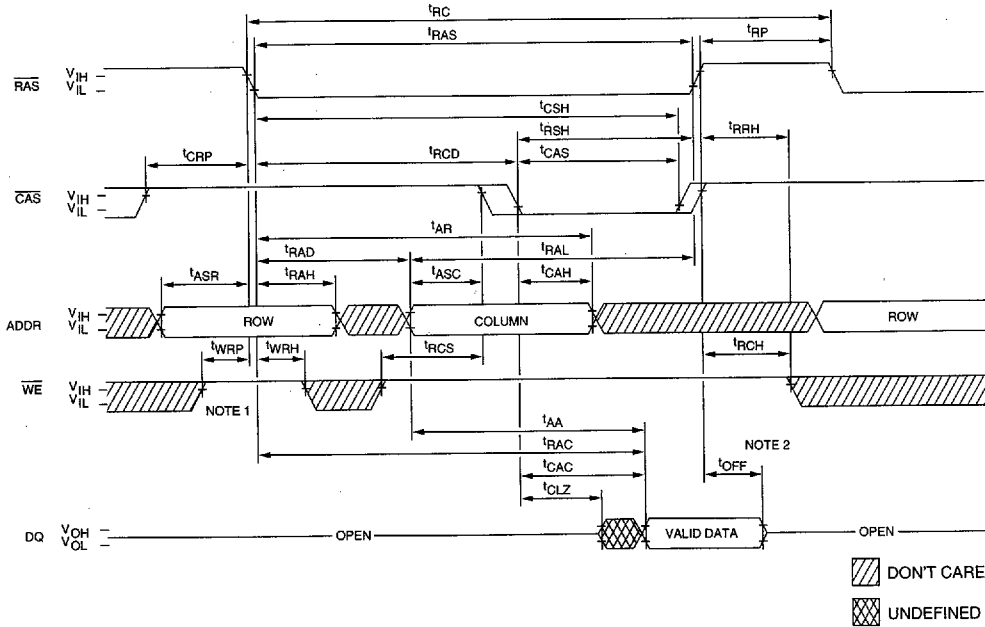
DON'T CARE
 UNDEFINED

FAST PAGE MODE **TIMING PARAMETERS**

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{AA}		30		35	ns
t_{AR}	45		50		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		15		20	ns
t_{CAH}	10		15		ns
t_{CAS}	15	10,000	20	10,000	ns
t_{CLZ}	0		0		ns
t_{CRP}	10		10		ns
t_{CSH}	60		70		ns
t_{OFF}	3	15	3	20	ns
t_{RAC}		60		70	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{RAD}	15	30	15	35	ns
t_{RAH}	10		10		ns
t_{RAL}	30		35		ns
t_{RAS}	60	10,000	70	10,000	ns
t_{RC}	110		130		ns
t_{RCD}	20	45	20	50	ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	40		50		ns
t_{RRH}	0		0		ns
t_{RSH}	15		20		ns

READ CYCLE (EDO PAGE MODE Module)



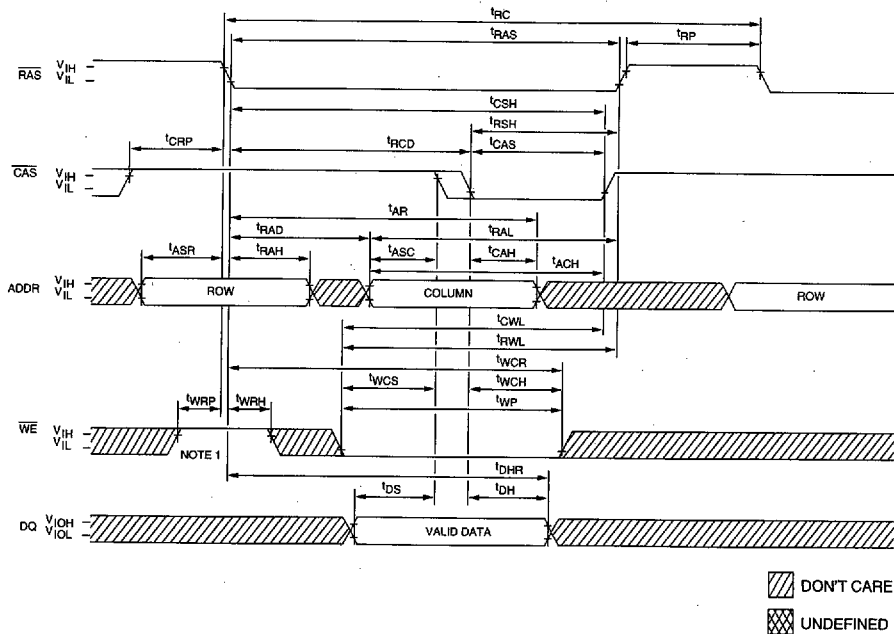
- NOTE:**
- Although \overline{WE} is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for $t'WRP$ and $t'WRH$. This design implementation will facilitate compatibility with future EDO DRAMs.
 - $t'OFF$ is referenced from rising edge of RAS or CAS, whichever occurs last.

EDO PAGE MODE TIMING PARAMETERS

SYM	-6		UNITS
	MIN	MAX	
t'AA		30	ns
t'AR	45		ns
t'ASC	0		ns
t'ASR	0		ns
t'CAC		17	ns
t'CAH	10		ns
t'CAS	13	10,000	ns
t'CLZ	3		ns
t'CRP	10		ns
t'CSH	50		ns
t'OFF	3	15	ns
t'RAC		60	ns
t'RAD	15	30	ns

SYM	-6		UNITS
	MIN	MAX	
t'RAH	10		ns
t'RAL	30		ns
t'RAS	60	10,000	ns
t'RC	110		ns
t'RCD	20	45	ns
t'RCH	0		ns
t'RCS	0		ns
t'RP	40		ns
t'RRH	0		ns
t'ASH	15		ns
t'WRH	10		ns
t'WRP	10		ns

EARLY WRITE CYCLE²⁷



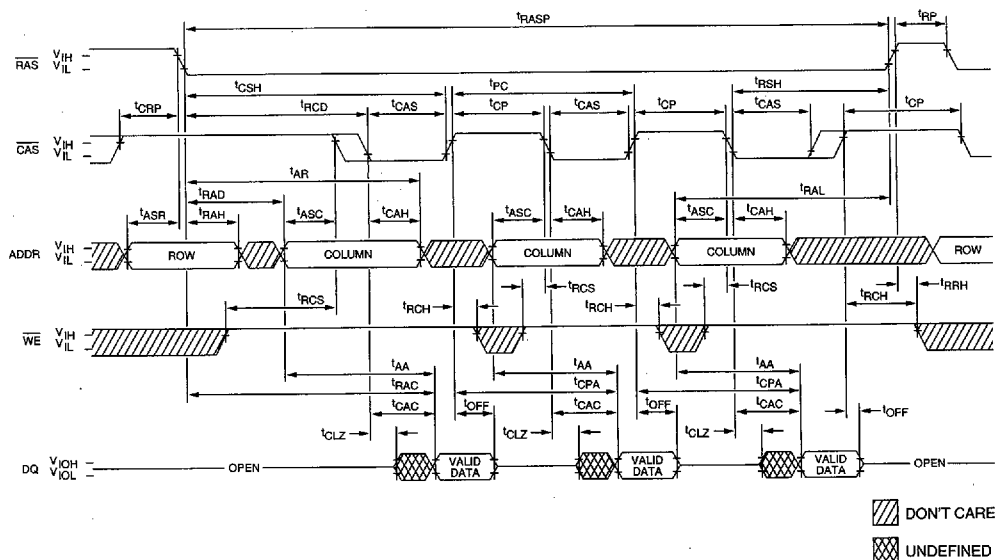
NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for WRP and WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ ACH (EDO)	15		—		ns
¹ AR	45		50		ns
¹ ASC	0		0		ns
¹ ASR	0		0		ns
¹ CAH	10		15		ns
¹ CAS (FPM)	15	10,000	20	10,000	ns
¹ CAS (EDO)	13	10,000	—	—	ns
¹ CRP	10		10		ns
¹ CSH (FPM)	60		70		ns
¹ CSH (EDO)	50		—		ns
¹ CWL	15		20		ns
¹ DH (FPM)	10		15		ns
¹ DH (EDO)	9		—		ns
¹ DHR	45		55		ns
¹ DS	0		0		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^t RAD	15	30	15	35	ns
^t RAH	10		10		ns
^t RAL	30		35		ns
^t RAS	60	10,000	70	10,000	ns
^t RC	110		130		ns
^t RCD	20	45	20	50	ns
^t RP	40		50		ns
^t RSH	15		20		ns
^t RWL	15		20		ns
^t WCH	10		15		ns
^t WCR	45		55		ns
^t WCS	0		0		ns
^t WP	10		15		ns
^t WRH	10		10		ns
^t WRP	10		10		ns

FAST-PAGE-MODE READ CYCLE



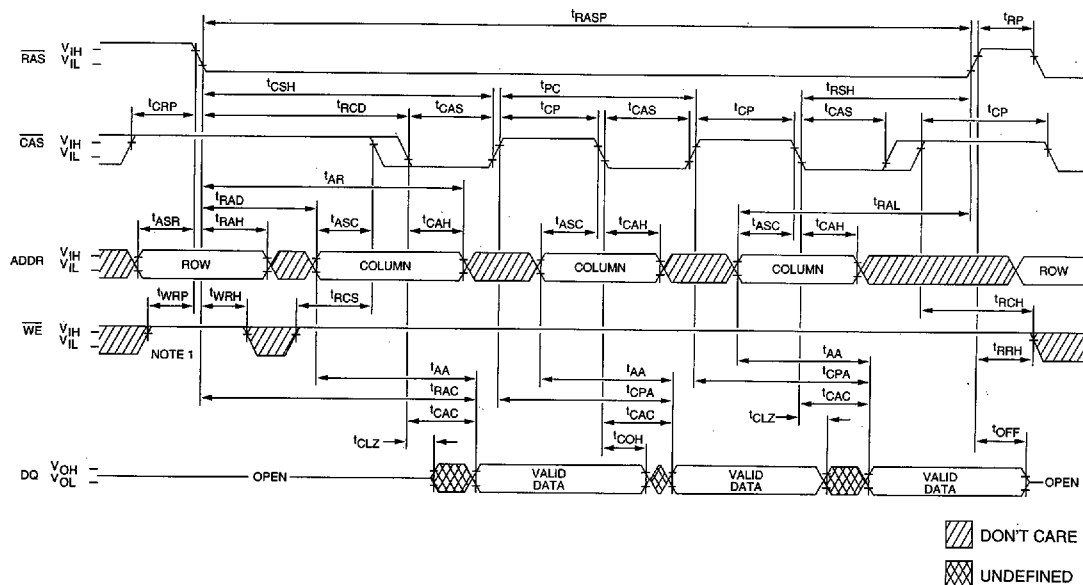
DRAM SIMM

**FAST PAGE MODE
TIMING PARAMETERS**

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	10		10		ns
tCSH	60		70		ns
tOFF	3	15	3	20	ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

EDO-PAGE-MODE READ CYCLE



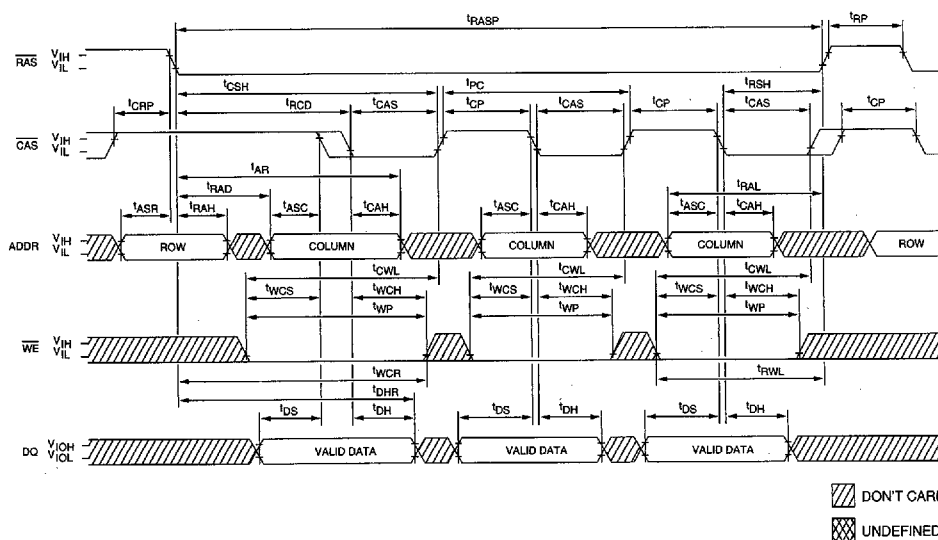
NOTE: 1. Although \overline{WE} is a “don’t care” at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMS.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
^t AA		30	ns
^t AR	45		ns
^t ASC	0		ns
^t ASR	0		ns
^t CAC		17	ns
^t CAH	10		ns
^t CAS	13	10,000	ns
^t CLZ	3		ns
^t COH	5		ns
^t CP	10		ns
^t CPA		35	ns
^t CRP	10		ns
^t CSH	50		ns
^t OFF	3	15	ns

	-6		
SYM	MIN	MAX	UNITS
¹ PC	26		ns
¹ RAC		60	ns
¹ RAD	15	30	ns
¹ RAH	10		ns
¹ RAL	30		ns
¹ RASP	60	100,000	ns
¹ RCD	20	45	ns
¹ RCH	0		ns
¹ RCS	0		ns
¹ RP	40		ns
¹ RRH	0		ns
¹ RSH	15		ns
¹ WRH	10		ns
¹ WRP	10		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE



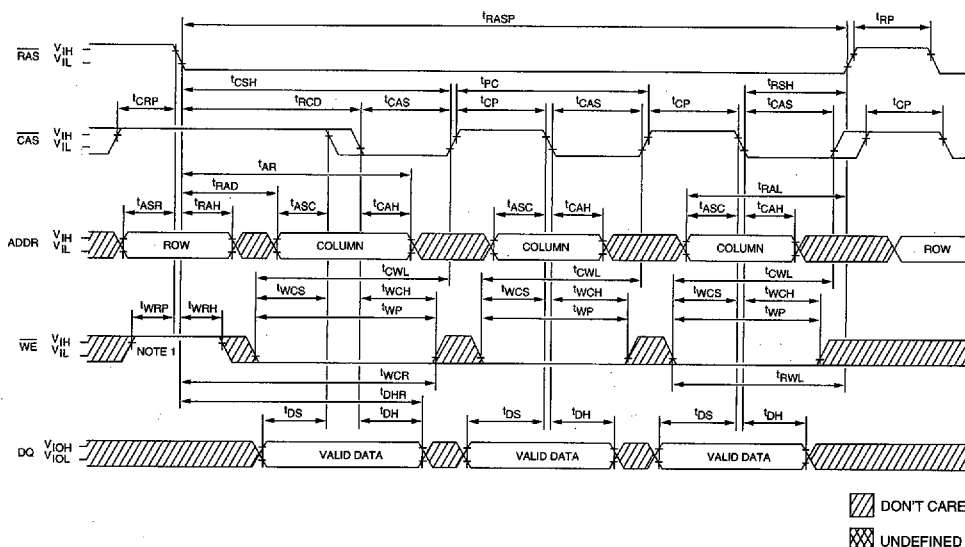
DRAW SIMM


FAST PAGE MODE TIMING PARAMETERS


	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^t AR	45		50		ns
^t ASC	0		0		ns
^t ASR	0		0		ns
^t CAH	10		15		ns
^t CAS	15	10,000	20	10,000	ns
^t CP	10		10		ns
^t CRP	10		10		ns
^t CSH	60		70		ns
^t CWL	15		20		ns
^t DH	10		15		ns
^t DHR	45		55		ns
^t DS	0		0		ns
^t PC	35		40		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
¹ RAD	15	30	15	35	ns
¹ RAH	10		10		ns
¹ RAL	30		35		ns
¹ RASP	60	100,000	70	100,000	ns
¹ RCD	20	45	20	50	ns
¹ RP	40		50		ns
¹ RSH	15		20		ns
¹ RWL	15		20		ns
¹ WCH	10		15		ns
¹ WCR	45		55		ns
¹ WCS	0		0		ns
¹ WP	10		15		ns

EDO-PAGE-MODE EARLY-WRITE CYCLE



 DON'T CARE

 UNDEFINED

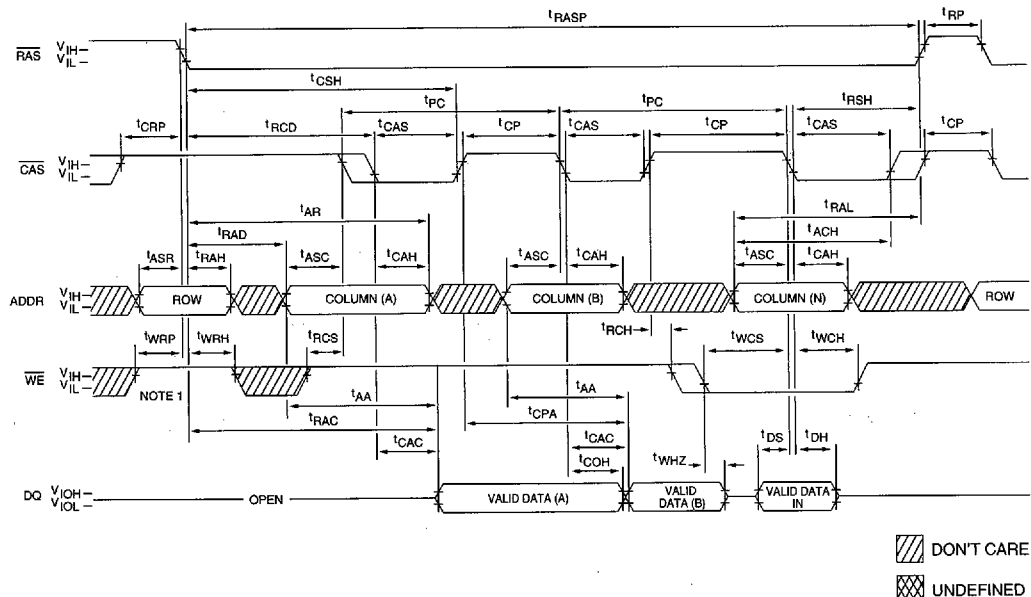
NOTE: 1. Although \overline{WE} is a “don’t care” at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
^t AR	45		ns
^t ASC	0		ns
^t ASR	0		ns
^t CAH	10		ns
^t CAS	13	10,000	ns
^t CP	10		ns
^t CRP	10		ns
^t CSH	50		ns
^t CWL	15		ns
^t DH	9		ns
^t DHR	45		ns
^t DS	0		ns
^t PC	26		ns
^t RAD	15	30	ns

	-6		
SYM	MIN	MAX	UNITS
¹ RAH	10		ns
¹ RAL	30		ns
¹ RASP	60	100,000	ns
¹ RCD	20	45	ns
¹ RP	40		ns
¹ RSH	15		ns
¹ RWL	15		ns
¹ WCH	10		ns
¹ WCR	45		ns
¹ WCS	0		ns
¹ WP	10		ns
¹ WRH	10		ns
¹ WRP	10		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY-WRITE)

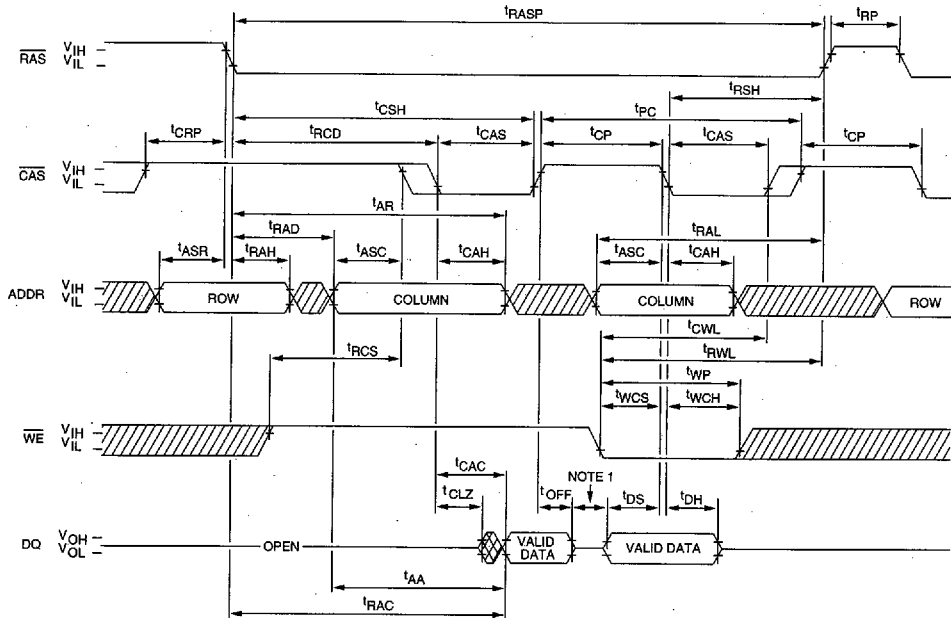


NOTE: 1. Although \overline{WE} is a “don’t care” at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		
SYM	MIN	MAX	UNITS
AA		30	ns
ACH	15		ns
AR	45		ns
ASC	0		ns
ASR	0		ns
CAC		17	ns
CAH	10		ns
CAS	13	10,000	ns
COH	5		ns
CP	10		ns
CPA		35	ns
CRP	10		ns
CSH	50		ns
DH	9		ns
DS	0		ns
PC	26		ns

	-6		
SYM	MIN	MAX	UNITS
¹ RAC		60	ns
¹ RAD	15	30	ns
¹ RAH	10		ns
¹ RAL	30		ns
¹ RASP	60	100,000	ns
¹ RCD	20	45	ns
¹ RCH	0		ns
¹ RCS	0		ns
¹ RP	40		ns
¹ RSH	15		ns
¹ WCH	10		ns
¹ WCS	0		ns
¹ WHZ	3	15	ns
¹ WRH	10		ns
¹ WRP	10		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)


DON'T CARE
 UNDEFINED

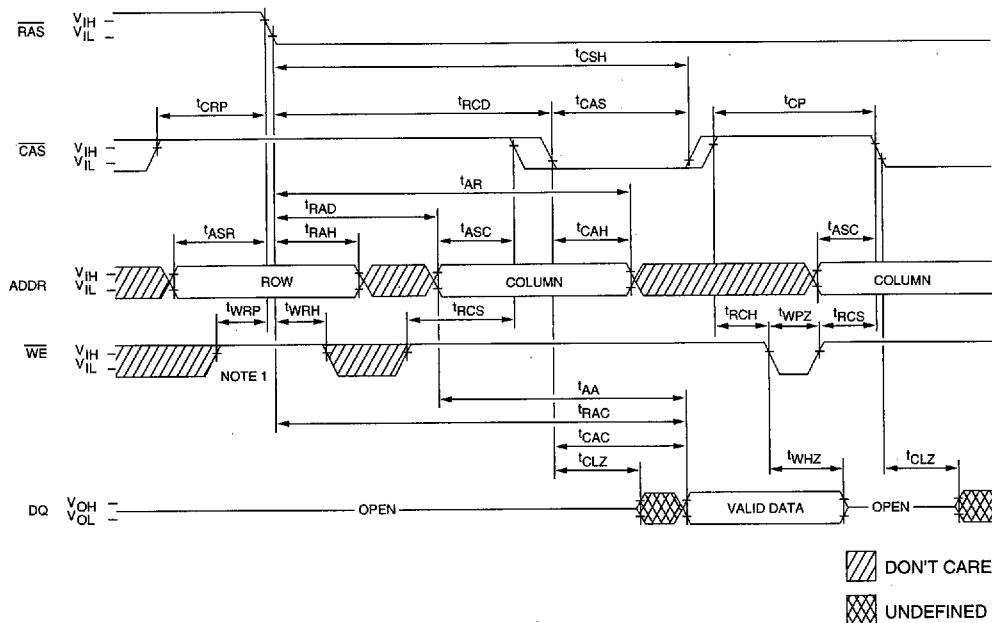
NOTE: 1. Do not drive data prior to tristate.

FAST PAGE MODE
TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCRP	10		10		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns
tOFF	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCS	0		0		ns
tWP	10		15		ns

EDO READ CYCLE (with \overline{WE} -controlled disable)



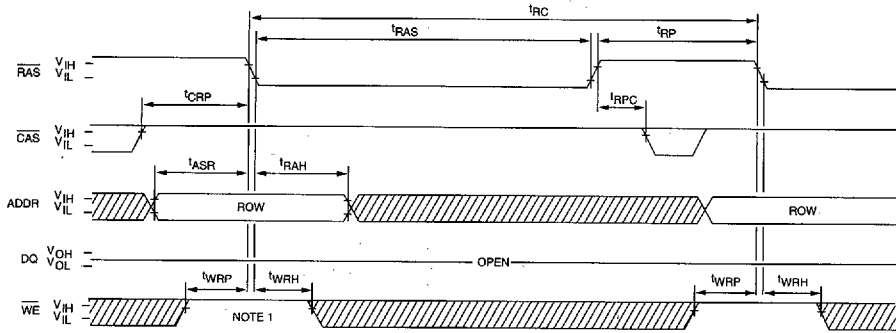
NOTE: 1. Although \overline{WE} is a "don't care" at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

SYM	-6		UNITS
	MIN	MAX	
t_{AA}		30	ns
t_{AR}	45		ns
t_{ASC}	0		ns
t_{ASR}	0		ns
t_{CAC}		17	ns
t_{CAH}	10		ns
t_{CAS}	13	10,000	ns
t_{CLZ}	3		ns
t_{CP}	10		ns
t_{CRP}	10		ns
t_{CSH}	50		ns

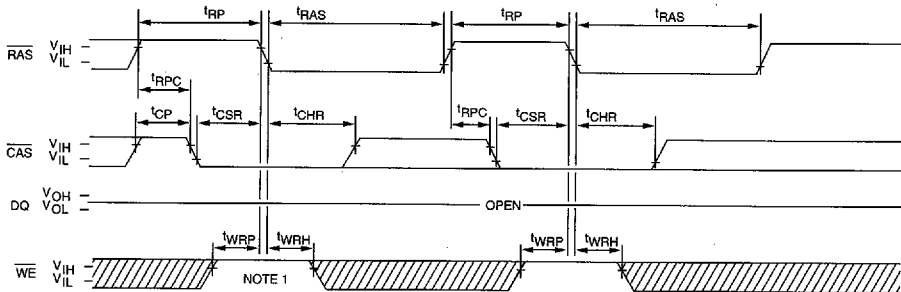
SYM	-6		UNITS
	MIN	MAX	
t_{RAC}		60	ns
t_{RAD}	15	30	ns
t_{RAH}	10		ns
t_{RCD}	20	45	ns
t_{RCH}	0		ns
t_{RCS}	0		ns
t_{WHZ}	3	15	ns
t_{WPZ}	10		ns
t_{WRH}	10		ns
t_{WRP}	10		ns

RAS-ONLY REFRESH CYCLE ²⁷



CBR REFRESH CYCLE ²⁹

(Addresses = DON'T CARE)



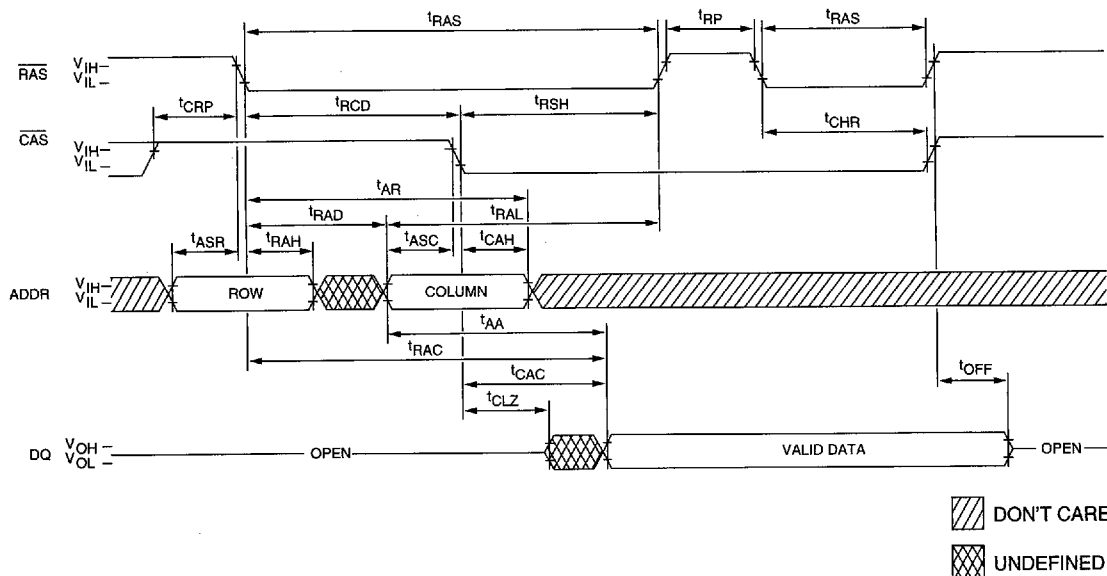
DON'T CARE
 UNDEFINED

NOTE: 1. Although \overline{WE} is a "don't care" at \overline{RAS} time during an access cycle (READ or WRITE), the system designer should implement \overline{WE} HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{ASR}	0		0		ns
t_{CHR}	10		10		ns
t_{CP}	10		10		ns
t_{CRP}	10		10		ns
t_{CSR}	10		10		ns
t_{RAH}	10		10		ns
t_{RAS}	60	10,000	70	10,000	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
t_{RC}	110		130		ns
t_{RP}	40		50		ns
t_{RPC} (FPM)	0		0		ns
t_{RPC} (EDO)	5		—		ns
t_{WRH}	10		10		ns
t_{WRP}	10		10		ns

HIDDEN REFRESH CYCLE ^{20, 27}
(WE = HIGH)

DRAM SIMM
FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		30		35	ns
t _{AR}	45		50		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC} (FPM)		15		20	ns
t _{CAC} (EDO)		17	—		ns
t _{CAH}	10		15		ns
t _{CHR}	10		10		ns
t _{CLZ}	3		3		ns
t _{CRP}	10		10		ns

SYM	-6		-7		UNITS
	MIN	MAX	MIN	MAX	
t _{OFF}	3	15	3	20	ns
t _{RAC}		60		70	ns
t _{RAD}	15	30	15	35	ns
t _{RAH}	10		10		ns
t _{RAL}	30		35		ns
t _{RAS}	60	10,000	70	10,000	ns
t _{RCD}	20	45	20	50	ns
t _{RP}	40		50		ns
t _{RSH}	15		20		ns