

**DESCRIPTION**

The LX1910 PWM buck regulator achieves very high efficiencies over a broad range of operating load conditions. The LX1910 implements a load-detection architecture and enters a power-saving PFM mode when driving small load currents ensuring optimal regulator efficiency over the entire output current range thus maximizing battery life.

The PWM operating mode implements a fixed frequency of 1MHz (typ), the transconductance error amplifier has 12 $\mu$ A of drive with an output voltage swing rail to rail. Compensation is external for maximum user flexibility.

The LX1910 does not require a minimum load current for stable operation. There is no Under Voltage Lockout for the input voltage, operational range includes 4V to 6V. The regulator is capable of providing an output dc load current of 850mA. The SHDN pin places the device in a sleep-mode drawing less than 1 $\mu$ A of quiescent current.

The LX1910 comes in space-saving MSOP package allowing a complete application circuit to occupy a very small PCB area. These features make the LX1910 ideal for use in SmartPhones, PDAs, or other battery-operated devices

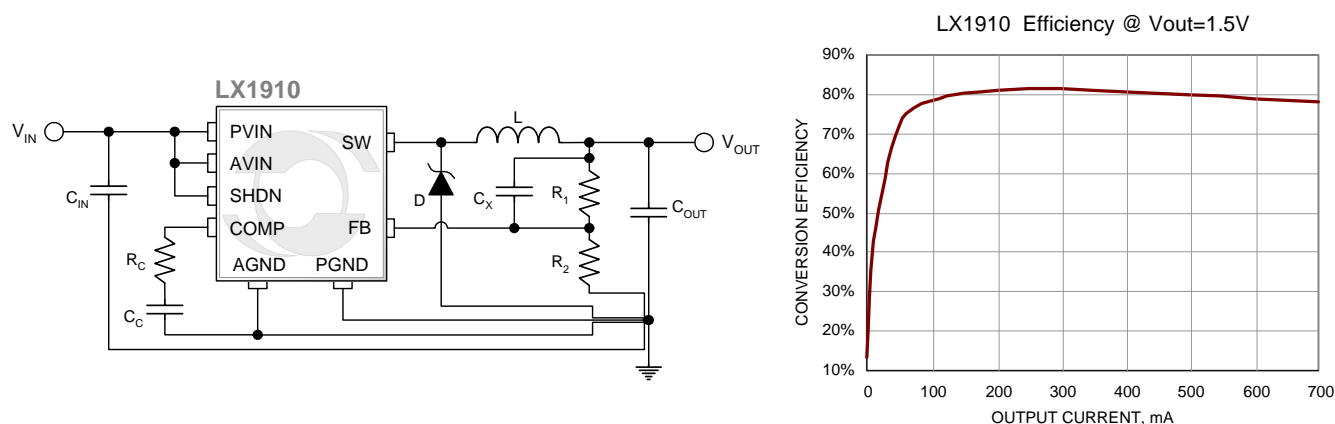
**KEY FEATURES**

- Internal Reference 1.17V  $\pm 2\%$  Accuracy (Line and Temperature)
- 4V to 6.0V Input Range
- Adj. Output From 1.17V to  $V_{IN}$
- Output Current ( $I_{DC} > 850mA$ )
- Quiescent Current  $< 300\mu A$
- 1MHz Operation Frequency
- MSOP 8-Pin

**APPLICATIONS/BENEFITS**

- Portable Microprocessor Core Voltage Supplies
- 5V to 3V

**IMPORTANT:** For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

**PRODUCT HIGHLIGHT**


**Figure 1 – LX1910 Circuit Topology and Typical Efficiency Performance**

**PACKAGE ORDER INFO**

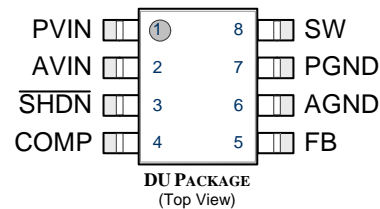
$T_J(^{\circ}C)$	Input Voltage	Output Voltage Range	<b>DU</b> Plastic MSOP 8-PIN RoHS Compliant / Pb-free
0 to 85	4.5V – 6.0V	1.17V to $V_{IN}$	<b>LX1910CDU</b>

Note: Available in Tape & Reel. Append the letters "TR" to the part number.  
(i.e. LX1910-13016CDU-TR)

**Step-Down Regulator**
**PRODUCTION DATA SHEET**
**ABSOLUTE MAXIMUM RATINGS**

Input Voltage (IN) or $\overline{\text{SHDN}}$ to GND .....	-0.3V to 7.0V
SW to GND.....	-0.3V to (V <sub>IN</sub> + 0.3V)
V <sub>FB</sub> to GND.....	-0.3V to +2V
SW Peak Current (Internally Limited) .....	1000mA
Operating Temperature Range.....	-40°C to +125°C
Storage Temperature Range, T <sub>A</sub> .....	-65°C to 150°C
Maximum Junction Temperature.....	150°C
RoHS / Pb-free Peak Package Solder Reflow Temperature (40 seconds maximum exposure) .....	260°C (+0, -5)

**Note:** Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

**PACKAGE PIN OUT**


RoHS / Pb-free 100% Matte Tin Lead Finish

**THERMAL DATA**
**DU Plastic MSOP 8-Pin**

**THERMAL RESISTANCE-JUNCTION TO AMBIENT,  $\theta_{JA}$**

**206°C/W**

Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ . The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

**FUNCTIONAL PIN DESCRIPTION**

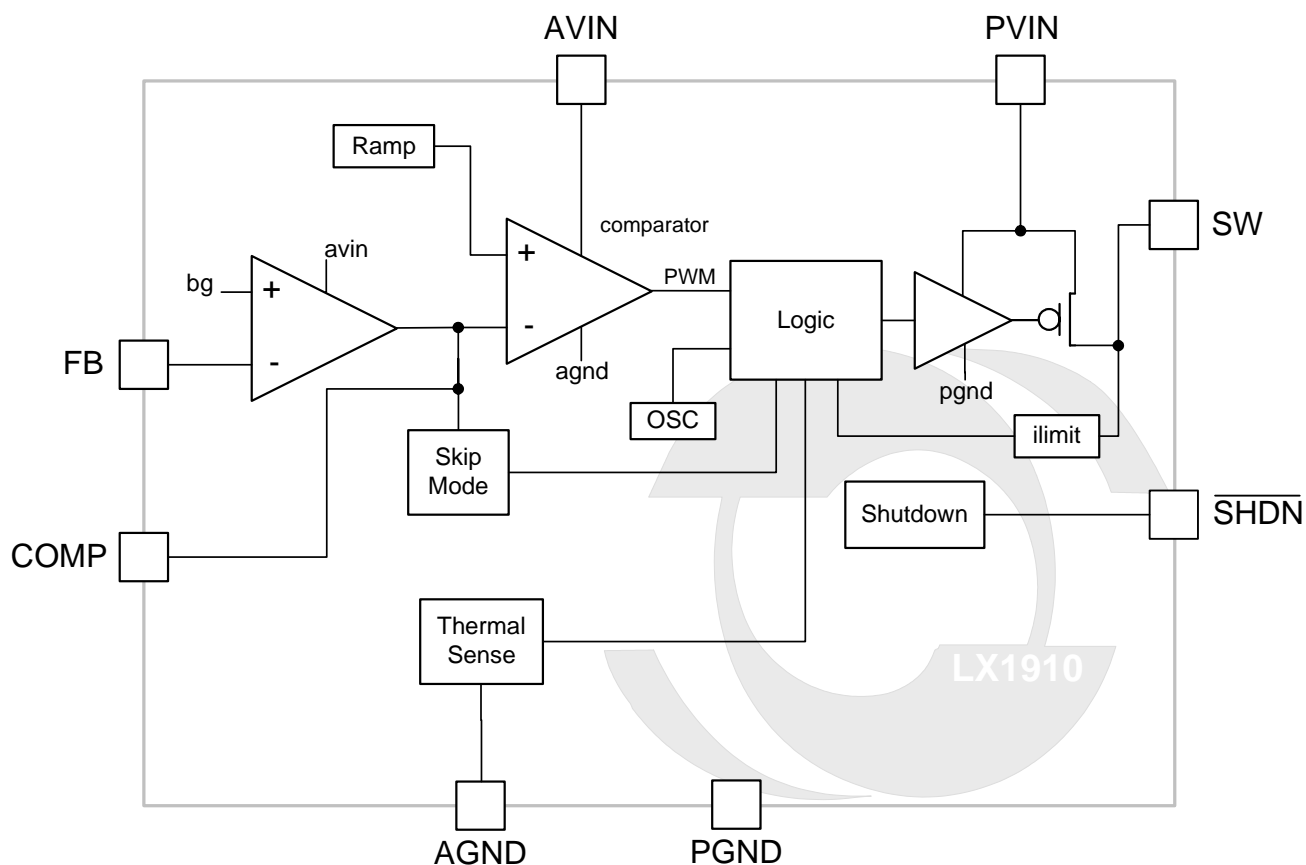
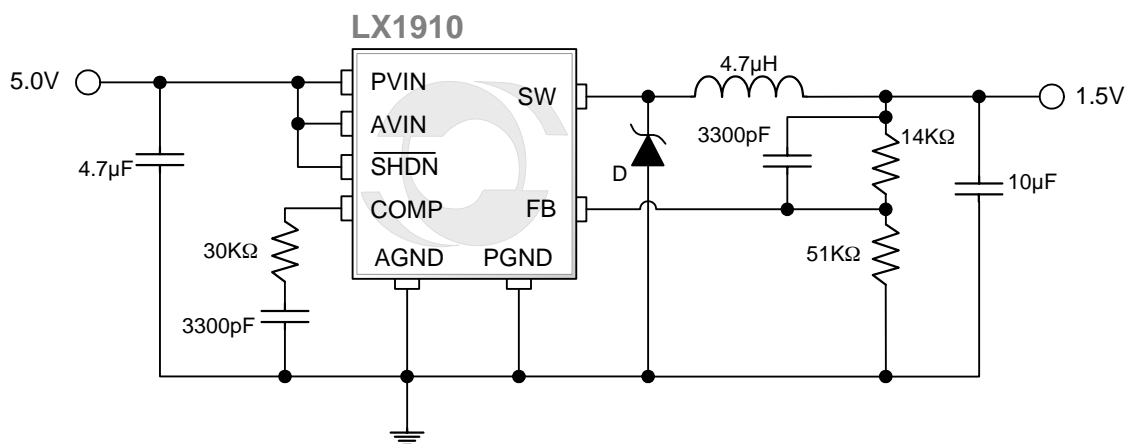
NAME	DESCRIPTION
SW	Inductor and commutation diode connection point. Connects to internal MOSFET drain.
AGND	Analog circuit ground providing bias for IC operation.
FB	Feedback input for setting adjustable output voltage
$\overline{\text{SHDN}}$	Enable control input. Reduces quiescent current to 1 $\mu$ A. Pin 8, Output becomes high impedance.
PVIN	Unregulated supply voltage input connected to PMOS Source. Input range from +2.7V to 6.0V
COMP	Frequency Compensation of the overall loop is effected by placing a series R/C combination between COMP pin and GND.
AVIN	Unregulated supply voltage input. Input range from +4V to 6.0V
PGND	Power ground (return path for internal PMOS gate driver).



#### ELECTRICAL CHARACTERISTICS

Specifications apply over junction temperature of:  $0^{\circ}\text{C} \leq T \leq 85^{\circ}\text{C}$  for  $V_{\text{IN}} = 5\text{V}$  (except where otherwise noted). Typical values are at  $T_A = 25^{\circ}\text{C}$ .

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Range	$V_{\text{IN}}$	Functional operation guaranteed by design	3.5		6.0	V
Output Voltage Range	$V_{\text{OUT}}$	Closed loop operating range	$V_{\text{FB}}$		$0.95 \cdot V_{\text{IN}}$	V
Feed Back Threshold	$V_{\text{FBT}}$	$4\text{V} \leq V_{\text{IN}} \leq 6\text{V}$	1.146	1.170	1.193	V
FB Input Current	$I_{\text{FB}}$	$V_{\text{FB}} = 1.2\text{V}$		300	500	nA
EA Drive Current (COMP Pin)	$I_{\text{SOURCE}}$	$V_{\text{FB}} - 125\text{mV}$ of Overdrive, $V_{\text{COMP}} = 2.5\text{V}$	10	16		$\mu\text{A}$
	$I_{\text{SINK}}$	$V_{\text{FB}} + 125\text{mV}$ of Overdrive, $V_{\text{COMP}} = 2.5\text{V}$	10	16		$\mu\text{A}$
EA Output Swing (COMP Pin)	$V_{\text{EA OUT}}$	VOL, Sinking $10\mu\text{A}$		95		mV
		VOH, Sourcing $10\mu\text{A}$		4.86		V
Quiescent Operating Current	$I_{\text{Q}}$	Pin 2 Supply Current		250	400	$\mu\text{A}$
Sleep (Shutdown Mode) Current	$I_{\text{QVINSD}}$	$V_{\text{SHDN}} = 0\text{V}$ , SW Pin open			1	$\mu\text{A}$
	$I_{\text{QVINSD}}$	$V_{\text{SHDN}} = 0\text{V}$ , SW grounded		2	5	$\mu\text{A}$
Shutdown Input Bias Current	$I_{\text{SD_IB}}$	$\overline{\text{SHDN}} = \text{GND}$ or $\overline{\text{SHDN}} = 5\text{V}$	-100		100	nA
Shutdown Voltage Threshold	$V_{\text{SD}}$	Device Off			$0.2 \cdot V_{\text{IN}}$	V
		Device On	$0.8 \cdot V_{\text{IN}}$			V
P-Channel Switch ON Resistance	$R_{\text{DS(ON)}}$	$I_{\text{SW}} = 0.5\text{A}$		0.53	0.8	$\Omega$
Maximum Duty Cycle	D	$I_{\text{SW}} = 0.5\text{A}$ (assured by design, not ATE tested)	80	100		%
SW Leakage Current	$I_{\text{LEAK}}$			1	5	$\mu\text{A}$
P-Channel Current Limit	$I_{\text{LIM}}$		900	950		mA
Frequency	$F_{\text{OP}}$		0.80	1.07	1.2	MHz
Closed Loop Load Regulation	Load Reg	$V_{\text{O}} = 1.5\text{V}$ , $5\text{mA} \leq I_{\text{O}} \leq 700\text{mA}$ , ckt figure 3		0.35	0.5	% $V_{\text{O}}$
Thermal Shutdown	$T_{\text{SD}}$		125	150		$^{\circ}\text{C}$

**SIMPLIFIED BLOCK DIAGRAM**

**Figure 2 – LX1910 Block Diagram**

**Figure 3 – Circuit for 1.5V Output Voltage**

**APPLICATION NOTE**
**FUNCTIONAL DESCRIPTION**

The LX1910 implements a PFM / PWM architecture that improves power management efficiency across the output load range.

**OUTPUT VOLTAGE PROGRAMMING**

Resistors R1 and R2 program the output voltage. An optional capacitor C<sub>X</sub> may be inserted across R1 to improve the transient response (see Figure 1). The value of R2 should be less than 100KΩ. The value of R1 can be determined using the following equation, note V<sub>REF</sub> is also referred to as V<sub>FBT</sub>.

$$R1 = R2 \left[ \left( \frac{V_{OUT}}{V_{REF}} \right) - 1 \right]$$

**DESIGN EXAMPLE:**

Let R2 equal 50K and the required V<sub>OUT</sub> equal to 3.0V.

$$R1 = 50K \left[ \left( \frac{3V}{1.17} \right) - 1 \right] = 78K\Omega$$

**DIODE SELECTION**

A Schottky diode is recommended for use with the LX1910 because it provides fast switching and superior reverse recovery performance. The **Microsemi** UPS5817 (20V @ 1A) makes an effective choice for most applications.

**INDUCTOR SELECTION**

Selecting the appropriate inductor type and value ensures optimal performance of the converter circuit for the intended application. This selection process requires the designer to make trade-offs between circuit performance and cost. A primary consideration requires the selection of an inductor that will not saturate at the peak current level. Other considerations that affect inductor choice include EMI, output voltage ripple, and overall circuit efficiency. The inductor that works best depends upon the application's requirements. Further, some experimentation with actual devices in-circuit is typically necessary to make the most effective choice.

The LX1910 allows for a broad selection of inductor values and choosing a value between 2.2μH and 30μH supports a majority of applications. Selecting a larger inductor value can increase efficiency and reduce output voltage ripple. Smaller inductors typically provide smaller package size (critical in many portable applications) at the expense of increasing output ripple current. Regardless of inductor value, selecting a device manufactured with a ferrite-core produces lower losses at higher switching frequencies and thus better overall performance.

**CAPACITOR SELECTION**

To minimize ripple voltage, output capacitors with a low series resistance (ESR) are recommended. Multi-layer ceramic capacitors with X5R or X7R dielectric make an effective choice because they feature small size, very low ESR, a temperature stable dielectric, and can be connected in parallel to increase capacitance. Typical capacitance values of 4.7 to 30μF have proven effective. Other low ESR capacitors such as solid tantalum, specialty polymer, or organic semiconductor, make effective choices provided that the capacitor is properly rated for the output voltage and ripple current. Finally, choose an input capacitor of sufficient size to effectively decouple the input voltage source impedance (e.g., C<sub>IN</sub> ≥ 4.7μF).

**LAYOUT CONSIDERATIONS**

The high peak currents and switching frequencies present in DC/DC converter applications require careful attention to device layout for optimal performance. Basic design rules include: (1) maintaining wide traces for power components (e.g., width > 50mils); (2) place C<sub>IN</sub>, C<sub>OUT</sub>, the Schottky diode, and the inductor close to the LX1910; (3) minimizing trace capacitance by reducing the etch area connecting the SW pin to the inductor; and (4) minimizing the etch length to the FB pin to reduce noise coupling into this high impedance sense input. Other considerations include placing a 0.1μF capacitor between the LX1910 V<sub>OUT</sub> pin and GND pin to reduce high frequency noise and decoupling the V<sub>IN</sub> pin using a 0.1μF capacitor.



#### CHARACTERISTIC CURVES

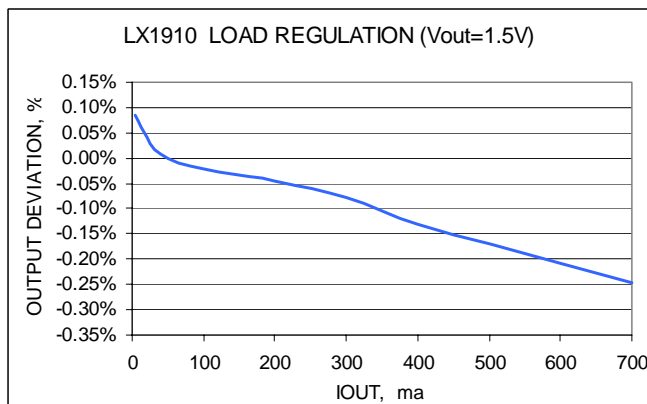


Figure 4

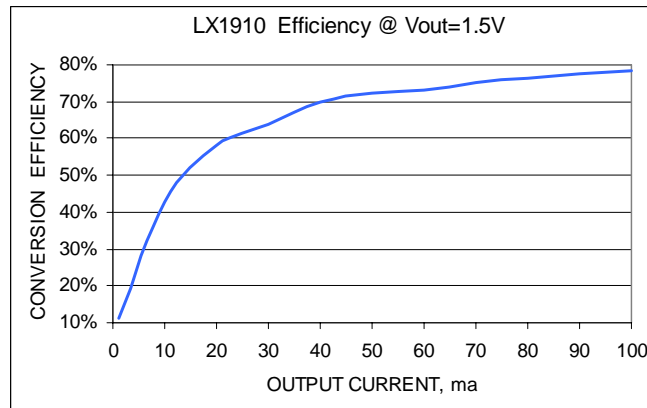


Figure 5

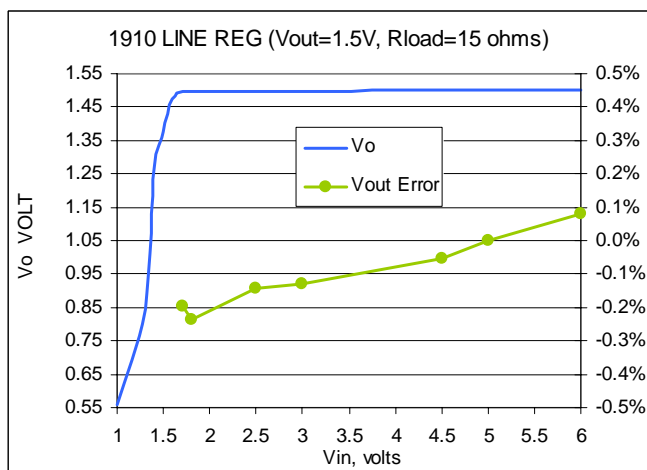


Figure 6

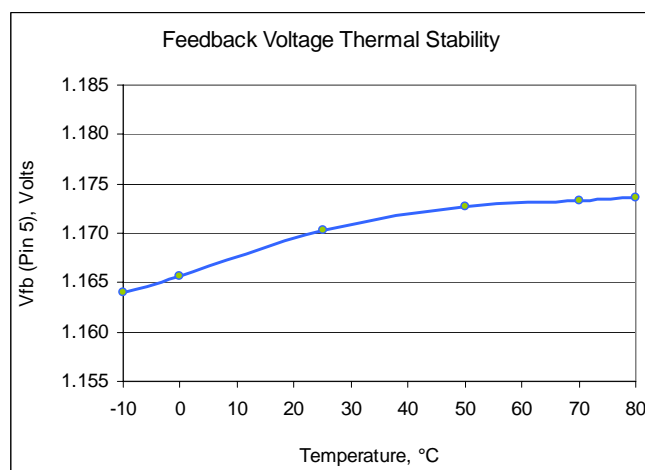
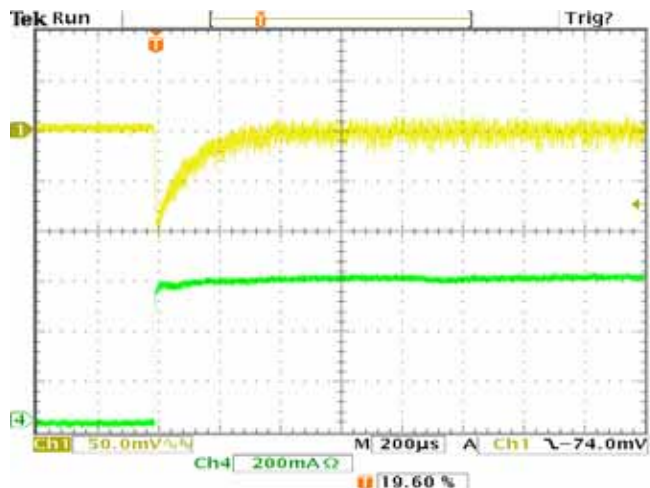
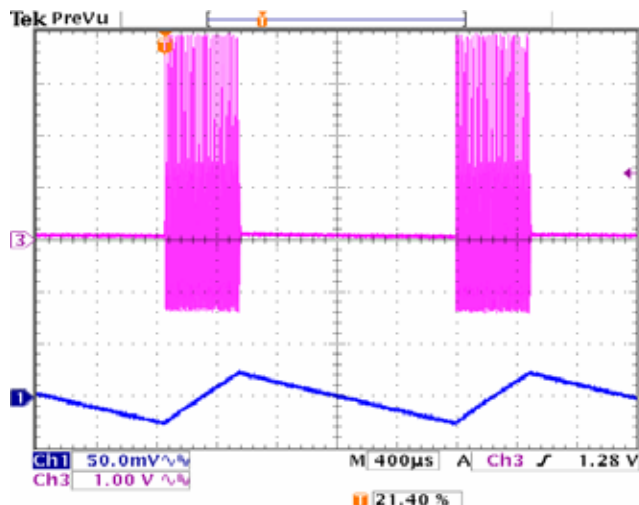


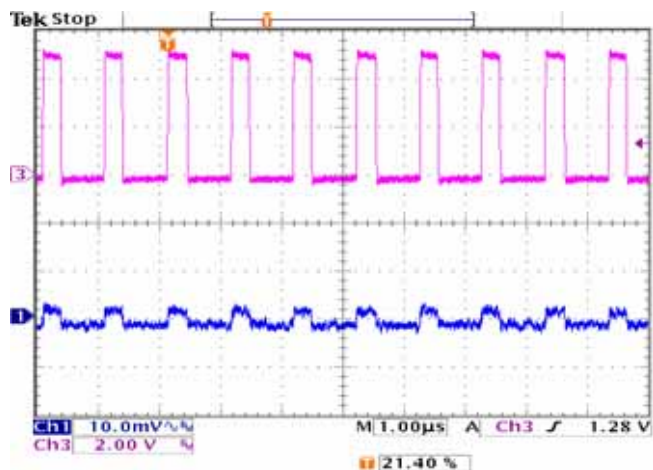
Figure 7

**CHARACTERISTIC CURVES**


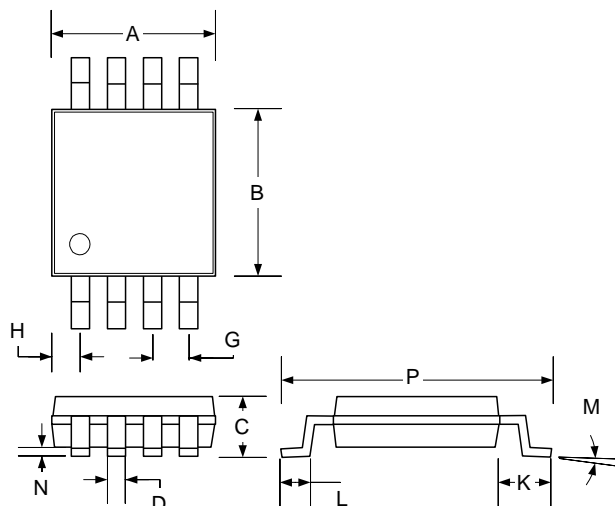
**Figure 9**– Output Load Step Response: CH1:  $V_{OUT}$  and CH4:  $I_{OUT}$ ; Condition:  $V_{IN} = 5.0V$ ;  $I_{STEP} = 50$  to  $600mA$



**Figure 10** – Switching Waveforms: PFM Mode  
CH3:  $V_{SW}$  (pin 8) and CH1:  $V_{OUT}$ ; ( $V_{IN} = 5.0V$ ;  $I_{OUT} = 1mA$ )



**Figure 11** – Switching Waveforms: PWM Mode  
CH3:  $V_{SW}$  (pin 8) and CH1:  $V_{OUT}$ ; ( $V_{IN} = 5.0V$ ;  $I_{OUT} = 10mA$ )

**PACKAGE DIMENSIONS**
**DU 8-Pin Miniature Shrink Outline Package (MSOP)**


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.85	3.05	.112	.120
B	2.90	3.10	.114	.122
C	—	1.10	—	0.043
D	0.25	0.40	0.009	0.160
G	0.65 BSC		0.025 BSC	
H	0.38	0.64	0.015	0.025
J	0.13	0.18	0.005	0.007
K	0.95 BSC		0.037 BSC	
L	0.40	0.70	0.016	0.027
M	3°		3°	
N	0.05	0.15	0.002	0.006
P	4.75	5.05	0.187	0.198

**Note:** Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(0.006") on any side. Lead dimension shall not include solder coverage.

**NOTES**

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