

## Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.



# M28352/M28353/M28354/M28356 (M2835x)

## *Dual/Triple/Quad/Hex DS3/E3/STS-1 Line Interface Unit with Integrated DJAT*

The M28352/M28353/M28354/M28356 (M2835x) is a 2/3/4/6-port Line Interface Unit (LIU) and Desynchronizer/Jitter Attenuator (DJAT) for DS3, E3, and STS-1 applications. This highly-integrated, multi-channel, low power solution is capable of receiving data over 1800 feet of AT&T 734/728 75 ohm type cables and provide standards compliant smooth/de-jittered clock and data to the system.

The M2835x includes diagnostics and quality monitoring functions for the detection of system and board level operating conditions and failures. The device provides the capability to monitor RLOS and RLOS integration per GR-253, transmit loss of signal, transmit open circuits, receiver line input opens and shorts, and clock quality and it includes a clock offset indicator. Diagnostics capabilities include Fixed and PRBS pattern generation/detection, single error insertion and detection, bit and error counters to support Bit Error Rate calculations, and full loopback capabilities.

Each M2835x channel can be independently configured for DS3, E3, or STS-1 applications as a LIU with desynchronizer, LIU with jitter attenuator, or LIU with DJAT disabled or powered down. Each channel can be independently powered down for low power operation.

### Applications

- ◆ Multi-service ATM switches
- ◆ Optical add-drop multiplexers
- ◆ Digital cross-connect systems (DACS)
- ◆ DS3 to STS-1 mappers
- ◆ E3 to STS-1 mappers
- ◆ High-end routers
- ◆ Metro-optical access switches

### Standards Compliant—Complies with all applicable DS3/E3/STS-1 standards:

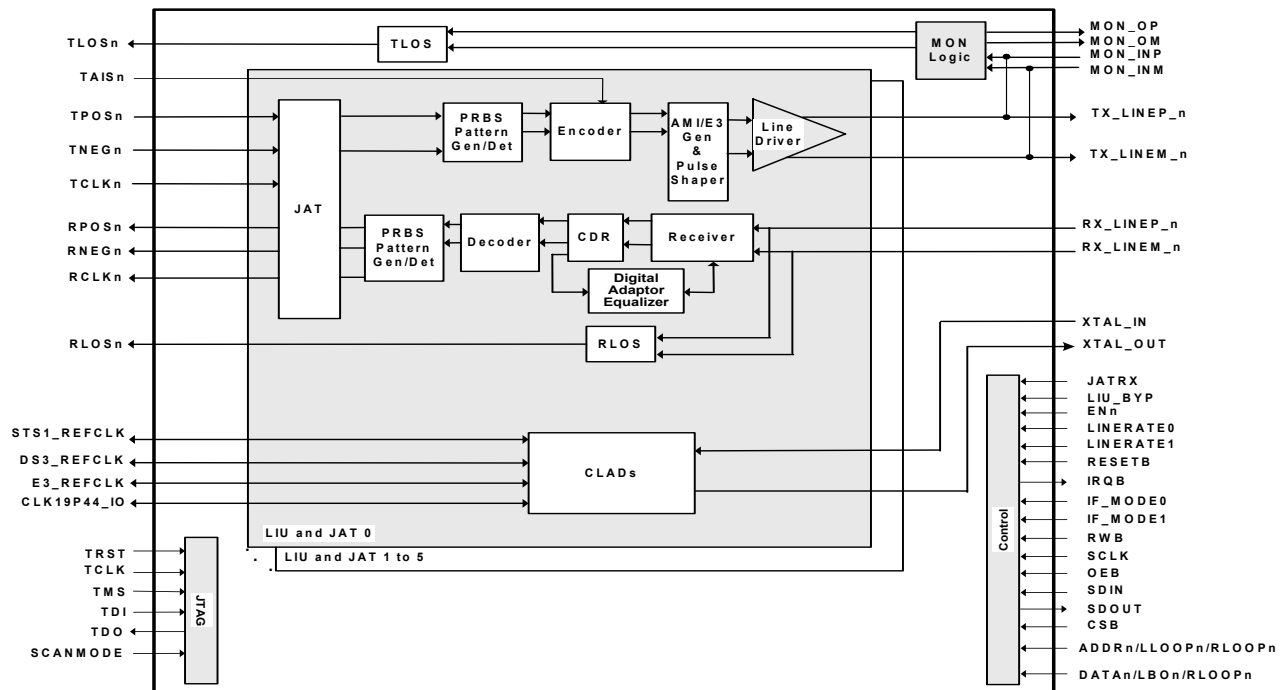
- ◆ Telcordia GR-253, GR-499
- ◆ ETSI TBR-24 and ETS 300
- ◆ ANSI T1.102, T1.105.03b, T1.404
- ◆ ITU-T G.703, G.751, G.755, G.783, G.823, G.824, 0.151
- ◆ AT&T TR54014

### Distinguishing Features

- ◆ Highly Integrated—Up to six independently configured LIUs with jitter attenuator/desynchronizer channels for DS3, E3 and STS-1 applications
- ◆ LIUs with Desynchronizers—For Category I interfaces, smoothes the jitter due to the demapping, bit stuffing, and pointer adjustments in the DS3 or E3 payloads extracted from the STS-1 frames, generating a standards compliant clock.
- ◆ LIUs with Jitter Attenuators—For Category II interfaces, the device synchronizes to jittered DS3, E3 or STS-1 clock and data input signals and produces a de-jittered standards compliant clock and data output.
- ◆ LIUs with Adaptive Equalization—Automatic adaptive equalization up to 1,800 feet for AT&T 734/728 75 ohm type cables
- ◆ Internally Synthesized Clocks—Three Clock Rate Adaptors (CLADs) providing DS3, E3 and/or STS-1 clock rates from a single 19.44 MHz crystal or external input.

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### Functional Block Diagram



## Ordering Information

Model Number	Number of Channels	Package	Operating Temperature
M28352	2	280-ball 19 mm FPBGA	–40 °C to 85 °C
M28353	3	280-ball 19 mm FPBGA	–40 °C to 85 °C
M28354	4	280-ball 19 mm FPBGA	–40 °C to 85 °C
M28356	6	452-ball 27 mm PBGA	–40 °C to 85 °C

## Revision History

Revision	Level	Date	Description
D	Preliminary	May 2003	Changed external reference clock accuracy to +/- 20 ppm.

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## Distinguishing Features

(continued from front page)

- ◆ Three Interfaces for Configuration:
  - Hardware interface pins
  - Serial microprocessor interface port
  - Parallel microprocessor interface port
- ◆ Qualify Monitoring
  - Determines the integrity of the signals
  - Continuously monitor the quality of the connections
  - RLOS receive loss of signal indicator circuit compliant with *ITU-T G.775*
  - TLOS internal or external transmit loss of signal indication
  - DC continuity check of receive input
  - *ITU-T G.772*-compliant monitoring circuit that monitors the performance of transmit signals
  - Clock meter indicates the quality of recovered receive clocks used to alert network operators of variations in the network
- ◆ Alarm Indication Signal—TAIS alarm indication signal for DS3 AIS and E3 AIS
- ◆ Suppression Encoding Error Counters
  - Line Code Violation (LCV) Counter
  - Bipolar Violation (BPV) Counter
  - Excessive Zeros (EXZ) Counter
- ◆ Event Latching—One-second timer for event latching of counters
- ◆ Diagnostics, Per Channel:
  - PRBS detection and/or generation
  - 3-bit Fixed Pattern detection and/or generation (B3ZS testing)
  - 4-bit Fixed Pattern detection and/or generation (HDB3 testing)
  - Single error insertion into generated pattern
  - Single bit error detection and counting
  - Received bit counting to support Bit Error Rate calculations
- ◆ Loopbacks, Per Channel:
  - Line loopback
  - Analog loopback (analog line receive data looped back to analog transmit data)
  - Source loopback
- ◆ JTAG Interface—JTAG (IEEE 1149.1) boundary scan
- ◆ Seamless Framer Interface —Interfaces seamlessly with other components in Mindspeed's DS3/E3 family of devices such as CX28365 and CX2834x (multiport) DS3/E3 framers.

## Operating Conditions

- ◆ Uses 3.3 V and 1.8 V supplies
- ◆ Operates from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

## Power Consumption

- ◆ Independent channel power-down control for low power operation

## Size

- ◆ 6-port device in a 27 mm PBGA package
- ◆ 2, 3, and 4-port devices in a 19 mm FPBGA package



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# 1.0 Product Description

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## 1.1 Overview

This section presents the pin assignments and pin descriptions for the 2835i devices.

[Table 1-1](#) and [Table 1-2](#) illustrate the pin assignments for the left and right halves respectively of the M28356 device in the PBGA package.

[Table 1-3](#) and [Table 1-4](#) illustrate the pin assignments for the left and right halves respectively of the M28354 device in the FPBGA package.

[Table 1-5](#) and [Table 1-6](#) illustrate the pin assignments for the left and right halves respectively of the M28353 device in the FPBGA package.

[Table 1-7](#) and [Table 1-8](#) illustrate the pin assignments for the left and right halves respectively of the M28352 device in the FPBGA package.

[Table 1-10](#) is the description of the pin functions.

## 1.2 Pin Diagrams

### 1.2.1 M28356

**Table 1-1. Pin Assignments for M28356 Device - Left-Hand Side**

	1	2	3	4	5	6	7	8	9	10	11	12	13					
A	JAT1_AVDD	JAT1_AVSS	VSS0	RPOS2/RNRZ2	RNEG2/RLCV2	EN2	TLOS2	JAT2_AVSS	VSS0	DVDD	ADDR8/LL00P4	ADDR5/LL00P1	ADDR4/LL00P0					
B	VSS0	VSS0	VSS0	VSS0	TPOS2/TNRZ2	TCLK2	TAIS2	JAT2_AVDD	VSS0	DVDD	ADDR9/LL00P5	ADDR7/LL00P3	ADDR3/RL00P5					
C	VSS0	TNEG1/NC	VSS0	VSS0	RCLK2	TNEG2/NC	RLOS2	VSS0	VSS0	DVDD	ADDR10	ADDR6/LL00P2	ADDR2/RL00P4					
D	RNEG1/RLCV1	TPOS1/TNRZ1	TCLK1	VSS0	VDDP	VDDP	DVDD	DVSS	DVSS	DVSS	DVDD	DVDD	VDDP					
E	RPOS1RNRZ1	RCLK1	EN1	VDDP														
F	TAIS1	RLOS1	TLOS1	VDDP														
G	JAT0_AVDD	JAT0_AVSS	VSS0	VDDP														
H	RLOS0	TAIS0	TLOS0	DVDD														
J	EN0	TCLK0	TNEG0/NC	DVSS										VSS0	VSS0	VSS0	VSS0	VSS0
K	VSS0	TPOS0/TNRZ0	RCLK0	DVSS										VSS0	VSS0	VSS0	VSS0	VSS0
L	VSS0	RNEG0/RLCV0	RPOS0/RNRZ0	DVSS										VSS0	VSS0	VSS0	VSS0	VSS0
M	TEST	TEST	TEST	DVDD										VSS0	VSS0	VSS0	VSS0	VSS0
N	TEST	TEST	TEST	DVDD										VSS0	VSS0	VSS0	VSS0	VSS0
P	TEST	IRQB	IF_MODE0	DVSS										VSS0	VSS0	VSS0	VSS0	VSS0
R	IF_MODE1	ENENCDEC	LINERATE1	DVSS	VSS0	VSS0	VSS0	VSS0	VSS0									
T	VSS0	JATRX	LINERATE0	VDDP	VSS0	VSS0	VSS0	VSS0	VSS0									
U	VDDP	VDDP	VDDP	VDDP	VSS0	VSS0	VSS0	VSS0	VSS0									
V	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0									
W	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0									
Y	TX_LINEM_0	TX_LINEP_0	TX_AVDD_0	VSS0														
AA	TX_AVSS3P3_0	TX_AVDD3P3_0	TX_AVSS_0	VSS0														
AB	RX_LINEM_0	RX_LINEP_0	RX_AVSS_0	VSS0														
AC	RX_AVDD_0	RX_AVDD_0	RX_AVSS_0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	MON_AVDD	LIU_BYP					
AD	TX_AVDD_1	TX_AVSS_1	RX_AVSS_1	RX_AVSS_1	TX_AVDD_2	TX_AVSS_2	RX_AVSS_2	RX_AVSS_2	VSS0	MON_AVSS	MON_AVSS	MON_AVDD	RBIAS_AVDD					
AE	TX_LINEP_1	TX_AVDD3P3_1	RX_LINEP_1	RX_AVDD_1	TX_LINEP_2	TX_AVDD3P3_2	RX_LINEP_2	RX_AVDD_2	VSS0	MON_INP	MON_AVDD3P3	MON_OP	RBIAS_AVDD					
AF	TX_LINEM_1	TX_AVSS3P3_1	RX_LINEM_1	RX_AVDD_1	TX_LINEM_2	TX_AVSS3P3_2	RX_LINEM_2	RX_AVDD_2	MONITOR_EN	MON_INM	MON_AVSS3P3	MON_OM	RBIAS_AVSS					
	1	2	3	4	5	6	7	8	9	10	11	12	13					

**Table 1-2. Pin Assignments for M28356 Device - Right-Hand Side**

14	15	16	17	18	19	20	21	22	23	24	25	26										
ADDR1/RLOOP3	DATA6/RLOOP0	CLAD2_AVSS	CLAD1_AVSS	DATA3/LB03	DATA1/LB01	RWB	JAT3_AVSS	JAT3_AVDD	RLOS3	TPOS3/TNRZ3	VSS0	JAT4_AVDD	A									
DATA7/RLOOP1	DATA5/LB05	CLAD2_AVDD	CLAD0_AVSS	DATA2/LB02	OEB	VSS0	EN3	TLOS3	TAIS3	RCLK3	VSS0	JAT4_AVSS	B									
ADDR0/RLOOP2	DATA4/LB04	CLAD1_AVDD	CLAD0_AVDD	DATA0/LB00	RESETB	RPOS3/RNRZ3	RNEG3/RLCV3	TNEG3/NC	TCLK3	RPOS4/RNRZ4	VSS0	VSS0	C									
VDDP	DVDD	DVDD	DVSS	DVSS	DVSS	DVDD	VDDP	VDDP	VSS0	RCLK4	RNEG4/RLCV4	TPOS4/TNRZ4	D									
<div></div>									VDDP	EN4	TCLK4	TNEG4/NC	E									
									VDDP	TLOS4	RLOS4	TAIS4	F									
									VDDP	RPOS5/RNRZ5	RNEG5/RLCV5	VSS0	G									
									DVDD	RCLK5	TPOS5/TNRZ5	VSS0	H									
									DVSS	TNEG5/NC	TCLK5	EN5	J									
									DVSS	TLOS5	TAIS5	RLOS5	K									
									DVSS	VSS0	JAT5_AVSS	JAT5_AVDD	L									
									DVDD	TDI	TEST	TDO	M									
									DVDD	TRST	TCK	TMS	N									
									DVSS	SCLK	CSB	SDOUT	P									
									DVSS	MON_CTRL2	TLOSMON	SDIN	R									
									VDDP	MON_CTRL0	MON_CTRL1	VSS0	T									
									VDDP	VDDP	VDDP	VDDP	U									
									VSS0	VSS0	VSS0	VSS0	V									
									VSS0	VSS0	VSS0	VSS0	W									
									VSS0	RX_AVSS_5	RX_AVDD_5	RX_AVDD_5	Y									
									VSS0	RX_AVSS_5	RX_LINEP_5	RX_LINEM_5	AA									
									VSS0	TX_AVSS_5	TX_AVDD3P3_5	TX_AVSS3P3_5	AB									
									DNC	XTAL_AVDD	XTAL_IN2	XTAL_BYP	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	TX_AVDD_5	TX_LINEP_5	TX_LINEM_5	AC
									XOEB	XTAL_AVSS	XTAL_IN1	CLAD_BYP	VSS0	TX_AVDD_3	TX_AVSS_3	RX_AVSS_3	RX_AVSS_3	TX_AVDD_4	TX_AVSS_4	RX_AVSS_4	RX_AVSS_4	AD
RBIAS_AVSS	RBIAS_AVDD3P3	E3_REFCLK	STS1_REFCLK	XTAL_AVDD3P3	TX_LINEP_3	TX_AVDD3P3_3	RX_LINEP_3	RX_AVDD_3	TX_LINEP_4	TX_AVDD3P3_4	RX_LINEP_4	RX_AVDD_4	AE									
RBIAS	RBIAS_AVSS3P3	DS3_REFCLK	CLK19P44_IO	XTAL_AVSS3P3	TX_LINEM_3	TX_AVSS3P3_3	RX_LINEM_3	RX_AVDD_3	TX_LINEM_4	TX_AVSS3P3_4	RX_LINEM_4	RX_AVDD_4	AF									
14	15	16	17	18	19	20	21	22	23	24	25	26										

## 1.2.2 M28354

**Table 1-3. Pin Assignments for M28354 Device - Left-Hand Side**

	1	2	3	4	5	6	7	8	9																																																		
A	VSS0	TX_LINEM_1	TX_AVSS_1	RX_LINEM_0	RX_AVDD_0	TX_LINEM_0	TX_AVDD3P3_0	IF_MODE0	IRQB																																																		
B	VSS0	TX_LINEP_1	TX_AVDD_1	RX_LINEP_0	RX_AVSS_0	TX_LINEP_0	TX_AVSS3P3_0	LINERATE1	TEST																																																		
C	TX_AVDD3P3_1	TX_AVSS3P3_1	RX_AVSS_1	RX_AVDD_0	RX_AVSS_0	TX_AVSS_0	TX_AVDD_0	TEST	LINERATE0																																																		
D	RX_LINEM_1	RX_LINEP_1	RX_AVSS_1	<table><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>DVDD</td><td>DVDD</td></tr><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>RBIAS</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>MON_AVDD3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>RBIAS_AVSS3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>XTAL_AVSS3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>XTAL_AVDD3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>TX_AVSS_3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>TX_AVDD_3</td><td>VSS0</td><td>VSS0</td><td>DVDD</td><td>DVDD</td></tr></table>						VSS0	VSS0	VSS0	DVDD	DVDD	VSS0	VSS0	VSS0	VSS0	VSS0	RBIAS	VSS0	VSS0	VSS0	VSS0	MON_AVDD3P3	VSS0	VSS0	VSS0	VSS0	RBIAS_AVSS3P3	VSS0	VSS0	VSS0	VSS0	XTAL_AVSS3P3	VSS0	VSS0	VSS0	VSS0	XTAL_AVDD3P3	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	TX_AVSS_3	VSS0	VSS0	VSS0	VSS0	TX_AVDD_3	VSS0	VSS0	DVDD	DVDD
VSS0	VSS0	VSS0	DVDD							DVDD																																																	
VSS0	VSS0	VSS0	VSS0							VSS0																																																	
RBIAS	VSS0	VSS0	VSS0							VSS0																																																	
MON_AVDD3P3	VSS0	VSS0	VSS0							VSS0																																																	
RBIAS_AVSS3P3	VSS0	VSS0	VSS0							VSS0																																																	
XTAL_AVSS3P3	VSS0	VSS0	VSS0							VSS0																																																	
XTAL_AVDD3P3	VSS0	VSS0	VSS0							VSS0																																																	
VSS0	VSS0	VSS0	VSS0							VSS0																																																	
TX_AVSS_3	VSS0	VSS0	VSS0							VSS0																																																	
TX_AVDD_3	VSS0	VSS0	DVDD	DVDD																																																							
E	MON_AVSS	MON_AVDD	RX_AVDD_1																																																								
F	MON_INM	MON_INP	RX_AVDD_1																																																								
G	RBIAS_AVDD	MONITOR_EN	RBIAS_AVSS																																																								
H	MON_OM	MON_OP	RBIAS_AVDD3P3																																																								
J	X0EB	LIU_BYP	DNC																																																								
K	XTAL_IN1	MON_AVSS3P3	XTAL_AVSS																																																								
L	XTAL_AVDD	CLAD_BYP	CLK19P44_IO																																																								
M	E3_REFCLK	DS3_REFCLK	VSS0																																																								
N	XTAL_IN2	STS1_REFCLK	VSS0																																																								
P	XTAL_BYP	VSS0	VSS0																																																								
R	TX_LINEP_3	TX_LINEM_3	RX_AVDD_3																																																								
T	TX_AVDD3P3_3	TX_AVSS3P3_3	RX_AVDD_3	RX_AVDD_2	RX_AVSS_2	TX_AVSS_2	TX_AVDD_2	MON_CTRL0	SDOUT																																																		
U	VSS0	RX_LINEM_3	RX_AVSS_3	RX_LINEM_2	RX_AVSS_2	TX_LINEM_2	TX_AVDD3P3_2	MON_CTRL1	TDI																																																		
V	VSS0	RX_LINEP_3	RX_AVSS_3	RX_LINEP_2	RX_AVDD_2	TX_LINEP_2	TX_AVSS3P3_2	CSB	SCLK																																																		
	1	2	3	4	5	6	7	8	9																																																		

**Table 1-4. Pin Assignments for M28354 Device - Right-Hand Side**

10	11	12	13	14	15	16	17	18	
TEST	TEST	TEST	RPOS0/ RNRZ0	TNEG0/NC	TCLK0	RLOS1	TPOS1/TNRZ1	TAIS1	<b>A</b>
TEST	IF_MODE1	RCLK0	RNEG0/RLCV0	EN0	RLOS0	TLOS0	DVSS	TCLK1	<b>B</b>
JATRX	ENENCDEC	TEST	DVSS	DVSS	TAIS0	TPOS0/TNRZ0	RCLK1	ADDR10	<b>C</b>
						RNEG1/RLCV1	RPOS1/ RNRZ1	ADDR9/LL00P3	<b>D</b>
						VDDP	EN1	ADDR8/LL00P2	<b>E</b>
						VDDP	TNEG1/NC	ADDR7	<b>F</b>
						VDDP	TLOS1	ADDR6	<b>G</b>
						ADDR0	ADDR1	ADDR5/LL00P1	<b>H</b>
						DVDD	DVDD	ADDR4/LL00P0	<b>J</b>
						CLAD2_AVDD	DVDD	ADDR3/RL00P3	<b>K</b>
						CLAD1_AVDD	DVDD	ADDR2/RL00P2	<b>L</b>
						CLAD0_AVDD	DVDD	DATA7/RL00P1	<b>M</b>
						TAIS2	OEB	DATA6/RL00P0	<b>N</b>
						TPOS2/TNRZ2	RCLK2	DATA5/LB03	<b>P</b>
						TCLK2	TNEG2/NC	DATA4/LB02	<b>R</b>
MON_CTRL2	TNEG3/NC	TLOSMON	JAT3_AVDD	RLOS3	EN3	EN2	RLOS2	DATA3	<b>T</b>
TCK	SDIN	TEST	TLOS3	TAIS3	RNEG3/RLCV3	RPOS2/RNRZ2	RNEG2/RLCV2	DATA2	<b>U</b>
TRST	TMS	TDO	TCLK3	RCLK3	TPOS3/TNRZ3	RPOS3/RNRZ3	DATA0/LB00	DATA1/LB01	<b>V</b>
10	11	12	13	14	15	16	17	18	

## 1.2.3 M28353

**Table 1-5. Pin Assignments for M28353 Device - Left-Hand Side**

	1	2	3	4	5	6	7	8	9																																																		
A	VSS0	TX_LINEM_1	TX_AVSS_1	RX_LINEM_0	RX_AVDD_0	TX_LINEM_0	TX_AVDD3P3_0	IF_MODE0	IRQB																																																		
B	VSS0	TX_LINEP_1	TX_AVDD_1	RX_LINEP_0	RX_AVSS_0	TX_LINEP_0	TX_AVSS3P3_0	LINERATE1	TEST																																																		
C	TX_AVDD3P3_1	TX_AVSS3P3_1	RX_AVSS_1	RX_AVDD_0	RX_AVSS_0	TX_AVSS_0	TX_AVDD_0	TEST	LINERATE0																																																		
D	RX_LINEM_1	RX_LINEP_1	RX_AVSS_1	<table><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>DVDD</td><td>DVDD</td></tr><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>RBIAS</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>MON_AVDD3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>RBIAS_AVSS3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>XTAL_AVSS3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>XTAL_AVDD3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>AVSS</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>AVDD</td><td>VSS0</td><td>VSS0</td><td>DVDD</td><td>DVDD</td></tr></table>						VSS0	VSS0	VSS0	DVDD	DVDD	VSS0	VSS0	VSS0	VSS0	VSS0	RBIAS	VSS0	VSS0	VSS0	VSS0	MON_AVDD3P3	VSS0	VSS0	VSS0	VSS0	RBIAS_AVSS3P3	VSS0	VSS0	VSS0	VSS0	XTAL_AVSS3P3	VSS0	VSS0	VSS0	VSS0	XTAL_AVDD3P3	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	AVSS	VSS0	VSS0	VSS0	VSS0	AVDD	VSS0	VSS0	DVDD	DVDD
VSS0	VSS0	VSS0	DVDD							DVDD																																																	
VSS0	VSS0	VSS0	VSS0							VSS0																																																	
RBIAS	VSS0	VSS0	VSS0							VSS0																																																	
MON_AVDD3P3	VSS0	VSS0	VSS0							VSS0																																																	
RBIAS_AVSS3P3	VSS0	VSS0	VSS0							VSS0																																																	
XTAL_AVSS3P3	VSS0	VSS0	VSS0							VSS0																																																	
XTAL_AVDD3P3	VSS0	VSS0	VSS0							VSS0																																																	
VSS0	VSS0	VSS0	VSS0							VSS0																																																	
AVSS	VSS0	VSS0	VSS0							VSS0																																																	
AVDD	VSS0	VSS0	DVDD	DVDD																																																							
E	MON_AVSS	MON_AVDD	RX_AVDD_1																																																								
F	MON_INM	MON_INP	RX_AVDD_1																																																								
G	RBIAS_AVDD	MONITOR_EN	RBIAS_AVSS																																																								
H	MON_OM	MON_OP	RBIAS_AVDD3P3																																																								
J	X0EB	LIU_BYP	DNC																																																								
K	XTAL_IN1	MON_AVSS3P3	XTAL_AVSS																																																								
L	XTAL_AVDD	CLAD_BYP	CLK19P44_IO																																																								
M	E3_REFCLK	DS3_REFCLK	VSS0																																																								
N	XTAL_IN2	STS1_REFCLK	VSS0																																																								
P	XTAL_BYP	VSS0	VSS0																																																								
R	TEST	TEST	AVDD																																																								
T	AVDD3P3	AVSS3P3	AVDD	RX_AVDD_2	RX_AVSS_2	TX_AVSS_2	TX_AVDD_2	MON_CTRL0	SDOUT																																																		
U	VSS0	TEST	AVSS	RX_LINEM_2	RX_AVSS_2	TX_LINEM_2	TX_AVDD3P3_2	MON_CTRL1	TDI																																																		
V	VSS0	TEST	AVSS	RX_LINEP_2	RX_AVDD_2	TX_LINEP_2	TX_AVSS3P3_2	CSB	SCLK																																																		
	1	2	3	4	5	6	7	8	9																																																		

**Table 1-6. Pin Assignments for M28353 Device - Right-Hand Side**

10	11	12	13	14	15	16	17	18				
TEST	TEST	TEST	RPOS0/RNRZ0	TNEG0/NC	TCLK0	RLOS1	TPOS1/TNRZ1	TAIS1	A			
TEST	IF_MODE1	RCLK0	RNEG0/RLCV0	EN0	RLOS0	TLOS0	DVSS	TCLK1	B			
JATRX	ENENCDEC	TEST	DVSS	DVSS	TAIS0	TPOS0/TNRZ0	RCLK1	ADDR10	C			
						RNEG1/RLCV1	RPOS1/RNRZ1	ADDR9	D			
						VDDP	EN1	ADDR8/LLOOP2	E			
						VDDP	TNEG1/NC	ADDR7	F			
						VDDP	TLOS1	ADDR6	G			
						ADDR0	ADDR1	ADDR5/LLOOP1	H			
						DVDD	DVDD	ADDR4/LLOOP0	J			
						CLAD2_AVDD	DVDD	ADDR3	K			
						CLAD1_AVDD	DVDD	ADDR2/RLOOP2	L			
						CLAD0_AVDD	DVDD	DATA7/RLOOP1	M			
						TAIS2	OEB	DATA6/RLOOP0	N			
DVDD	DVSS	DVSS	NC	TLOS2					TPOS2/TNRZ2	RCLK2	DATA5	P
									TCLK2	TNEG2/NC	DATA4/LB02	R
MON_CTRL2	NC	TLOSMON	NC	NC	NC	EN2	RLOS2	DATA3	T			
TCK	SDIN	TEST	NC	NC	NC	RPOS2/RNRZ2	RNEG2/RLCV2	DATA2	U			
TRST	TMS	TDO	NC	NC	NC	NC	DATA0/LB00	DATA1/LB01	V			
10	11	12	13	14	15	16	17	18				

## 1.2.4

## M28352

**Table 1-7. Pin Assignments for M28352 Device - Left-Hand Side**

	1	2	3	4	5	6	7	8	9																																																		
A	VSS0	TX_LINEM_1	TX_AVSS_1	RX_LINEM_0	RX_AVDD_0	TX_LINEM_0	TX_AVDD3P3_0	IF_MODE0	IRQB																																																		
B	VSS0	TX_LINEP_1	TX_AVDD_1	RX_LINEP_0	RX_AVSS_0	TX_LINEP_0	TX_AVSS3P3_0	LINERATE1	TEST																																																		
C	TX_AVDD3P3_1	TX_AVSS3P3_1	RX_AVSS_1	RX_AVDD_0	RX_AVSS_0	TX_AVSS_0	TX_AVDD_0	TEST	LINERATE0																																																		
D	RX_LINEM_1	RX_LINEP_1	RX_AVSS_1	<table><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>DVDD</td><td>DVDD</td></tr><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>RBIAS</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>MON_AVDD3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>RBIAS_AVSS3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>XTAL_AVSS3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>XTAL_AVDD3P3</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>AVSS</td><td>VSS0</td><td>VSS0</td><td>VSS0</td><td>VSS0</td></tr><tr><td>AVDD</td><td>VSS0</td><td>VSS0</td><td>DVDD</td><td>DVDD</td></tr></table>						VSS0	VSS0	VSS0	DVDD	DVDD	VSS0	VSS0	VSS0	VSS0	VSS0	RBIAS	VSS0	VSS0	VSS0	VSS0	MON_AVDD3P3	VSS0	VSS0	VSS0	VSS0	RBIAS_AVSS3P3	VSS0	VSS0	VSS0	VSS0	XTAL_AVSS3P3	VSS0	VSS0	VSS0	VSS0	XTAL_AVDD3P3	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	VSS0	AVSS	VSS0	VSS0	VSS0	VSS0	AVDD	VSS0	VSS0	DVDD	DVDD
VSS0	VSS0	VSS0	DVDD							DVDD																																																	
VSS0	VSS0	VSS0	VSS0							VSS0																																																	
RBIAS	VSS0	VSS0	VSS0							VSS0																																																	
MON_AVDD3P3	VSS0	VSS0	VSS0							VSS0																																																	
RBIAS_AVSS3P3	VSS0	VSS0	VSS0							VSS0																																																	
XTAL_AVSS3P3	VSS0	VSS0	VSS0							VSS0																																																	
XTAL_AVDD3P3	VSS0	VSS0	VSS0							VSS0																																																	
VSS0	VSS0	VSS0	VSS0							VSS0																																																	
AVSS	VSS0	VSS0	VSS0							VSS0																																																	
AVDD	VSS0	VSS0	DVDD	DVDD																																																							
E	MON_AVSS	MON_AVDD	RX_AVDD_1																																																								
F	MON_INM	MON_INP	RX_AVDD_1																																																								
G	RBIAS_AVDD	MONITOR_EN	RBIAS_AVSS																																																								
H	MON_OM	MON_OP	RBIAS_AVDD3P3																																																								
J	XOEB	LIU_BYP	DNC																																																								
K	XTAL_IN1	MON_AVSS3P3	XTAL_AVSS																																																								
L	XTAL_AVDD	CLAD_BYP	CLK19P44_IO																																																								
M	E3_REFCLK	DS3_REFCLK	VSS0																																																								
N	XTAL_IN2	STS1_REFCLK	VSS0																																																								
P	XTAL_BYP	VSS0	VSS0																																																								
R	TEST	TEST	AVDD																																																								
T	AVDD3P3	AVSS3P3	AVDD	AVDD	AVSS	AVSS	AVDD	MON_CTRL0	SDOUT																																																		
U	VSS0	TEST	AVSS	TEST	AVSS	TEST	AVDD3P3	MON_CTRL1	TDI																																																		
V	VSS0	TEST	AVSS	TEST	AVDD	TEST	AVSS3P3	CSB	SCLK																																																		
	1	2	3	4	5	6	7	8	9																																																		



**Table 1-8. Pin Assignments for M28352 Device - Right-Hand Side**

10	11	12	13	14	15	16	17	18		
TEST	TEST	TEST	RPOS0/RNRZ0	TNEG0/NC	TCLK0	RLOS1	TPOS1/TNRZ1	TAIS1	A	
TEST	IF_MODE1	RCLK0	RNEG0/RLCV0	EN0	RLOS0	TLOS0	DVSS	TCLK1	B	
JATRX	ENENCDEC	TEST	DVSS	DVSS	TAIS0	TPOS0/TNRZ0	RCLK1	ADDR10	C	
						RNEG1/RLCV1	RPOS1/RNRZ1	ADDR9	D	
						VDDP	EN1	ADDR8	E	
						VDDP	TNEG1/NC	ADDR7	F	
						VDDP	TLOS1	ADDR6	G	
						ADDR0	ADDR1	ADDR5/LLOOP1	H	
						DVDD	DVDD	ADDR4/LLOOP0	J	
						CLAD2_AVDD	DVDD	ADDR3	K	
						CLAD1_AVDD	DVDD	ADDR2	L	
						CLAD0_AVDD	DVDD	DATA7/RLOOP1	M	
						NC	OEB	DATA6/RLOOP0	N	
DVDD	DVSS	DVSS	NC	NC			NC	NC	DATA5	P
						NC	NC	DATA4	R	
MON_CTRL2	NC	TLOSMON	NC	NC	NC	NC	NC	DATA3	T	
TCK	SDIN	TEST	NC	NC	NC	NC	NC	DATA2	U	
TRST	TMS	TDO	NC	NC	NC	NC	DATA0/LB00	DATA1/LB01	V	
10	11	12	13	14	15	16	17	18		

## 1.3 Pin Definitions

Table 1-9 lists pin type definitions and abbreviations used in Table 1-10, Pin Descriptions.

**Table 1-9. Pin Type Abbreviations and Definitions**

Abbreviation	Definition
DNC	Pin present but <b>DO NOT CONNECT</b>
NC	Pin present but does not require connection
IPD	Digital input, CMOS levels, internal pull-down resistor
IPU	Digital input, CMOS levels, internal pull-up resistor
ID/OD	Digital bidirectional
OD	Digital output, CMOS levels, 12 mA drive, 32 $\Omega$ equivalent drive impedance
ODO	Open drain output, no internal pull up. 12 mA current sink
Z	Digital high impedance output
PD	Digital power
GD	Digital ground
PA	Analog power
GA	Analog ground
IA	Analog input
OA	Analog output

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (1 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
Digital Data						
A13	A13	A13	L3	RPOS0/ RNRZ0	OD/Z	Receive positive rail or NRZ data. Receive negative rail or line code violation Resynchronized receive data strobed out by the corresponding RCLK. ENENCDEC = 0, the outputs are positive and negative AMI data, i.e. RPOS and RNEG ENENCDEC = 1, the outputs are decoded NRZ data and line code violation.
B13	B13	B13	L2	RNEG0/ RLCV0	OD/Z	
D17	D17	D17	E1	RPOS1/ RNRZ1	OD/Z	
D16	D16	D16	D1	RNEG1/ RLCV1	OD/Z	
	U16	U16	A4	RPOS2/ RNRZ2	OD/Z	
	U17	U17	A5	RNEG2/ RLCV2	OD/Z	
		V16	C20	RPOS3/ RNRZ3	OD/Z	
		U15	C21	RNEG3/ RLCV3	OD/Z	
			C24	RPOS4/ RNRZ4	OD/Z	
			D25	RNEG4/ RLCV4	OD/Z	
			G24	RPOS5/ RNRZ5	OD/Z	
			G25	RNEG5/ RLCV5	OD/Z	
B12	B12	B12	K3	RCLK0	OD/Z	Recovered clock from each channel receiver for strobing the corresponding receive data into a companion framer or logic
C17	C17	C17	E2	RCLK1	OD/Z	
	P17	P17	C5	RCLK2	OD/Z	
		V14	B24	RCLK3	OD/Z	
			D24	RCLK4	OD/Z	
			H24	RCLK5	OD/Z	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (2 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
C16	C16	C16	K2	TPOS0/ TNRZ0	IPU	Transmit positive rail or NRZ data. Transmit negative rail or line code violation. Synchronized transmit data strobed in by the corresponding TCLK. ENENCDEC = 0, the inputs are positive and negative AMI data, i.e. TPOS and TNEG ENENCDEC = 1, the inputs are decoded NRZ data and no connects.
A14	A14	A14	J3	TNEG0/NC	IPU	
A17	A17	A17	D2	TPOS1/ TNRZ1	IPU	
F17	F17	F17	C2	TNEG1/NC	IPU	
	P16	P16	B5	TPOS2/ TNRZ2	IPU	
	R17	R17	C6	TNEG2/NC	IPU	
		V15	A24	TPOS3/ TNRZ3	IPU	
		T11	C22	TNEG3/NC	IPU	
			D26	TPOS4/ TNRZ4	IPU	
			E26	TNEG4/NC	IPU	
			H25	TPOS5/ TNRZ5	IPU	
			J24	TNEG5/NC	IPU	
A15	A15	A15	J2	TCLK0	IPU	Transmit bit clock inputs for strobing transmit data bits into the device.
B18	B18	B18	D3	TCLK1	IPU	
	R16	R16	B6	TCLK2	IPU	
		V13	C23	TCLK3	IPU	
			E25	TCLK4	IPU	
			J25	TCLK5	IPU	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (3 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
Analog Line - Inputs						
B4	B4	B4	AB2	RX_LINEP_0	IA	Positive and negative receive data. Differential inputs for each channel from its respective receive coax line. The receiver expects balanced differential inputs, usually achieved using a 1:1 transformer. The inputs are internally DC biased to 1.5 Volts.
A4	A4	A4	AB1	RX_LINEM_0	IA	
D2	D2	D2	AE3	RX_LINEP_1	IA	
D1	D1	D1	AF3	RX_LINEM_1	IA	
	V4	V4	AE7	RX_LINEP_2	IA	
	U4	U4	AF7	RX_LINEM_2	IA	
		V2	AE21	RX_LINEP_3	IA	
		U2	AF21	RX_LINEM_3	IA	
			AE25	RX_LINEP_4	IA	
			AF25	RX_LINEM_4	IA	
			AA25	RX_LINEP_5	IA	
			AA26	RX_LINEM_5	IA	
Analog Line - Outputs						

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (4 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
B6	B6	B6	Y2	TX_LINEP_ 0	OA	Positive and negative transmit data. Differential, coax driver balanced outputs for pulse shaped AMI B3ZS/HDB3 encoded waveforms for each channel. These pins should be connected to the primary side of the 1:1 transformer through two back matched resistors. The outputs are internally DC biased to VDD/2 volts
A6	A6	A6	Y1	TX_LINEM_ 0	OA	
B2	B2	B2	AE1	TX_LINEP_ 1	OA	
A2	A2	A2	AF1	TX_LINEM_ 1	OA	
	V6	V6	AE5	TX_LINEP_ 2	OA	
	U6	U6	AF5	TX_LINEM_ 2	OA	
		R1	AE19	TX_LINEP_ 3	OA	
		R2	AF19	TX_LINEM_ 3	OA	
			AE23	TX_LINEP_ 4	OA	
			AF23	TX_LINEM_ 4	OA	
			AC25	TX_LINEP_ 5	OA	
			AC26	TX_LINEM_ 5	OA	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (5 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
RLOS						
B15	B15	B15	H1	RLOS0	OD	Receive Loss of Signal indication for each channel. Signal loss is indicated when RLOS <sub>n</sub> = V <sub>dd</sub> .
A16	A16	A16	F2	RLOS1	OD	
	T17	T17	C7	RLOS2	OD	
		T14	A23	RLOS3	OD	
			F25	RLOS4	OD	
			K26	RLOS5	OD	
Transmit AIS						
C15	C15	C15	H2	TAIS0	IPD	Transmission of Alarm Indication Signal for each channel. Replaces the transmit data with AIS.  1 = AIS mode enabled 0 = AIS mode disabled <b>Note:</b> In software mode, this pin must be left unconnected or pulled low.
A18	A18	A18	F1	TAIS1	IPD	
	N16	N16	B7	TAIS2	IPD	
		U14	B23	TAIS3	IPD	
			F26	TAIS4	IPD	
			K25	TAIS5	IPD	
Transmit Monitoring						
G2	G2	G2	AF9	MONITOR_EN	IPD	Enable transmit channel monitor. This control line activates monitoring lines. 1 = channel monitor enabled 0 = channel monitor disabled
F2	F2	F2	AE10	MON_INP	IA	Optional positive and negative transmit monitor input for TLOS.
F1	F1	F1	AF10	MON_INM	IA	
H2	H2	H2	AE12	MON_OP	OA	Current TPOS and TNEG signals being monitored for TLOS.
H1	H1	H1	AF12	MON_OM	OA	
T8	T8	T8	T24	MON_CTR L0	OD	Output control bit for external monitoring scheme Refer to appendix A
U8	U8	U8	T25	MON_CTR L1	OD	
T10	T10	T10	R24	MON_CTR L2	OD	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (6 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
TLOS						
B16	B16	B16	H3	TLOS0	OD	Transmit Loss of Signal indication for each channel. Signal loss is indicated when TLOS <sub>n</sub> = V <sub>dd</sub> .
G17	G17	G17	F3	TLOS1	OD	
	P14	P14	A7	TLOS2	OD	
		U13	B22	TLOS3	OD	
			F24	TLOS4	OD	
			K24	TLOS5	OD	
T12	T12	T12	R25	TLOSMON	OD	TLOS monitor signal
Control Signals						
C11	C11	C11	R2	ENENCDEC	IPU	Enable/disable the encoder/decoder for all channels.  0 = Dual rail format (encoder/decoder disabled). Input transmit data pins are interpreted as TPOS and TNEG, encoded positive and negative rail data. Output receive data pins are interpreted as RPOS and RNEG. RPOS pulsed for every positive AMI pulse and RNEG pulsed for every negative AMI pulse.  1 = NRZ format (encoder/decoder enabled). Input transmit data pins are interpreted as TNRZ and NC. Output receive data pins are interpreted as RNRZ and RLCV. Line code violations are signalled with a high going pulse on RLCV. <b>Note:</b> When in software mode, this pin should be left unconnected or pulled high..
J1	J1	J1	AD14	XOEB	IPD	Transmit output enable for all channels.  0 = Transmit line output drivers enabled  1 = Transmit line output drivers set to high impedance state <b>Note:</b> In software mode, this pin should be left unconnected or pulled low.



**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (7 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
B8	B8	B8	R3	LINERATE1	IPD	Selects the device operating mode for all channels. LINERATE[1:0] = 00 selects STS-1 mode LINERATE[1:0] = 01 selects DS3 mode LINERATE[1:0] = 1x selects E3 mode In E3 mode, the pulse shaper is changed, the LBO settings are ignored, and the encoder/decoder is set to HDB3 line coding.
C9	C9	C9	T3	LINERATE0	IPU	
N14	N14	N14	C19	RESETB	IPU	Asynchronous device reset - active low. The device will be in reset when pulled to V <sub>ss</sub> .
B11	B11	B11	R1	IF_MODE1	IPD	Selects the uP interface mode. IF_MODE[1:0] = 00 selects Hardware mode IF_MODE[1:0] = 01 Reserved IF_MODE[1:0] = 10 selects Parallel mode IF_MODE[1:0] = 11 selects Serial mode
A8	A8	A8	P3	IF_MODE0	IPD	
C10	C10	C10	T2	JATRX	IPD	DJAT direction for all channels 0 = DJAT enabled in the transmit direction 1 = DJAT enabled in the receive direction
J2	J2	J2	AC13	LIU_BYP	IPD	LIU bypass for all channels. 0 = LIU not bypassed 1 = LIU bypassed LIU bypass is used to verify that TPOS <sub>n</sub> and TCLK <sub>n</sub> inputs (NRZ Mode) or TPOS <sub>n</sub> and TNEG <sub>n</sub> inputs are seen on the TX_LINEP <sub>n</sub> and TX_LINEM <sub>n</sub> outputs respectively. <b>Note:</b> In this test, DJAT, CLAD and XTAL blocks must be set to bypass mode.

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (8 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
Channel Enables						
B14	B14	B14	J1	EN0	IPU	Channel enable.  0 = Channel disabled 1 = Channel enabled  When a channel is disabled, all receive and transmit analog circuitry power down. Analog inputs are ignored and analog outputs set to a high impedance state. Digital inputs of a powered down channel are still active, but ignored. Device noise can be lowered by not switching the digital inputs of a powered down channel.  <b>Note:</b> In software mode, this pin must be left unconnected or pulled high.
E17	E17	E17	E3	EN1	IPU	
	T16	T16	A6	EN2	IPU	
		T15	B21	EN3	IPU	
			E24	EN4	IPU	
			J26	EN5	IPU	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (9 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
Oscillator and CLAD Control						
K1	K1	K1	AD16	XTAL_IN1	IA	Crystal oscillator input. This pin is paired with the XTAL_IN2 pin as balanced inputs (i.e., no polarity requirements) for the 19.44 MHz crystal.
N1	N1	N1	AC16	XTAL_IN2	OA	Crystal oscillator input. This pin is paired with the XTAL_IN1 pin as balanced inputs (i.e., no polarity requirements) for the 19.44 MHz crystal. <b>NOTES:</b> 1. The 19.44 MHz crystal connected across the XTAL_IN1 and XTAL_IN2 pins must have an accuracy of +/- 10 ppm--refer to Section 4.5 for details. 2. For DS3 and E3 applications, refer to Section 4.5 for details on the 19.44 MHz crystal jitter specifications.
L3	L3	L3	AF17	CLK19P44_IO	IA/ OA	19.44 MHz ±20 ppm clock input or output. Input or output direction is controlled by the XTAL_BYP pin. <b>NOTES:</b> 1. When the pin is configured as an input and the CLADs are enabled (not bypassed), the external 19.44 MHz reference clock must have an accuracy of +/- 20 ppm--refer to Section 4.5 for details. 2. For DS3 and E3 applications, refer to Section 4.5 for details on the clock jitter specifications. 3. When the pin is configured as an input and the CLADs are bypassed, an external clock must be provided to the pin; the maximum acceptable rate of the external clock is 26-MHz; and it may be derived by dividing an external STS-1, DS3, or E3 clock by two. Refer to the notes in Section 2.2.1 for details.
P1	P1	P1	AC17	XTAL_BYP	IPD	Internal crystal oscillator bypass. The internal 19.44 MHz oscillator circuitry is bypassed and disabled. 1 = bypassed: CLK19P44_IO pin is an input 0 = not bypassed: CLK19P44_IO pin is an output

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (10 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
N2	N2	N2	AE17	STS1_REFCLK	IA/OA	STS-1 clock input or output. Input or output direction is controlled by the CLAD_BYP pin. <b>NOTE:</b> If the CLADs are bypassed, an external reference clock must be supplied to this pin; however, a slower rate reference clock (e.g., DS3 reference clock) may be used to meet the requirement if the STS-1 line rate mode is not used. Refer to Section 2.2.1 for details.
M2	M2	M2	AF16	DS3_REFCLK	IA/OA	DS3 clock input or output. Input or output direction is controlled with CLAD_BYP pin. <b>NOTE:</b> Refer to Section 2.2.1 for more details.
M1	M1	M1	AE16	E3_REFCLK	IA/OA	E3 clock input or output. Input or output direction is controlled with CLAD_BYP pin. <b>NOTE:</b> Refer to Section 2.2.1 for more details.
L2	L2	L2	AD17	CLAD_BYP	IPD	CLAD bypass for all three (3) CLADs. 0 = CLADs are enabled and the three line reference clock pins (i.e., STS1_REFCLK, DS3_REFCLK, and E3_REFCLK pins) are clock outputs. 1 = CLADs are bypassed and the three line reference clock pins are inputs. <b>NOTES:</b> 1. When the CLAD are bypassed, an external reference clock must be connected to the STS1_REFCLK even if STS-1 line mode is not used. Refer to Section 2.2.1 for details. 2. In software mode, the CLAD_BYP pin must be used to configure the three line reference clock pins as outputs or inputs.
<b>References</b>						
G5	G5	G5	AF14	RBIAS <sup>(1)</sup>	IA/OA	Bias resistor for the current generator. Very sensitive DC analog signal.
1. Connect a 12.1 Kohm 1% 0402 surface mount resistor between the RBIAS pin and the RBIAS_AVSS pin. The resistor should be mounted as close as possible to the pins to reduce noise coupling and thereby ensure optimum performance. The pin pattern allows room for mounting the resistor on the opposite side of the board between the pins underneath the device. If you cannot mount the resistors close to the pins, then provide shielding by routing a ground plane connected to the RBIAS_AVSS pin along the length of the RBIAS trace in the layer immediately beneath the RBIAS trace. In addition, pairs of spaced vias along the length of the ground plane should come out of the ground plane up to the RBIAS trace layer on either side of the trace.						
J3	J3	J3	AC14	DNC	OA	Analog output of the temperature sensor.

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (11 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
Host Interface Control						
V8	V8	V8	P25	CSB	IPU	Chip Select, active low. Used for both serial and parallel data transfers.
M14	M14	M14	A20	RWB	IPU	Read / Write strobe selects the data bus transfer direction. 1 = Read 0 = Write Used for parallel data transfers.
N17	N17	N17	B19	OEB	IPU	Output enable, active low. Enables the output drivers on the data bus during a read cycle. When high, the data bus is placed in a high impedance state. Used for parallel data transfers.
A9	A9	A9	P2	IRQB	OD	Interrupt Request. The common output for all interrupt sources within the device.
Serial Interface						
V9	V9	V9	P24	SCLK	IPU	Serial clock input from a master device.
U11	U11	U11	R26	SDIN	IPU	Serial data input.
T9	T9	T9	P26	SDOUT	OD	Serial data output.

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (12 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
M28352/3/4 Parallel Interface						
H16	H16	H16		ADDR0	IPU	Parallel bus mode: These pins are configured as an eleven (11) bit wide address bus.  Hardware mode: LLOOPn – Local (Source) Loopback. The transmit data is looped back immediately from the encoder to the decoder in place of the received data.  1 = local (source) loopback enabled 0 = local (source) loopback disabled  RLOOPn – Remote (Line) Loopback. The receive data, retimed after clock recovery, is looped back into the AMI generator in place of the transmit data.  1 = remote (line) loopback enabled 0 = remote (line) loopback disabled
H17	H17	H17		ADDR1	IPU	
L18	L18	L18		ADDR2/ RLOOP2	IPU	
K18	K18	K18		ADDR3/ RLOOP3	IPU	
J18	J18	J18		ADDR4/ LLOOP0	IPU	
H18	H18	H18		ADDR5/ LLOOP1	IPU	
G18	G18	G18		ADDR6	IPU	
F18	F18	F18		ADDR7	IPU	
E18	E18	E18		ADDR8/ LLOOP2	IPU	
D18	D18	D18		ADDR9/ LLOOP3	IPU	
C18	C18	C18		ADDR10	IPU	
V17	V17	V17		DATA0/ LB00	IPU/ OD	Parallel bus mode: These pins are configured as an eight(8) bit wide data bus.  Hardware mode: LBO n – enables the line build out function.  1 = line build out enabled 0 = line build out disabled  LBO is generally enabled for transmission line lengths <450 feet and disabled if >450 feet  RLOOPn – Remote (Line) Loopback. The receive data, retimed after clock recovery, is looped back into the AMI generator in place of the transmit data.  1 = remote (line) loopback enabled 0 = remote (line) loopback disabled
V18	V18	V18		DATA1/ LB01	IPU/ OD	
U18	U18	U18		DATA2	IPU/ OD	
T18	T18	T18		DATA3	IPU/ OD	
R18	R18	R18		DATA4/ LB02	IPU/ OD	
P18	P18	P18		DATA5/ LB03	IPU/ OD	
N18	N18	N18		DATA6/ RLOOP0	IPU/ OD	
M18	M18	M18		DATA7/ RLOOP1	IPU/ OD	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (13 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
M28356 Parallel Interface						
			C14	ADDR0/ RLOOP2	IPU	Parallel bus mode: These pins are configured as an eleven (11) bit wide address bus. Hardware mode: LLOOPn – Local (source) Loopback. The transmit data is looped back immediately from the encoder to the decoder in place of the received data. 1 = local (source) loopback enabled 0 = local (source) loopback disabled RLOOPn – Remote (Line) Loopback. The receive data, retimed after clock recovery, is looped back into the AMI generator in place of the transmit data. 1 = remote (line) loopback enabled 0 = remote (line) loopback disabled
			A14	ADDR1/ RLOOP3	IPU	
			C13	ADDR2/ RLOOP4	IPU	
			B13	ADDR3/ RLOOP5	IPU	
			A13	ADDR4/ LLOOP0	IPU	
			A12	ADDR5/ LLOOP1	IPU	
			C12	ADDR6/ LLOOP2	IPU	
			B12	ADDR7/ LLOOP3	IPU	
			A11	ADDR8/ LLOOP4	IPU	
			B11	ADDR9/ LLOOP5	IPU	
			C11	ADDR10	IPU	
			C18	DATA0/ LB00	IPU/ OD	Parallel bus mode: These pins are configured as an eight(8) bit wide data bus. Hardware mode: LBO n – enables the line build out function. 1 = line build out enabled 0 = line build out disabled LBO is generally enabled for transmission line lengths <450 feet and disabled if >450 feet RLOOPn – Remote (Line) Loopback. The receive data, retimed after clock recovery, is looped back into the AMI generator in place of the transmit data. 1 = remote (line) loopback enabled 0 = remote (line) loopback disabled
			A19	DATA1/ LB01	IPU/ OD	
			B18	DATA2/ LB02	IPU/ OD	
			A18	DATA3/ LB03	IPU/ OD	
			C15	DATA4/ LB04	IPU/ OD	
			B15	DATA5/ LB05	IPU/ OD	
			A15	DATA6/ RLOOP0	IPU/ OD	
			B14	DATA7/ RLOOP1	IPU/ OD	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (14 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
JTAG Interface						
V10	V10	V10	N24	TRST	IPD	JTAG reset
U10	U10	U10	N25	TCK	IPU	JTAG clock
V11	V11	V11	N26	TMS	IPU	JTAG mode select
U9	U9	U9	M24	TDI	IPU	JTAG data input
V12	V12	V12	M26	TDO	OD	JTAG data output



**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (15 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
Power and Ground						
C7	C7	C7	Y3	TX_AVDD_0	PA	1.8 volt power pins for each channel transmitter circuitry
B3	B3	B3	AD1	TX_AVDD_1	PA	
	T7	T7	AD5	TX_AVDD_2	PA	
		P5	AD19	TX_AVDD_3	PA	
			AD23	TX_AVDD_4	PA	
			AC24	TX_AVDD_5	PA	
C6	C6	C6	AA3	TX_AVSS_0	GA	Ground pins for each channel transmitter circuitry
A3	A3	A3	AD2	TX_AVSS_1	GA	
	T6	T6	AD6	TX_AVSS_2	GA	
		N5	AD20	TX_AVSS_3	GA	
			AD24	TX_AVSS_4	GA	
			AB24	TX_AVSS_5	GA	
A7	A7	A7	AA2	TX_AVDD3_P3_0	PA	3.3 volt power pins for each channel output line driver
C1	C1	C1	AE2	TX_AVDD3_P3_1	PA	
	U7	U7	AE6	TX_AVDD3_P3_2	PA	
		T1	AE20	TX_AVDD3_P3_3	PA	
			AE24	TX_AVDD3_P3_4	PA	
			AB25	TX_AVDD3_P3_5	PA	

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (16 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
B7	B7	B7	AA1	TX_AVSS3 P3_0	GA	Ground pins for each channel output line buffer
C2	C2	C2	AF2	TX_AVSS3 P3_1	GA	
	V7	V7	AF6	TX_AVSS3 P3_2	GA	
		T2	AF20	TX_AVSS3 P3_3	GA	
			AF24	TX_AVSS3 P3_4	GA	
			AB26	TX_AVSS3 P3_5	GA	
A5, C4	A5, C4	A5, C4	AC1, AC2	RX_AVDD_ 0	PA	1.8 volt power pins for each channel receiver circuitry
E3, F3	E3, F3	E3, F3	AE4, AF4	RX_AVDD_ 1	PA	
	V5, T4	V5, T4	AE8, AF8	RX_AVDD_ 2	PA	
		R3, T3	AE22, AF22	RX_AVDD_ 3	PA	
			AE26, AF26	RX_AVDD_ 4	PA	
			Y25, Y26	RX_AVDD_ 5	PA	
B5, C5	B5, C5	B5, C5	AB3, AC3	RX_AVSS_ 0	GA	Ground pins for each channel receiver circuitry
C3, D3	C3, D3	C3, D3	AD3, AD4	RX_AVSS_ 1	GA	
	T5, U5	T5, U5	AD7, AD8	RX_AVSS_ 2	GA	
		U3, V3	AD21, AD22	RX_AVSS_ 3	GA	
			AD25, AD26	RX_AVSS_ 4	GA	
			Y24, AA24	RX_AVSS_ 5	GA	
E2	E2	E2	AC12, AD12	MON_AVD D	PA	Monitor 1.8 volt power

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (17 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
H5	H5	H5	AE11	MON_AVD D3P3	PA	Monitor 3.3 volt power
E1	E1	E1	AD10, AD11	MON_AVS S	GA	Monitor ground
K2	K2	K2	AF11	MON_AVS S3P3	GA	Monitor ground for the output buffer
L1	L1	L1	AC15	XTAL_AVD D	PA	Crystal 1.8 volt power
L5	L5	L5	AE18	XTAL_AVD D3P3	PA	Crystal 3.3 volt power
K3	K3	K3	AD15	XTAL_AVS S	GA	Crystal ground
K5	K5	K5	AF18	XTAL_AVS S3P3	GA	Crystal ground
M16	M16	M16	C17	CLAD0_AV DD	PA	CLAD 1.8 volt power
L16	L16	L16	C16	CLAD1_AV DD	PA	
K16	K16	K16	B16	CLAD2_AV DD	PA	
L13	L13	L13	B17	CLAD0_AV SS	GA	CLAD ground
K13	K13	K13	A17	CLAD1_AV SS	GA	
J13	J13	J13	A16	CLAD2_AV SS	GA	
G1	G1	G1	AD13, AE13	RBIAS_AV DD	PA	RBIAS 1.8 volt power
H3	H3	H3	AE15	RBIAS_AV DD3P3	PA	RBIAS 3.3 volt power
G3	G3	G3	AE14, AF13	RBIAS_AV SS	GA	RBIAS 1.8 volt ground
J5	J5	J5	AF15	RBIAS_AV SS3P3	GA	RBIAS 3.3 volt ground

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (18 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
E13	E13	E13	G1	JAT0_AVD D	PA	1.8 volt power pins for each channel DJAT circuitry
F14	F14	F14	A1	JAT1_AVD D	PA	
	M13	M13	B8	JAT2_AVD D	PA	
		T13	A22	JAT3_AVD D	PA	
			A26	JAT4_AVD D	PA	
			L26	JAT5_AVD D	PA	
E14	E14	E14	G2	JAT0_AVS S	GA	Ground pins for each channel DJAT circuitry
F13	F13	F13	A2	JAT1_AVS S	GA	
	N13	N13	A8	JAT2_AVS S	GA	
		P13	A21	JAT3_AVS S	GA	
			B26	JAT4_AVS S	GA	
			L25	JAT5_AVS S	GA	
E8 P8 E9 P9 E10 P10 G14 J16 J17 K17 L17 M17	E8 P8 E9 P9 E10 P10 G14 J16 J17 K17 L17 M17	E8 P8 E9 P9 E10 P10 G14 J16 J17 K17 L17 M17	A10 B10 C10 H4 M4 N4 D7 D11 D12 D15 D16 D20 H23 M23 N23	DVDD	PD	+1.8V core power supply

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (19 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
E11	E11	E11	J4	DVSS		Core ground
F11	F11	F11	K4			
N11	N11	N11	L4			
P11	P11	P11	P4			
E12	E12	E12	R4			
F12	F12	F12	D8			
J12	J12	J12	D9			
K12	K12	K12	D10			
N12	N12	N12	D17			
P12	P12	P12	D18			
C13	C13	C13	D19			
H13	H13	H13	J23			
C14	C14	C14	K23			
H14	H14	H14	L23			
J14	J14	J14	P23			
B17	B17	B17	R23			
G11	G11	G11	U1	VDDP	PD	+3.3V IO supply
H11	H11	H11	U2			
J11	J11	J11	U3			
K11	K11	K11	E4			
L11	L11	L11	F4			
M11	M11	M11	G4			
G12	G12	G12	T4			
H12	H12	H12	U4			
L12	L12	L12	D5			
M12	M12	M12	D6			
G13	G13	G13	D13			
K14	K14	K14	D14			
L14	L14	L14	D21			
E16	E16	E16	D22			
F16	F16	F16	E23			
G16	G16	G16	F23			
			G23			
			T23			
			U23			
			U24			
			U25			
			U26			

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (20 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
A1, B1	A1, B1	A1, B1	A9, B1	VSS0	GD	IO ground
U1, V1	U1, V1	U1, V1	C1, K1			
P2, M3	P2, M3	P2, M3	L1, T1			
N3, P3	N3, P3	N3, P3	V1, W1			
E5, F5	E5, F5	E5, F5	B2, V2			
M5, E6	M5, E6	M5, E6	W2, A3			
F6, G6	F6, G6	F6, G6	B3, C3			
H6, J6	H6, J6	H6, J6	G3, V3			
K6, L6	K6, L6	K6, L6	W3, B4			
M6, N6	M6, N6	M6, N6	C4, D4			
P6, E7	P6, E7	P6, E7	W4, Y4			
F7, G7	F7, G7	F7, G7	AA4, AB4			
H7, J7	H7, J7	H7, J7	AC4, AC5			
K7, L7	K7, L7	K7, L7	AC6, AC7			
M7, N7	M7, N7	M7, N7	AC8, AC9			
P7, F8	P7, F8	P7, F8	AC10, AC11			
G8, H8	G8, H8	G8, H8	B9, C9			
J8, K8	J8, K8	J8, K8	J9, K9			
L8, M8	L8, M8	L8, M8	L9, M9			
N8, F9	N8, F9	N8, F9	N9, P9			
G9, H9	G9, H9	G9, H9	R9, T9			
J9, K9	J9, K9	J9, K9	U9, V9			
L9, M9	L9, M9	L9, M9	J10, K10			
N9, F10	N9, F10	N9, F10	L10, M10			
G10, H10	G10, H10	G10, H10	N10, P10			
J10, K10	J10, K10	J10, K10	R10, T10			
L10, M10	L10, M10	L10, M10	U10, V10			
N10	N10	N10	J11, K11			

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (21 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
			L11, M11 N11, P11 R11, T11 U11, V11 J12, K12 L12, M12 N12, P12 R12, T12 U12, V12 J13, K13 L13, M13 N13, P13 R13, T13 U13, V13 J14, K14 L14, M14 N14, P14 R14, T14 U14, V14 J15, K15 L15, M15 N15, P15 R15, T15	VSSO cont.	GD	IO ground

**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (22 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
			U15, V15 J16, K16 L16, M16 N16, P16 R16, T16 U16, V16 A25, B25 C25, V25 W25, C26 G26, H26 T26, V26 W26, V4 C8, AD9 AE9, B20 J17, K17 L17, M17 N17, P17 R17, T17 U17, V17 J18, K18 L18, M18 N18, P18 R18, T18 U18, V18 AC18, AD18 AC19, AC20 AC21, AC22 D23, V23 W23, Y23 AA23, AB23 AC23, L24 V24, W24	VSSO cont.	GD	IO ground



**Table 1-10. M28352/M28353/M28354/M28356 - Pin Descriptions (23 of 23)**

Pin #				Name	Type	Description
M28352	M28353	M28354	M28356			
No Connects						
T11, M13 N13, P13 T13, U13 V13, P14 T14, U14 V14, T15 U15, V15 N16, P16 R16, T16 U16, V16 P17, R17 T17, U17	T11, P13 T13, U13 V13, T14 U14, V14 T15, U15 V15, V16			NC	NC	No connect
Reserved						
A10, A11, A12, B9, B10, C8, C12 R1, R2 U2, V2 U4, V4 U6, V6 U12	A10, A11, A12, B9, B10, C8, C12 R1, R2 U2, V2 U12	A10, A11, A12, B9, B10, C8, C12 U12	M1, M2, M3, N1, N2, N3, P1, M25	TEST	DNC	Factory test – <b>Do Not Connect</b>
Analog Power and Grounds						
R3, T3 T4, P5 V5, T7	R3, T3 P5				PA	1.8 volt analog power
T1, U7	T1				PA	3.3 volt analog power
U3, V3 N5, T5 U5, T6	U3, V3 N5				GA	1.8 volt analog grounds
T2, V7	T2				GA	3.3 volt analog grounds



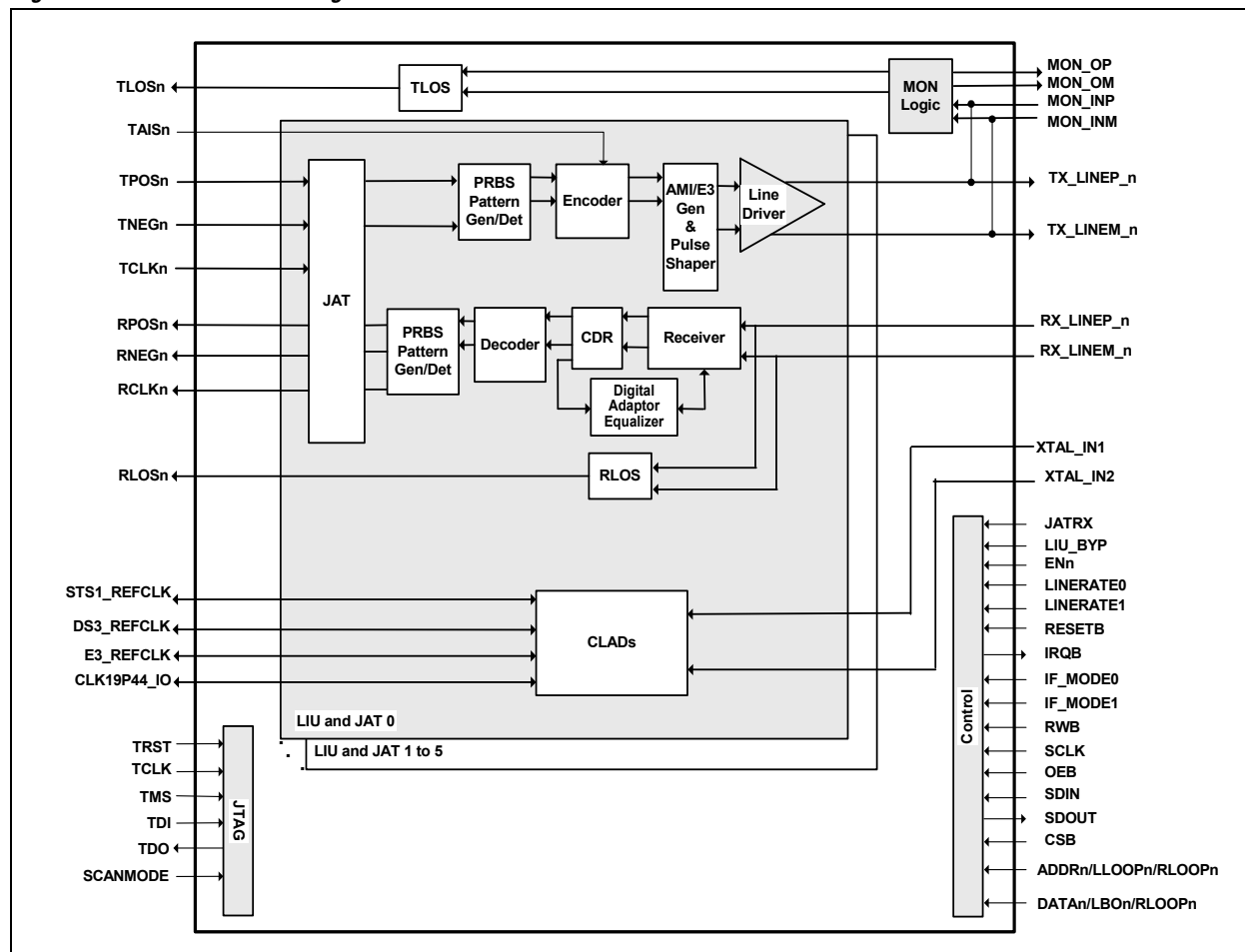


## 2.0 Functional Description

### 2.1 Overview

The M2835x is a family of fully integrated line interface units (LIUs) and desynchronizer/jitter attenuators (DJAT) for DS3, E3 and STS-1 applications. It is designed to connect to the line through pulse transformers or via series capacitors and baluns. A novel feature of the device is that the extracted receive clock or a gapped SONET STS-1 clock or SDH STM0 clock is dejittered without external VCO, and may then be used as a transmit clock. Figure 2-1 illustrates a block diagram of the M2835x.

Figure 2-1. M2835x Block Diagram



The description of the following features is for a single LIU. However, all features are the same for all the channels available in the device.

- ◆ Programmable jitter attenuator (DJATs) for each channel
- ◆ Automatic adaptive equalizer up to 1,800 feet for AT&T 734/728 75 ohm type cables
- ◆ Two PRBS pattern generators/detectors per channel
- ◆ ITU-T G.772 compliant monitoring circuit that monitors transmit signal performance
- ◆ ITU-T G.775 compliant RLOS receive loss of signal indicator
- ◆ TLOS transmit loss of signal indication
- ◆ DC continuity check that monitors the DC path between RLINE\_M and RLINE\_P terminations (one channel at a time) in order to isolate line-side faults
- ◆ Transmitter pulse shaper
- ◆ Receive clock recovery
- ◆ AMI, B3ZS and HDB3 data encoding and decoding
- ◆ Parallel or serial microprocessor interface compatible with Motorola SPI
- ◆ Clock offset indicates the quality of the recovered receive and transmit clocks
- ◆ Clock rate adaptors (CLADs) that provide DS3, E3 and STS-1 clocks simultaneously from a single 19.44 MHz crystal or external clock input
- ◆ Analog loopback from Receiver to Transmitter without retiming
- ◆ Line and source loopback capabilities
- ◆ Programmable FIFO depth optimal for SONET/SDH applications
- ◆ Programmable clocking of both input and output data on either the rising or falling edge
- ◆ Bit error counter per channel
- ◆ TAIS alarm indication signal
- ◆ Three configuration and control options:
  - Hardware control
  - Serial control interface
  - Parallel control interface
- ◆ One-second timer for event latching.
- ◆ Uses 3.3 V and 1.8 V power supplies
- ◆ Interrupts supporting:
  - FIFO underflow
  - FIFO overflow
  - DJAT frequency detection (signals when DJAT is close to underflow or overflow)
  - Out-of-lock detection
- ◆ 24-bit receive counters for LCV, EXZ, and BPV
- ◆ Power-down control for each channel
- ◆ Ability to independently reset each DJAT channel
- ◆ Asynchronous global reset
- ◆ Ability to independently bypass the DJAT for each channel
- ◆ JTAG (*IEEE 1149.1*) test interface

## 2.2 Clock Rate Adaptor – CLAD

### 2.2.1 Overview

The M2835x device contains three (3) Clock Rate Adaptors (CLADs) to synthesize clocks for the three supported line rates of DS3, E3 and STS-1 from one common external timing reference. The device also contains internal crystal oscillator circuitry that generates the 19.44 MHz clock used by the CLADs. The oscillator circuitry is fed from an external 19.44 MHz (+/- 10 ppm) crystal via the XTAL\_IN1 and XTAL\_IN2 pins. In addition, the oscillator circuitry may be bypassed by setting the XTAL\_BYP pin to "1". This allows an external 19.44 MHz (+/- 20 ppm) clock source to directly feed the CLADs via the CLK19P44\_IO pin. No additional clocks are needed to operate the device. The three CLADs may be bypassed by setting the CLAD\_BYP pin to "1". This allows the M2835x to use external DS3, E3, and/or STS-1 line rate reference clocks supplied via the DS3\_REFCLK, E3\_REFCLK, and STS1\_REFCLK pins for the three supported line rates. The external line rate reference clocks must also have an accuracy of +/- 20 ppm..

**NOTE:**

1. Operation of the device requires that the STS-1 line rate clock always be generated internally by the CLAD or supplied externally to the STS1\_REFCLK pin. A slower rate reference clock (e.g., DS3 reference clock) may be used to meet the requirement of always supplying a clock to the STS1\_REFCLK pin if the STS-1 line rate mode is not used.
2. Device operation requires that an external clock be supplied to the CLK19P44\_IO pin for the device to operate properly when the CLADs are bypassed (CLAD\_BYP) and the internal crystal oscillator circuitry is bypassed (XTAL\_BYP pin = 1). The maximum allowable rate of this clock is 26 MHz. To meet this requirement, a line rate reference clock (STS\_REFCLK, DS3\_REFCLK, or E3\_REFCLK) may be divided down by two and used to drive the CLK19P44\_IO pin. The operation of the device in this configuration (e.g., a 22.368 MHz clock driving the CLK19P44\_IO pin) will not violate any standards or adversely affect the operation of the device; however, it will cause the timing in the transmit monitoring circuitry to be inaccurate.
3. Do not connect external reference clocks to the DS3\_REFCLK, E3\_REFCLK, or STS1\_REFCLK pins when they are configured as outputs (i.e. CLAD\_BYP pin = 0).
4. When the crystal oscillator circuitry is bypassed, a 19.44 MHz crystal may remain connected to the XTAL\_IN1 and XTAL\_IN2 pins; otherwise, the pins must remain unconnected.
5. Do not connect higher speed reference clocks to slower line rate reference clock input pins. For example, do not connect a 51.84 MHz STS- reference clock to the DS3\_REFCLK or E3\_REFCLK pins. However, a slower clock may be connected to a high line rate reference clock pin if the line mode supported by that higher rate clock is not used. For example, a 44.736 MHz DS3 reference clock may be connected to the STS1\_REFCLK pin if the STS-1 line mode is not used.

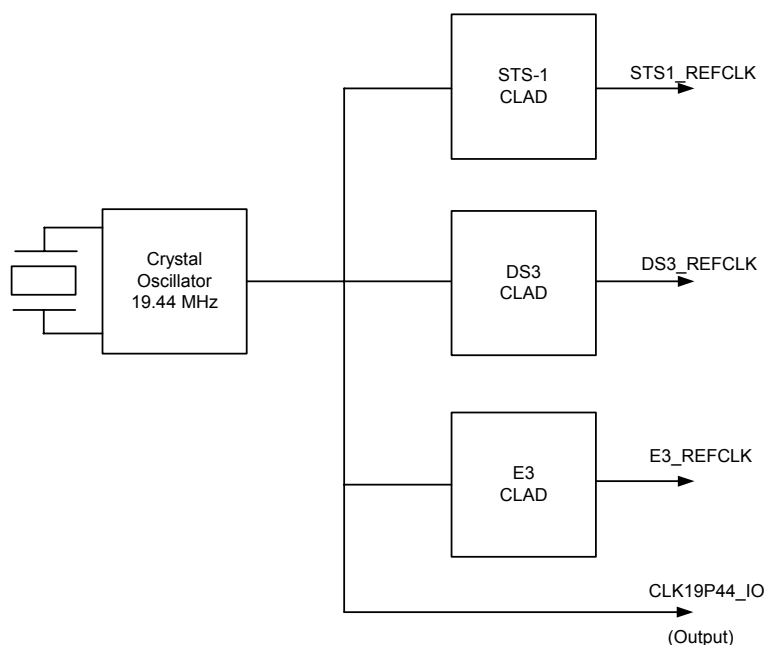
## 2.2.2 Crystal Oscillator Circuitry Enabled

### 2.2.2.1 Crystal Oscillator Circuitry Not Bypassed and the CLADs Enabled

When the M2835x crystal oscillator circuitry is enabled (not bypassed), each enabled (not bypassed) CLAD uses the internally generated 19.44 MHz clock to synthesize its line rate clock. The oscillator circuitry also supplies the 19.44 MHz clock to the CLK19P44\_IO pin which acts as an output when the circuitry is enabled.

Figure 2-2 below, illustrates the oscillator circuitry when it is “not bypassed” and all three CLADs are enabled (i.e., CLAD\_BYP pin = “0”). Each CLAD generates its respective line rate clock for use by the device and each CLAD drives its reference clock pin (i.e., the DS3\_REFCLK, E3\_REFCLK, and STS1\_REFCLK). In this configuration, each CLAD can be independantly powered down by setting its PDB\_CLAD bit to “0” in register CLADSTS1 control, CLADDS3 control, or CLADE3 control. When powered down, the reference line clock pins remain outputs.

**Figure 2-2. Crystal Circuitry “Not Bypassed” and CLAD Enabled**

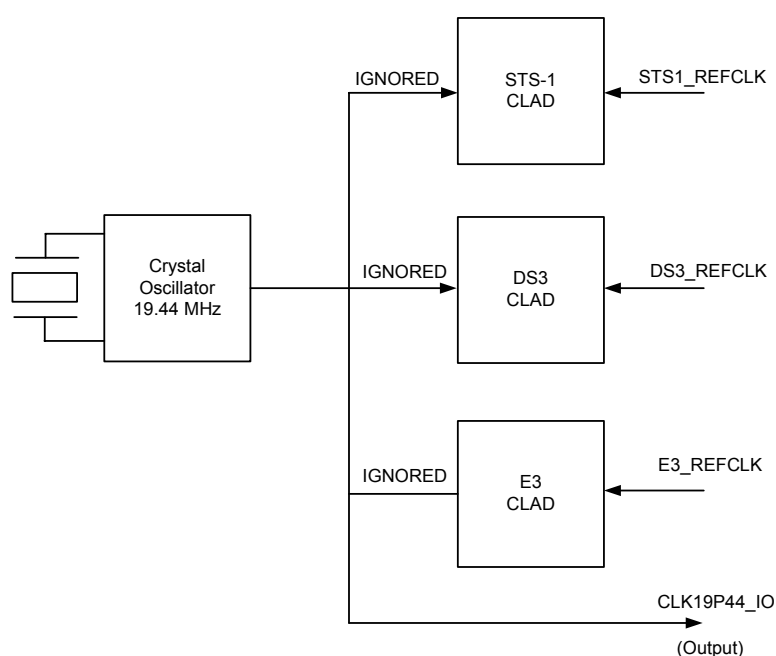


### 2.2.2.2 Crystal Oscillator Circuitry Not Bypassed and the CLADs Disabled

When the three CLADs are disabled (i.e. CLAD\_BYP pin = “1”), they ignore the 19.44 MHz clock supplied by the M2835x crystal oscillator circuitry. Each CLAD then requires an external line rate reference clock if the related line rate is required for operation. The required reference clocks must drive their respective input pin (the DS3\_REFCLK, E3\_REFCLK, and/or STS1\_REFCLK). While the internal crystal oscillator circuitry is still enabled, it continues to supply a 19.44 MHz clock at the output of the CLK19P44\_IO pin even when the CLADs are disabled.

Figure 2-3 below, illustrates the oscillator circuitry when it is “not bypassed” and the CLADs are disabled.

**Figure 2-3. Crystal Circuitry “Not Bypassed” and CLAD Disabled**



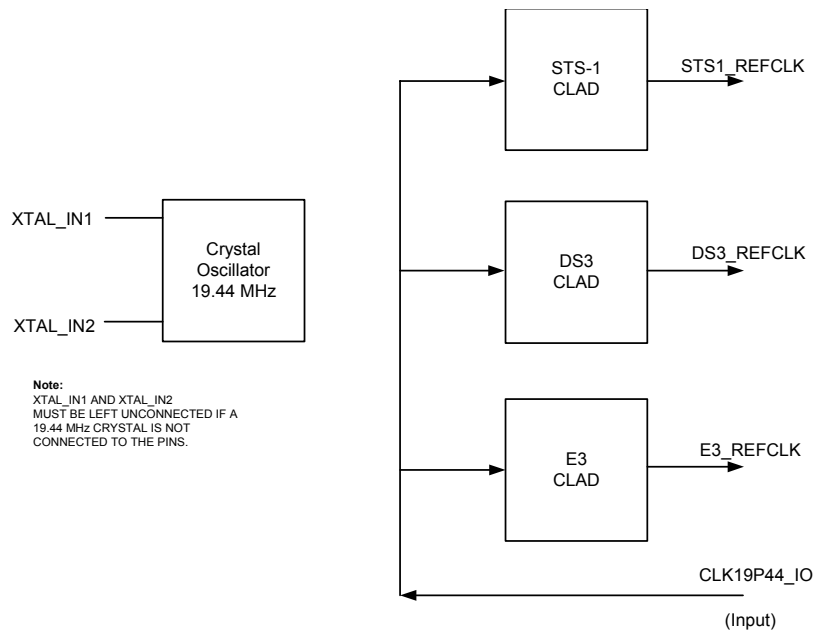
## 2.2.3 Crystal Oscillator Circuitry Disabled

### 2.2.3.1 Crystal Oscillator Circuitry Bypassed and the CLADs Enabled

When the M2835x crystal oscillator circuitry is bypassed (XTAL\_BYP pin = “1”) and the CLADs are enabled (i.e. CLAD\_BYP pin = “0”), the device requires that an external 19.44 MHz (+/- 20 ppm) clock source drive the CLK19P44\_IO pin. (The CLK19P44\_IO pin becomes an input pin when the oscillator circuitry is disabled.) When bypassed, the oscillator circuitry is powered down and a 19.44 MHz crystal may remain connected to the XTAL\_IN1 and XTAL\_IN2 pins. If the 19.44 MHz crystal is not connected to the XTAL\_IN1 and XTAL\_IN2 pins, then the pins must be left unconnected.

Figure 2-4 below, illustrates the bypassed crystal oscillator circuitry with all three CLADs enabled.

**Figure 2-4. Crystal Circuitry “Bypassed” and CLAD Enabled**



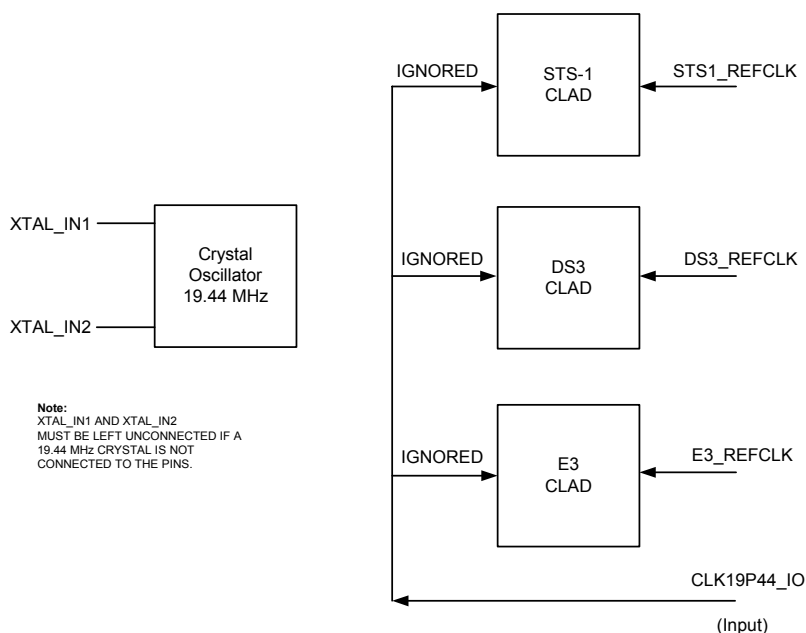


### 2.2.3.2 Crystal Oscillator Circuitry Bypassed and the CLADs Disabled

When the crystal oscillator is bypassed (XTAL\_BYP pin = “1”) and the CLADs are disabled (i.e. CLAD\_BYP pin = “1”), the M2835x requires that external line rate reference clocks drive the corresponding reference clock input pin of the supported line rates (i.e., the DS3\_REFCLK, E3\_REFCLK, and STS1\_REFCLK). The XTAL\_IN1 and XTAL\_IN2 pins must remain unconnected unless a 19.44 MHz (+/- 20 ppm) crystal is attached to the pins.

Figure 2-5 below, illustrates the bypassed crystal oscillator with the CLADs disabled.

**Figure 2-5. Crystal Circuitry “Bypassed” and CLAD Disabled**



## 2.3 Line Interface Unit – LIU

### 2.3.1 Overview

M2835x incorporates E3/DS3/STS-1 Line Interface Unit (LIU) per channel. It is the physical layer interface between the data framer (or other terminal-side equipment) and the electrical cable used for data transmission.

The M2835x LIU consists of independent data transceivers for each channel that can operate over type 734/728 coaxial cable at the rates of 34.368 Mbps (E3), 44.736 Mbps (DS3), and 51.84 Mbps (STS-1).

The transmit side takes an NRZ or encoded dual rail input and encodes the signal into AMI B3ZS for DS3/STS-1 or HDB3 for E3 analog waveforms to be transmitted over the coaxial cable. The receiver side takes in the attenuated and distorted analog receive signal and equalizes, slices, and resynchronizes the signal before decoding it to the NRZ output or sending out a non-decoded dual rail.

The architecture of the M2835x includes the following internal functions for each channel:

**Transmitter:**

- AMI B3ZS/HDB3 encoder
- Pulse shaper
- Line driver
- Alarm Indication Signal (AIS) insertion
- Transmit monitor

**Receiver:**

- Automatic Gain Control (AGC)
- Receive equalizer
- Clock Recovery circuit
- Loss Of Signal (LOS) detector
- B3ZS/HDB3 decoder with bipolar violation detector
- Data squelching
- Clock offset indicator

**Additional Functions:**

- Bias generator
- Power-on reset
- Loopback MUXes

In addition, each channel has the ability to perform line and source loopbacks. Each port can be controlled and configured by the software interface mode through a parallel or serial port or by hardware interface mode through dedicated pins.

The M2835x is used as a data transceiver over a type 734/728 coaxial cable that is up to 1800 feet long (for Type 735 up to 675 feet) in an on-premise environment within any public or private networks that use these data rates.

## 2.3.2 Transmitter

### 2.3.2.1

#### AMI/B3ZS/HDB3 Encoder

The encoder mode is configured by the `enencdec` (enable encoder/decoder) and `E3` mode control bits.

When `TXENC_EN`, bit 0 in register `TXENDEC_CTRL` at address offset `0xn55`, is set, the encoder is enabled. In this configuration, the incoming signal is treated as non-encoded NRZ data on TPOS alone, and `TNEG` is ignored as a no connect. The data is encoded into a representation of a three-level B3ZS (`LINERATE[1:0] = 0X`) or HDB3 signal (E3 mode – `LINERATE[1:0] = 1X`), conforming to the coding rules in [Section 2.7](#) and passed on to the pulse AMI generator or to the pulse E3 generator in the form of two binary signals representing the positive and negative three-level pulses.

When TXENC\_EN, bit 0 in register TXENDEC\_CTRL at address offset 0xn55, is cleared, the encoder is disabled. The encoder then treats the incoming signal as encoded data over TPOS and TNEG, and simply passes it on to the AMI generator or to the E3 generator, with the exception that if TPOS and TNEG are simultaneously high, the AMI pulse state changes.

Data latency is constant between all modes of operation and is 4 symbol periods for E3 and is 3 symbol periods for DS3/STS-1 after the data is latched in. The transmit digital data is clocked via a rising TCLK edge, and is expected to be running at the proper symbol rate. There is a small delay added to the data, to provide a small amount of negative data hold time. AIS overrides transmit data and replaces it with all 1's for E3 and framed AIS for DS3.

### 2.3.2.2 Pulse Shaper

#### Line Build Out – LBO

The LBO, line build out, is controlled with bit0 in the TX\_AMI register at address offset 0xn03. LBO is meant to be asserted for short cables (<450') in order to simulate a waveform that has been reduced in amplitude (and distorted) by the cable.

In the hardware mode, this feature is controlled via the LBO pins

### 2.3.2.3 Line Driver

The differential line driver takes the shaped differential waveform from the E3/AMI generators, amplifies the waveform to the proper level, and drives the transmit transformer. The inductor represents a low impedance load. The coaxial cable itself (with a proper termination) represents 75ohms load. Using a transformer turns ratio of 1:1 and two external discrete back matching resistors of 37.5ohms each aids in line matching and output return loss.

However, the series termination resistors cause a 6dB loss at the coaxial line. The driver provides a variable gain to overcome the 6dB loss and the low AMI amplitude output. The limited bandwidth of the line driver creates a low pass filter, providing additional waveform shaping.

The output common mode voltage (at TLINEP, TLINEM) is centered between ground and the 3.3V supply, to maximize the output voltage dynamic range.

In addition to affecting the AMI timing, the status of the LBO control bit coupled with 4 bits gain control of the line driver affects the pulse amplitude sent out of the line driver.

A de-emphasis of the signal is implemented through a 4-bit control signal. These controls smooth the shape of the generated waveform and introduces an exponential decay in the up/down slopes.

The TX\_LD register at address offset 0xn04, contains the bits necessary to control the line driver de-emphasis and gain as shown in [Table 2-1](#) Line Driver Capacitance Control and 2-x.

## Line Driver Capacitance Control

**Table 2-1. Line Driver Capacitance Control**

LD_FILTER[3:0]	Capacitance + constant cap=200f
0000	0
0001	100f
0010	200f
0011	300f
0100	400f
0101	500f
0110	600f
0111	700f
1000	800f
1001	900f
1010	1.0p
1011	1.1p
1100	1.2p
1101	1.3p
1110	1.4p
1111	1.5p

## Line Driver Gain Control

**Table 2-2. Line Driver Gain Control (1 of 2)**

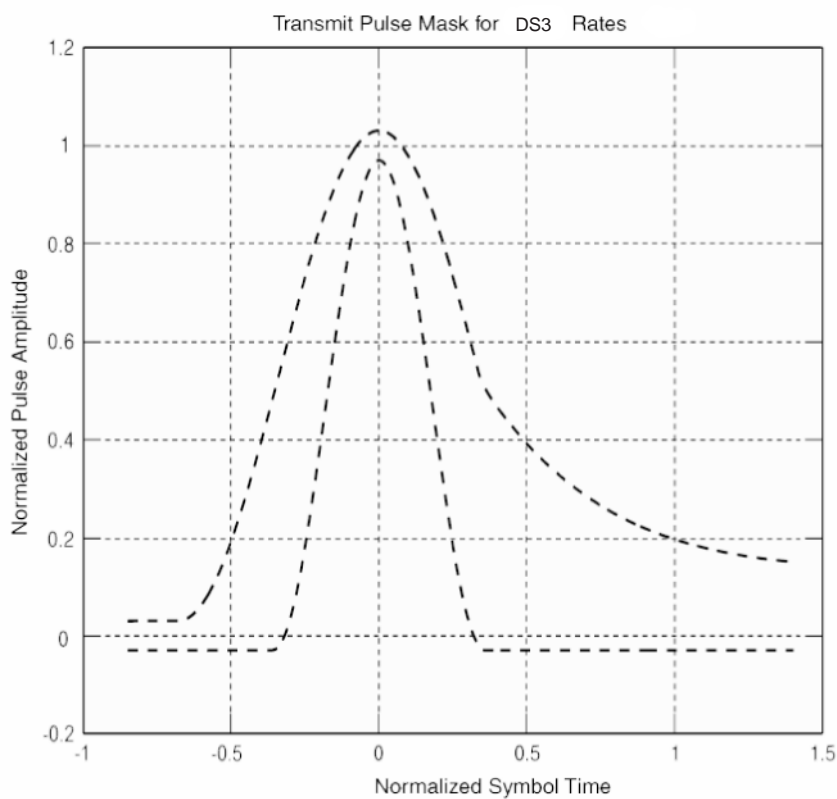
LD_GAIN[3:0]	Gain (lin)	Gain(dB)
0000	1.4	2.922
0001	1.5	3.521
0010	1.6	4.082
0011	1.7	4.608
0100	1.8	5.105
0101	1.9	5.575
0110	2.0	6.020
0111	2.1	6.444
1000	2.2	6.848

**Table 2-2. Line Driver Gain Control (2 of 2)**

1001	2.3	7.234
1010	2.4	7.604
1011	2.5	7.958
1100	2.6	8.299
1101	2.7	8.627
1110	2.8	8.943
1111	2.9	9.247

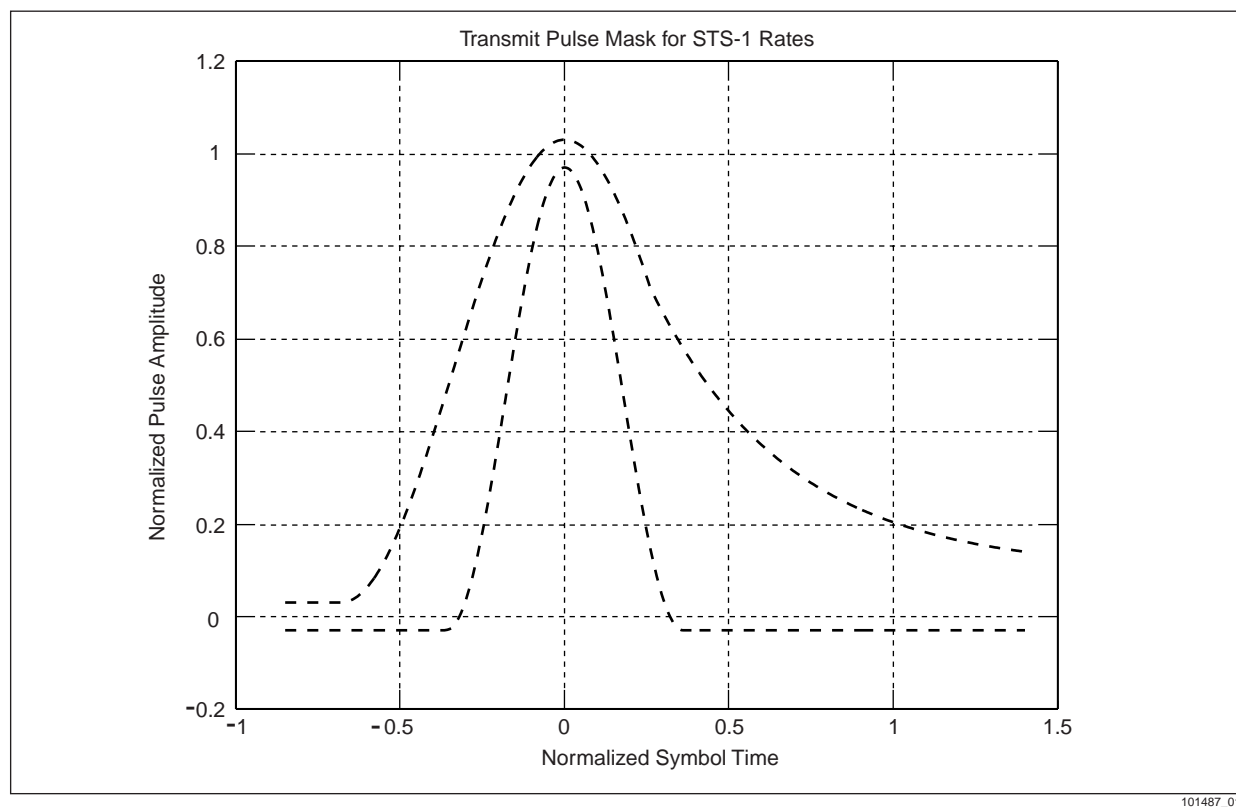
**Transmit Pulse Mask Templates**

The following figures and tables define the bounds for the transmit pulse masks for DS3, STS-1, and E3 rates respectively.

**Figure 2-6. Transmit Pulse Mask for DS3 Rates**

**Table 2-3. DS3 Transmit Template Specifications**

Time Axis Range (UI)	Normalized Amplitude Equation
<b>Upper Curve</b>	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.34)]\}$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 e^{-1.84(T - 0.36)}$
<b>Lower Curve</b>	
$-0.85 \leq T \leq -0.36$	-0.03
$-0.36 \leq T \leq 0.36$	$-0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.18)]\}$
$0.36 \leq T \leq 1.4$	-0.03

**Figure 2-7. Transmit Pulse Mask for STS-1 Rates**

101487\_013

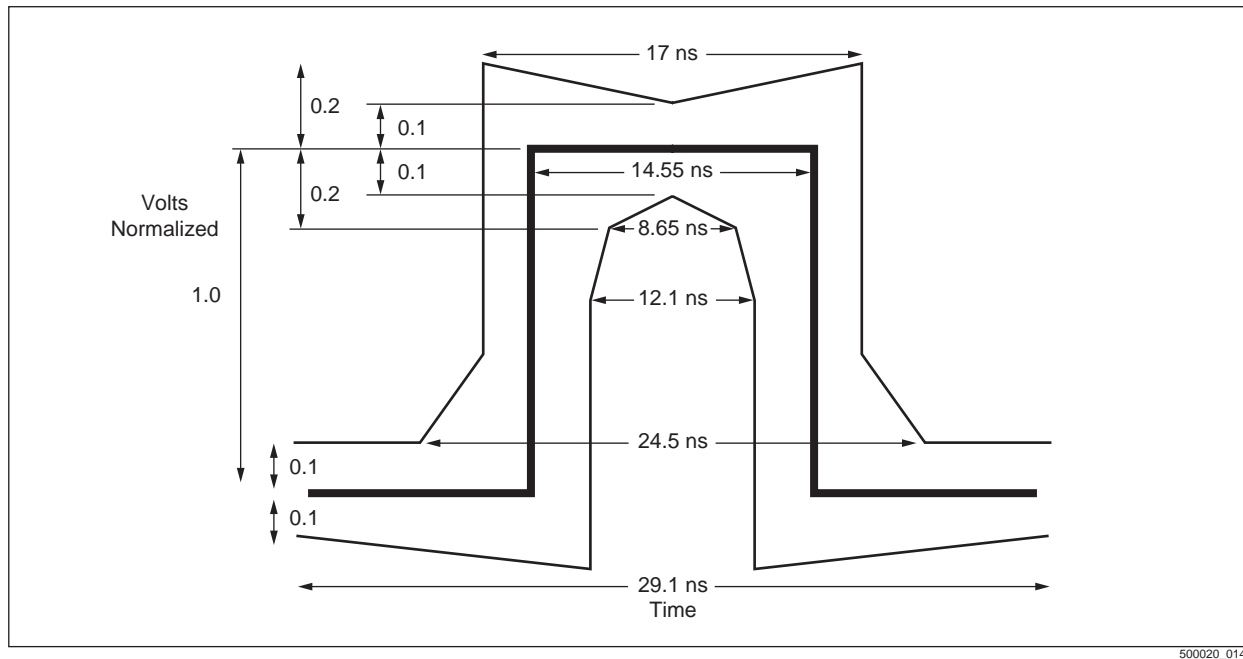
**Table 2-4. STS-1 Transmit Template Specifications**

Time Axis Range (T)	Normalized Amplitude Equation
<b>Upper Curve</b>	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.34)]\}$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 e^{-2.4(T - 0.26)}$

**Table 2-4. STS-1 Transmit Template Specifications**

Time Axis Range (T)	Normalized Amplitude Equation
<b>Lower Curve</b>	
$-0.85 \leq T \leq -0.38$	-0.03
$-0.38 \leq T \leq 0.36$	$-0.03 + 0.5 \{1 + \sin [(\pi / 2)(1 + T / 0.18)]\}$
$0.36 \leq T \leq 1.4$	-0.03

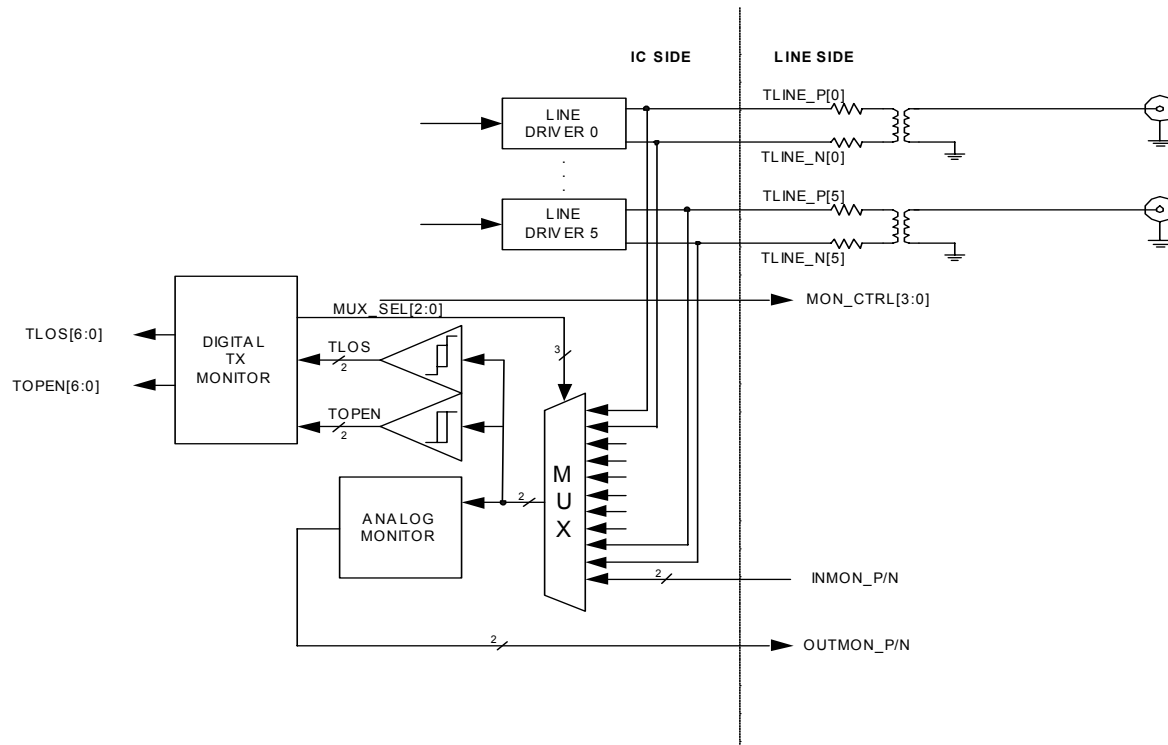
**Figure 2-8. Transmit Pulse Mask for E3 Rate**



#### 2.3.2.4 Transmit Monitor

## Overview

The transmit monitor block monitors six transmission lines for Loss of Signal (LOS) defect and Open defect by cycling through each line at 1 ms intervals. The monitor block generates six Loss of Signal and Open interrupts reflecting the status of each of the six transmission lines. A mode is also available for an additional external transmit line input that may be monitored continuously.

**Figure 2-9. Internal Transmit Monitor**

### Loss of Signal – TLOS

The Loss of Signal alarm is asserted when no transitions are observed on transmit data for at least 32 consecutive clock cycles. TLOS is de-asserted as soon as a transition on transmit data is observed. To ensure the monitor functions even when the transmit clock is lost, the counters are clocked by the 19.44MHz crystal clock.

To enable the transmit loss of signal function, TLOS\_EN is set, bit 5 in the TLOS\_CONTROL register at address 0x00F. As can be deduced from Figure 2-9. Internal Transmit Monitor, each of the six transmit channels are sampled for LOS. The control of the selection process is accomplished with TLOS\_CTRL[3:0], bits 3:0 also in the TLOS\_CONTROL register. By default the six channels are sampled every  $2^{13}$  clock cycles or approximately 420  $\mu$ s.

Monitoring one channel continuously can be selected by TLOS\_CTRL[3:0] to the channel number, 0x0 – 0x5.

Each of the seven TLOS[6:0] and TOPEN[6:0] alarms are latched independently and only when the corresponding channel is selected to be monitored by the detectors. If a channel is not selected, the TLOS<sub>n</sub> / TOPEN<sub>n</sub> alarms for that channel will hold the current value. When the internal MUX output changes, a hold-off counter is enabled preventing TLOS<sub>n</sub> / TOPEN<sub>n</sub> values from being updated until the counter expires. This ensures the TLOS<sub>n</sub> / TOPEN<sub>n</sub> detection circuit has enough time to determine the correct state of the transmit line. This is to prevent false TLOS<sub>n</sub> / TOPEN<sub>n</sub> toggling.

The TLOS / TOPEN function can be disabled by setting TLOS\_EN low, bit 5 in the TLOS\_CONTROL register at address offset 0x00F. When disabled, all TLOS<sub>n</sub> /



TOPENn alarms are set to 0. After reset, all the TLOS<sub>n</sub> / TOPEN<sub>n</sub> alarms default to high or the TLOS/TOPEN detector acquired value.

### Transmit Line Open – TOPEN

The Loss of Signal alarm is asserted when no transitions are observed on transmit data for at least 32 consecutive clock cycles. TOPEN is de-asserted as soon as a transition on transmit data is observed. To ensure the monitor functions even when the transmit clock is lost, the counters are clocked by the 19.44MHz crystal clock.

### External Monitoring

There is a special mode where an external transmission signal may be monitored via the MON\_INP and MON\_INM pads. To monitor, TLOS\_CTRL[3:0] is written 0xC.

“External” on page 5-2 illustrates a possible scenario for using this external monitor feature.

When bit MON\_EXT in register TXMON\_ANACTRL1 is set, the transmit line being monitored is routed externally via pads MON\_INP and MON\_INM using relays that are controlled by output pins MON\_CTRL[2:0]. TLOS\_CTRL[3:0] in the TLOS\_CONTROL register is used to set the state of pads MON\_CTRL[2:0].

MON\_CTRL[2:0] cycle through the states 0x0 to 0x5 then rolling over to 0x0. This can then be decoded to switch in a transmit line pair, via relays or a MUX, to the MON\_INP/M pads.

When the MON\_CTRL[2:0] outputs change state, a hold-off counter is enabled. This prevents the latched values from being updated until the counter expires. This ensures enough time for the relays contacts to debounce and the TLOS/TOPEN detect circuit to determine the correct state of the transmit line and prevent false toggling.

**NOTE:** It is not possible to choose one channel for external monitoring.

**NOTE:** When using this feature with the M28352/3/4 devices, the MON\_CTRL[2:0] also cycle through the states 0x0 to 0x5 rolling over to 0x0 as with the six (6) channel device. For proper use with the 2, 3, or 4 channel devices, decode according to the following schedule.

**Table 2-5. External Decoding**

Port	Decode
0	0x0
1	0x1
2	0x4
3	0x5

When bit MON\_EXT is cleared, output pins MON\_CTRL[2:0] are driven low.

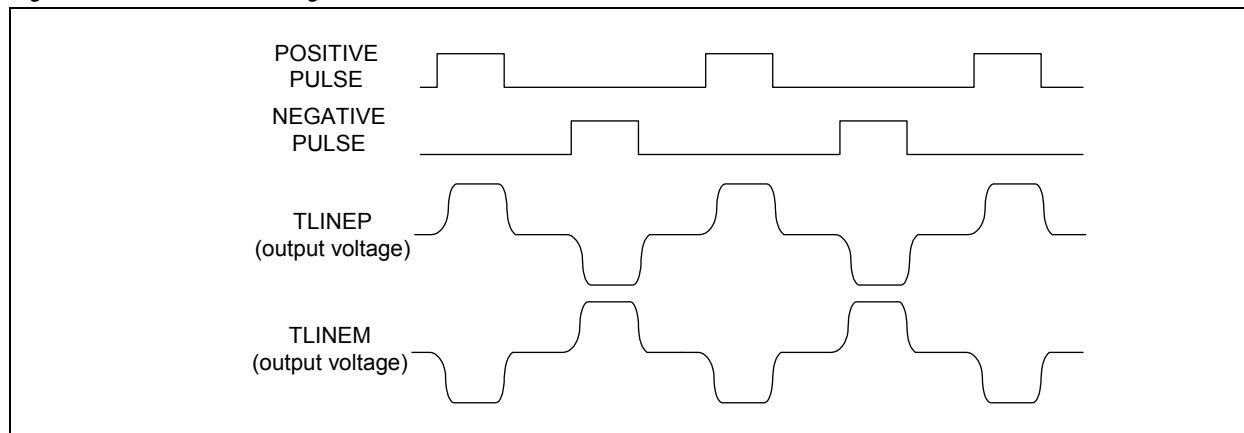
### 2.3.2.5 Alarm Indication Signal Generator – AIS

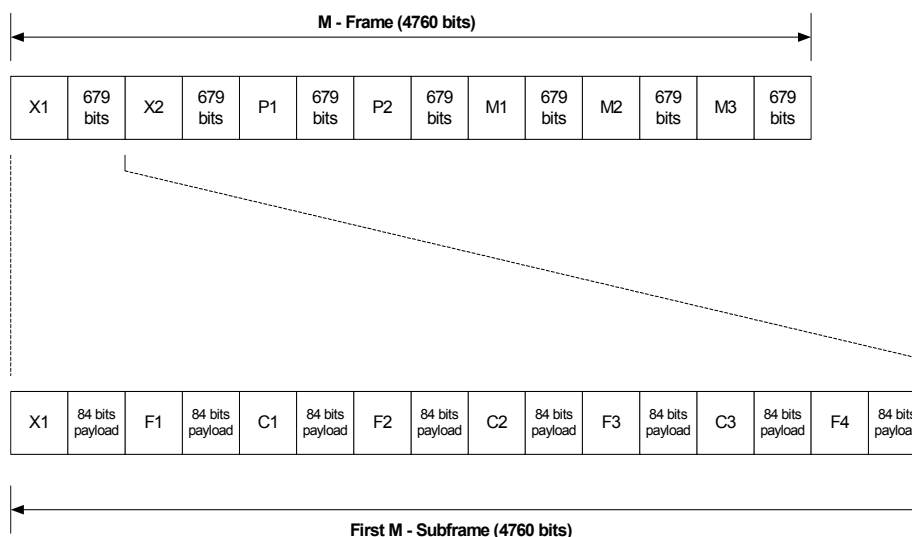
When TAIS is asserted, an AIS replaces the transmit data at TPOS<sub>n</sub> and TNEG<sub>n</sub>. In the E3 or STS-1 modes, an AIS signal of all 1s is transmitted. In three-level signal form, this is a continuously alternating positive and negative pulse stream, as if the transmit data were a continuous string of logical 1s. [Figure 2-8](#) illustrates the AIS signal. The TAIS pin has the same data latency as the TX data pins and can be used to replace single symbols within a data stream. When the encoder is disabled (TXENC\_EN, bit 0 in register TXENDEC\_CTRL at address offset 0xn55, is set), the TAIS mode maintains the proper phase, based on the polarity of the last 1 received.

In DS3 mode, the device will transmit a framed AIS. The frame will have a valid M-frame alignment channel, M-subframe alignment channel, and valid P channel bits. The payload bits follow a 1010...1010 sequence. As shown in [Figure 2-11 DS3 Framed AIS](#), starting with one after each M-frame alignment bit, M-subframe alignment bit, X-bit, P-bit and C-bit channel. The C-bits [2] are set to zero (C1 = 0, C2 = 0, C3 = 0). The X-bits are also set to one (X1 = 1, X2 = 1).

The device will continuously send the AIS signal until the TAIS pin input goes low. The AIS signal follows the same path as the TX data during line or source loopback.

**Figure 2-10. E3/STS-1 AIS Signal**



**Figure 2-11. DS3 Framed AIS**

Overhead bit sequence for entire M - Frame

X1	F1	C1	F2	C2	F3	C3	F4
X2	F1	C1	F2	C2	F3	C3	F4
P1	F1	C1	F2	C2	F3	C3	F4
P2	F1	C1	F2	C2	F3	C3	F4
M1	F1	C1	F2	C2	F3	C3	F4
M2	F1	C1	F2	C2	F3	C3	F4
M3	F1	C1	F2	C2	F3	C3	F4

For a DS3 AIS frame the following bit positions are set:

M-Frame alignment: M1 = 0, M2 = 1, M3 = 0.  
M-Subframe alignment: F1 = 1, F2 = 0, F3 = 0, F4 = 1.  
Remote alarm indicator: X1 = 1, X2 = 1.  
Bit stuffing control: C1 = 0, C2 = 0, C3 = 0.  
84 payload bits: 1010 ..... 1010  
M-Frame parity: P1 = 1, P2 = 1.

## 2.3.3 Receiver

### 2.3.3.1 Overview

The receiver recovers data from the coaxial cable that is attenuated due to the frequency-dependent characteristics of the cable. In addition, the receiver compensates for the flat loss (across all frequencies) in the various electrical components and the variation in transmitted signal power.

The M2835x can recover data that has been attenuated by a maximum of 1800 feet of coax, having characteristics and attenuation consistent with *ANSI T1.102-1993*, Annex C, Figure C.2. This approximates the characteristics of AT&T type 734/728 cable; almost the same attenuation characteristic is achieved by a 900 foot length of AT&T type 735 cable.

### 2.3.3.2 AGC/VGA Block

The Variable Gain Amplifier (VGA) receives the AMI input signal from the coaxial cable. The VGA supplies flat gain (independent of frequency) to make up for various flat losses in the transmission channel and for loss at one-half the symbol rate that cannot be made up

by the equalizer. The VGA gain is controlled by a feedback loop which senses the amplitude of the equalizer output, acts as an amplitude servo for optimal slicing.

### 2.3.3.3 Receive Equalizer

The receive equalizer receives the differential signal from a variable gain amplifier (VGA) and acts to boost the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) to the point that correct decisions can be made by the slicer with a minimum of jitter in the recovered data.

The ISI is caused by the inherent frequency distortion (high frequency loss) of the cable. The amount of frequency distortion is dependent on the length of the cable. The equalizer block is an adaptive design. It is intended to correct for the ISI introduced into the input signal by variable lengths of cable. Since the equalizer is adaptive, there will not be residual ISI due to the mismatch in equalizer setting and the actual length of cable that the input signal has been transmitted through.

The equalizer architecture insures a proper equalization up to 1800 feet.

### 2.3.3.4 PLL Clock Recovery

The clock recovery circuit (RX PLL) extracts the embedded clock from the sliced data and provides it and the retimed data to the decoder (data mode). Upon startup (after the internal reset is deasserted), the RX PLL uses a reference clock (CLAD or REFCLK, running at the symbol rate) and a phase-frequency detector to lock to the correct data rate (reference mode). During reference mode, the data outputs are squelched (set to 0). The RX PLL is kept in reference mode until a valid input is detected.

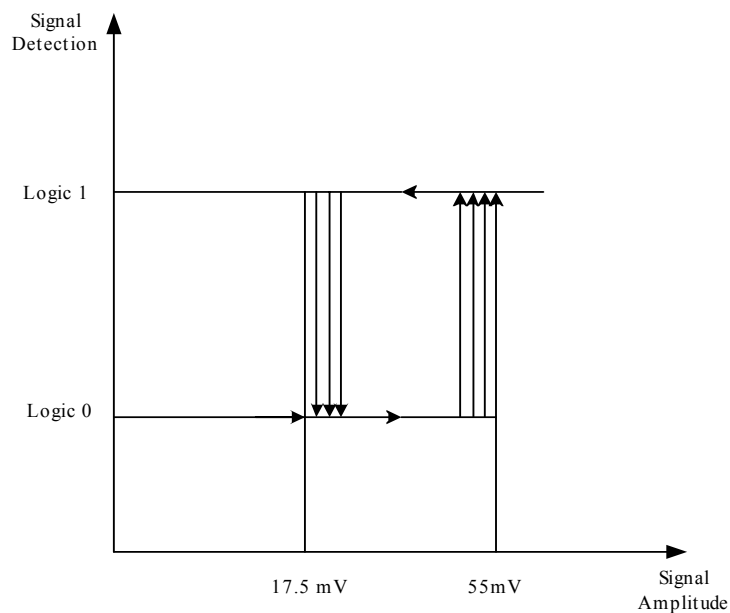
After the above condition is met, the RX PLL will switch to data mode and attempt to phase lock to the incoming data. In data mode, the RX PLL compares the data frequency to the REFCLK frequency. If the frequency of RCLK is more than  $\pm 6\%$  from the REFCLK reference frequency, then the RX PLL will switch back to reference mode and go through the above sequence again.

The RX PLL meets the extensive jitter requirements, [Section 2.5](#).

### 2.3.3.5 Loss of Signal Detector – RLOS

The RLOS detector circuitry consists of two functional blocks: the analog section and the digital section.

The Analog RLOS detector monitors the signal at the input of the receiver. If the signal amplitude drops below 17.5mV, a “receive loss of signal” flag is set. It will be reset if the signal amplitude increases above 55mV.

**Figure 2-12. RLOS Hysteresis**

In the analog section, three bits control the declare and clear levels for each channel, see [Table 2-6](#).

A bit for each channel, RDx (RLOS Disable), is used to decide if RLOS should disable data squelching. These two set and reset levels can be changed by 3 control bits in the RX path miscellaneous control register, RX\_MISC1[2:0], as listed in [Table 2-6](#).

**Table 2-6. RLOS Hysteresis**

Bit2	Bit1	Bit0	RLOS Declared(mV)	RLOS Cleared (mV)
0	0	0	0	0
0	0	1	17.5	17.5
0	1	0	17.5	55
0	1	1	35	110
1	0	0	35	35
1	0	1	25	48
1	1	0	30	40
1	1	1	25	75

The Receive Loss Of Signal (RLOS) digital section monitors the retimed data from the clock recovery block. The AMI data is checked for a continuous run of 0s. When a continuous run of 128 consecutive 0s occurs, the RLOS signal is asserted, then a 1s count is made on every block of 128 AMI symbols. The RLOS signal is deasserted when the 1s count within a block of 128 symbols is at least:

- Minimum 1s density =  $43 \pm 1$  count out of 128 (~33.6%)
- A SONET NE shall declare a LOS failure when the LOS defect persists for 2.5 ( $\pm 0.5$ ) seconds.
- A SONET NE shall clear a LOS failure when the LOS defect is absent for 10 ( $\pm 0.5$ ) seconds.

The detector is not affected by the state of line or source looping.

### 2.3.3.6

### Data Squelching

#### Overview

A counter in the receiver counts the number of consecutive symbol periods without a valid data pulse. When 128 or more consecutive 0s are counted, the receiver assumes it has lost the signal and resets itself to try to regain the signal. While the receiver is reacquiring the signal, the clock recovery block locks to the reference clock, and data squelching is achieved by forcing the data bits to 0. The data squelching is true in both NRZ and dual rail mode. When the input signal has been properly amplified and equalized, the clock recovery PLL then switches to the incoming data.

#### Control

Control of the data squelching feature is accomplished with bits [6:5] in the CH\_CTRL1 register, 0xn01. By setting these bits to either 10 or 11 will enable data squelching when RLOS is detected.

### 2.3.3.7

#### AMI/B3ZS/HDB3 Decoder

In the M2835x device, when ENDECDis = 0 (encoder/decoder enabled), the decoder takes the output from the clock recovery circuit and decodes the data (HDB3 or B3ZS) into a single retimed NRZ data signal. The data signal is then sent out of the M2835x RNRZ (RPOS) pin. Any detected Line Code Violations (LCV) are sent over the corresponding RLCV (RNEG) pin. The RLCV pin is asserted for one symbol period at the time the violation appears on the RX output pin (RNRZ).

The following shows data sequence criteria for LCV; violations are indicated in bold text. A valid bipolar pulse is indicated by a B. A bipolar violation (non-alternating positive or negative) pulse is indicated by a V.

- Excessive zeros: 0, 0, 0, **0** (HDB3) or 0, 0, **0** (B3ZS). These violations are passed on as 0 data on the RNRZ pin..M28335 Data Sheet Functional Description
- Bipolar violation: B, 0, **V** (i.e., +1, 0, +1 or -1, 0, -1 for HDB3) B, **V** (B3ZS and HDB3). These violations are passed on as 1 data on the RNRZ pin.
- Coding violation: 0, 0, **V** (HDB3) or 0, **V** (B3ZS) with an even number of Bs since the last valid 0 substitution V (follows coding rule). These violations are passed on as 0 data on the RNRZ pin.

The even/odd counter (used to count the number of Bs between Vs) will count a bipolar violation as a B. A coding violation or a valid 0 substitution resets the counter.

When ENDECDis = 1, the decoder is disabled, and the retimed slicer outputs are sent out over RPOS (RNRZ) and RNEG (RLCV) pins. These outputs are then decoded by the Framer or other downstream device. LCVs are not detected in this mode of operation. The decoder is configurable for either:

- E3 mode using HDB3 coding (E3MODE = 1), or
- DS3/STS-1 mode using B3ZS coding (E3MODE = 0).

The receiver digital data outputs are centered on the rising edge of RCLK.

### 2.3.3.8

#### Counters

There are three counters available for counting coding violations on the transmission line. They include line code violations, LCV, excessive zeroes, EXZ, and bipolar violations, BPV.

In addition, there are zero substitutions not adhering to the odd B's between V's rule. Zero substitution errors, ZVIOL, keeps track of these errors.

The following assumptions and effect on the data stream are implemented in order to determine the Line Code Violation errors:

1. EXZ - Excessive zeros: 0,0,0,0 (HDB3)/0,0,0 (B3ZS). These violations are passed on as 0 data on the NRZ pin. Excessive zeros is the occurrence of exactly 3 (B3ZS), 4 (HDB3) consecutive zeros. There may be consecutive EXZ and depending on the bit LCVZERO\_MODE in the LCV\_CTRL1 register at address offset 0xn25, input will be either counted as one or separate. Excessive zeros will reset the zero substitution
2. BPV - Bipolar violation: B,0,V (i.e. +1,0,+1 or -1,0,-1 for HDB3)/B,V (i.e. +1,+1 or -1,-1 for both B3ZS and HDB3). These violations are passed on as 1 data on the NRZ pin. BPV violations will be considered in the odd or even pulse counting

3. ZVIOL - Zero substitution violation. The ZVIOL are not counted separately, but rather in addition to either LCVs or BPVs as defined in the LCV configuration register. These will be passed as 0 data on the NRZ data out pin.

**NOTE:**

The B0(0)V monitoring window is a sliding window that will detect embedded zero substitutions and are passed as 0's on the data stream

### Counter Control and Configuration

The control bits LVCNT\_CFG[4:0] in the register LCV\_CTRL0 at address offset 0xn24 are used to direct which violation goes to what counter as shown in [Table 2-7](#). LCV Counter Control. Unused bit states are reserved.

**Table 2-7. LCV Counter Control**

Control Bits	Description
BVPCNT_CFG[1:0]	BVP counter configuration 01b = BPV errors are added to the BPV counter 10b = ZVIOL errors are added to the BPV counter
LVCNT_CFG[2:0]	LCV counter configuration 001b = EXZ errors are added to the LCV counter 010b = BPV errors are added to the LCV counter 100b = ZVIOL errors are added to the LCV counter

The bit LCVZERO\_MODE in the register LCV\_CTRL1 at address offset 0xn25 controls how consecutive zero violations are counted. When clear, every 3/4 consecutive zero violation is reported as an error. Setting this bit results in multiple 3/4 consecutive zero violations being counted only once.

To control the update frequency of the counters, the bits EXZCNT\_SEL, BPVCNT\_SEL and LVCNT\_SEL are used. To select real-time updating, set this bit. To select one second updates, clear this bit.

In the case where one or more of these counters were to overflow, there are bits that reflect this condition in the CH\_LST0 register at address offset 0xn10. The bits EXZCNT\_OF, BPVCNT\_OF, and LVCNT\_OF will set when the respective counters overflow.

When the overflow condition occurs, there are interrupts available in the CH\_INTST0 register at address offset 0xn14, EXZCNT\_OF\_INT, BPVCNT\_OF\_INT and LVCNT\_OF\_INT. To enable these interrupts, the bits EXZCNT\_OF\_INT\_EN,



BPVCNTOFINT\_EN, and LVCNTOFINT\_EN in the register CH\_INTEN0 at address offset 0xn18 must be set.

**NOTE:**

When any of the 3 error counter overflows, it sets an overflow bit field in the associated status register. The 24-bit counters will reset upon overflow or the rising edge of the one-second timer, depending on which event occurs first.

**Line Code Violation – LCV Counter**

The line code violations counter is 24 bits in length. The counter registers for line code violations are located at address offsets 0xn34 – 0xn36,

**Bipolar Violation – BPV Counter**

The bipolar violations counter is 24 bits in length. The counter register for bipolar violations are located at address offsets 0xn38 – 0xn3A.

**Excessive Zeroes – EXV Counter**

The excessive zeroes counter is 24 bits in length. The counter register for excessive zeroes are located at address offsets 0xn3C – 0xn3E.

**2.3.3.9****DC Continuity Check**

The RX path contains a function that detects the DC conditions of the receiver input. Specifically, it detects opens or shorts on the line. When an open or short is detected, an indication will be provided at the output. Use register RX\_MISC1, bit field RX\_HI\_R[1:0] ([Section 3.3.10](#)) to vary the open resistance detection values. The short detection level is fixed at 500 Ohms. Additionally, you must use register CH\_CTRL0, bit field EN\_DC\_CONT ([Section 3.3.1](#)) to enable the DC continuity check.

**2.4****Jitter Attenuator****2.4.1****Jitter Attenuation and Desynchronizer Overview**

The M2835x contains DS3/E3/STS-1 jitter attenuator and STS-1-to-DS3 or -E3 desynchronizer for each channel. It benefits the designer through ease of use, flexible configuration, and error monitoring while enabling a system design to comply with jitter standards and specifications.

The M28356/4/3/2 supports the following features:

- 6/4/3/2-channel jitter attenuator and desynchronizer device for DS3, E3, and STS-1 applications
- Crystal-less jitter attenuation
- One independent jitter attenuator (DJAT)/desynchronizer per channel
- Programmable clocking of both input and output data on either the rising or falling edge
- Ability to dejitter AMI or NRZ input data
- Two programmable PRBS generator/detectors per channel
- Fixed pattern generation/detection
- Bit error counter per channel

- One-second timer for event latching. This clock is internally generated.
- Interrupts
- FIFO underflow
- FIFO overflow
- DJAT frequency detection (signals when DJAT is close to underflow or overflow)
- Out-of-lock detection
- Power-down control for each channel
- Ability to independently reset each DJAT channel
- Ability to independently bypass the DJAT for each channel

## 2.4.2 JAT Configuration

### 2.4.2.1 Hardware Configuration

When the M2835x device is used in the hardware mode, there is **limited control** of the DJAT circuitry. The JATR<sub>X</sub> pin controls the placement of the DJAT in the transmit or receive path. The pin is internally pulled to V<sub>cc</sub>, placing the DJAT in the receive path by default. Pulling this pin to ground will enable the DJAT in the transmit path.

The DJAT is enabled in all hardware modes. There is no bypass or disabling feature available.

### 2.4.2.2 Software Configuration

## 2.4.3 Configuration

### 2.4.3.1 Register Settings

[Table 2-8](#) gives the basic setting for each of the three symbol rates. There are numerous additional registers available to customize the various DJAT properties.

**Table 2-8. DJAT Control Bits**

Register	Addr Offset	Bit(s)	Name								
Symbol Rate <sup>1</sup>	0xn00	1:0	LINERATE[1:0]								
JAT RX / TX <sup>2</sup>	0xn00	2	JAT_SEL								
JAT Reset	0xn5B	1	RB_JAT								
JAT Pwr Dn	0xn5B	0	PDB_JAT								
JAT Enable	0xn5B	3	JAT_EN								
WCLK Edge <sup>3</sup>	0xn5B	7	IN_SMP								
RCLK Edge <sup>3</sup>	0xn5B	6	OUT_SMP								
<b>Notes:</b> <sup>1</sup> Symbol Rate: <table border="1" data-bbox="487 814 1141 928"> <thead> <tr> <th></th><th>DS3</th><th>E3</th><th>STS-1</th></tr> </thead> <tbody> <tr> <td>LINERATE[1:0]</td><td>01 (default)</td><td>1x</td><td>00</td></tr> </tbody> </table>					DS3	E3	STS-1	LINERATE[1:0]	01 (default)	1x	00
	DS3	E3	STS-1								
LINERATE[1:0]	01 (default)	1x	00								
<sup>2</sup> Chooses the path where the DJAT is inserted: JAT_SEL = 0 Receive path JAT_SEL = 1 Transmit path (default) <sup>3</sup> Selects the sampling edge for the incoming or outgoing data stream: 0 = Falling edge (default) 1 = Rising edge											

### 2.4.3.2

### FIFO Length Settings

By default, the FIFO length is 24 bits deep. This is not directly accessible by the end user.

## 2.4.4 DJAT Mode Performance

### 2.4.4.1 E3 Line Timing

The E3 line timing mode suppresses jitter that is generated along a length of E3 line due to time-varying propagation delays of the line. The M28356/4/3/2 DJAT meets the listed standards applicable to this mode:

- Jitter tolerance: ETSI TBR 24, G.823
- Jitter transfer: G.751
- Intrinsic jitter: G.751
- Output jitter: ETSI TBR 24, G.823

#### E3 Line Timing Jitter Tolerance

This section presents the jitter tolerance performance of the M28356/4/3/2 DJAT.

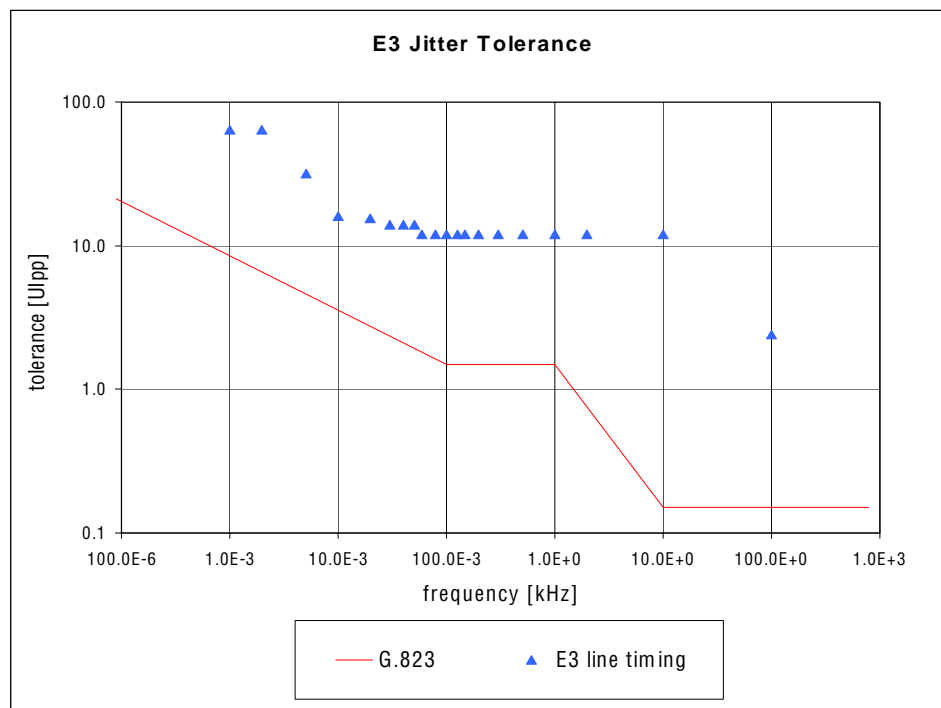
The performance of the M28356/4/3/2 DJAT system is shown in [Table 2-9](#).

**Table 2-9. E3 Line Timing Jitter Tolerance Data**

Frequency [Hz]	UI (peak-to-peak)
1	>64
2	>64
5	31.939
10	15.939
20	15.564
30	14.064
40	14.064
50	14.064
60	12.064
80	12.064
100	12.064
125	12.064
150	12.064
200	12.064
300	12.064
500	12.064
1000	12.064
2000	12.064
10000	12.064
100000	2.394

The performance of the M28356/4/3/2 DJAT system is illustrated in [Figure 2-13](#), in comparison to the applicable standards. The ETSI TBR 24 standard is not shown because it is identical to G.823 with the exception that G.823 includes frequencies under 100 Hz.

**Figure 2-13. E3 Jitter Tolerance**



### E3 Line Timing Jitter Transfer

The E3 line timing jitter transfer performance of the device is shown in [Table 2-10](#).

**Table 2-10. E3 Line Timing Jitter Transfer Data (1 of 2)**

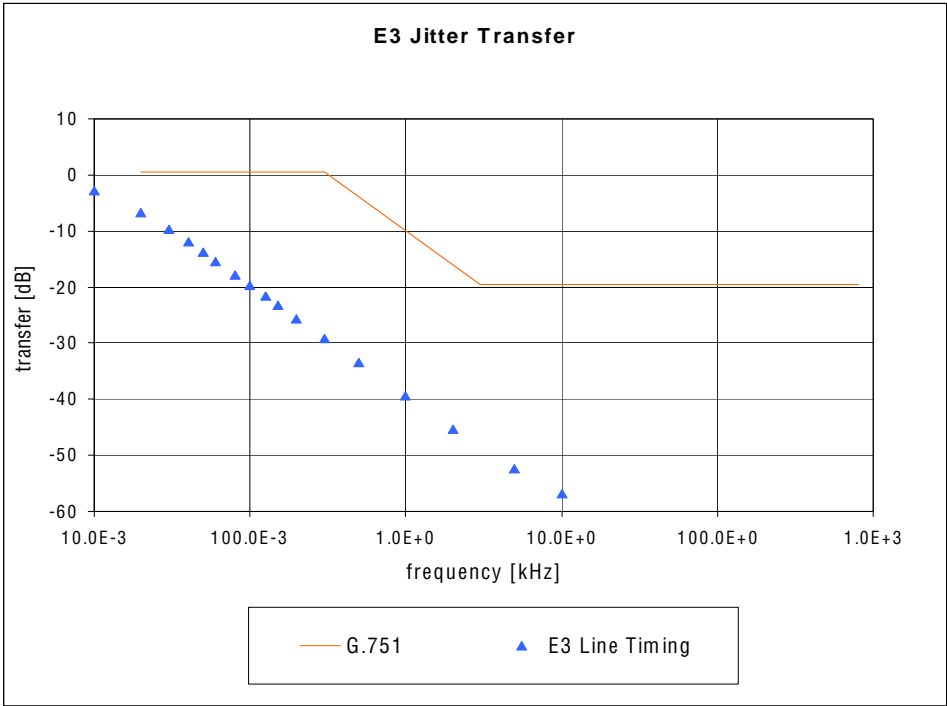
Frequency [Hz]	Input Jitter Amplitude [UI <sub>pp</sub> ]	Jitter Gain [dB]
10	10	-2.80
20	10	-6.73
30	10	-9.70
40	10	-11.95
50	10	-13.79
60	10	-15.35
80	10	-17.81
100	10	-19.72
125	10	-21.61
150	10	-23.17
200	10	-25.63
300	10	-29.12

Table 2-10. E3 Line Timing Jitter Transfer Data (2 of 2)

Frequency [Hz]	Input Jitter Amplitude [UI <sub>pp</sub> ]	Jitter Gain [dB]
500	10	−33.47
1000	10	−39.45
2000	10	−45.29
5000	10	−52.42
10000	10	−56.84

The jitter transfer performance of the M28356/4/3/2 DJAT is illustrated in [Figure 2-14](#), graphed versus the G.751 standard.

Figure 2-14. E3 Jitter Transfer



E3 Line Timing Intrinsic Jitter

The intrinsic jitter performance of the M28356/4/3/2 DJAT is shown compared to the G.751 intrinsic jitter standard in [Table 2-11](#).

Table 2-11. E3 Line Timing Intrinsic Jitter

Measurement Band	G.751 Maximum Intrinsic Jitter [UI <sub>pp</sub> ]	M28356/4/3/2 DJAT Intrinsic Jitter [UI <sub>pp</sub> ]
10 Hz to 800 kHz	0.300	0.040
10 kHz to 800 kHz	0.050	0.040

### E3 Line Timing Output Jitter

The output jitter performance of the M28356/4/3/2 DJAT is shown compared to the two applicable jitter standards in [Table 2-12](#).

**Table 2-12. E3 Line Timing Output Jitter**

Measurement Band	ETSI TBR 24 Maximum Output Jitter [UI <sub>pp</sub> ]	G.823 Maximum Output Jitter [UI <sub>pp</sub> ]	M28356/4/3/2 DJAT Maximum Output Jitter [UI <sub>pp</sub> ]
100 Hz to 800 kHz	0.400	1.500	0.37
10 kHz to 800 kHz	0.150	0.150	0.05

#### 2.4.4.2

### E3 Demapping

The E3 demapping mode meets the requirements of attenuating jitter that arises from demapping an E3 payload from a VC-3 embedded into an STS-1 signal. This mapping process is described by G.709. The demapping of the E3 signal results in a gapped clock that has a clock period of a 51.84 MHz STS-1 clock but contains enough gaps that the data rate is effectively that of E3, or 34.368 Mbit/s. The M28356/4/3/2 DJAT attenuates the jitter of this gapped clock down to the levels required by G.783. It attenuates the raw demapping jitter and attenuates the demapping jitter that arises from the pointer adjustment sequences specified by G.783 for the SPE within an STS-1 frame.

The performance of the M28356/4/3/2 DJAT versus the applicable standard is shown in [Table 2-13](#).

**Table 2-13. E3 Demapping Mode Output Jitter**

Pointer Adjustment Pattern Name	Measurement Band	G.783 Maximum Output Jitter [UI <sub>pp</sub> ]	M28356/4/3/2 DJAT Output Jitter [UI <sub>pp</sub> ]	Timing Parameter <sup>(1)</sup> [seconds]
No pointer adjustments	100 Hz to 800 kHz	under study	0.111	n/a
	10 kHz to 800 kHz	0.075	0.07	n/a
Single pointers of opposite polarity	100 Hz to 800 kHz	0.4	0.117	10
	10 kHz to 800 kHz	0.075	0.07	41.93
Regular pointers plus one double pointer	100 Hz to 800 kHz	0.4	0.119	2.588
	10 kHz to 800 kHz	0.075	0.07	10
Regular pointers with one missing pointer	100 Hz to 800 kHz	0.4	0.116	0.173
	10 kHz to 800 kHz	0.075	0.070	0.173
Double pointers of opposite polarity	100 Hz to 800 kHz	0.75	0.115	41.93
	10 kHz to 800 kHz	0.075	0.07	10.00
<b>NOTE:</b> <sup>(1)</sup> The timing parameter is the value of the variable pointer adjustment interval that produces the maximum output jitter from the M28356/4/3/2 DJAT. The variable interval is specified in the applicable standards.				

### 2.4.4.3

### DS3 Line Timing

The DS3 line timing mode suppresses jitter that is generated along a length of DS3 line due to time-varying propagation delays of the line. The M28356/4/3/2 DJAT meets the listed standards applicable to this mode:

- Jitter tolerance: GR-499 (CAT II), G.824, TR 54014
- Jitter transfer: G.755, GR-499 (CAT II), TR 54014
- Intrinsic jitter: G.755, GR-253, TR 54014
- Output jitter: GR-499 input jitter attenuated to levels of T1.404 network interface for CI type I equipment

### DS3 Line Timing Jitter Tolerance

This section presents the jitter tolerance performance of the M28356/4/3/2 DJAT.

The performance of the M28356/4/3/2 DJAT is shown in [Table 2-14](#). For frequencies of 300 Hz and less, the device's jitter tolerance exceeds the maximum jitter generated by the test equipment.

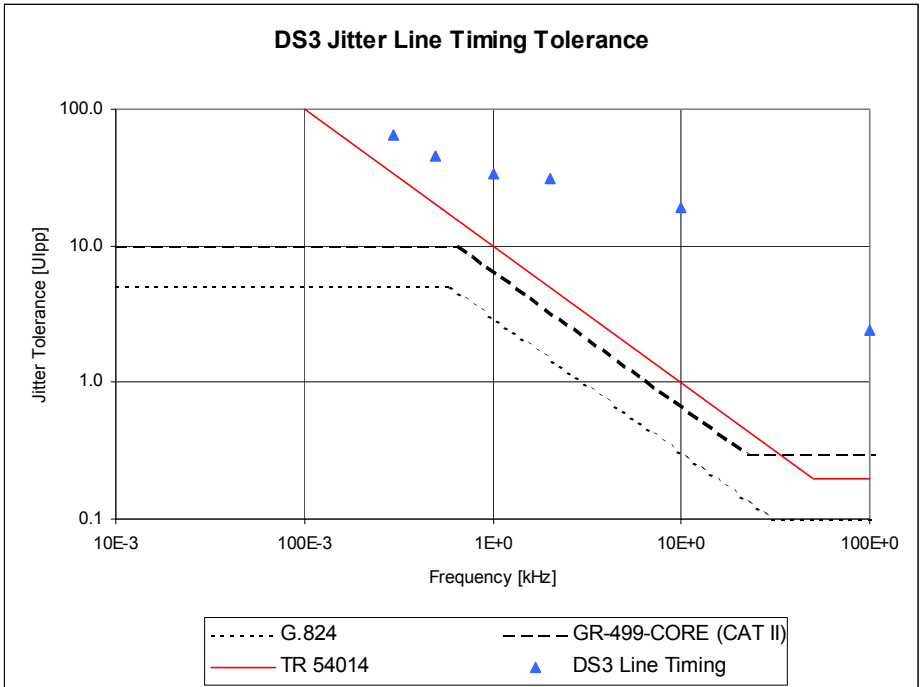
**Table 2-14. DS3 Line Timing Jitter Tolerance**

Frequency [Hz]	UI (peak to peak)
1	>64
2	>64
5	>64
10	>64
20	>64
30	>64
40	>64
50	>64
60	>64
80	>64
100	>64
125	>64
150	>64
200	>64
300	>64
500	45
1000	34
2000	31
10000	19
100000	2.394

The performance of the M28356/4/3/2 DJAT system is illustrated in [Figure 2-15](#), in comparison to the applicable standards.



Figure 2-15. DS3 Jitter Tolerance



**DS3 Line Timing Jitter Transfer**

The DS3 line timing jitter transfer performance of the device is shown in [Table 2-15](#).

Table 2-15. DS3 Line Timing Jitter Transfer (1 of 2)

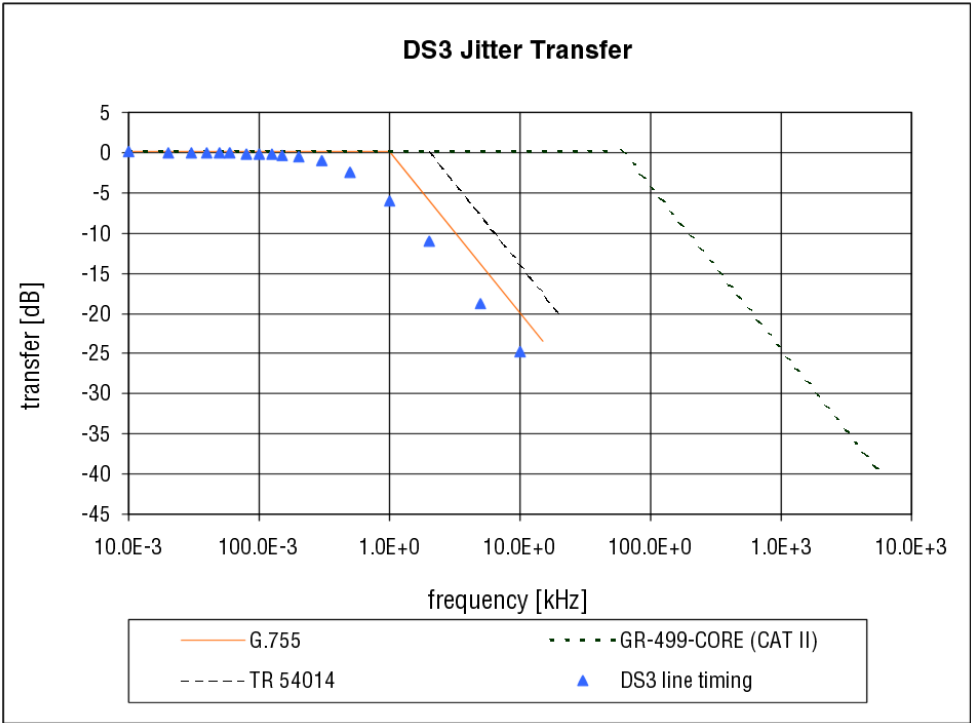
Frequency [Hz]	Input Jitter Amplitude [U <sub>pp</sub> ]	Jitter Gain [dB]
10	10	0.08
20	10	0.03
30	10	−0.03
40	10	−0.01
50	10	−0.07
60	10	−0.09
80	10	−0.13
100	10	−0.14
125	10	−0.20
150	10	−0.28
200	10	−0.46
300	10	−1.00
500	10	−2.39

Table 2-15. DS3 Line Timing Jitter Transfer (2 of 2)

Frequency [Hz]	Input Jitter Amplitude [UI <sub>pp</sub> ]	Jitter Gain [dB]
1000	10	−5.95
2000	10	−11.06
5000	10	−18.78
10000	10	−24.74

The jitter transfer performance of the M28356/4/3/2 DJAT is shown in [Figure 2-16](#), graphed versus the applicable standards.

Figure 2-16. DS3 Jitter Transfer



**DS3 Line Timing Intrinsic Jitter**

The intrinsic jitter performance of the M28356/4/3/2 DJAT is shown compared to the applicable standards in [Table 2-16](#).

Table 2-16. DS3 Line Timing Intrinsic Jitter

Measurement Band	Maximum Intrinsic Jitter [UI <sub>pp</sub> ]			M28356/4/3/2 DJAT Intrinsic Jitter [UI <sub>pp</sub> ]
	G.755	GR-253	TR 54014	
10 Hz to 400 kHz	0.300	0.100	0.050	0.038
30 kHz to 400 kHz			0.025	0.015

### DS3 Line Timing Output Jitter

Applications that require GR-499 levels of input jitter to be attenuated to levels of T1.404 network interface for CI type I equipment must use the part in DS3 demapping mode.

#### 2.4.4.4

### DS3 Demapping

The DS3 demapping mode meets the requirements of attenuating jitter that arises from demapping a DS3 payload embedded in an STS-1 signal. This mapping process is described by GR-253. The demapping of the DS3 signal results in a gapped clock that has a clock period of a 51.84 MHz STS-1 clock but contains enough gaps that the effective data rate is that of DS3, or 44.736 Mbit/s. The M28356/4/3/2 DJAT attenuates the jitter of this gapped clock down to the levels required by GR-253, G.783, and TR 54014. It attenuates the raw demapping jitter and attenuates the demapping jitter that arises from the pointer adjustment sequences specified by GR-253 for the SPE within an STS-1 frame.

The M28356/4/3/2 DJAT meets the listed standards applicable to this mode:

- Jitter transfer: GR-499, GR-253
- Demapping output jitter: GR-253, G.783, TR 54014

### DS3 Demapping Jitter Transfer

Category I jitter transfer for DS3 signals is defined as the transfer of jitter from the input to the output of the process that maps and demaps DS3 signals to and from STS-1 signals and then desynchronizes the demapped DS3 signal from its gapped STS-1 clock. The mapping of the DS3 signal into the STS-1 signal is the input of the process. The desynchronization of the DS3 signal from its gapped STS-1 clock is the output of the process. The input jitter is increased or decreased by varying the jitter on the DS3 signal relative to the STS-1 signal prior to the mapping operation. The performance of the M28356/4/3/2 DJAT is measured by applying jitter to the mapped signal and measuring the amount of jitter that is transferred to the output of the M28356/4/3/2 DJAT.

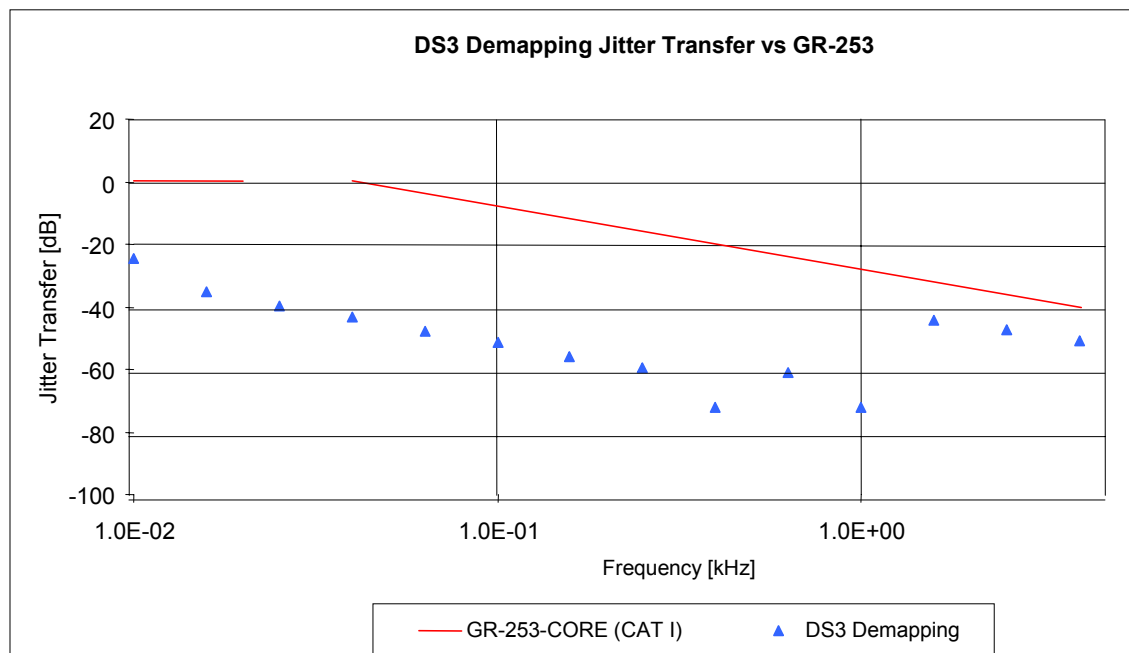
[Table 2-17](#) shows the demapping jitter transfer performance of the M28356/4/3/2 DJAT.

**Table 2-17. DS3 Demapping Jitter Transfer**

Frequency [Hz]	Input Jitter Amplitude [UIpp]	Jitter Gain [dB]
10	10	-24.35
15.8	10	-35.42
25.1	10	-39.59
39.8	10	-43.31
63.1	10	-47.96
100	64	-51.64
158	63.1	-56.14
251	39.81	-59.66
398	25.12	-72.23
631	15.85	-61.14
1000	10	-72.08
1580	6.31	-44.23
2510	3.98	-47.27
3980	2.51	-50.88

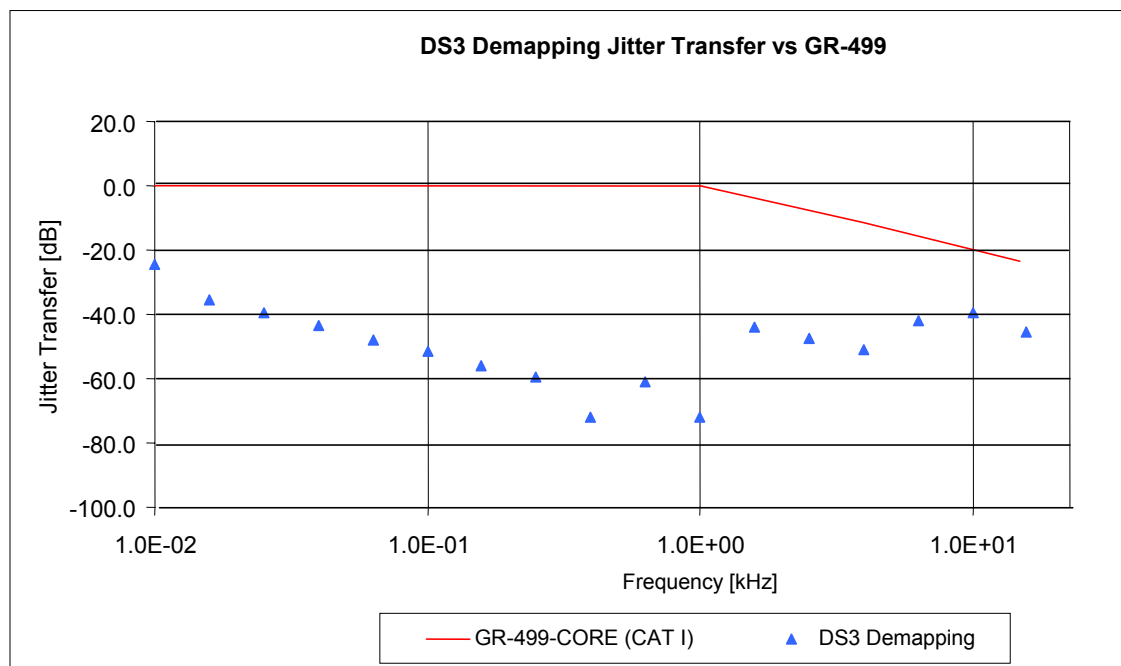
The performance of the M28356/4/3/2 DJAT is graphed versus the GR-253 standard in Figure 2-17.

**Figure 2-17. Jitter Transfer versus the GR-253 Standard**



The performance of the M28356/4/3/2 DJAT is graphed versus the GR-499 standard in Figure 2-14.

**Figure 2-18. DS3 Jitter Transfer versus the GR-499 Standard**



### DS3 Demapping Mode Category I Output Jitter

The performance of the M28356/4/3/2 DJAT demapping output jitter versus the applicable standards is shown in [Table 2-18](#).

**Table 2-18. DS3 Demapping Mode Output Jitter**

Pointer Adjustment Pattern Name	Measurement Band	Maximum Output Jitter [UI <sub>pp</sub> ]			M28356/4/3/2 DJAT Output Jitter [UI <sub>pp</sub> ]	Timing Parameter <sup>(1)</sup> [seconds]
		GR-253	G.783	TR 54014		
(no pointer adjustments)	10 Hz to 400 kHz	0.4	0.4	—	0.113	n/a
(no pointer adjustments)	30 kHz to 400 kHz	—	0.1	—	0.036	n/a
single	10 Hz to 400 kHz	A0 + 0.3 <sup>(2)</sup>	—	—	0.33	39.585
maximum rate burst	10 Hz to 400 kHz	1.3	—	—	0.699	39.585
phase transient burst	10 Hz to 400 kHz	1.2	—	—	0.578	30
87 – 3	10 Hz to 400 kHz	1.0	—	—	0.698	0.106
87 – 3 add	10 Hz to 400 kHz	1.3	—	—	0.727	0.106
87 – 3 cancel	10 Hz to 400 kHz	1.3	—	—	0.862	0.106
periodic – continuous	10 Hz to 400 kHz	1.0	—	—	0.221	0.106
periodic – add	10 Hz to 400 kHz	1.3	—	—	0.402	0.106
periodic – cancel	10 Hz to 400 kHz	1.3	—	—	0.36	0.016
<b>NOTE:</b>						
<sup>(1)</sup> The timing parameter is the value of the variable pointer adjustment interval that produces the maximum output jitter from the M28356/4/3/2 DJAT. The variable interval is specified in the applicable standards.						
<sup>(2)</sup> The maximum for the single pointer adjustment is 0.3 UI <sub>pp</sub> plus the measurement of the DUT for no pointer adjustments						

### DS3 Demapping Mode Category II Output Jitter

The DS3 demapping mode must also be used for applications that require GR-499 levels of input jitter to be attenuated to levels of T1.404 network interface for CI type I equipment. The intended performance of the M28356/4/3/2 DJAT is shown in comparison to the T1.404 standard in [Table 2-19](#).

**Table 2-19. DS3 Demapping Mode Maximum Output Jitter**

Measurement Band	T1.404 Maximum Output Jitter [UI <sub>pp</sub> ] for CI type I	M28356/4/3/2 DJAT Maximum Output Jitter [UI <sub>pp</sub> ]
10 Hz to 400 kHz	0.50	0.115
30 kHz to 400 kHz	0.05	0.038

## 2.4.4.5

### STS-1 Line Timing

The STS-1 line timing mode suppresses jitter that is generated along a length of STS-1 electrical line due to time-varying propagation delays of the line. The M28356/4/3/2 DJAT meets the listed standards applicable to this mode:

- jitter tolerance: GR-253, T1.105.03-1994
- jitter transfer: GR-253
- output jitter: GR-253, T1.105.03-1994

### STS-1 Line Timing Jitter Tolerance

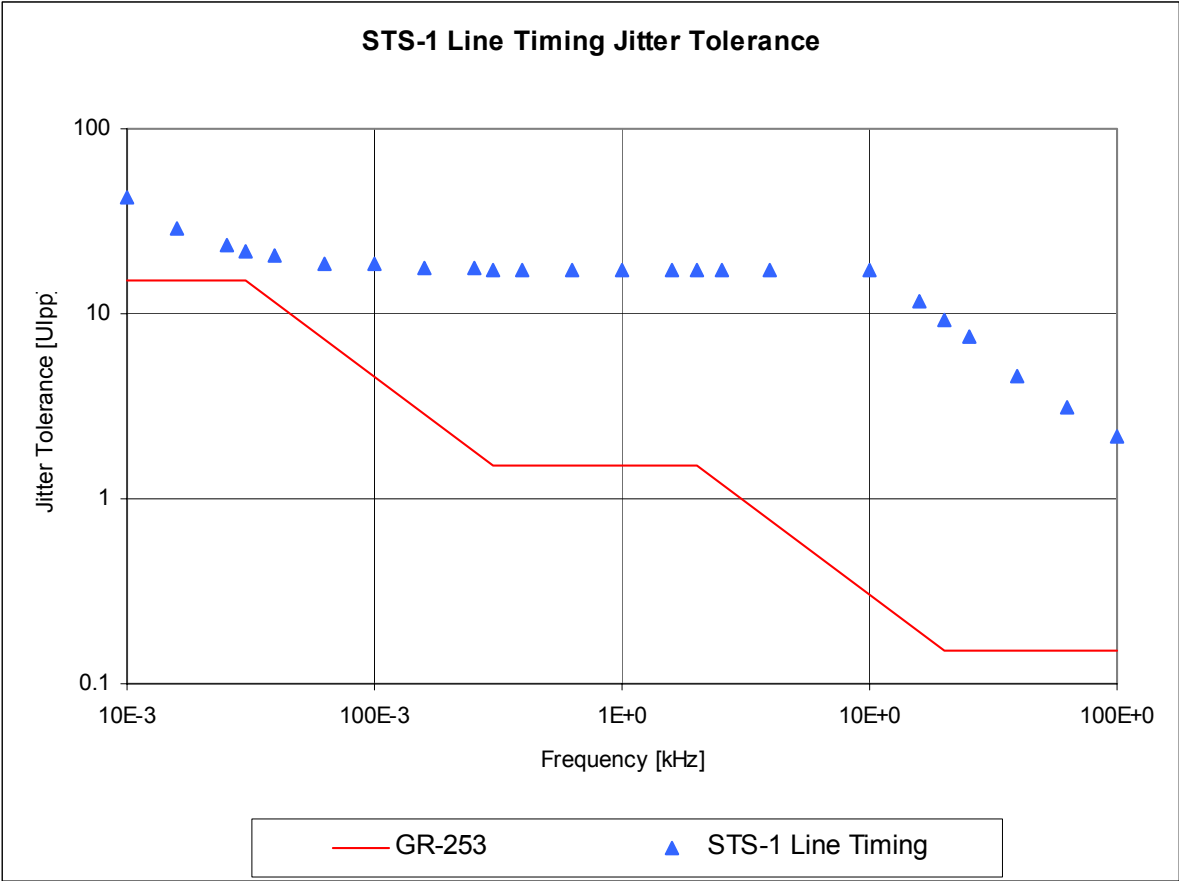
This section presents the jitter tolerance performance of the M28356/4/3/2 DJAT. The applicable standards are GR-253 and T1.105.03-1994. The performance of the M28356/4/3/2 DJAT is shown in [Table 2-20](#).

**Table 2-20. STS-1 Line Timing Jitter Tolerance**

Frequency [Hz]	UI (peak-to-peak)
10	43.12
15.8	29.06
25.1	23.43
30	21.56
39.8	20.48
63.1	18.71
100	18.56
158	17.75
251	17.45
300	17.25
398	17.25
631	17.25
1000	17.25
1580	17.25
2000	17.25
2510	17.25
3980	17.25
6310	17.76
10000	17.4
15800	11.78
20000	9.3
25100	7.5
39800	4.65
63100	3.15
100000	2.17

The performance of the M28356/4/3/2 DJAT system is shown in [Figure 2-19](#) in comparison to the GR-253 standard. The T1.105.03-1994 standard is not shown but is identical to GR-253.

Figure 2-19. STS-1 Line Timing Jitter Tolerance





**STS-1 Line Timing Jitter Transfer**

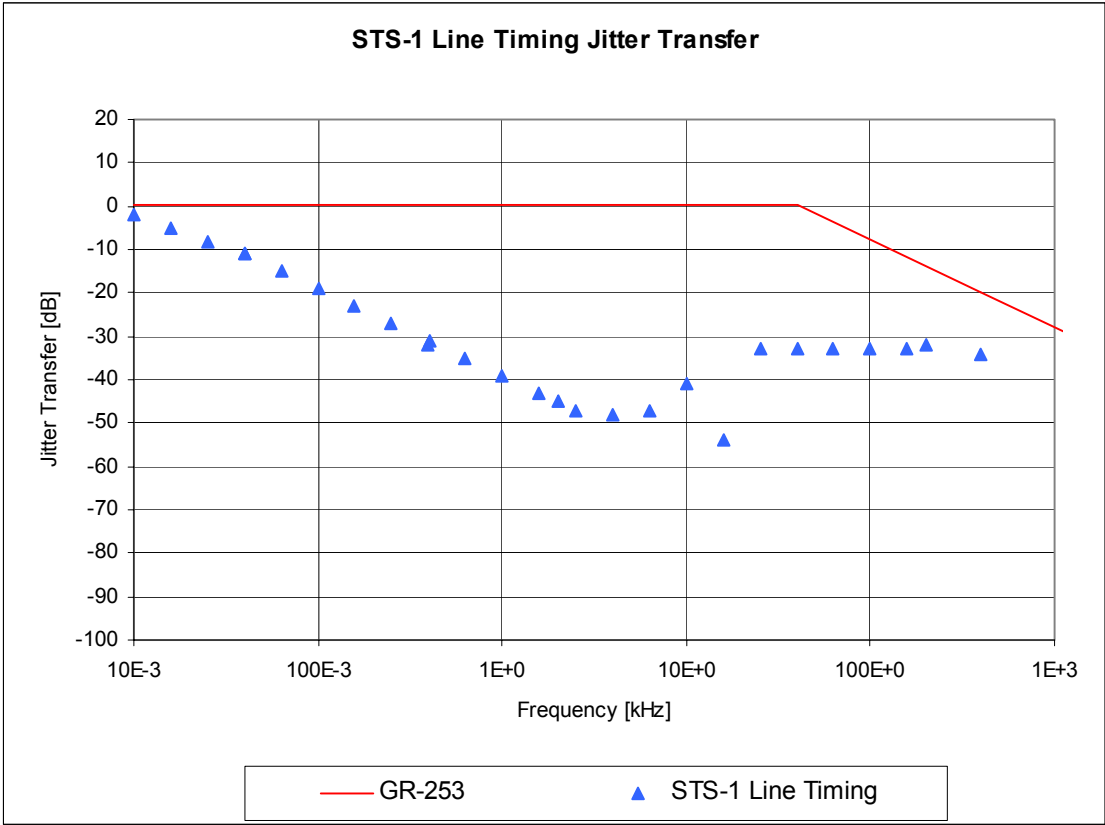
The DS3 line timing jitter transfer performance of the device is shown in [Table 2-21](#). The applicable standard is GR-253.

**Table 2-21. STS-1 Line Timing Jitter Transfer**

Frequency [Hz]	Input Jitter Amplitude [ $UI_{pp}$ ]	Jitter Gain [dB]
10	15	-2
15.8	15	-5
25.1	15	-8
39.8	11.3	-11
40	11.25	-11
63.1	7.13	-15
100	4.5	-19
158	2.84	-23
251	1.79	-27
398	1.5	-32
400	1.5	-31
631	1.5	-35
1000	1.5	-39
1580	1.5	-43
2000	1.5	-45
2510	1.19	-47
3980	0.75	-48
4000	0.75	-49
6310	0.48	-47
10000	0.3	-41
15800	0.19	-54
25100	0.15	-33
39800	0.15	-33
63100	0.15	-33
100000	0.15	-33
158000	0.15	-33
200000	0.15	-32
398000	0.15	-34

The jitter transfer performance of the M28356/4/3/2 DJAT is shown in [Figure 2-20](#), graphed versus the GR-253 standard:

Figure 2-20. STS-1 Line Timing Jitter Transfer



STS-1 Line Timing Output Jitter

The intended output jitter performance of the M28356/4/3/2 DJAT is shown compared to the GR-253 standard in Table 2-22. The T1.105.03-1994 standard is not shown but is identical to GR-253.

Table 2-22. STS-1 Line Timing Output Jitter

Measurement Band	GR-253 Maximum Output Jitter [UI <sub>pp</sub> ]	M28356/4/3/2 DJAT Maximum Output Jitter [UI <sub>pp</sub> ]
100 Hz to 400 kHz	1.500	1.450
20 kHz to 400 kHz	0.150	0.060

## 2.5 Configuration and Control

### 2.5.1 Mode Selection

There are three configuration control interfaces: hardware interface, parallel interface, and serial interface. The parallel interface and serial interface modes are collectively called software modes. The M2835x is configured for one of these modes using the IF\_MODE[1:0] pins on power-up according to [Table 2-23](#).

**Table 2-23. Configuration Control Selection**

IF_MODE1	IF_MODE0	Interface Mode
0	0	Hardware Mode
0	1	Reserved
1	0	Parallel Mode
1	1	Serial Mode

### 2.5.2 Hardware Mode

To operate the M2835x in hardware mode, the device must be configured on power-up with IF\_MODE[1:0] = 00. The pins listed in [Table 2-24](#) are then used to configure each LIU and DJAT.

**Operation Note:**

The DJAT is always enabled and configured for demapping mode when the device is in hardware mode.

**Table 2-24. Configuration Options in Hardware Mode**

Pins	Configuration
LINE_RATE1 LINE_RATE0	<p>Selects DS3, E3, or STS-1 device operation.</p> <p>LINERATE[1:0] = 00 selects STS-1 mode</p> <p>LINERATE[1:0] = 01 selects DS3 mode</p> <p>LINERATE[1:0] = 1x selects E3 mode</p> <p>In E3 mode, the pulse shaper is changed, the LBO settings are ignored and the encoder/decoder is set to HDB3 line coding.</p> <p><b>Note:</b> These pins are ignored in software mode.</p>
JATRX	<p>Enables the DJAT in the receive or the transmit direction for all channels.</p> <p>1 = DJAT enabled in the receive direction</p> <p>0 = DJAT enabled in the transmit direction</p> <p><b>Note:</b> This pin is ignored in software mode.</p>
ENn	<p>Each pin enables a data channel.</p> <p>1 = Channel enabled</p> <p>0 = Channel disabled</p> <p><b>Note:</b> In software mode, this pin must be left unconnected or pulled high.</p>
LIU_BYP	<p>Used for test purposes. Refer to the description of the LIU_BYP pin in Table 1-10 for more details.</p> <p>Bypasses the LIUs for all channels.</p> <p>1 = LIU bypass enabled</p> <p>0 = LIU bypass disabled</p> <p><b>Note:</b> In software mode, this pin must be used to bypass the LIUs.</p>
ENENCDEC	<p>Enables/disables the encoder/decoder for all channels.</p> <p>0 = Dual rail format (Encoder/decoder disabled)</p> <p>1 = NRZ format (Encoder/decoder enabled)</p> <p><b>Note:</b> In software mode, this pin must be left unconnected or pulled high.</p>
TAIS	<p>Replaces the transmit data with AIS for each channel.</p> <p>1 = AIS mode enabled</p> <p>0 = AIS mode disabled</p> <p><b>Note:</b> In software mode, this pin must be left unconnected or pulled low.</p>
LBO <sub>n</sub>	<p>Enables the channel line build out filter function.</p> <p>1 = line build out filter enabled</p> <p>0 = line build out filter disabled</p> <p><b>Note:</b> In parallel software mode, these pins are used as the microprocessor interface data (DATAn) pins. In serial software mode, these pins are ignored.</p>
RESETB	<p>Asynchronously resets the M2835x device – active low.</p> <p>1 = Device released from reset.</p> <p>0 = Device placed in reset.</p> <p><b>NOTE:</b> This pin is operational in software mode.</p>
XOEB	<p>Enables transmit output drivers for all channels.</p> <p>1 = Transmit line output drivers set to high impedance state.</p> <p>0 = Transmit line output drivers enabled.</p> <p><b>Note:</b> In software mode, this pin should be left unconnected or pulled low.</p>

**Table 2-24. Configuration Options in Hardware Mode**

XTAL_BYP	Bypasses the internal crystal oscillator circuitry. 1 = oscillator disabled and CLK19P44_IO is an input. 0 = oscillator enabled and CLK19P44_IO is an output. <b>NOTE:</b> In software mode, this pin must be used to bypass the crystal oscillator.
CLAD_BYP	Bypasses all three (3) CLADs. 0 = CLADs are enabled and STS1_REFCLK, DS3_REFCLK, and E3_REFCLK pins are configured as outputs pins. 1 = CLADs are bypassed and the STS1_REFCLK, DS3_REFCLK, and E3_REFCLK pins are configured as inputs. In addition, the external reference clock(s) must be provided via the STS1_REFCLK, DS3_REFCLK, and/or E3_REFCLK pins. <b>Note:</b> In software mode, this pin must be set to “1” to configure the three line reference clock pins (i.e. STS1_REFCLK, DS3_REFCLK, and E3_REFCLK) as inputs.
RLOOPn	Enables Remote (Line) Loopback. 1 = remote (line) loopback enabled 0 = remote (line) loopback disabled <b>Note:</b> In parallel software mode, these pins are used as the microprocessor interface address (ADDRn) or data (DATAn) pins. In serial software mode, these pins are ignored.
LLOOP	Enables Local (Source) Loopback. 1 = local (source) loopback enabled 0 = local (source) loopback disabled <b>Note:</b> In parallel software mode, these pins are used as the microprocessor interface address (ADDRn) pins. In serial software mode, these pins are ignored.

Hardware mode pins control only the basic DJAT and LIU functionality. To use the PRBS and the advanced DJAT functions, including control and status signals, one of the software control modes must be implemented.

## 2.5.3 Software Interface Mode

The M2835x may be operated in either the parallel or serial software interface mode at power up depending on the external IF\_MODE[1:0] pin configurations. To operate the M2835x in parallel interface mode, the device must be configured on power-up with IF\_MODE[1:0] = 10. To operate the M2835x in serial interface mode, the device must be configured on power-up with IF\_MODE[1:0] = 11.

### Operation Notes:

1. Upon powering up the M2835x and prior to attempting to access its registers, allow it to come out of reset by waiting at least 30 milliseconds (30 ms) after power is applied to the device.
2. To support optimum microprocessor interface operation when the device is in software interface mode, it is recommended that the STS-1 line rate clock always be generated internally or supplied externally.

The M2835x serial and parallel interfaces use an internal clock to resynchronize signals coming into the interface. The internal clock used for resynchronization operates at the

frequency of the fastest reference clock present in the device or it operates at 19.44 MHz if reference clocks are not present (i.e., the three CLADs are bypassed and external reference clocks are not present).

The reference clock pins (x\_REFCLK) and their rates are: STS1\_REFCLK = 51.84 MHz, DS3\_REFCLK = 44.736 MHz, or E3\_REFCLK = 34.368 MHz. Each of the three reference clocks are generated either internally by their CLAD or if the three CLADs are bypassed by setting the CLAD\_BYP pin to “1”, the user externally supplies the reference clocks to the x\_REFCLK pins.

The M2835x uses internal crystal oscillator circuitry to generate the 19.44 MHz clock from an external 19.44 MHz crystal that is connected to the XTAL\_IN1 and XTAL\_IN2 pins. Alternatively, if the internal crystal oscillator is bypassed, the user supplies the 19.44 MHz through the CLK19P44\_IO pins.

The operation of the parallel software interface mode is described in [Section 2.5.3.1](#) below. The operation of the serial software interface mode is described in [Section 2.5.3.2](#) below. Timing tables for each of the four clock resynchronization rates are included in [Section 2.5.3.1](#) and [Section 2.5.3.2](#) to aid the user in obtaining optimum microprocessor interface performance.

### 2.5.3.1

#### Parallel Interface Mode

When the M2835x is configured to operate in parallel interface mode (IF\_MODE[1:0] = 10 on power-up), the pins listed in Table 2-25 are then used to configure, control, and monitor the device functions. In addition, refer to Table 2-24 for the hardware pin configurations required during software mode.

#### Operation Notes:

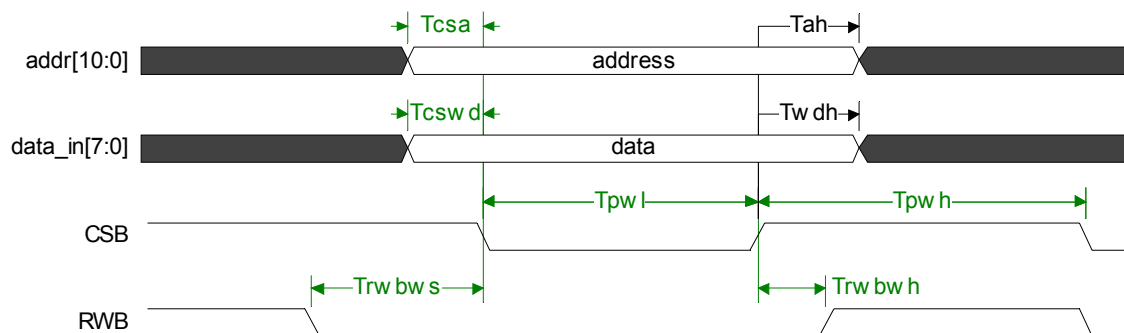
1. The parallel interface does not support Burst access. The chip select (CSB) signal must go inactive (i.e., high) at the end of each read or write cycle.
2. During the read cycle, the read data output drivers are controlled by the chip select (CSB) and the driver output enable (OEB) signals. When both the CSB and OEB are active, the read data output drivers are enabled. When either the CSB or OEB is inactive, the read data output drivers are disabled and go into the high impedance state.
3. The parallel interface register address pin ADDR10 is the most significant bit (MSB) and the pin ADDR0 is the least significant bit (LSB). The interface data pin DATA7 is the MSB and the pin DATA0 is the LSB.

**Table 2-25.** Parallel Mode Interface Control Signals

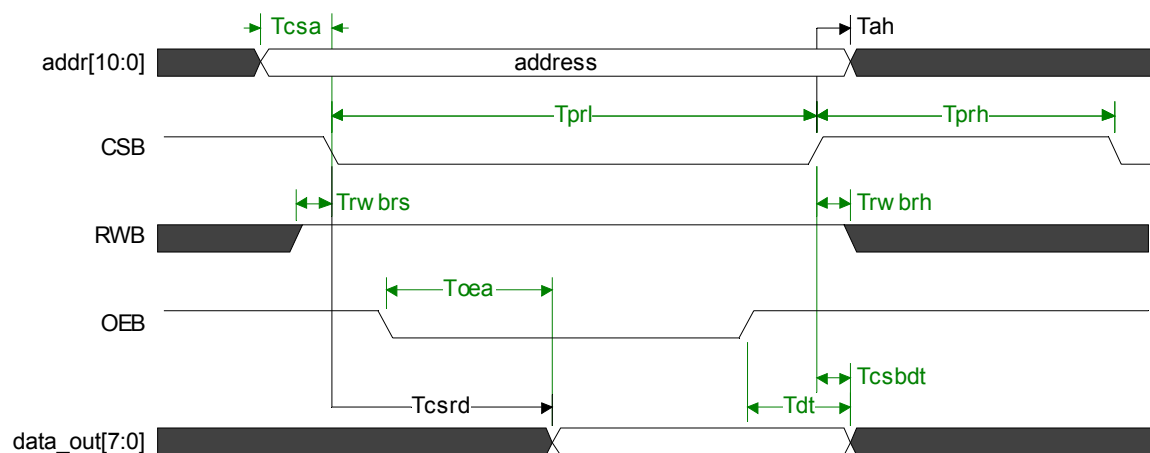
Pin	Function
CSB	Chip select
OEB	Output enable
RWB	Read / Write control
ADDR[10:0]	Register address bus
DATA[7:0]	Data bus

Figure 2-21 and Figure 2-22 (below), illustrate the AC timing for the parallel interface write cycle and read cycle, respectively.

**Figure 2-21. Parallel Mode Write Timing**



**Figure 2-22. Parallel Mode Read Timing**



### 51.84 MHz Parallel AC Interface Timing (Fastest “x\_REFCLK” clock is 51.84 MHz)

Table 2-26 specifies the parallel interface write cycle AC timing for 51.84 MHz.

**Table 2-26. 51.84 MHz Parallel Write Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address setup before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{cswd}$	Write data setup before CSB falling edge	0	
$T_{wdh}$	Write data hold after CSB rising edge	0	
$T_{rwbws}$	RWB low before CSB falling edge	0	
$T_{rwbwh}$	RWB write low hold time after CSB rising edge	0	
$T_{pwl}$	CSB low time in write cycle	59	
$T_{pwh}$	CSB high time in write cycle	59	

Table 2-27 specifies the parallel interface read cycle AC timing for 51.84 MHz.

**Table 2-27. 51.84 MHz Parallel Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address setup before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{csrd}$	Read data valid after CSB falling edge	78	
$T_{oea}$	OEB low before read data valid		10
$T_{dt}$	OEB rising edge before output disabled	3	11
$T_{rwbrs}$	RWB read high setup time before CSB falling edge	0	
$T_{rwbrh}$	RWB read high hold time after CSB rising edge	0	
$T_{csbdt}$	CSB rising edge before output disabled	2.5	7
$T_{prl}$	CSB low time in read cycle	83	
$T_{prh}$	CSB high time in read cycle	83	



#### 44.736 MHz Parallel AC Interface Timing (Fastest “x\_REFCLK” clock is 44.736 MHz)

Table 2-28 specifies the parallel interface write cycle AC timing for 44.736 MHz.

**Table 2-28. 44.736 MHz Parallel Write Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address setup before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{cswd}$	Write data setup before CSB falling edge	0	
$T_{wdh}$	Write data hold after CSB rising edge	0	
$T_{rwbws}$	RWB low before CSB falling edge	0	
$T_{rwbwh}$	RWB write low hold time after CSB rising edge	0	
$T_{pwl}$	CSB low time in write cycle	68	
$T_{pwh}$	CSB high time in write cycle	68	

Table 2-29 specifies the parallel interface read cycle AC timing for 44.736 MHz.

**Table 2-29. 44.736 MHz Parallel Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address setup before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{csrd}$	Read data valid after CSB falling edge	89	
$T_{oea}$	OEB low before read data valid		10
$T_{dt}$	OEB rising edge before output disabled	3	11
$T_{rwbrs}$	RWB read high setup time before CSB falling edge	0	
$T_{rwbrh}$	RWB read high hold time after CSB rising edge	0	
$T_{csbdt}$	CSB rising edge before output disabled	2.5	7
$T_{prl}$	CSB low time in read cycle	94	
$T_{prh}$	CSB high time in read cycle	94	

### 34.368 MHz Parallel AC Interface Timing (Fastest “x\_REFCLK” clock is 34.368 MHz)

Table 2-30 specifies the parallel interface write cycle AC timing for 34.368 MHz.

**Table 2-30. 34.368 MHz Parallel Write Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address setup before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{cswd}$	Write data setup before CSB falling edge	0	
$T_{wdh}$	Write data hold after CSB rising edge	0	
$T_{rwbws}$	RWB low before CSB falling edge	0	
$T_{rwbwh}$	RWB write low hold time after CSB rising edge	0	
$T_{pwl}$	CSB low time in write cycle	88	
$T_{pwh}$	CSB high time in write cycle	88	

Table 2-31 specifies the parallel interface read cycle AC timing for 34.368 MHz.

**Table 2-31. 34.368 MHz Parallel Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address valid before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{csrd}$	Read data valid after CSB falling edge	112	
$T_{oea}$	OEB low before read data valid		10
$T_{dt}$	OEB rising edge before output disabled	3	11
$T_{rwbrs}$	RWB read high setup time before CSB falling edge	0	
$T_{rwbrh}$	RWB read high hold time after CSB rising edge	0	
$T_{csbdt}$	CSB rising edge before output disabled	2.5	7
$T_{prl}$	CSB low time in read cycle	117	
$T_{prh}$	CSB high time in read cycle	117	

### 19.44 MHz Parallel AC Interface Timing (No “x\_REFCLK” clocks are present)

Table 2-32 specifies the parallel interface write cycle AC timing for 19.44 MHz.

**Table 2-32. 19.44 MHz Parallel Write Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address setup before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{cswd}$	Write data setup before CSB falling edge	0	
$T_{wdh}$	Write data hold after CSB rising edge	0	
$T_{rwbws}$	RWB low before CSB falling edge	0	
$T_{rwbwh}$	RWB write low hold time after CSB rising edge	0	
$T_{pwl}$	CSB low time in write cycle	155	
$T_{pwh}$	CSB high time in write cycle	155	

Table 2-33 specifies the parallel interface read cycle AC timing for 19.44 MHz.

**Table 2-33. 19.44 MHz Parallel Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{csa}$	Address setup before CSB falling edge	0	
$T_{ah}$	Address hold after CSB rising edge	0	
$T_{csrd}$	Read data valid after CSB falling edge	191	
$T_{oea}$	OEB low before read data valid		10
$T_{dt}$	OEB rising edge before output disabled	3	11
$T_{rwbrs}$	RWB read high setup time before CSB falling edge	0	
$T_{rwbrh}$	RWB read high hold time after CSB rising edge	0	
$T_{csbdt}$	CSB rising edge before output disabled	2.5	7
$T_{prl}$	CSB low time in read cycle	206	
$T_{prh}$	CSB high time in read cycle	206	

### 2.5.3.2

### Serial Interface Mode

When the M2835x is configured to operate in serial interface mode (IF\_MODE[1:0] = 11 on power-up), the pin listed in [Table 2-34](#) are used to configure, control, and monitor the device functions. In addition, refer to [Table 2-24](#) for the hardware pin configurations required during software mode.

**Table 2-34. Serial Mode Interface Control Signals**

Pin	Function
SCLK	Serial clock from the master device
SDI	Serial data input
SDO	Serial data output
CSB	Chip select

The M2835x serial interface has four operating cycles. The four cycles are the “write address offset” cycle, “read address offset” cycle, “write register data” cycle, and “read register data cycle.” All four cycles have a fixed length of 16 SCLK clock periods. Refer to [Table 2-35](#) below.

The “write address offset” cycle selects the address space to be written or read. There are seven address spaces. They are the global register space and the six channel control register spaces. The “read address offset” cycle reads back the last address offset written during the “write address offset” cycle. The “write register data” cycle selects the device register to be written and it writes data to that register. The “read register data” cycle selects the device register to be read and it reads data from that device registers.

The serial data format is transmitted and received least significant bit (LSB) first and has a standard non-return to zero (NRZ) format. During the serial write operation, data needs to be valid on the SDI pin at the rising edge of SCLK. During the serial read operation, data is valid on the SDO pin at the rising edge of SCLK. (Refer to section [Section 2.5.3.5](#)). Each serial data frame begins with a read/write bit (R\_WB) followed by the register address offset bit (O\_DB). The R\_WB and O\_DB bits select each of the four serial operating cycles as described in [Table 2-35](#)

**Table 2-35. SPI Operational Modes**

R_WB	O_DB	Description
0	0	Write register data. Data is written to the register referenced by the addition of ADD[5:0] and the stored register offset.
0	1	Write address offset. The register address offset is programmed with ADD[19:6] following R_WB and O_DB.
1	0	Read register data. Data is read from the register referenced by the addition of ADD[5:0] and the stored register address offset.
1	1	Read address offset. the register address offset is read with ADD[19:6] following R_WB and O_DB.
<b>NOTE:</b> The R_WB and O_DB bits are the first two bits on the SDI (serial data input) pin that occur immediately following the assertion of the CSB (active low chip select) pin.		

### 2.5.3.3 Serial Write Operation

A serial write operation is used to write M2835x registers. It consists of a Write Address Offset cycle followed by a Write Register Data cycle. Both cycles have a fixed length of 16 SCLK periods.

The Write Address Offset cycle selects the M2835x address space to be written. It selects either the Global register space (0x000) or one of 6 Channel Control register spaces (0x100 through 0x600). Referring to [Figure 2-19](#), which illustrates the Write Address Offset cycle, the bits add6 (LSB) through add10 (MSB) contain the address offset for the selected register space. The bits are set according to [Table 2-36](#). Note that bits add6 and add7 are required to be set to zero (0).

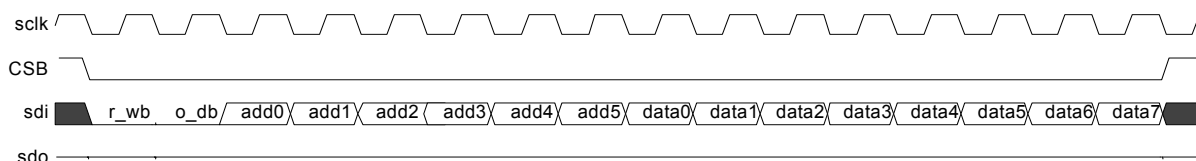
**Table 2-36. Write Address Offset Bits**

Address Space	Address Offset	Address Offset Bits				
		add6	add7	add8	add9	add10
Global Registers	0x000	0	0	0	0	0
Channel 0 Control	0x100	0	0	1	0	0
Channel 1 Control	0x200	0	0	0	1	0
Channel 2 Control	0x300	0	0	1	1	0
Channel 3 Control	0x400	0	0	0	0	1
Channel 4 Control	0x500	0	0	1	0	1
Channel 5 Control	0x600	0	0	0	1	1

Regarding the bits add11 through add19, they are required to be set to zero.

The Write Register Data cycle selects the device address to be written and writes the data to that address. Referring to [Figure 2-24](#), which illustrates the Write Register Data cycle, the bits add0 (LSB) through add5 (MSB) carry the address of the register to be written and bits data0 (LSB) through data7 (MSB) carry the data that will be written to that register. Note that once an address space has been selected by the Write Address Offset cycle, multiple Write Register Data cycles may occur until a different address space needs to be accessed. At that time, another Write Address Offset cycle is required prior to writing a register in the new address space.

For example, to enable only the DJAT PLL lock detect interrupt in the second port (channel no. 1) of the M2835x, set bit 6 to “1” in the Channel Interrupt Enable1 register (3.3.19) for the Channel 1 Control space (i.e., the “Address Offset” plus “Register Address” is 0x219 Hex and the value of 0x40 Hex should be written to the register). In serial interface mode, use the Write Address Offset cycle to select the Channel 1 Control space by setting bits add6 to add10 = 00010 Binary and by setting bits add11 to add19 = 000000000 Binary. Use the Write Register Data cycle to select the register address by setting bits add0 to add5 = 100110 Binary. Within the same Write Register Data cycle, enable the interrupt by setting the data bits data0 to data7 = 00000010 Binary.

**Figure 2-23. Write Address Offset Cycle Timing Diagram****Figure 2-24. Write Register Data Cycle Timing Diagram**

#### 2.5.3.4

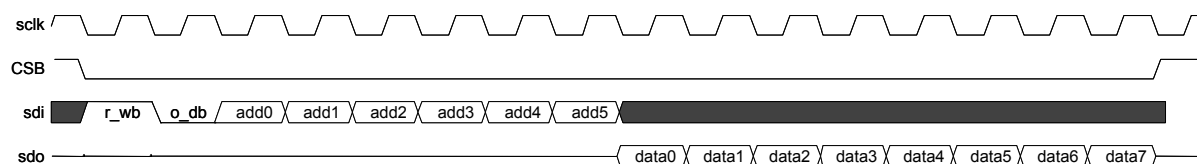
#### Serial Read Operation

The serial read operation is used to read the M2835x registers or to read the currently selected device address space. A Write Address Offset cycle followed by a Read Register Data cycle is used to read the device registers. The Read Address Offset cycle is used to read the last address offset written during the Write Address Offset cycle. Each of the cycles has a fixed length of 16 SCLK periods.

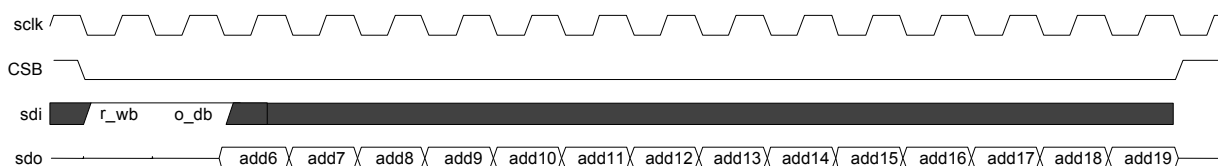
The Write Address Offset cycle selects the address space to be read. It selects either the Global register space (0x000) or one of 6 Channel Control register spaces (0x100 through 0x600). [Figure 2-23](#) illustrates the Write Address Offset cycle.

The Read Register Data cycle selects the register to be read and reads the data in that register. Referring to [Figure 2-25](#), which illustrates the Read Register Data cycle, the eight SDI bits that follow bit add5 are ignored. Note that once an address space has been selected by the Write Address Offset cycle, multiple Read Register Data cycles may occur until a different address space needs to be accessed. At that time, another Write Address Offset cycle is required prior to reading a register in the new address space.

The Read Address Offset cycle is used to read the currently selected device address space (i.e., the last address offset written during the Write Address Offset cycle). Referring to [Figure 2-26](#), which illustrates the Read Address Offset cycle, the fourteen SDI bits that follow the R\_WB and 0\_DB bits are ignored.

**Figure 2-25. Read Register Data Cycle Timing Diagram**

The address offset can be read back by performing a Read Address Offset cycle illustrated in [Figure 2-26](#).

**Figure 2-26. Read Address Offset Cycle Timing Diagram**

### 2.5.3.5

### Serial Mode Write and Read Timing Diagrams

The serial mode timing is specified in the following timing diagram figures and parameter tables. [Figure 2-27](#) specifies the timing relationship of the interface signals for the write serial mode operation. [Figure 2-28](#) specifies the timing relationship of the interface signals for the read serial mode operation. The timing parameters are specified in the following tables: [Table 2-37](#) for a 51.84 MHz serial clock (SCLK), [Table 2-38](#) for a 44.736 MHz SCLK, [Table 2-39](#) for a 34.368 MHz SCLK, and [Table 2-40](#) for a 19.44 MHz SCLK.

Figure 2-27. Serial Mode Write Timing

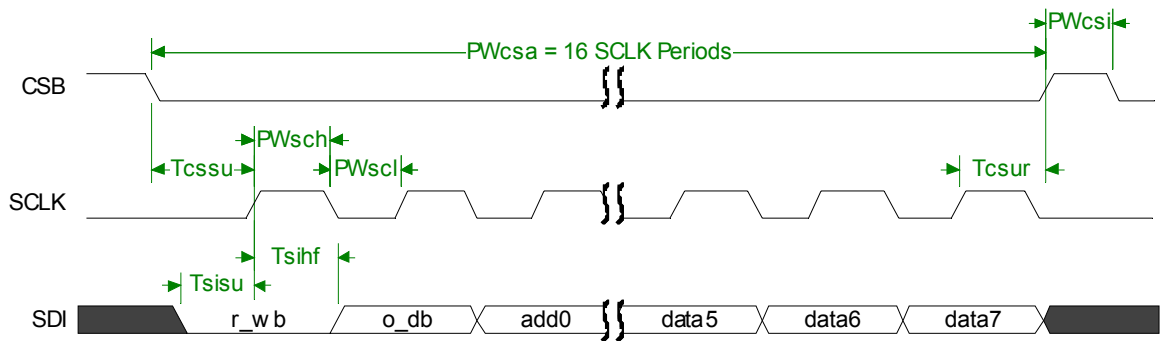
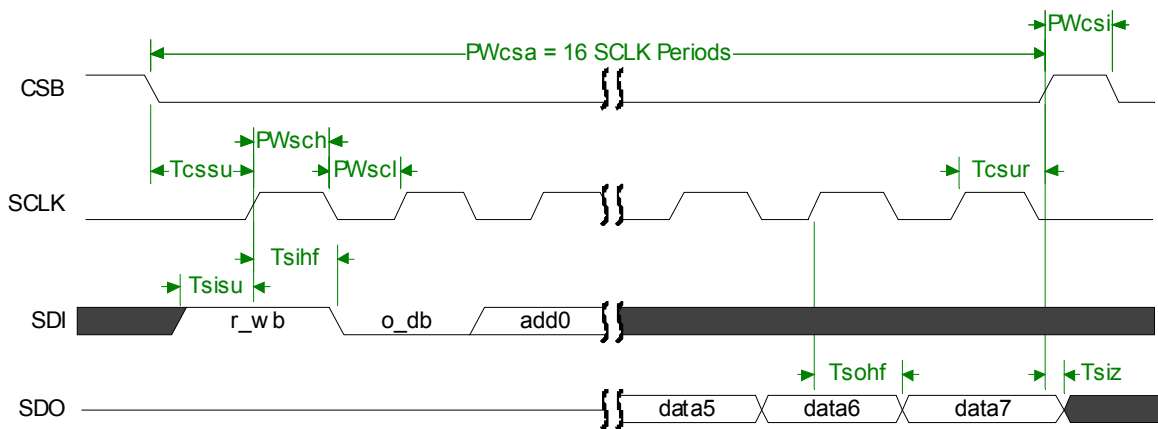


Figure 2-28. Serial Mode Read Timing





### 51.84 MHz Serial AC Interface Timing

Table 2-37 specifies the serial interface write and read cycle AC timing for the 51.84 MHz SCLK.

**Table 2-37. 51.84 MHz Serial Write and Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{cssu}$	CSB setup time to SCLK rising edge	39	
$T_{csur}$	CSB hold time after SCLK rising edge	20	
$PW_{sch}$	Pulse width SCLK high	50	
$PW_{scl}$	Pulse width SCLK low	50	
$T_{sisu}$	SDI setup time to SCLK rising edge	4	
$T_{sihf}$	SDI hold time after SCLK rising edge	0	
$T_{sohf}$	SDO hold time after SCLK rising edge	50	
$T_{siz}$	SDO High Impedance State after CSB inactive	0	59
$PW_{csa}$	CSB active pulse width is fixed at 16 SCLK periods	NA	NA
$PW_{csi}$	CSB inactive pulse width	20	

#### 44.736 MHz Serial AC Interface Timing

Table 2-38 specifies the serial interface write and read cycle AC timing for the 44.736 MHz SCLK.

**Table 2-38. 44.736 MHz Serial Write and Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{cssu}$	CSB setup time to SCLK rising edge	44	
$T_{csur}$	CSB hold time after SCLK rising edge	20	
$PW_{sch}$	Pulse width SCLK high	50	
$PW_{scl}$	Pulse width SCLK low	50	
$T_{sisu}$	SDI setup time to SCLK rising edge	4	
$T_{sihf}$	SDI hold time after SCLK rising edge	0	
$T_{sohf}$	SDO hold time after SCLK rising edge	57	
$T_{siz}$	SDO High Impedance State after CSB inactive	0	66
$PW_{csa}$	CSB active pulse width is fixed at 16 SCLK periods	NA	NA
$PW_{csi}$	CSB inactive pulse width	23	

### 34.368 MHz Serial AC Interface Timing

Table 2-39 specifies the serial interface write and read cycle AC timing for the 34.368 MHz SCLK.

**Table 2-39. 34.368 MHz Serial Write and Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{CSSU}$	CSB setup time to SCLK rising edge	54	
$T_{CSUR}$	CSB hold time after SCLK rising edge	20	
$PW_{SCH}$	Pulse width SCLK high	60	
$PW_{SCL}$	Pulse width SCLK low	60	
$T_{SISU}$	SDI setup time to SCLK rising edge	4	
$T_{SIHF}$	SDI hold time after SCLK rising edge	0	
$T_{SOHF}$	SDO hold time after SCLK rising edge	74	
$T_{SIZ}$	SDO High Impedance State after CSB inactive	0	83
$PW_{CSA}$	CSB active pulse width is fixed at 16 SCLK periods	NA	NA
$PW_{CSI}$	CSB inactive pulse width	30	

### 19.44 MHz Serial AC Interface Timing

Table 2-40 specifies the serial interface write and read cycle AC timing for the 19.44 MHz SCLK.

**Table 2-40. 19.44 MHz Serial Write and Read Cycle Timing Parameters**

Parameter	Description	min (ns)	max (ns)
$T_{cssu}$	CSB setup time to SCLK rising edge	88	
$T_{csur}$	CSB hold time after SCLK rising edge	20	
$PW_{sch}$	Pulse width SCLK high	105	
$PW_{scl}$	Pulse width SCLK low	105	
$T_{sisu}$	SDI setup time to SCLK rising edge	4	
$T_{sihf}$	SDI hold time after SCLK rising edge	0	
$T_{sohf}$	SDO hold time after SCLK rising edge	130	
$T_{siz}$	SDO High Impedance State after CSB inactive	0	139
$PW_{csa}$	CSB active pulse width is fixed at 16 SCLK periods	NA	NA
$PW_{csi}$	CSB inactive pulse width	52	

## 2.6 Pseudo Random Bit Sequence – PRBS

### 2.6.1 Overview

The test pattern generation module employs test pattern generators, and the corresponding error detection module detects mismatches between incoming data stream and the recovered data. Together they generate/detect digital bit patterns for analyzing, evaluating and troubleshooting digital communications systems.

ITU Recommendation 0.151 [5] specifies that a  $2^{23}-1$  PRBS pattern should be used for error and jitter measurements at E3 bit rates (34.368 Mbps). The pattern should be generated in a twenty-three-stage shift register, whose 17<sup>th</sup> and 22<sup>nd</sup> stage outputs are added in a modulo-two addition stage with the result of which fed back into the input of stage zero,

ITU Recommendation 0.151 [5] specifies that a  $2^{15}-1$  PRBS pattern should be used for error and jitter measurements at DS3 bit rates (44.736 Mbps). The pattern should be generated in a fifteen-stage shift register whose 13<sup>th</sup> and 14<sup>th</sup> stage outputs are added in a modulo-two addition stage with the result of which fed back into the input of stage zero.

In order to improve testability, error insertion capability is available. This function can deliberately make one bit error into the data stream, [Section 2.6.4 Error Insertion](#).

- Programmable polynomial length, it can be up to 32 bits
- Programmable feedback tap, it can be up to 32 bits
- Unframed patterns (PRBS & fixed pattern) for generator
- Unframed pattern (PRBS & fixed pattern) detector
- $2^{20}-1$  (QRSS) with the choice of suppressing more than 14 consecutive zeroes
- Detector will reseed if 32 consecutive zeroes are detected or error is found in the first 96 bits
- DS3 bit rate (44.736Mbps) and E3 bit rate (34.368Mbps)
- Programmable user-defined pattern and length for the generation of any fixed pattern up to 32 bits in length
- Test error insertion single bit or at a fixed rate

### 2.6.2 Configuration and Control

Each PRBS block can be configured as a pattern generator, detector or bypassed by setting the bits [6:5] in the RXPRBS\_CTRL1 and TXPRBS\_CTRL1 registers, address offsets 0xn1F and 0xn41 respectively as described in [Table 2-41](#).

**NOTE:** When changing patterns, the PRBS block must be disabled.

**Table 2-41. PRBS Control**

<b>TXMODE_SEL[1:0] RXMODE_SEL[1:0]</b>	<b>Description</b>
00	PRBS generator and detector are both disabled, incoming data are passed through – default
01	PRBS generator is enabled
10	PRBS detector is enabled, incoming data are passed through
11	PRBS generator and detector are both disabled, incoming data are passed through

When using the PRBS generator on the receive side of the channel, the transmit side must be set up as the detector and vice versa. The counters for BER, LCV, EXZ, etc., are shared between the two sides of the channel.

The receive generator will produce PRBS patterns that are sent out through the digital portion of the M2835x via RPOS<sub>n</sub> / RNEG<sub>n</sub> / RCLK<sub>n</sub> pins. The transmit detector then expects to see the pattern on TPOS<sub>n</sub> / TNEG<sub>n</sub> / TCLK<sub>n</sub> pins.

Using the transmit generator will send the PRBS patterns out through the analog side of the M2835x via TX\_LINEP<sub>n</sub> / TX\_LINEM<sub>n</sub> pins. In this case, the receive detector expects the pattern to be looped back to RX\_LINEP<sub>n</sub> / RX\_LINEM<sub>n</sub> pins.

The PRBS blocks are each controlled by an enable bit. TXPRBS\_EN, bit 0 in register TXPRBS\_CTRL1 controls the TX PRBS block, and RXPRBS\_EN, bit 0 in register RXPRBS\_CTRL1 controls the RX PRBS block. The enable bit must be written to 1 to enable PRBS operation after the other PRBS registers have been configured. With the enable bit set to 0, data is passed through unaffected.

**Table 2-42. PRBS Enable**

<b>TXPRBS_EN RXPRBS_EN</b>	<b>Description</b>
0	PRBS generator/detector block is disabled, incoming data are passed through
1	PRBS generator/detector block is enabled.

## 2.6.3 User Specified Patterns

The pattern generator can be configured to generate or detect pseudorandom patterns or repetitive patterns as described in [Table 2-43](#).

**Table 2-43. PRBS Pattern Configuration**

<b>TXPAT_CTRL RXPAT_CTRL</b>	<b>Description</b>
0	Fixed pattern generator
1	PRBS pattern generator

The user defined patterns can be up to 32 bits long and entered in registers address offsets 0xn26:0xn29 for the RXUSR\_PATn and 0xn48:0xn4B for TXUSR\_PATn. When this mode is selected, the fixed pattern is repeated continuously.

**NOTE:**

After defining the pattern to use, but before loading the pattern, the RXTAPA[4:0] / TXTAPA[4:0] bits in the RXPRBS\_CTRL2 and TXPRBS\_CTRL2 registers at offsets 0xn20 and 0xn42, respectively, need to be loaded with the pattern length minus one.

## 2.6.4 Error Insertion

For error insertion, there is two built-in capabilities. The first is a single error insertion, which will insert only one error when the RXERRIN or TXERRIN bits are set, bit 4 in the RXPRBS\_CTRL1 and TXPRBS\_CTRL1 control registers.

The second is the insertion of errors at a regular rate determined by the value of RXAER[2:0] and TXAER[2:0], bits [5:3] in registers RXPRBS\_CTRL0 and TXPRBS\_CTRL0. Refer to [Table 2-44](#). Error Insertion Rates. As an example, when set for the insertion rate  $0x1 - 10^{-1}$ , 1 in 10 bits will be in error, the insertion rate  $0x2 - 10^{-2}$  yields 1 in a 100 bits will be errored, etc.

**Table 2-44. Error Insertion Rates**

RXAER[2:0] TXAER[2:0]	Error Insertion Rate
000	No errors inserted
001	$10^{-1}$
010	$10^{-2}$
011	$10^{-3}$
100	$10^{-4}$
101	$10^{-5}$
110	$10^{-6}$
111	$10^{-7}$

## 2.7 JTAG

The JTAG (Joint Test Action Group) interface will fulfill the requirements of IEEE 1149.1a-1993. This interface is predominantly used for board test, and it should consist of a minimum of 5 pins: Boundary Scan Data Input (BSTDI), Boundary Scan Data Output (BSTDO), Boundary Scan Clock (BSTCLK), Boundary Scan TAP (Test Access Port) controller input (BSTMS), and Boundary Scan Reset (BSTRST). Controller instructions supported should include BYPASS, SAMPLE / PRELOAD, EXTEST, IDCODE, and HIGHZ. Only digital input/output/bidirectional pins should be included in the boundary scan chain.



## 2.8 Interrupts

### 2.8.1 General Structure

The INTR\_N output pin is an active-low output that provides a common interrupt request for all of the interrupt sources in the device. A global interrupt enable bit enables interrupts to drive the INTR\_N pin low. A two level interrupt structure is the source of interrupts that drive the INTR\_N pin when the interrupts in the structure are enabled. The processor must read the low-level interrupt status register to clear all latched interrupt bits associated with a channel. The processor must read the TXMONINTSTAT interrupt status register to clear all transmit monitoring latched interrupt bits.

Figure 2-29 shows the interrupt structure within the M2835x. It provides an example of the interrupt structure. It does not show all of the interrupt status registers nor all of the interrupt enable registers.

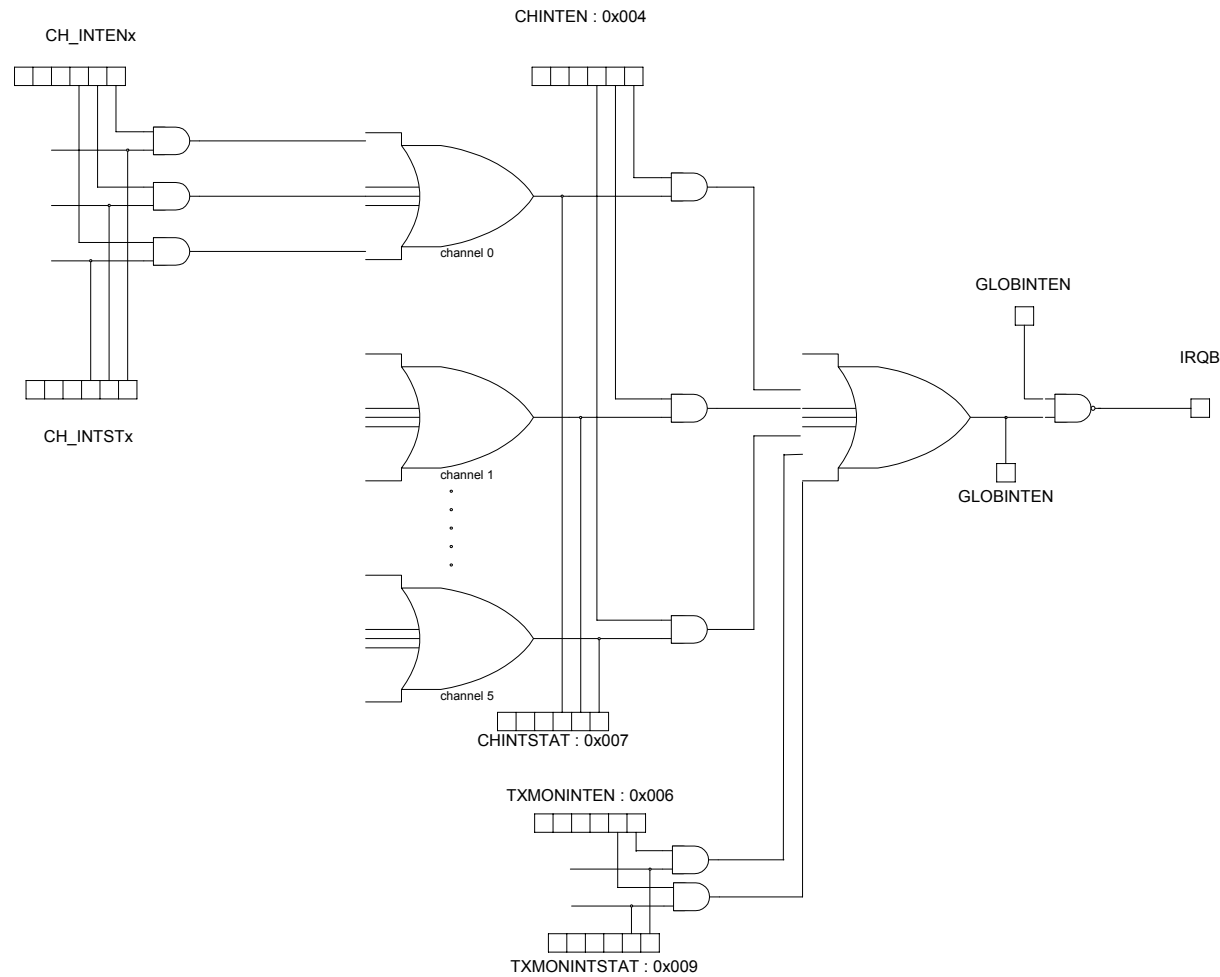
#### 2.8.1.1 Low-Level Interrupts

The low-level interrupt status registers are CH\_INTST0, CH\_INTST1, CH\_INTST2, CH\_INTST3, and CH\_INTST4. The low-level interrupt enable registers are CH\_INTEN0, CH\_INTEN1, CH\_INTEN2, and CH\_INTEN3. The bits in the four low-level interrupt enable registers control the masking of the bits in the five low-level interrupt status registers. Each interrupt enable bit unmask its interrupt when the enable bit is set to one (1) allowing the interrupt to pass to its top-level interrupt. When the enable bit is set to zero (0), the interrupt will be masked and will not be detected by its top-level interrupt. All of the low-level interrupts in a channel are logically ORed together to generate a single top-level channel interrupt. All of the low-level interrupt status bits are latched and processor must read the interrupt status register to clear all the latched bits.

#### 2.8.1.2 Top-Level Interrupts

The top-level interrupt status registers are CHINTSTAT and TXMONINTSTAT. The top-level interrupt enable registers are CHINTEN and TXMONINTEN. The bits in the top-level interrupt enable registers control the masking of the bits in the top-low-level interrupt status registers. The top-level interrupts consists of up to six channel interrupts with bit indications in the CHINTSTAT register, one for each channel in the device, and two transmit monitoring interrupts with bit indications in the TXMONINTSTAT register. The transmit monitoring interrupts are the TOPEN interrupt and the TLOS interrupt. They provide the TOPEN and TLOS interrupt status from the Transmit Monitoring block. Each channel interrupt status bit provides a common interrupt indication for all of the low-level interrupts in the channel. Each interrupt enable bit unmask its interrupt when the enable bit is set to one (1) allowing the interrupt to drive the INTR\_N pin if the global interrupt is enabled. When the interrupt enable bit is set to zero (0), the interrupt will be masked and will not drive the INTR\_N pin even if the global interrupt is enabled. All of the top-level interrupts are logically ORed together to generate a single interrupt that drives the INTR\_N pin when the global interrupt is enabled. The TXMONINTSTAT interrupt status bits are latched and processor must read this register to clear all the latched bits. The CHINTSTAT interrupt status bits are not latched, and the processor must read the corresponding low-level interrupt status registers to clear bits in the CHINTSTAT register.

Figure 2-29. Interrupt Structure



## 2.9 Loopbacks

The M2835x provides a complete set of loopbacks for diagnostics, maintenance, and troubleshooting of each channel. There are three (3) loopback modes available, line (remote) loopback, source (local) loopback, and analog loopback. All loopbacks perform clock and data switching, if necessary. The activation and deactivation of a specific loopback is done through programmable control bits.

**NOTE:**

There are no priorities for the loopbacks. It is possible to place the device in a closed loop where there is no running clock, i.e. a line (remote) loopback in conjunction with a source loopback. This must be avoided.

### 2.9.1 Line (Remote) Loopback

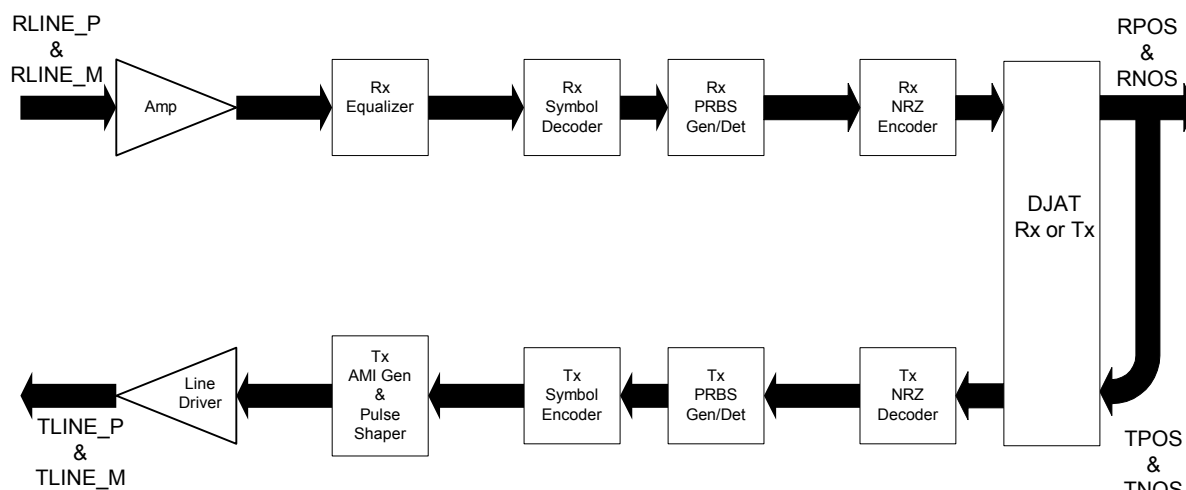
The receive data is retimed after clock recovery, but not decoded, is looped back into the AMI generator in place of the transmit data.

**NOTE:**

When AIS generation is enabled, the AIS signal will overwrite the data through the TX path.

To place the device into the line (remote) loopback mode, the LB0\_EN is set, bit 1 in the CH\_CTRL1 register at address offset 0xn01.

**Figure 2-30. Line (Remote) Loopback**



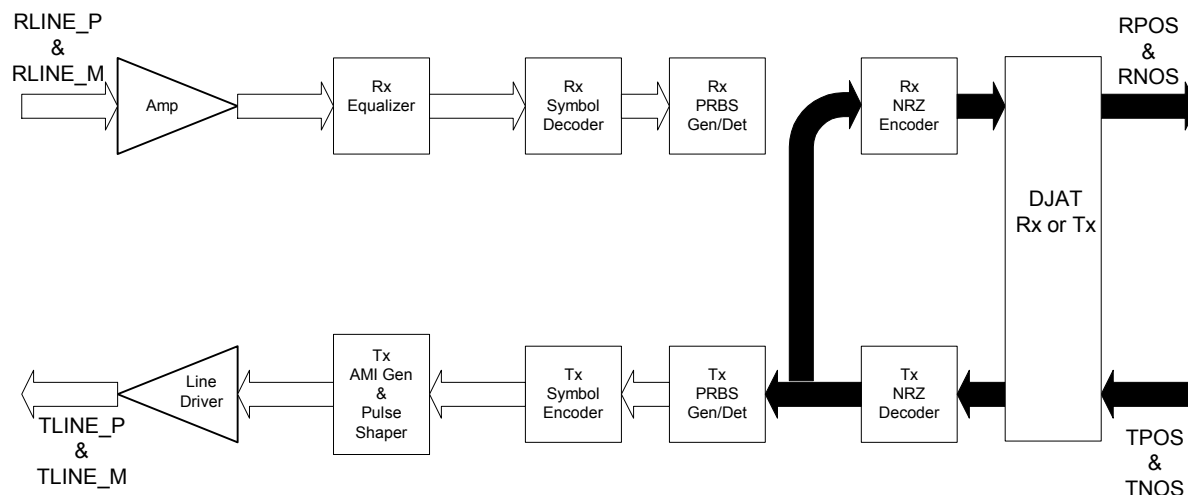
## 2.9.2 Source (Local) Loopback

The transmit data is looped back into the receive data path in lieu of the received data on the line side of the device.

**NOTE:** When AIS generation is enabled, the AIS signal will overwrite the data through the TX path.

To place the device into the source (local) loopback mode, the LB1\_EN is set, bit 2 in the CH\_CTRL1 register at address offset 0xn01.

**Figure 2-31. Source (Local) Loopback**



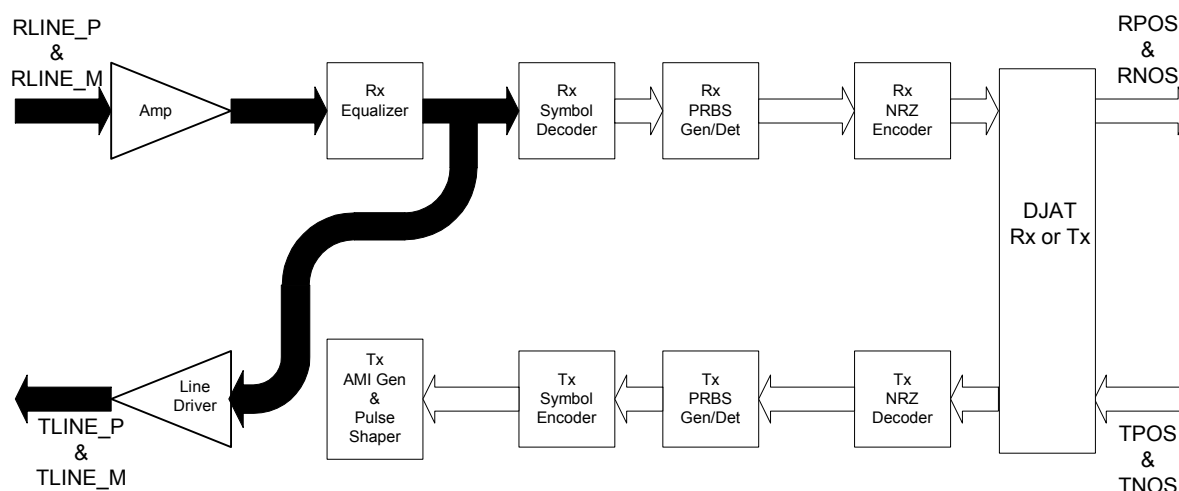
## 2.9.3 Analog Loopback

The receive data is looped back into the transmit data path without retiming.

**NOTE:** If AIS generation is enabled, the receive data will overwrite the AIS signal generated.

To place the device into the analog loopback mode, the TXMUX[1:0] must be set to 11, bits 3:2 in the TX\_ANACTRL register at address offset 0xn02, **and** the RXMUX[1:0] must be set to 10, bits 2:1 in the RX\_ANACTRL register at address offset 0xn06.

**Figure 2-32. Analog Loopback**







## 3.0 Registers

### 3.1 Register Map



Reserved registers and reserved bits must not be modified

**NOTE:**

For –11 devices only: refer to product bulletin XXXXXXXX.

**NOTE:**

To properly read device counters with multiple registers, the least significant byte must be read first. This will latch the remaining higher order bytes and preserve the correct counts.

#### 3.1.1 Register Partitioning

**Table 3-1. Register Partitioning for 6 Port Device**

Address	Name	Address	Name
0x000 – 0x07F	Global Register Space	0x080 – 0x0FF	Reserved
0x100 – 0x17F	Channel 0 Control	0x180 – 0x1FF	Reserved
0x200 – 0x27F	Channel 1 Control	0x280 – 0x2FF	Reserved
0x300 – 0x37F	Channel 2 Control	0x380 – 0x3FF	Reserved
0x400 – 0x47F	Channel 3 Control	0x480 – 0x4FF	Reserved
0x500 – 0x57F	Channel 4 Control	0x580 – 0x5FF	Reserved
0x600 – 0x67F	Channel 5 Control	0x680 – 0x6FF	Reserved
0x700 – 0xFFFF	Not used		

**Table 3-2. Register Partitioning for 2/3/4 Port Devices**

Address	Name	Address	Name
0x000 – 0x07F	Global Register Space	0x080 – 0x0FF	Reserved
0x100 – 0x17F	Channel 0 Control	0x180 – 0x1FF	Reserved
0x200 – 0x27F	Channel 1 Control	0x280 – 0x2FF	Reserved
0x300 – 0x37F	Reserved	0x380 – 0x3FF	Reserved
0x400 – 0x47F	Reserved	0x480 – 0x4FF	Reserved
0x500 – 0x57F	Channel 2 Control	0x580 – 0x5FF	Reserved
0x600 – 0x67F	Channel 3 Control	0x680 – 0x6FF	Reserved
0x700 – 0xFFF	Not Used		



## 3.1.2 Register Tables

**Table 3-3. Global Control Register Table - Alpha by Register Name (1 of 2)**

Address	Name	Description	Default	Page
0x03D ~ 0x03F	Reserved		NA	
0x004	CHINTEN	Channel [0:5] interrupts enable	0x00	<a href="#">page 3-17</a>
0x007	CHINTSTAT	Channel [0:5] interrupt status	NA	<a href="#">page 3-19</a>
0x030	CLADDS3CTRL1	CLADDS3 control1	0x3F	<a href="#">page 3-28</a>
0x037	CLADDS3FSMSTAT	CLADDS3 FSM status	NA	<a href="#">page 3-29</a>
0x035	CLADDS3MON2	CLADDS3 monitor2	NA	<a href="#">page 3-29</a>
0x040	CLADE3CTRL1	CLADE3 control1	0x3F	<a href="#">page 3-29</a>
0x047	CLADE3FSMSTAT	CLADE3 FSM status	NA	<a href="#">page 3-30</a>
0x045	CLADE3MON2	CLADE3 monitor2	NA	<a href="#">page 3-30</a>
0x020	CLADSTS1CTRL1	CLADSTS1 control1	0x3F	<a href="#">page 3-28</a>
0x027	CLADSTS1FSMSTAT	CLADSTS1 FSM status	NA	<a href="#">page 3-28</a>
0x025	CLADSTS1MON2	CLADSTS1 monitor2	NA	<a href="#">page 3-28</a>
0x000	DEVID		0x5x	<a href="#">page 3-15</a>
0x003	GLOBCTRL	Global control	0x00	<a href="#">page 3-16</a>
0x015	HWCTRL	Hardware control	NA	<a href="#">page 3-27</a>
0x01D ~ 0x01F	Not used		0x00	
0x02D ~ 0x02F	Not used		0x00	
0x04D ~ 0x07F	Not used		0x00	
0x014	Reserved		NA	
0x016 ~ 0x1C	Reserved		NA	
0x021 ~ 0x024	Reserved		NA	
0x026	Reserved		NA	
0x028 ~ 0x02C	Reserved		NA	
0x031 ~ 0x034	Reserved		NA	
0x036	Reserved		NA	
0x038 ~ 0x03C	Reserved		NA	
0x041 ~ 0x044	Reserved		NA	
0x046	Reserved		NA	
0x048 ~ 0x04C	Reserved		NA	

**Table 3-3. Global Control Register Table - Alpha by Register Name (2 of 2)**

Address	Name	Description	Default	Page
0x005	Reserved		NA	
0x008	Reserved		NA	
0x002	REVID	Revision ID	TBD	<a href="#">page 3-15</a>
0x00A	SECTIMCTRL	Onesec timer control	0x00	<a href="#">page 3-20</a>
0x00B	SECTIMCYCLE0	Onesec timer cycle [7:0]	0x00	<a href="#">page 3-21</a>
0x00C	SECTIMCYCLE1	Onesec timer cycle [15:8]	0x04	<a href="#">page 3-21</a>
0x00D	SECTIMCYCLE2	Onesec timer cycle [23:16]	0x17	<a href="#">page 3-22</a>
0x00E	SECTIMCYCLE3	Onesec timer cycle [31:24]	0x03	<a href="#">page 3-22</a>
0x00F	TLOS_CONTROL	TLOS control	0x0F	<a href="#">page 3-23</a>
0x010	TMON_ANACTRL1	TX monitor analog control1	0x06	<a href="#">page 3-24</a>
0x011	TMON_ANACTRL2	TX monitor analog control2	0x28	<a href="#">page 3-25</a>
0x012	TMON_ANACTRL3	TX monitor analog control3	0x07	<a href="#">page 3-26</a>
0x013	TXJITTER	TX jitter demodulator control	0x00	<a href="#">page 3-26</a>
0x006	TXMONINTEN	Extended TX monitor interrupt enable	0x00	<a href="#">page 3-18</a>
0x009	TXMONINTSTAT	Extended TX monitor interrupt status	NA	<a href="#">page 3-19</a>

**Table 3-4. Global Control Register Table - Numeric by Register Address (1 of 2)**

Address	Name	Description	Default	Page
0x000	DEVID		0x5x	<a href="#">page 3-15</a>
0x002	REVID	Revision ID	TBD	<a href="#">page 3-15</a>
0x003	GLOBCTRL	Global control	0x00	<a href="#">page 3-16</a>
0x004	CHINTEN	Channel [0:5] interrupts enable	0x00	<a href="#">page 3-17</a>
0x005	Reserved		NA	
0x006	TXMONINTEN	Extended TX monitor interrupt enable	0x00	<a href="#">page 3-18</a>
0x007	CHINTSTAT	Channel [0:5] interrupt status	NA	<a href="#">page 3-19</a>
0x008	Reserved		NA	
0x009	TXMONINTSTAT	Extended TX monitor interrupt status	NA	<a href="#">page 3-19</a>
0x00A	SECTIMCTRL	Onesec timer control	0x00	<a href="#">page 3-20</a>
0x00B	SECTIMCYCLE0	Onesec timer cycle [7:0]	0x00	<a href="#">page 3-21</a>
0x00C	SECTIMCYCLE1	Onesec timer cycle [15:8]	0x04	<a href="#">page 3-21</a>
0x00D	SECTIMCYCLE2	Onesec timer cycle [23:16]	0x17	<a href="#">page 3-22</a>
0x00E	SECTIMCYCLE3	Onesec timer cycle [31:24]	0x03	<a href="#">page 3-22</a>
0x00F	TLOS_CONTROL	TLOS control	0x0F	<a href="#">page 3-23</a>
0x010	TMON_ANACTRL1	TX monitor analog control1	0x06	<a href="#">page 3-24</a>
0x011	TMON_ANACTRL2	TX monitor analog control2	0x28	<a href="#">page 3-25</a>
0x012	TMON_ANACTRL3	TX monitor analog control3	0x07	<a href="#">page 3-26</a>
0x013	TXJITTER	TX jitter demodulator control	0x00	<a href="#">page 3-26</a>
0x014	Reserved		NA	
0x015	HWCTRL	Hardware control	NA	<a href="#">page 3-27</a>
0x016 ~ 0x1C	Reserved		NA	
0x01D ~ 0x01F	Not used		0x00	
0x020	CLADSTS1CTRL1	CLADSTS1 control1	0x3F	<a href="#">page 3-28</a>
0x021 ~ 0x024	Reserved		NA	
0x025	CLADSTS1MON2	CLADSTS1 monitor2	NA	<a href="#">page 3-28</a>
0x026	Reserved		NA	
0x027	CLADSTS1FSMSTAT	CLADSTS1 FSM status	NA	<a href="#">page 3-28</a>
0x028 ~ 0x02C	Reserved		NA	

**Table 3-4. Global Control Register Table - Numeric by Register Address (2 of 2)**

Address	Name	Description	Default	Page
0x02D ~ 0x02F	Not used		0x00	
0x030	CLADDS3CTRL1	CLADDS3 control1	0x3F	<a href="#">page 3-28</a>
0x031 ~ 0x034	Reserved		NA	
0x035	CLADDS3MON2	CLADDS3 monitor2	NA	<a href="#">page 3-29</a>
0x036	Reserved		NA	
0x037	CLADDS3FSMSTAT	CLADDS3 FSM status	NA	<a href="#">page 3-29</a>
0x038 ~ 0x03C	Reserved		NA	
0x03D ~ 0x03F	Reserved		NA	
0x040	CLADE3CTRL1	CLADE3 control1	0x3F	<a href="#">page 3-29</a>
0x041 ~ 0x044	Reserved		NA	
0x045	CLADE3MON2	CLADE3 monitor2	NA	<a href="#">page 3-30</a>
0x046	Reserved		NA	
0x047	CLADE3FSMSTAT	CLADE3 FSM status	NA	<a href="#">page 3-30</a>
0x048 ~ 0x04C	Reserved		NA	
0x04D ~ 0x07F	Not used		0x00	

**Table 3-5. Global Test Register Table**

Address	Label	Name	Default	Group
0x080	Reserved		NA	
0x081~0x09F	Not used		0x00	
0x0A0 ~ 0x0AD	Reserved		NA	
0x0AE	Not used		0x00	
0x0AF ~ 0x0BD	Reserved		NA	
0x0BE	Not used		0x00	
0x0BF ~ 0x0CD	Reserved		NA	
0x0CE	Not used		0x00	
0x0CF	Reserved		NA	
0x0D0 ~ 0x0FF	Not used		0x00	

**Table 3-6. Channel Control Register Table - Alpha by Register Name (1 of 4)**

Address	Name	Description	Default	Page
0xn38	BPVCNT_ST0	BPV counter [7:0] status	NA	<a href="#">page 3-58</a>
0xn39	BPVCNT_ST1	BPV counter [15:8] status	NA	<a href="#">page 3-58</a>
0xn3A	BPVCNT_ST2	BPV counter [23:16] status	NA	<a href="#">page 3-59</a>
0xn00	CH_CTRL0	Channel control0	0x05	<a href="#">page 3-32</a>
0xn01	CH_CTRL1	Channel control1	0x01	<a href="#">page 3-33</a>
0xn18	CH_INTEN0	Channel interrupt enable0	0x00	<a href="#">page 3-45</a>
0xn19	CH_INTEN1	Channel interrupt enable1	0x00	<a href="#">page 3-46</a>
0xn1A	CH_INTEN2	Channel interrupt enable2	0x00	<a href="#">page 3-47</a>
0xn1B	CH_INTEN3	Channel interrupt enable3	0x00	<a href="#">page 3-48</a>
0xn14	CH_INTST0	Channel interrupt status0	NA	<a href="#">page 3-42</a>
0xn15	CH_INTST1	Channel interrupt status1	NA	<a href="#">page 3-43</a>
0xn16	CH_INTST2	Channel interrupt status2	NA	<a href="#">page 3-44</a>
0xn23	CH_INTST3	RX path PRBS interrupt status	NA	<a href="#">page 3-52</a>
0xn45	CH_INTST4	TX path PRBS interrupt status	NA	<a href="#">page 3-63</a>
0xn11	CH_LST1	Channel live status1	NA	<a href="#">page 3-41</a>
0xn12	CH_LST2	Channel live status2	NA	<a href="#">page 3-41</a>
0xn57	COI_CTRL	COI control	0x00	<a href="#">page 3-68</a>
0xn58	COI_OFFSET1	COI status1	NA	<a href="#">page 3-69</a>
0xn59	COI_OFFSET2	COI status2	NA	<a href="#">page 3-69</a>
0xn3C	EXZCNT_ST0	EXZ counter [7:0] status	NA	<a href="#">page 3-59</a>
0xn3D	EXZCNT_ST1	EXZ counter [15:8] status	NA	<a href="#">page 3-59</a>
0xn3E	EXZCNT_ST2	EXZ counter [23:16] status	NA	<a href="#">page 3-59</a>
0xn5B	JATCTRL0	DJAT control 0	0x0F	<a href="#">page 3-70</a>
0xn5F	JATMON2	DJAT Monitor 2	NA	<a href="#">page 3-70</a>
0xn61	JATnCTRL1	DJAT Control n1	0x00	<a href="#">page 3-71</a>
0xn24	LCV_CTRL0	LCV counter control0	0x1F	<a href="#">page 3-53</a>
0xn25	LCV_CTRL1	LCV counter control1	0x00	<a href="#">page 3-54</a>
0xn34	LCVCNT1_ST0	LCV counter [7:0] status	NA	<a href="#">page 3-57</a>
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				

**Table 3-6. Channel Control Register Table - Alpha by Register Name (2 of 4)**

Address	Name	Description	Default	Page
0xn35	LCVCNT1_ST1	LCV counter [7:0] status	NA	<a href="#">page 3-58</a>
0xn36	LCVCNT1_ST2	LCV counter [7:0] status	NA	<a href="#">page 3-58</a>
0xn13	Not used		0x00	
0xn17	Not used		0x00	
0xn1D	Not used		0x00	
0xn2A	Not used		0x00	
0xn2B	Not used		0x00	
0xn37	Not used		0x00	
0xn3B	Not used		0x00	
0xn3F	Not used		0x00	
0xn46	Not used		0x00	
0xn54	Not used		0x00	
0xn5A	Not used		0x00	
0xn07	Reserved		NA	
0xn09	Reserved		NA	
0xn0D ~ 0xn0E	Reserved		NA	
0xn10	Reserved		NA	
0xn5C	Reserved		NA	
0xn5D ~ 0xn6E	Reserved		NA	
0xn70 ~ 0xnCF	Reserved		NA	
0xn56	RLOS_CTRL	RLOS control	0x00	<a href="#">page 3-68</a>
0xn06	RX_ANACTRL	RX path analog control	0x17	<a href="#">page 3-37</a>
0xn05	RX_DC	RX DC status	NA	<a href="#">page 3-36</a>
0xn0C	RX_EQCAP	RX path equalization coefficient status	NA	<a href="#">page 3-39</a>
0xn0A	RX_MISC0	RX path miscellaneous control0	0x00	<a href="#">page 3-38</a>
0xn0B	RX_MISC1	RX path miscellaneous control1	0x02	<a href="#">page 3-39</a>
0xn0F	RX_ST	RX/TX path status	NA	<a href="#">page 3-40</a>
0xn08	RX_VGAGAINOUT	RX path VGA gain out status	NA	<a href="#">page 3-38</a>
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				

**Table 3-6. Channel Control Register Table - Alpha by Register Name (3 of 4)**

Address	Name	Description	Default	Page
0xn2C	RXBECNT_ST0	RX path Bit Error counter[7:0] status	NA	<a href="#">page 3-55</a>
0xn2D	RXBECNT_ST1	RX path Bit Error counter[15:8] status	NA	<a href="#">page 3-56</a>
0xn2E	RXBECNT_ST2	RX path Bit Error counter[23:16] status	NA	<a href="#">page 3-56</a>
0xn2F	RXBECNT_ST3	RX path Bit Error counter[31:24] status	NA	<a href="#">page 3-56</a>
0xn30	RXBITCNT_ST0	RX path bit counter [7:0] status	NA	<a href="#">page 3-56</a>
0xn31	RXBITCNT_ST1	RX path bit counter [15:8] status	NA	<a href="#">page 3-57</a>
0xn32	RXBITCNT_ST2	RX path bit counter [23:16] status	NA	<a href="#">page 3-57</a>
0xn33	RXBITCNT_ST3	RX path bit counter [31:24] status	NA	<a href="#">page 3-57</a>
0xn1C	RXENDEC_CTRL	RX path encoder/decoder control	0x06	<a href="#">page 3-49</a>
0xn1E	RXPRBS_CTRL0	RX path PRBS control0	0x00	<a href="#">page 3-50</a>
0xn1F	RXPRBS_CTRL1	RX path PRBS control1	0x02	<a href="#">page 3-50</a>
0xn20	RXPRBS_CTRL2	RX path PRBS control2	0x16	<a href="#">page 3-50</a>
0xn21	RXPRBS_CTRL3	RX path PRBS control3	0x11	<a href="#">page 3-51</a>
0xn22	RXPRBS_CTRL4	RX path PRBS control4	0x00	<a href="#">page 3-51</a>
0xn26	RXUSR_PAT0	RX path fixed pattern [7:0]	0x00	<a href="#">page 3-54</a>
0xn27	RXUSR_PAT1	RX path fixed pattern [15:8]	0x00	<a href="#">page 3-55</a>
0xn28	RXUSR_PAT2	RX path fixed pattern [23:16]	0x00	<a href="#">page 3-55</a>
0xn29	RXUSR_PAT3	RX path fixed pattern [31:24]	0x00	<a href="#">page 3-55</a>
0xn03	TX_AMI	TX path AMI control	0x05	<a href="#">page 3-35</a>
0xn02	TX_ANACTRL	TX path analog control	0x71	<a href="#">page 3-34</a>
0xn04	TX_LD	TX path LD control	0x64	<a href="#">page 3-36</a>
0xn47	TXAIS_CTRL	TX AIS control	0x00	<a href="#">page 3-64</a>
0xn4C	TXBECNT_ST0	TX path Bit Error counter[7:0] status	NA	<a href="#">page 3-65</a>
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				

**Table 3-6. Channel Control Register Table - Alpha by Register Name (4 of 4)**

Address	Name	Description	Default	Page
0xn4D	TXBECNT_ST1	TX path Bit Error counter[15:8] status	NA	<a href="#">page 3-65</a>
0xn4E	TXBECNT_ST2	TX path Bit Error counter[23:16] status	NA	<a href="#">page 3-66</a>
0xn4F	TXBECNT_ST3	TX path Bit Error counter[31:24] status	NA	<a href="#">page 3-66</a>
0xn50	TXBITCNT_ST0	TX path bit counter [7:0] status	NA	<a href="#">page 3-66</a>
0xn51	TXBITCNT_ST1	TX path bit counter [15:8] status	NA	<a href="#">page 3-66</a>
0xn52	TXBITCNT_ST2	TX path bit counter [23:16] status	NA	<a href="#">page 3-67</a>
0xn53	TXBITCNT_ST3	TX path bit counter [31:24] status	NA	<a href="#">page 3-67</a>
0xn55	TXENDEC_CTRL	TX encoder/decoder control	0x05	
0xn40	TXPRBS_CTRL0	TX path PRBS control0	0x00	<a href="#">page 3-60</a>
0xn41	TXPRBS_CTRL1	TX path PRBS control1	0x02	<a href="#">page 3-61</a>
0xn42	TXPRBS_CTRL2	TX path PRBS control2	0x16	<a href="#">page 3-61</a>
0xn43	TXPRBS_CTRL3	TX path PRBS control3	0x11	<a href="#">page 3-62</a>
0xn44	TXPRBS_CTRL4	TX path PRBS control4	0x00	<a href="#">page 3-62</a>
0xn48	TXUSR_PAT0	TX path fixed pattern [7:0]	0x00	<a href="#">page 3-64</a>
0xn49	TXUSR_PAT1	TX path fixed pattern [15:8]	0x00	<a href="#">page 3-64</a>
0xn4A	TXUSR_PAT2	TX path fixed pattern [23:16]	0x00	<a href="#">page 3-65</a>
0xn4B	TXUSR_PAT3	TX path fixed pattern [31:24]	0x00	<a href="#">page 3-65</a>
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				



**Table 3-7. Channel Control Register Table - Numeric by Register Address (1 of 4)**

Address	Name	Description	Default	Page
0xn00	CH_CTRL0	Channel control0	0x05	<a href="#">page 3-32</a>
0xn01	CH_CTRL1	Channel control1	0x01	<a href="#">page 3-33</a>
0xn02	TX_ANACTRL	TX path analog control	0x71	<a href="#">page 3-34</a>
0xn03	TX_AMI	TX path AMI control	0x05	<a href="#">page 3-35</a>
0xn04	TX_LD	TX path LD control	0x64	<a href="#">page 3-36</a>
0xn05	RX_DC	RX DC status	NA	<a href="#">page 3-36</a>
0xn06	RX_ANACTRL	RX path analog control	0x07	<a href="#">page 3-37</a>
0xn07	Reserved		NA	
0xn08	RX_VGAGAINOUT	RX path VGA gain out status	NA	<a href="#">page 3-38</a>
0xn09	Reserved		NA	
0xn0A	RX_MISC0	RX path miscellaneous control0	0x00	<a href="#">page 3-38</a>
0xn0B	RX_MISC1	RX path miscellaneous control1	0x02	<a href="#">page 3-39</a>
0xn0C	RX_EQCAP	RX path equalization coefficient status	NA	<a href="#">page 3-39</a>
0xn0D ~ 0xn0E	Reserved		NA	
0xn0F	RX_ST	RX/TX path status	NA	<a href="#">page 3-40</a>
0xn10	Reserved		NA	
0xn11	CH_LST1	Channel live status1	NA	<a href="#">page 3-41</a>
0xn12	CH_LST2	Channel live status2	NA	<a href="#">page 3-41</a>
0xn13	Not used		0x00	
0xn14	CH_INTST0	Channel interrupt status0	NA	<a href="#">page 3-42</a>
0xn15	CH_INTST1	Channel interrupt status1	NA	<a href="#">page 3-43</a>
0xn16	CH_INTST2	Channel interrupt status2	NA	<a href="#">page 3-44</a>
0xn17	Not used		0x00	
0xn18	CH_INTEN0	Channel interrupt enable0	0x00	<a href="#">page 3-45</a>
0xn19	CH_INTEN1	Channel interrupt enable1	0x00	<a href="#">page 3-46</a>
0xn1A	CH_INTEN2	Channel interrupt enable2	0x00	<a href="#">page 3-47</a>
0xn1B	CH_INTEN3	Channel interrupt enable3	0x00	<a href="#">page 3-48</a>
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				

**Table 3-7. Channel Control Register Table - Numeric by Register Address (2 of 4)**

Address	Name	Description	Default	Page
0xn1C	RXENDEC_CTRL	RX path encoder/decoder control	0x06	<a href="#">page 3-49</a>
0xn1D	Not used		0x00	
0xn1E	RXPRBS_CTRL0	RX path PRBS control0	0x00	<a href="#">page 3-50</a>
0xn1F	RXPRBS_CTRL1	RX path PRBS control1	0x02	<a href="#">page 3-50</a>
0xn20	RXPRBS_CTRL2	RX path PRBS control2	0x16	<a href="#">page 3-50</a>
0xn21	RXPRBS_CTRL3	RX path PRBS control3	0x11	<a href="#">page 3-51</a>
0xn22	RXPRBS_CTRL4	RX path PRBS control4	0x00	<a href="#">page 3-51</a>
0xn23	CH_INTST3	RX path PRBS interrupt status	NA	<a href="#">page 3-52</a>
0xn24	LCV_CTRL0	LCV counter control0	0x1F	<a href="#">page 3-53</a>
0xn25	LCV_CTRL1	LCV counter control1	0x00	<a href="#">page 3-54</a>
0xn26	RXUSR_PAT0	RX path fixed pattern [7:0]	0x00	<a href="#">page 3-54</a>
0xn27	RXUSR_PAT1	RX path fixed pattern [15:8]	0x00	<a href="#">page 3-55</a>
0xn28	RXUSR_PAT2	RX path fixed pattern [23:16]	0x00	<a href="#">page 3-55</a>
0xn29	RXUSR_PAT3	RX path fixed pattern [31:24]	0x00	<a href="#">page 3-55</a>
0xn2A	Not used		0x00	
0xn2B	Not used		0x00	
0xn2C	RXBECNT_ST0	RX path Bit Error counter[7:0] status	NA	<a href="#">page 3-55</a>
0xn2D	RXBECNT_ST1	RX path Bit Error counter[15:8] status	NA	<a href="#">page 3-56</a>
0xn2E	RXBECNT_ST2	RX path Bit Error counter[23:16] status	NA	<a href="#">page 3-56</a>
0xn2F	RXBECNT_ST3	RX path Bit Error counter[31:24] status	NA	<a href="#">page 3-56</a>
0xn30	RXBITCNT_ST0	RX path bit counter [7:0] status	NA	<a href="#">page 3-56</a>
0xn31	RXBITCNT_ST1	RX path bit counter [15:8] status	NA	<a href="#">page 3-57</a>
0xn32	RXBITCNT_ST2	RX path bit counter [23:16] status	NA	<a href="#">page 3-57</a>
0xn33	RXBITCNT_ST3	RX path bit counter [31:24] status	NA	<a href="#">page 3-57</a>
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				

**Table 3-7. Channel Control Register Table - Numeric by Register Address (3 of 4)**

Address	Name	Description	Default	Page
0xn34	LCVCNT1_ST0	LCV counter [7:0] status	NA	<a href="#">page 3-57</a>
0xn35	LCVCNT1_ST1	LCV counter [7:0] status	NA	<a href="#">page 3-58</a>
0xn36	LCVCNT1_ST2	LCV counter [7:0] status	NA	<a href="#">page 3-58</a>
0xn37	Not used		0x00	
0xn38	BPVCNT_ST0	BPV counter [7:0] status	NA	<a href="#">page 3-58</a>
0xn39	BPVCNT_ST1	BPV counter [15:8] status	NA	<a href="#">page 3-58</a>
0xn3A	BPVCNT_ST2	BPV counter [23:16] status	NA	<a href="#">page 3-59</a>
0xn3B	Not used	Reserved	0x00	
0xn3C	EXZCNT_ST0	EXZ counter [7:0] status	NA	<a href="#">page 3-59</a>
0xn3D	EXZCNT_ST1	EXZ counter [15:8] status	NA	<a href="#">page 3-59</a>
0xn3E	EXZCNT_ST2	EXZ counter [23:16] status	NA	<a href="#">page 3-59</a>
0xn3F	Not used	Reserved	0x00	
0xn40	TXPRBS_CTRL0	TX path PRBS control0	0x00	<a href="#">page 3-60</a>
0xn41	TXPRBS_CTRL1	TX path PRBS control1	0x02	<a href="#">page 3-61</a>
0xn42	TXPRBS_CTRL2	TX path PRBS control2	0x16	<a href="#">page 3-61</a>
0xn43	TXPRBS_CTRL3	TX path PRBS control3	0x11	<a href="#">page 3-62</a>
0xn44	TXPRBS_CTRL4	TX path PRBS control4	0x00	<a href="#">page 3-62</a>
0xn45	CH_INTST4	TX path PRBS interrupt status	NA	<a href="#">page 3-63</a>
0xn46	Not used		0x00	
0xn47	TXAIS_CTRL	TX AIS control	0x00	<a href="#">page 3-64</a>
0xn48	TXUSR_PAT0	TX path fixed pattern [7:0]	0x00	<a href="#">page 3-64</a>
0xn49	TXUSR_PAT1	TX path fixed pattern [15:8]	0x00	<a href="#">page 3-64</a>
0xn4A	TXUSR_PAT2	TX path fixed pattern [23:16]	0x00	<a href="#">page 3-65</a>
0xn4B	TXUSR_PAT3	TX path fixed pattern [31:24]	0x00	<a href="#">page 3-65</a>
0xn4C	TXBECNT_ST0	TX path Bit Error counter[7:0] status	NA	<a href="#">page 3-65</a>
0xn4D	TXBECNT_ST1	TX path Bit Error counter[15:8] status	NA	<a href="#">page 3-65</a>
0xn4E	TXBECNT_ST2	TX path Bit Error counter[23:16] status	NA	<a href="#">page 3-66</a>
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				

**Table 3-7. Channel Control Register Table - Numeric by Register Address (4 of 4)**

Address	Name	Description	Default	Page
0xn4F	TXBECNT_ST3	TX path Bit Error counter[31:24] status	NA	<a href="#">page 3-66</a>
0xn50	TXBITCNT_ST0	TX path bit counter [7:0] status	NA	<a href="#">page 3-66</a>
0xn51	TXBITCNT_ST1	TX path bit counter [15:8] status	NA	<a href="#">page 3-66</a>
0xn52	TXBITCNT_ST2	TX path bit counter [23:16] status	NA	<a href="#">page 3-67</a>
0xn53	TXBITCNT_ST3	TX path bit counter [31:24] status	NA	<a href="#">page 3-67</a>
0xn54	Not used		0x00	
0xn55	TXENDEC_CTRL	TX encoder/decoder control	0x05	
0xn56	RLOS_CTRL	RLOS control	0x00	<a href="#">page 3-68</a>
0xn57	COI_CTRL	COI control	0x00	<a href="#">page 3-69</a>
0xn58	COI_OFFSET1	COI status1	NA	<a href="#">page 3-69</a>
0xn59	COI_OFFSET2	COI status2	NA	<a href="#">page 3-69</a>
0xn5A	Not used		0x00	
0xn5B	JATCTRL	DJAT control	0x0F	<a href="#">page 3-70</a>
0xn5C	Reserved		NA	
0xn5D ~ 0xn6E	Reserved		NA	
0xn5F	JATnMON2	DJAT Monitor 2	NA	<a href="#">page 3-70</a>
0xn61	JATnCTRL1	DJAT Control n1	0x00	<a href="#">page 3-71</a>
0xn70 ~ 0xnCF	Reserved		NA	
<b>Note:</b> For the general control registers, the proper address offset must be substituted for the placeholder n. Refer to tables 3.1 and 3.2 for channel distribution.				

## 3.2 Global Register Bit Descriptions

### 3.2.1 Device ID (DEVID: Address 0x000)

**Table 3-8. Device ID (DEVID: Address 0x000)**

Bits	Type	Default	Label	Description
7:0	R	0x5x	DEV_ID [7:0]	Device ID Returns 0x56: M28356 0x54: M28354 0x53: M28353 0x52: M28352

### 3.2.2 Revision Identification (REVID: Address 0x002)

**Table 3-9. Revision Identification (REVID: Address 0x002)**

Bits	Type	Default	Label	Description
7:0	R	NA	REV_ID[7:0]	Revision ID: 0x01 for device marked -11

### 3.2.3 Global Control (GLOBCTRL: Address 0x003)

**Table 3-10. Global Control (GLOBCTRL: Address 0x003)**

Bits	Type	Default	Label	Description
7:4		0		Unused
3	R	NA	RSTB_JAT_MON	DJAT Reset status 0 = DJATs are in reset 1 = DJATs are out of reset
2	R	NA	GLOBINTST	Global interrupt status 1 = global interrupt pending 0 = no interrupt pending
1	RW	0	GLOBINTEN	Global interrupt enable 1 = enable 0 = disable
0	RW	0	GLOB_RST	Global Soft Reset 1 = Resets all channel registers and most global registers to their default values. (self-clearing)

### 3.2.4 Channel Interrupt Enable (CHINTEN: Address 0x004)

**Table 3-11. Channel Interrupt Enable (CHINTEN: Address 0x004)**

Bits	Type	Default	Label	Description																								
7:6		0		Unused																								
5:0	RW	0x00	CHINTEN[5:0]	<p>Interrupt enable for channels 5 through 0: 0= disable 1= enable</p> <p><b>NOTE:</b> For the M28356 device the control for the channels follows the order given in this subtable:</p> <table><tr><th>Channel</th><th>Bit No.</th></tr><tr><td>0</td><td>CHINTEN[0]</td></tr><tr><td>1</td><td>CHINTEN[1]</td></tr><tr><td>2</td><td>CHINTEN[2]</td></tr><tr><td>3</td><td>CHINTEN[3]</td></tr><tr><td>4</td><td>CHINTEN[4]</td></tr><tr><td>5</td><td>CHINTEN[5]</td></tr></table> <p><b>NOTE:</b> For the M28352/3/4 devices the control for the channels follows the order given in this subtable:</p> <table><tr><th>Channel</th><th>Bit No.</th></tr><tr><td>0</td><td>CHINTEN[0]</td></tr><tr><td>1</td><td>CHINTEN[1]</td></tr><tr><td>2</td><td>CHINTEN[4]</td></tr><tr><td>3</td><td>CHINTEN[5]</td></tr></table>	Channel	Bit No.	0	CHINTEN[0]	1	CHINTEN[1]	2	CHINTEN[2]	3	CHINTEN[3]	4	CHINTEN[4]	5	CHINTEN[5]	Channel	Bit No.	0	CHINTEN[0]	1	CHINTEN[1]	2	CHINTEN[4]	3	CHINTEN[5]
Channel	Bit No.																											
0	CHINTEN[0]																											
1	CHINTEN[1]																											
2	CHINTEN[2]																											
3	CHINTEN[3]																											
4	CHINTEN[4]																											
5	CHINTEN[5]																											
Channel	Bit No.																											
0	CHINTEN[0]																											
1	CHINTEN[1]																											
2	CHINTEN[4]																											
3	CHINTEN[5]																											

### 3.2.5 Extended TX Monitor Interrupt Enable (TXMONINTEN: Address 0x006)

**Table 3-12. Extended TX Monitor Interrupt Enable (TXMONINTEN: Address 0x006)**

Bits	Type	Default	Label	Description
7:2		0		Unused
1	RW	0	TOPENINTEN	<p>TOPEN interrupt enable  0 = disable  1 = enable</p> <p>When set this allows the TOPENINTST bit in the TXMONINTSTAT register to propagate towards the IRQB pin.</p>
0	RW	0	TLOSINTEN	<p>TLOS interrupt enable  0 = disable  1 = enable</p> <p>When set this allows the TLOSINTST bit in the TXMONINTSTAT register to propagate towards the IRQB pin.</p>



### 3.2.6 Channel Interrupt Status (CHINTSTAT: Address 0x007)

**Table 3-13. Channel Interrupt Status (CHINTSTAT: Address 0x007)**

Bits	Type	Default	Label	Description																								
7:6		0		Unused																								
5:0	R	0x00	CHINTST[5:0]	<p>Interrupt status for channels 5 through 0. The interrupts in the register Channel Interrupt Enable (CHINTEN: Address 0x004) need to be enabled for the status bits to be active.</p> <p>0= No channel interrupt pending 1= Channel interrupt pending</p> <p><b>NOTE:</b> For the M28356 device the status for the channels follows the order given in this subtable:</p> <table><tr><th>Channel</th><th>Bit No.</th></tr><tr><td>0</td><td>CHINTST[0]</td></tr><tr><td>1</td><td>CHINTST[1]</td></tr><tr><td>2</td><td>CHINTST[2]</td></tr><tr><td>3</td><td>CHINTST[3]</td></tr><tr><td>4</td><td>CHINTST[4]</td></tr><tr><td>5</td><td>CHINTST[5]</td></tr></table> <p><b>NOTE:</b> For the M28352/3/4 devices the status for the channels follows the order given in this subtable:</p> <table><tr><th>Channel</th><th>Bit No.</th></tr><tr><td>0</td><td>CHINTST[0]</td></tr><tr><td>1</td><td>CHINTST[1]</td></tr><tr><td>2</td><td>CHINTST[4]</td></tr><tr><td>3</td><td>CHINTST[5]</td></tr></table>	Channel	Bit No.	0	CHINTST[0]	1	CHINTST[1]	2	CHINTST[2]	3	CHINTST[3]	4	CHINTST[4]	5	CHINTST[5]	Channel	Bit No.	0	CHINTST[0]	1	CHINTST[1]	2	CHINTST[4]	3	CHINTST[5]
Channel	Bit No.																											
0	CHINTST[0]																											
1	CHINTST[1]																											
2	CHINTST[2]																											
3	CHINTST[3]																											
4	CHINTST[4]																											
5	CHINTST[5]																											
Channel	Bit No.																											
0	CHINTST[0]																											
1	CHINTST[1]																											
2	CHINTST[4]																											
3	CHINTST[5]																											

### 3.2.7 Extended TX Monitor Interrupts Status (TXMONINTSTAT: Address 0x009)

**NOTE:** These interrupts reflect the status of the external monitor pins MON\_INP and MON\_INM

**Table 3-14. Extended TX Monitor Interrupts Status (TXMONINTSTAT: Address 0x009)**

Bits	Type	Default	Label	Description
7:2		0		Unused
1	RC	NA	TOPENINTST	<p>TOPEN interrupt status</p> <p>0 = no interrupt pending 1 = interrupt pending</p>
0	RC	NA	TLOSINTST	<p>TLOS interrupt status</p> <p>0 = no interrupt pending 1 = interrupt pending</p>

### 3.2.8 1-sec. Timer Control (SECTIMCTRL: Address 0x00A)

**Table 3-15. 1-sec. Timer Control (SECTIMCTRL: Address 0x00A)**

Bits	Type	Default	Label	Description																														
7:6	R	NA	LINERATE[1:0]	Interface line clock rate. 00 = STS-1 rate of 51.840 MHz 01 = DS3 rate of 44.736 MHz 1x = E3 rate of 34.368 MHz  A clock mux will choose the fastest clock from the three CLAD output clocks or refclk when the CLAD is being bypassed. This clock is used for both microprocessor interface and the 1-sec. timer.																														
5:3		0		Unused																														
2	RW	0	SECLATMODE	Counter value selection 0 = reading real time counter value 1 = reading one-second latched counter value <b>NOTE:</b> To configure a counter for “one-second value”, this bit and the one-second bit associated with the specific counter must be asserted. For example: <table><tr><th colspan="3">Enabling all Counters for One-second Value</th></tr><tr><th>Register</th><th>Bit Field</th><th>Value</th></tr><tr><td>SECTIMCTRL</td><td>SECLATMODE</td><td>1</td></tr><tr><td>LCV_CTRL1</td><td>EXZCNT_SEL</td><td>1</td></tr><tr><td>LCV_CTRL1</td><td>BPVCNT_SEL</td><td>1</td></tr><tr><td>LCV_CTRL1</td><td>LCVCNT_SEL</td><td>1</td></tr><tr><td>RXPRBS_CTRL4</td><td>RXBITCNT_SEL</td><td>1</td></tr><tr><td>RXPRBS_CTRL4</td><td>RXBECNT_SEL</td><td>1</td></tr><tr><td>TXPRBS_CTRL4</td><td>TXBITCNT_SEL</td><td>1</td></tr><tr><td>TXPRBS_CTRL4</td><td>TXBECNT_SEL</td><td>1</td></tr></table>	Enabling all Counters for One-second Value			Register	Bit Field	Value	SECTIMCTRL	SECLATMODE	1	LCV_CTRL1	EXZCNT_SEL	1	LCV_CTRL1	BPVCNT_SEL	1	LCV_CTRL1	LCVCNT_SEL	1	RXPRBS_CTRL4	RXBITCNT_SEL	1	RXPRBS_CTRL4	RXBECNT_SEL	1	TXPRBS_CTRL4	TXBITCNT_SEL	1	TXPRBS_CTRL4	TXBECNT_SEL	1
Enabling all Counters for One-second Value																																		
Register	Bit Field	Value																																
SECTIMCTRL	SECLATMODE	1																																
LCV_CTRL1	EXZCNT_SEL	1																																
LCV_CTRL1	BPVCNT_SEL	1																																
LCV_CTRL1	LCVCNT_SEL	1																																
RXPRBS_CTRL4	RXBITCNT_SEL	1																																
RXPRBS_CTRL4	RXBECNT_SEL	1																																
TXPRBS_CTRL4	TXBITCNT_SEL	1																																
TXPRBS_CTRL4	TXBECNT_SEL	1																																
1	RW	0	SECCLK_ENB	One sec. timer enable 0 = one sec. timer enabled 1 = one sec. timer disabled																														
0	RW	0	SECCLK_OEB	0 = enable 1-sec. clock output 1 = disable 1-sec. clock output																														

### 3.2.9 SECTIMCYCLE[0:3]

**NOTE:**

The following registers control the length of the 1 second period used for the 1 second interrupt, counter latching and counter clearing.

The default line rate used for the 1 second timer is the STS-1 clock of 51.840 MHz. Please note, this is the default setting for the SECTIMCYCLEn registers. The following table gives the proper SECTIMCYCLEn contents necessary for each line rate.

**Table 3-16. SECTIMCYCLE[0:3]**

Clock	Hz	Hexadecimal Equivalent	SECTIMCYCLEn			
			0	1	2	3
STS-1 (default)	51840000	0x03170400	0x00	0x04	0x17	0x03
DS3	44736000	0x02AA9E00	0x00	0x9E	0xAA	0x02
E3	34368000	0x020C6A00	0x00	0x6A	0x0C	0x02

### 3.2.10 1-sec. Timer Period Control 0 (SECTIMCYCLE0: Address 0x00B)

**Table 3-17. 1-sec. Timer Period Control 0 (SECTIMCYCLE0: Address 0x00B)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	SECTIMCYCLE[7:0]	1-sec. timer period [7:0]

### 3.2.11 1-sec. Timer Period Control 1 (SECTIMCYCLE1: Address 0x00C)

**Table 3-18. 1-sec. Timer Period Control 1 (SECTIMCYCLE1: Address 0x00C)**

Bits	Type	Default	Label	Description
7:0	RW	0x04	SECTIMCYCLE[15:8]	1-sec. timer period [15:8]

### 3.2.12 1-sec. Timer Period Control 2 (SECTIMCYCLE2: Address 0x00D)

**Table 3-19. 1-sec. Timer Period Control 2 (SECTIMCYCLE2: Address 0x00D)**

Bits	Type	Default	Label	Description
7:0	RW	0x17	SECTIMCYCLE[23:16]	1-sec. timer period [23:16]

### 3.2.13 1-sec. Timer Period Control 3 (SECTIMCYCLE3: Address 0x00E)

**Table 3-20. 1-sec. Timer Period Control 2 (SECTIMCYCLE2: Address 0x00E)**

Bits	Type	Default	Label	Description
7:0	RW	0x03	SECTIMCYCLE[31:24]	1-sec. timer period [31:24]

### 3.2.14 TX Monitor Digital Control (TLOS\_CONTROL: Address 0x00F)

**Table 3-21. TX Monitor Digital Control (TLOS\_CONTROL: Address 0x00F)**

Bits	Type	Default	Label	Description
7	R	NA	TOPEN_EXT	Transmit path open monitored in live status on the external channel, MON_INP and MON_INM
6	R	NA	TLOS_EXT	TLOS alarm status monitored in live status on the external channel, MON_INP & MON_INM 1 = loss of signal occurred
5	RW	0	EN_GLOBAL	Enables the digital and analog transmit monitoring blocks and enables all other analog monitoring functions including the analog transmit MON_OP and MON_OM pin drivers and the temperature sensor. . NOTE: To enable the analog and digital transmit monitoring blocks, the EN_LOSOPEN bit in the TXMON_ANACTRL3 register must also be set to 1. 0 = disable 1 = enable
4		NA		Reserved
3:0	RW	0xF	TLOS_CTRL[3:0]	Mux control: 0000: Select channel 0. 0001: Select channel 1. 0010: Select channel 2. 0011: Select channel 3. 0100: Select channel 4. 0101: Select channel 5. 0111: Sample channels 0 to 5 every $2^{13}$ clock periods (420 us). 1000: Sample channels 0 to 5 every $2^{13}$ clock periods (420 us). 1001: Sample channels 0 to 5 every $2^{13}$ clock periods (420 us). 1010: Sample channels 0 to 5 every $2^{13}$ clock periods (420 us). 1011: Sample channels 0 to 5 every $2^{13}$ clock periods (420 us). 1100: Select channel 6 from input pads MON_INP, MON_INM. 1101: Sample channels 0 to 5 every $2^7$ clock periods (6.5 us). 1110: Sample channels 0 to 5 every $2^{15}$ clock periods (1.68 ms). 1111: Sample channels 0 to 5 every $2^{13}$ clock periods (420 us).

### 3.2.15 TX Monitor Analog Control1 (TXMON\_ANACTRL1: Address 0x010)

**Table 3-22. TX Monitor Analog Control1 (TXMON\_ANACTRL1: Address 0x010)**

Bits	Type	Default	Label	Description																																																			
7:5		0		Unused																																																			
4	RW	0	MON_EXT	<p>Routes the mux controls to the MON_CTRLn pins for external monitoring of the transmission lines. These signals can then be used for a custom monitoring scheme.</p> <p>The default condition is to use the internal mux and transmission lines and the MON_CTRLn pins are driven low. When selected for external monitoring, the pins MON_INP and MON_INM are continuously monitored.</p> <p>0 = monitor internally routed transmission lines 1 = monitor externally routed transmission lines</p>																																																			
3:0	RW	0x6	LD_GAIN[3:0]	<p>Control bits for line driver gain in the monitor path. 16 linear steps with a step size of 0.1Vpp as shown in the accompanying table.</p> <p><b>NOTE:Table 2-2 Line Driver Gain Control Repeated</b></p> <table><tr><th>LD_GAIN[3:0]</th><th>Gain (lin)</th><th>Gain (dB)</th></tr><tr><td>0000</td><td>1.4</td><td>2.922</td></tr><tr><td>0001</td><td>1.5</td><td>3.521</td></tr><tr><td>0010</td><td>1.6</td><td>4.082</td></tr><tr><td>0011</td><td>1.7</td><td>4.608</td></tr><tr><td>0100</td><td>1.8</td><td>5.105</td></tr><tr><td>0101</td><td>1.9</td><td>5.575</td></tr><tr><td>0110</td><td>2.0</td><td>6.020</td></tr><tr><td>0111</td><td>2.1</td><td>6.444</td></tr><tr><td>1000</td><td>2.2</td><td>6.848</td></tr><tr><td>1001</td><td>2.3</td><td>7.234</td></tr><tr><td>1010</td><td>2.4</td><td>7.604</td></tr><tr><td>1011</td><td>2.5</td><td>7.958</td></tr><tr><td>1100</td><td>2.6</td><td>8.299</td></tr><tr><td>1101</td><td>2.7</td><td>8.627</td></tr><tr><td>1110</td><td>2.8</td><td>8.943</td></tr><tr><td>1111</td><td>2.9</td><td>9.247</td></tr></table>	LD_GAIN[3:0]	Gain (lin)	Gain (dB)	0000	1.4	2.922	0001	1.5	3.521	0010	1.6	4.082	0011	1.7	4.608	0100	1.8	5.105	0101	1.9	5.575	0110	2.0	6.020	0111	2.1	6.444	1000	2.2	6.848	1001	2.3	7.234	1010	2.4	7.604	1011	2.5	7.958	1100	2.6	8.299	1101	2.7	8.627	1110	2.8	8.943	1111	2.9	9.247
LD_GAIN[3:0]	Gain (lin)	Gain (dB)																																																					
0000	1.4	2.922																																																					
0001	1.5	3.521																																																					
0010	1.6	4.082																																																					
0011	1.7	4.608																																																					
0100	1.8	5.105																																																					
0101	1.9	5.575																																																					
0110	2.0	6.020																																																					
0111	2.1	6.444																																																					
1000	2.2	6.848																																																					
1001	2.3	7.234																																																					
1010	2.4	7.604																																																					
1011	2.5	7.958																																																					
1100	2.6	8.299																																																					
1101	2.7	8.627																																																					
1110	2.8	8.943																																																					
1111	2.9	9.247																																																					

### 3.2.16 TX Monitor Analog Control2 (TXMON\_ANACTRL2: Address 0x011)

**Table 3-23. TX Monitor Analog Control2 (TXMON\_ANACTRL2: Address 0x011)**

Bits	Type	Default	Label	Description
7:6		0		Unused
5:4	RW	0x2	THR_OPEN[1:0]	Control bits to adjust the threshold for TOPEN 00: 1.175V 01: 1.295V 10: 1.356V 11: 1.4V  If the output amplitude exceeds the reference signal, TOPEN is declared.  This function only usable for the transmit output amplitudes from 1.9 to 2.2V as set by bits LD_GAIN[3:0] in register TXMON_ANACTRL1.
3:2	RW	0x2	THR_TLOS[1:0]	Control bits to adjust the threshold for TLOS 00: 100mV 01: 128mV 10: 200mV 11: 260mV  If the output amplitude falls below the reference signal for 32 clock cycles, TLOS is declared.
1	RW	0	CTL_REFMUX_ML	Control bits for the Ref Mux in TXMON. Toggle between 0.9v and 0.65v 0: 0.65V 1: 0.9V
0	RW	0	CTL_REFMUX_HM	Control bits for the Ref Mux in TXMON. Toggle between 1.15v and 0.9v 0: 0.9V 1: 1.15V

### 3.2.17 TX Monitor Analog Control3 (TXMON\_ANACTRL3: Address 0x012)

**Table 3-24. TX Monitor Analog Control3 (TXMON\_ANACTRL3: Address 0x012)**

Bits	Type	Default	Label	Description
7:5		0		Unused
4	RW	0	EN_LOSOPEN	Enables the digital and analog transmit monitoring blocks only. NOTE: To enable the analog and digital transmit monitoring blocks, the EN_GLOBAL bit in the TLOS_CONTROL register must also be set to 1. 0 = disable 1 = enable
3	RW	0	EN_LD	Enable for the output pads MON_OP and MON_OM line driver 0 = disable 1 = enable
2:0	RW	0x7	BW_SEL[2:0]	Controls bits to adjust the bandwidth for TX jitter (Not Used in this REV)

### 3.2.18 TX Jitter Control and Status (TXJITTER: Address 0x013)

**Table 3-25. TX Jitter Control and Status (TXJITTER: Address 0x013)**

Bits	Type	Default	Label	Description
7:3	R	NA	TXJITTER[4:0]	TX Jitter Indicator <b>(Not available in device revision - 11)</b>
2:1		0		Unused
0	RW	0	EN_JITDEMO	TX Jitter Demodulator enable <b>(Not available in device revision -11)</b> 0 = disable 1 = enable



### 3.2.19 Hardware Control (HWCTRL: Address 0x015)

**Table 3-26. Hardware Control (HWCTRL: Address 0x015)**

Bits	Type	Default	Label	Description
7:4		0		Unused
3	R	NA	LIU_BYP	<p>Status of the LIU_BYP hardware control pad for all the channels</p> <p>1 = bypassed 0 = not bypassed</p> <p>LIU bypass is used to verify that TPOS<sub>n</sub> and TCLK<sub>n</sub> inputs (NRZ Mode) or TPOS<sub>n</sub> and TNEG<sub>n</sub> inputs are seen on the TX_LINEP<sub>n</sub> and TX_LINEM<sub>n</sub> outputs respectively.</p> <p><b>Note:</b> In this test, DJAT, CLAD and XTAL blocks must be set to bypass mode.</p>
2	R	NA	XTAL_BYP	<p>Status of XTAL_BYP hardware control pad to bypass the crystal</p> <p>1 = bypassed 0 = not bypassed</p> <p>Crystal bypass – crystal circuitry is disabled</p> <p>If not bypassed, CLK19P44_IO is an output.</p> <p>If bypassed, CLK19P44_IO is an input.</p>
1	R	NA	CLAD_BYP	<p>Status of CLAD_BYP hardware control pad to bypass all three (3) CLADs</p> <p>1 = bypassed 0 = not bypassed</p> <p>When the CLADs are not bypassed, DS3_REFCLK, E3_REFCLK, and STS1_REFCLK are outputs.</p> <p>When the CLADs are bypassed, external reference clock(s) must be provided via DS3_REFCLK, E3_REFCLK, and/or STS1_REFCLK.</p>
0	R	NA	XOEB	<p>Status of XOEB hardware control pad for all the line drivers</p> <p>1 = disabled 0 = enabled</p> <p><b>Note:</b> Status of bit3, XOEB_LOC, in the register CH_CTRL0 at address offsets 0xn00 are not reflected in this bit.</p>

## 3.2.20 CLAD Control and Status

### 3.2.20.1 STS-1 CLAD Control

**Table 3-27. CLADSTS1 Control (CLADSTS1CTRL1: Address 0x020)**

Bits	Type	Default	Label	Description
7:1		0011 111		Reserved
0	RW	1	PDB_CLAD	Master Power-down (reset all digital CLAD logic) 0 = CLAD powered down 1 = CLAD powered up <b>Note:</b> To use external line reference clocks, all three line reference clock pins (i.e. STS1_REFCLK, DS3_REFCLK, and E3_REFCLK) must be configured as inputs by setting the CLAD_BYP pin to “1” (high). The software CLAD “power down” bits (i.e. the PDB_CLAD bit in the CLADSTS1 control [3.2.20.1], CLADDS3 control [3.2.20.2], and CLADE3 Control [3.2.20.3] registers power down their respective CLADs but they do not configure the line reference clock pins as inputs.

**Table 3-28. CLADSTS1 Monitor2 (CLADSTS1MON2: Address 0x025)**

Bits	Type	Default	Label	Description
7	R	NA	FNPLL_LD	PLL lock detect Status 0 = no PLL lock detected 1 = PLL lock detected
6:0		NA		Reserved

**Table 3-29. CLADSTS1 FSM Status (CLADSTS1FSMSTAT: Address 0x027)**

Bits	Type	Default	Label	Description
7:0	R	NA	FSM_STAT[7:0]	CLAD finite state machine status

### 3.2.20.2 DS3 CLAD Control

**Table 3-30. CLADDS3 Control (CLADDS3CTRL1: Address 0x030)**

Bits	Type	Default	Label	Description
7:1		0011 111		Reserved

**Table 3-30. CLADDS3 Control (CLADDS3CTRL1: Address 0x030)**

Bits	Type	Default	Label	Description
0	RW	1	PDB_CLAD	<p>Master Power-down (reset all digital CLAD logic)</p> <p>0 = CLAD powered down</p> <p>1 = CLAD powered up</p> <p><b>Note:</b> To use external line reference clocks, all three line reference clock pins (i.e. STS1_REFCLK, DS3_REFCLK, and E3_REFCLK) must be configured as inputs by setting the CLAD_BYP pin to “1” (high). The software CLAD “power down” bits (i.e. the PDB_CLAD bit in the CLADSTS1 control [3.2.20.1], CLADDS3 control [3.2.20.2], and CLADE3 Control [3.2.20.3] registers power down their respective CLADs but they do not configure the line reference clock pins as inputs.</p>

**Table 3-31. CLADDS3 Monitor2 (CLADDS3MON2: Address 0x035)**

Bits	Type	Default	Label	Description
7	R	NA	FNPLL_LD	<p>PLL lock detect Status</p> <p>0 = no PLL lock detected</p> <p>1 = PLL lock detected</p>
6:0		NA		Reserved

**Table 3-32. CLADDS3 FSM Status (CLADDS3FSMSTAT: Address 0x037)**

Bits	Type	Default	Label	Description
7:0	R	NA	FSM_STAT[7:0]	CLAD finite state machine status

### 3.2.20.3 E3 CLAD Control

**Table 3-33. CLADE3 Control (CLADE3CTRL1: Address 0x040)**

Bits	Type	Default	Label	Description
7:1		0011 111		Reserved

**Table 3-33. CLADE3 Control (CLADE3CTRL1: Address 0x040)**

Bits	Type	Default	Label	Description
0	RW	1	PDB_CLAD	<p>Master Power-down (reset all digital CLAD logic)</p> <p>0 = CLAD powered down</p> <p>1 = CLAD powered up</p> <p><b>Note:</b> To use external line reference clocks, all three line reference clock pins (i.e. STS1_REFCLK, DS3_REFCLK, and E3_REFCLK) must be configured as inputs by setting the CLAD_BYP pin to “1” (high). The software CLAD “power down” bits (i.e. the PDB_CLAD bit in the CLADSTS1 control [3.2.20.1], CLADDS3 control [3.2.20.2], and CLADE3 Control [3.2.20.3] registers power down their respective CLADs but they do not configure the line reference clock pins as inputs.</p>

**Table 3-34. CLADE3 Monitor2 (CLADE3MON2: Address 0x045)**

Bits	Type	Default	Label	Description
7	R	NA	FNPLL_LD	<p>PLL lock detect Status</p> <p>0 = no PLL lock detected</p> <p>1 = PLL lock detected</p>
6:0		NA		Reserved

**Table 3-35. CLADE3 FSM Status (CLADE3FSMSTAT: Address 0x047)**

Bits	Type	Default	Label	Description
7:0	R	NA	FSM_STAT[7:0]	CLAD finite state machine status

### 3.3 Channel Offset Register Bit Descriptions

**NOTE:**

The following registers affect or control the individual channels within the M28356/4/3/2 family of devices.

Channel No.	Base Addr.			
	M28356	M28354	M28353	M28352
0	0x100	0x100	0x100	0x100
1	0x200	0x200	0x200	0x200
2	0x300	0x500	0x500	
3	0x400	0x600		
4	0x500			
5	0x600			

### 3.3.1 Channel Control0 (CH\_CTRL0: 0x100-0x600)

**Table 3-36. Channel Control0 (CH\_CTRL0: 0x100-0x600)**

Bits	Type	Default	Label	Description
7		0		Reserved
6	RW	0	EN_DC_CONT	Enable control for RX DC continuity check 0 = disable 1 = enable
5:4		0		Reserved
3	RW	0	XOEB_LOC	Software control for the transmit line output driver 0 = enable transmit line output driver 1 = disable transmit line output drivers, set to high impedance state. <b>Note:</b> In software mode, the XOEB pin should be left unconnected or pulled low.
2	RW	1	JAT_SEL	DJAT mode control 1 = TX 0 = RX Setting this bit allows the DJAT to function in the transmit path of the M2835x. Clearing this bit places the DJAT in the receive path. In software mode, this setting takes precedence over the hardware setting via the JATRX pin.
1:0	RW	0x1	LINERATE[1:0]	Line rate control sets the data mode used for the channel. 00 = STS-1 mode 01 = DS3 mode 1X = E3 mode In software mode, this setting takes precedence over the hardware settings via the pins LINERATE0 and LINERATE1.

### 3.3.2 Channel Control1 (CH\_CTRL1: 0x101-0x601)

**Table 3-37. Channel Control1 (CH\_CTRL1: 0x101-0x601)**

Bits	Type	Default	Label	Description
7	RW	0	EN_TXBYP_ANA	Transmit analog bypass 0 = TX analog section enabled 1 = Set TX analog section in bypass mode
6:5	RW	0x0	RLOSSEL[1:0]	RLOS data inhibitor 0X – pass through 10 – turn-on data inhibiting for RLOS 11 – inhibit data when RLOS=1
4	RW	0	LOCK_SEL	CDR data inhibitor 0 = normal mode 1 = inhibits data to 1 when CDR-Lock=0
3	RW	0	LB2_EN	Analog line loopback 0 = Disable 1 = Enable <b>Note:</b> Refer to section <a href="#">Section 2.9.3</a> for a description of analog loopback.
2	RW	0	LB1_EN	Source (local) Loopback 0 = Disable 1 = Enable The transmit data on pads TPOSn/TNEGn are looped back through the DJAT to output pads RPOSn/RNEGn. This mode allows for the AIS to be sourced on output pads TX_LINEP_n and TX__LINEM_n. <b>Note:</b> When AIS is enabled, the AIS signal will replace the data going out the transmit line (i.e., TX_LINEP_n/LINEM_n).
1	RW	0	LBO_EN	Line (remote) loopback The receive line data is looped back and replaces the transmit line data. The loopback occurs after the data is retimed in clock recovery (i.e., the data is regenerated) but it is not decoded (i.e., the receive line decoder is disabled). 0 = Disable 1 = Enable <b>Note:</b> When AIS is enabled, the AIS signal will replace the looped back data going out the transmit line (i.e., TX_LINEP_n/LINEM_n).
0	RW	1	CH_EN	Channel Enable - resets channel to default values 0 = disable channel 1 = enable channel

### 3.3.3 TX Path Analog Control (TX\_ANACTRL: Address 0x102-0x602)

**Table 3-38. TX Path Analog Control (TX\_ANACTRL: Address 0x102-0x602)**

Bits	Type	Default	Label	Description
7:4		NA		Reserved
3:2	RW	0x0	TXMUX[1:0]	Control for the mux in front of the line driver in TX path 00 = DS3/STS-1 modes 01 = E3 mode 10 = Reserved 11 = Analog loopback mode. Used in conjunction with bits RXMUX[1:0] in register RX_ANACTRL. <b>Note:</b> In loopback mode receive data will overwrite any AIS signal generated.
1	RW	0	EN_TXBYP	Bypass mode Control for TX digital path 0 = not bypassed 1 = bypassed
0	RW	1	TX_EN	TX enable for the entire data path 0 = disable 1 = enable



### 3.3.4 TX Path AMI Control (TX\_AMI: Address 0x103, 0x603)

**Table 3-39. TX Path AMI Control (TX\_AMI: Address 0x103, 0x603)**

Bits	Type	Default	Label	Description
7:5		NA		Reserved
4	RW	0	EN_EXTRAI	<p>Enables the extra current required to have a 25% rising edge instead of 37.5%.</p> <p>0: 37.5% LBO on 1: 25% LBO off</p> <p><b>Note:</b> Used in conjunction with LBO. For correct performance bit EN_EXTRAI and bit LBO should be set opposite of each other.</p>
3:1	RW	0x2	CAP_AMI[2:0]	<p>Controls the capacitors values for the internal switched capacitor current generator in the AMI clock. Sets the generated current for the AMI generator to one of 7 values. The values progress in linear steps with a step size of 5%.</p> <p>000: -15% 001: -10% 010: -5% 011: 0 % 100: 5% 101: 10% 11x: 15%</p>
0	RW	1	LBO	<p>Line build out control</p> <p>Used in DS3/STS1 rates in order to change the time base of the rising/falling edges from 25% to 37.5%.</p> <p><b>Note:</b> Used in conjunction with EN_EXTRAI. For correct performance bit EN_EXTRAI and bit LBO should be set opposite of each other.</p>

### 3.3.5 TX Path LD Control (TXn\_LD: Address 0x104-0x604)

**Table 3-40. TX Path LD control (TXn\_LD: Address 0x104-0x604)**

Bits	Type	Default	Label	Description																																																			
7:4	RW	0x6	LD_GAIN[3:0]	<p>Control bits for line driver gain in the TX path. 16 linear steps with a step size of 0.1Vpp.</p> <p><b>Table 3-41. Line Driver Gain Control</b></p> <table><tr><th>LD_GAIN[3:0]</th><th>Gain (lin)</th><th>Gain(dB)</th></tr><tr><td>0000</td><td>1.4</td><td>2.922</td></tr><tr><td>0001</td><td>1.5</td><td>3.521</td></tr><tr><td>0010</td><td>1.6</td><td>4.082</td></tr><tr><td>0011</td><td>1.7</td><td>4.608</td></tr><tr><td>0100</td><td>1.8</td><td>5.105</td></tr><tr><td>0101</td><td>1.9</td><td>5.575</td></tr><tr><td>0110</td><td>2.0</td><td>6.020</td></tr><tr><td>0111</td><td>2.1</td><td>6.444</td></tr><tr><td>1000</td><td>2.2</td><td>6.848</td></tr><tr><td>1001</td><td>2.3</td><td>7.234</td></tr><tr><td>1010</td><td>2.4</td><td>7.604</td></tr><tr><td>1011</td><td>2.5</td><td>7.958</td></tr><tr><td>1100</td><td>2.6</td><td>8.299</td></tr><tr><td>1101</td><td>2.7</td><td>8.627</td></tr><tr><td>1110</td><td>2.8</td><td>8.943</td></tr><tr><td>1111</td><td>2.9</td><td>9.247</td></tr></table>	LD_GAIN[3:0]	Gain (lin)	Gain(dB)	0000	1.4	2.922	0001	1.5	3.521	0010	1.6	4.082	0011	1.7	4.608	0100	1.8	5.105	0101	1.9	5.575	0110	2.0	6.020	0111	2.1	6.444	1000	2.2	6.848	1001	2.3	7.234	1010	2.4	7.604	1011	2.5	7.958	1100	2.6	8.299	1101	2.7	8.627	1110	2.8	8.943	1111	2.9	9.247
LD_GAIN[3:0]	Gain (lin)	Gain(dB)																																																					
0000	1.4	2.922																																																					
0001	1.5	3.521																																																					
0010	1.6	4.082																																																					
0011	1.7	4.608																																																					
0100	1.8	5.105																																																					
0101	1.9	5.575																																																					
0110	2.0	6.020																																																					
0111	2.1	6.444																																																					
1000	2.2	6.848																																																					
1001	2.3	7.234																																																					
1010	2.4	7.604																																																					
1011	2.5	7.958																																																					
1100	2.6	8.299																																																					
1101	2.7	8.627																																																					
1110	2.8	8.943																																																					
1111	2.9	9.247																																																					
3:0	RW	0x4	LD_FILTER[3:0]	<p>Control bits for line driver de-emphasis. 16 linear steps with a step size of 100fF.</p> <p>0000: 250fF</p> <p>.</p> <p>.</p> <p>.</p> <p>1111: 1.75pF</p>																																																			

### 3.3.6 RX\_DC (RX\_DC: Address 0x105-0x605)

**Table 3-42. RX\_DC (RX\_DC: Address 0x105-0x605)**

Bits	Type	Default	Label	Description
7:2		NA		Reserved
1	R	NA	RX_OPEN	RX DC open indicator
0	R	NA	RX_SHORT	RX DC short indicator

### 3.3.7 RX Path Analog Control (RX\_ANACTRL: Address 0x106-0x606)

**Table 3-43. RX Path Analog Control (RX\_ANACTRL: Address 0x106-0x606)**

Bits	Type	Default	Label	Description
7:3		NA		Reserved
2:1	RW	0x3	RXMUX[1:0]	Control for the MUX used for analog loop back from the RX to the TX line driver 0X = Reserved 10 = For analog loopback mode, the TX_MUX[1:0] in TX_ANACTRL register must be set to 11b 11 = Pass through <b>Note:</b> In loopback mode receive data will overwrite any AIS signal generated.
0	RW	1	RX_EN	RX path enable 0 = disable 1 = enable

### 3.3.8 RX Path VGA Gain Out (RXn\_VGAGAINOUT: Address 0x108-0x608)

**Table 3-44. RX Path VGA Gain Out (RXn\_VGAGAINOUT: Address 0x108-0x608)**

Bits	Type	Default	Label	Description
7		NA		Reserved
6	R	NA	CDR_LOCK	CDR lock status 1 = in lock 0 = loss of lock
5:0	R	NA	VGA_GAINOUT[5:0]	VGA gain output status. Gray coded. 000000: -10dB ... 100000: +30dB

### 3.3.9 RX Path Miscellaneous Control0 (RX\_MISC0: Address 0x10A-0x60A)

**Table 3-45. RX Path Miscellaneous Control0 (RX\_MISC0: Address 0x10A-0x60A)**

Bits	Type	Default	Label	Description
7:6		NA		Reserved
5:2	RW	0x0	SLIC_THR[3:0]	Control bits to adjust the slicer threshold. 16 linear steps with a step size of 2%. 0000: +36% ... 1111: +66%
1:0		NA		Reserved

### 3.3.10 RX Path Miscellaneous Control1 (RX\_MISC1: Address 0x10B - 0x60B)

**Table 3-46. RX Path Miscellaneous Control1 (RX\_MISC1: Address 0x10B - 0x60B)**

Bits	Type	Default	Label	Description
7:5		NA		Reserved
4:3	RW	0	RX_HI_R[1:0]	Control bits to adjust the threshold for DC continuity check for the open detection. 4 linear steps with a step size of 6660hms. 00: 1.6Kohms 01: 2.266Kohms 10: 2.932Kohms 11: 3.6Kohms
2:0	RW	0x2	RX_LOSTHR[2:0]	Control bits to adjust the set/clear threshold for RLOS. 8 steps described below: 000: 0/0 001: 17.5mV/17.5mV 010: 17.5mV/55mV 011: 35mV/110mV 100: 35mV/35mV 101: 25mV/48mV 110: 30mV/40mV 111: 25mV/75mV

### 3.3.11 RX EQ Cap (RX\_EQCAP: Address 0x10C- 0x60C)

**Table 3-47. RX EQ Cap (RX\_EQCAP: Address 0x10C- 0x60C)**

Bits	Type	Default	Label	Description
7:0	R	NA	EQ_CAP[7:0]	Status bits from the adaptor equalization. 256 linear steps with a step size of 8.75fF. 00000000: 8.75fF ... 11111111: 2.2pF

### 3.3.12 RX Path Status: (RX\_ST: address 0x10F - 0x60F)

**Table 3-48. RX Path Status: (RX\_ST: address 0x10F - 0x60F)**

Bits	Type	Default	Label	Description
7:2		NA		Reserved
1	R	NA	ADPT_FAIL	Adaptive process fail status used for debugging 0 = no failure 1 = fail
0	R	NA	ADPT_START	Adaptive process start status used for debugging 0 = not start 1 = start

### 3.3.13 Channel Live Status1 (CH\_LST1: Address 0x111 - 0x611)

**Table 3-49. Channel Live Status1 (CH\_LST1: Address 0x111 - 0x611)**

Bits	Type	Default	Label	Description
7		NA		Reserved
6	R	NA	FNPLL_LD	DJAT DIG PLL lock detect Status 0 = no PLL lock detected 1 = PLL lock detected
5		NA		Reserved
4	R	NA	FIFO_STAT[2] (JATPOSFD)	DJAT positive frequency status 0 = not detected 1 = positive frequency detected
3	R	NA	FIFO_STAT[1] (JATNEGFD)	DJAT negative frequency status 0 = not detected 1 = negative frequency detected
2:0		NA		Reserved

### 3.3.14 Channel Live Status 2 (CH\_LST2: Address 0x112 - 0x612)

**Table 3-50. Channel Live Status 2 (CH\_LST2: Address 0x112 - 0x612)**

Bits	Type	Default	Label	Description
7:5		NA		Unused
4	R	NA	TOPEN	Transmit path open monitored on TX_LINEP_n and TX_LINEM_n live status
3	R	NA	TLOS	Transmit loss of signal monitored on TX_LINEP_n and TX_LINEM_n live status 1 = loss of signal
2	R	NA	RLOS	Receive loss of signal live status 1 = loss of signal
1:0	R	NA		Reserved
Note: Bits 3 and 4, TLOS and TOPEN, are only valid when the channel is selected to be monitored via the TLOS_CONTROL register at address offset 0x00F.				

### 3.3.15 Channel Interrupt Status 0 (CH\_INTST0: Address 0x114 - 0x614)

**Table 3-51. Channel Interrupt Status 0 (CH\_INTST0: Address 0x114 - 0x614)**

Bits	Type	Default	Label	Description
7	RC	NA	ADPRSTART_INT	Digital Adapter start indication interrupt status 0 = no interrupt 1 = interrupt
6	RC	NA	TXBITOVF_INT	TX bit counter overflow interrupt status 0 = no interrupt 1 = interrupt
5	RC	NA	RXBITOVF_INT	RX bit counter overflow interrupt status 0 = no interrupt 1 = interrupt
4	RC	NA	TXBEOF_INT	TX Bit Error counter overflow interrupt status 0 = no interrupt 1 = interrupt
3	RC	NA	RXBECNTOF_INT	RX Error counter overflow interrupt status 0 = no interrupt 1 = interrupt
2	RC	NA	EXZCNTOF_INT	EXZ counter overflow interrupt status 0 = no interrupt 1 = interrupt
1	RC	NA	BPVCNTOF_INT	BPV counter overflow interrupt status 0 = no interrupt 1 = interrupt
0	RC	NA	LCVCNTOF_INT	LCV counter overflow interrupt status 0 = no interrupt 1 = interrupt



### 3.3.16 Channel Interrupt Status1 (CH\_INTST1: Address 0x115 - 0x615)

**Table 3-52. Channel Interrupt Status1 (CH\_INTST1: Address 0x115 - 0x615)**

Bits	Type	Default	Label	Description
7	RC	NA	AGCOF_INT	AGC overflow interrupt status 0 = no interrupt 1 = interrupt
6	RC	NA	PLLLD_INT	DJAT PLL lock detect interrupt status 0 = no interrupt 1 = interrupt
5	RC	NA	FIFOSTAT_INT[3]	DJAT FIFO overflow interrupt status 0 = no interrupt 1 = interrupt
4	RC	NA	FIFOSTAT_INT[2]	DJAT positive frequency detection status 0 = no interrupt 1 = interrupt
3	RC	NA	FIFOSTAT_INT[1]	DJAT negative frequency detection status 0 = no interrupt 1 = interrupt
2	RC	NA	FIFOSTAT_INT[0]	DJAT FIFO Underflow interrupt status 0 = no interrupt 1 = interrupt
1	RC	NA	EQCOEFOF_INT	Equalization coefficient overflow interrupt status 0 = no interrupt 1 = interrupt
0	RC	NA	EQCOEFUF_INT	Equalization coefficient underflow interrupt status 0 = no interrupt 1 = interrupt

### 3.3.17 Channel Interrupt Status2 (CH\_INTST2: Address 0x116 - 0x616)

**Table 3-53.** Channel Interrupt Status2 (CH\_INTST2: Address 0x116 - 0x616)

Bits	Type	Default	Label	Description
7	RC	0	ADPTFAIL_INT	Digital Adapter fail interrupt status 0 = no interrupt 1 = interrupt
6:5		NA		Reserved
4	RC	0	TOPEN_INT	Transmit path open interrupt status 0 = no interrupt 1 = interrupt
3	RC	0	TLOS_INT	Transmit loss of signal interrupt status 0 = no interrupt 1 = interrupt
2	RC	0	RLOS_INT	Receive loss of signal interrupt status 0 = no interrupt 1 = interrupt
1	RC	0	SECTIMER_INT	Onesec timer rising edge interrupt status 0 = no interrupt 1 = interrupt
0	RC	0	PPMRDY_INT	PPM offset ready interrupt status 0 = no interrupt 1 = interrupt PPM indicating offset register is ready to be read
Note: Bits 3 and 4, TLOS_INT and TOPEN_INT, are only valid when the channel is selected to be monitored via the TLOS_CONTROL register at address offset 0x00F.				

### 3.3.18 Channel Interrupt Enable 0(CH\_INTEN0: 0x118 - 0x618)

**Table 3-54. Channel Interrupt Enable 0(CH\_INTEN0: 0x118 - 0x618)**

Bits	Type	Default	Label	Description
7		NA		Unused
6	RW	0	TXBITOVFINT_EN	TX bit counter overflow interrupt enable 0 = disable 1 = enable
5	RW	0	RXBITOVFINT_EN	RX bit counter overflow interrupt enable 0 = disable 1 = enable
4	RW	0	TXBEOFINT_EN	TX Bit Error counter overflow interrupt enable 0 = disable 1 = enable
3	RW	0	RXBECNTOFINT_EN	RX Bit Error counter overflow interrupt enable 0 = disable 1 = enable
2	RW	0	EXZCNTOFINT_EN	EXZ counter overflow interrupt enable 0 = disable 1 = enable
1	RW	0	BPVCNTOFINT_EN	BPV counter overflow interrupt enable 0 = disable 1 = enable
0	RW	0	LCVCNTOF_INT_EN	LCV counter overflow interrupt enable 0 = disable 1 = enable

### 3.3.19 Channel Interrupt Enable1 (CH\_INTEN1: Address 0x119 - 0x619)

**Table 3-55. Channel Interrupt Enable1 (CH\_INTEN1: Address 0x119 - 0x619)**

Bits	Type	Default	Label	Description
7	RW	0	AGCOFINT_EN	AGCOF detect enable 0 = disable 1 = enable
6	RW	0	PLLLDINT_EN	DJAT PLL lock detect enable 0 = disable 1 = enable
5	RW	0	FIFOSTAT_EN[3]	DJAT FIFO overflow enable 0 = disable 1 = enable
4	RW	0	FIFOSTAT_EN[2]	DJAT positive frequency detection enable 0 = disable 1 = enable
3	RW	0	FIFOSTAT_EN[1]	DJAT negative frequency detection enable 0 = disable 1 = enable
2	RW	0	FIFOSTAT_EN[0]	DJAT FIFO Underflow enable 0 = disable 1 = enable
1	RW	0	EQCOEFOFINT_EN	Equalization coefficient overflow enable 0 = disable 1 = enable
0	RW	0	EQCOEFUFINT_EN	Equalization coefficient underflow enable 0 = disable 1 = enable

### 3.3.20 Channel Interrupt Enable2 (CH\_INTEN2: Address 0x11A - 0x61A)

**Table 3-56. Channel Interrupt Enable2 (CH\_INTEN2: Address 0x11A - 0x61A)**

Bits	Type	Default	Label	Description
7		NA		
6	RW	0	ADPTSTART_EN	Adapter start interrupt enable 0 = disable 1 = enable
5	RW	0	ADPTFAIL_EN	Adapter fail interrupt enable 0 = disable 1 = enable
4	RW	0	TOPENINT_EN	Transmit path open interrupt enable 0 = disable 1 = enable
3	RW	0	TLOSINT_EN	Transmit loss of signal interrupt enable 0 = disable 1 = enable
2	RW	0	RLOSINT_EN	Receive loss of signal interrupt enable 0 = disable 1 = enable
1	RW	0	SECTIMERINT_EN	Onesec timer rising edge interrupt enable 0 = disable 1 = enable
0	RW	0	PPMRDYINT_EN	PPM ready interrupt enable 0 = disable 1 = enable

### 3.3.21 Channel Interrupt Enable3 (CH\_INTEN3: Address 0x11B - 0x61B)

**Table 3-57. Channel Interrupt Enable3 (CH\_INTEN3: Address 0x11B - 0x61B)**

Bits	Type	Default	Label	Description
7		NA		
6		NA		
5	RW	0	ALL_ONESINT_EN	PRBS ALL ones detection interrupt enable 0 = disable 1 = enable
4	RW	0	ALL_ZEROSINT_EN	PRBS All zeros detection interrupt enable 0 = disable 1 = enable
3	RW	0	LOSS_PATN_EN	PRBS loss pattern interrupt enable 0 = disable 1 = enable
2	RW	0	ERRDETINT_EN	PRBS Error detect interrupt enable 0 = disable 1 = enable
1	RW	0	RESYNCINT_EN	PRBS resync interrupt enable 0 = disable 1 = enable
0		NA		Reserved

### 3.3.22 RX Path Encoder/Decoder Control (RXENDEC\_CTRL: 0x11C - 0x61C)

**Table 3-58. RX Path Encoder/Decoder Control (RXENDEC\_CTRL: 0x11C - 0x61C)**

Bits	Type	Default	Label	Description
7:3		NA		
2	RW	1	RXAMI_RAIL	RX Decoder control active when RXDEC_EN is set 0 = AMI decoding 1 = HDB3 or B3ZS decoding.
1	RW	1	RXDEC_EN	RX path decoder enable 0 = Dual rail 1 = NRZ
0				Reserved

### 3.3.23 RX Path PRBS Control 0 (RXPRBS\_CTRL0: Address 0x11E - 0x61E)

**Table 3-59. RX Path PRBS Control 0 (RXPRBS\_CTRL0: Address 0x11E - 0x61E)**

Bits	Type	Default	Label	Description																																				
7:6		NA		Reserved																																				
5:3	RW	0x0	RXAER[2:0]	Auto Error insertion interval setting <table><tr><th>[2]</th><th>[1]</th><th>[0]</th><th>Inserted Error Rate</th></tr><tr><td>0</td><td>0</td><td>0</td><td>No auto inserted errors</td></tr><tr><td>0</td><td>0</td><td>1</td><td>10<sup>-1</sup></td></tr><tr><td>0</td><td>1</td><td>0</td><td>10<sup>-2</sup></td></tr><tr><td>0</td><td>1</td><td>1</td><td>10<sup>-3</sup></td></tr><tr><td>1</td><td>0</td><td>0</td><td>10<sup>-4</sup></td></tr><tr><td>1</td><td>0</td><td>1</td><td>10<sup>-5</sup></td></tr><tr><td>1</td><td>1</td><td>0</td><td>10<sup>-6</sup></td></tr><tr><td>1</td><td>1</td><td>1</td><td>10<sup>-7</sup></td></tr></table>	[2]	[1]	[0]	Inserted Error Rate	0	0	0	No auto inserted errors	0	0	1	10 <sup>-1</sup>	0	1	0	10 <sup>-2</sup>	0	1	1	10 <sup>-3</sup>	1	0	0	10 <sup>-4</sup>	1	0	1	10 <sup>-5</sup>	1	1	0	10 <sup>-6</sup>	1	1	1	10 <sup>-7</sup>
[2]	[1]	[0]	Inserted Error Rate																																					
0	0	0	No auto inserted errors																																					
0	0	1	10 <sup>-1</sup>																																					
0	1	0	10 <sup>-2</sup>																																					
0	1	1	10 <sup>-3</sup>																																					
1	0	0	10 <sup>-4</sup>																																					
1	0	1	10 <sup>-5</sup>																																					
1	1	0	10 <sup>-6</sup>																																					
1	1	1	10 <sup>-7</sup>																																					
2	RW	0	RXAUTO_RSYNC	RX PRBS auto resync 0 = no resync 1 = resync automatically																																				
1		NA		Reserved																																				
0	RW	0	RXMAN_RSYNC	RX PRBS manual resync (reset) PRBS 0 = not resync 1 = manual resync																																				

### 3.3.24 RX Path PRBS Control 1 (RXPRBS\_CTRL1: Address 0x11F - 0x61F)

**Table 3-60. RX Path PRBS Control 1 (RXPRBS\_CTRL1: Address 0x11F - 0x61F)**

Bits	Type	Default	Label	Description
7	RW	0	RXOUT_CTRL	RXPRBS pattern control 0 = not inverted PRBS pattern 1 = inverted PRBS pattern
6:5	RW	0	RXMODE_SEL[1:0]	PRBS mode control 00 (11) = bypass mode 01 = generator mode 10 = detector
4	RW	0	RXERRIN	PRBS error insertion, cleared upon error insertion 0 = error insertion disabled 1 = insert an error
3	RW	0	RXFRAM_EN	PRBS framed pattern generation control 0 = generate unframed pattern 1 = generate framed pattern (for DS3 mode)
2	RW	0	RXZERO_LMT	PRBS zero limit control 0 = normal mode 1 = 14 consecutive zeros suppression mode
1	RW	1	RXPAT_CTRL	PRBS/fixed pattern control 0 = fixed pattern generator 1 = PRBS pattern generator
0	RW	0	RXPRBS_EN	RXPRBS enable 1 = enable 0 = disable

### 3.3.25 RX Path PRBS Control 2 (RXPRBS\_CTRL2: Address 0x120 - 0x620)

**Table 3-61. RX Path PRBS Control 2 (RXPRBS\_CTRL2: Address 0x120 - 0x620)**

Bits	Type	Default	Label	Description
7:5		0x1		
4:0	RW	0x6	RXTAPA[4:0]	Defines the first back stage in PRBS generation



### 3.3.26 RX Path PRBS Control 3 (RXPRBS\_CTRL3: Address 0x121 - 0x621)

**Table 3-62. RX Path PRBS Control 3 (RXPRBS\_CTRL3: Address 0x121 - 0x621)**

Bits	Type	Default	Label	Description
7:5		NA		
4:0	RW	0x11	RXTAPB[4:0]	Define the second back stage in PRBS generation

### 3.3.27 RX Path PRBS Control 4 (RXPRBS\_CTRL4: Address 0x122 - 0x622)

**Table 3-63. RX Path PRBS Control 4 (RXPRBS\_CTRL4: Address 0x122 - 0x622)**

Bits	Type	Default	Label	Description
7:3		NA		
2	RW	0	RXOVF_FREEZE	RX Bit Counter (RXBITCNT_STn) and Bit Error (RXBECNT_STn) saturation mode selection 0 = roll count to zero after saturation 1 = freeze count at saturation until register is read
1	RW	0	RXPRBS_ONESEC	RX Bit Counter (RXBITCNT_STn) and Bit Error (RXBECNT_STn) read mode selection 0 = live status value 1 = 1-sec value
0		0		Reserved
<b>Warning:</b> Both bits, RXBITCNT_SEL and RXBECNT_SEL must be set or cleared together for proper operation.				

### 3.3.28 RX PRBS Status (CH\_INTST3: Address 0x123 - 0x623)

**NOTE:**

Interrupts must be enabled in the CH\_INTEN3 register at offset 0xn1B for the bits to properly function

**Table 3-64. RX PRBS Status (CH\_INTST3: Address 0x123 - 0x623)**

Bits	Type	Default	Label	Description
7:6		0		Unused
5	RC	0	RXALL_ONES_INT	PRBS detects 32 consecutive ones 0 = no interrupt 1 = interrupt
4	RC	0	RXALL_ZEROS_INT	PRBS detects 32 consecutive zeros 0 = no interrupt 1 = interrupt
3	RC	0	RXLOSS_PTRN_INT	PRBS detector received more than 6 errors in a 64 bit window (pattern sync is lost) 0 = no interrupt 1 = interrupt
2	RC	0	RXERRDET_INT	PRBS detects mismatch between incoming data and recovered data 0 = no interrupt 1 = interrupt
1:0		NA		Reserved

### 3.3.29 LCV Counter Control0 (LCV\_CTRL0: Address 0x124 - 0x624)

**Table 3-65. LCV Counter Control0 (LCV\_CTRL0: Address 0x124 - 0x624)**

Bits	Type	Default	Label	Description																				
7:6		0		Unused																				
4:3	RW	11b	BPVCNT_CFG[1:0]	BPV counter configuration: <table><tr><th colspan="3">Bit Position</th></tr><tr><th>[4]</th><th>[3]</th><th>Description</th></tr><tr><td>X</td><td></td><td>ZVIOL are added to the BPV counter</td></tr><tr><td></td><td>X</td><td>BPV are added to the BPV counter</td></tr></table>	Bit Position			[4]	[3]	Description	X		ZVIOL are added to the BPV counter		X	BPV are added to the BPV counter								
Bit Position																								
[4]	[3]	Description																						
X		ZVIOL are added to the BPV counter																						
	X	BPV are added to the BPV counter																						
2:0	RW	111b	LCVCNT_CFG[2:0]	LCV counter configuration: <table><tr><th colspan="4">Bit Position</th></tr><tr><th>[2]</th><th>[1]</th><th>[0]</th><th>Description</th></tr><tr><td>X</td><td></td><td></td><td>ZVIOL are added to the LCV counter</td></tr><tr><td></td><td>X</td><td></td><td>BPV are added to the LCV counter</td></tr><tr><td></td><td></td><td>X</td><td>EXZ are added to the LCV counter</td></tr></table>	Bit Position				[2]	[1]	[0]	Description	X			ZVIOL are added to the LCV counter		X		BPV are added to the LCV counter			X	EXZ are added to the LCV counter
Bit Position																								
[2]	[1]	[0]	Description																					
X			ZVIOL are added to the LCV counter																					
	X		BPV are added to the LCV counter																					
		X	EXZ are added to the LCV counter																					

### 3.3.30 LCV Counter Control1 (LCV\_CTRL1: Address 0x125 - 0x625)

**Table 3-66. LCV Counter Control1 (LCV\_CTRL1: Address 0x125 - 0x625)**

Bits	Type	Default	Label	Description
7:4		NA		Reserved
3	RW	0	LCVZERO_MODE	0 = every 3(4) consecutive 0's reported as 1 error 1 = multiple 3(4) consecutive zeros reported as 1 error.
2	RW	0	EXZCNT_SEL	EXZ counter read value selection 0 = real time value 1 = 1-sec. value <b>NOTE:</b> To configure for 1-sec. Value, bit SECLATMODE in register SECTIMCTRL must be set to one.
1	RW	0	BPVCNT_SEL	BPV counter read mode selection 0 = real time value 1 = 1-sec. value <b>NOTE:</b> To configure for 1-sec. Value, bit SECLATMODE in register SECTIMCTRL must be set to one.
0	RW	0	LCVCNT_SEL	LCV counter read mode selection 0 = real time value 1 = 1-sec. value <b>NOTE:</b> To configure for 1-sec. Value, bit SECLATMODE in register SECTIMCTRL must be set to one.

### 3.3.31 RX Path Fixed Pattern Control 0 (RXUSR\_PAT0: Address 0x126 - 0x626)

**NOTE:**

For -11 devices, refer to the product bulletin.  
The RXUSR\_PATn registers are big endian.

**Table 3-67. RX Path Fixed Pattern Control 0 (RXUSR\_PAT0: Address 0x126 - 0x626)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	RXUSR_PAT[7:0]	RX fixed pattern bits 7:0

### 3.3.32 RX Path Fixed Pattern Control 1 (RXUSR\_PAT1: Address 0x127 - 0x627)

**Table 3-68. RX Path Fixed Pattern Control 1 (RXUSR\_PAT1: Address 0x127 - 0x627)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	RXUSR_PAT[15:8]	RX fixed pattern bits 15:8

### 3.3.33 RX Path Fixed Pattern Control 2 (RXUSR\_PAT2: Address 0x128 - 0x628)

**Table 3-69. RX Path Fixed Pattern Control 2 (RXUSR\_PAT2: Address 0x128 - 0x628)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	RXUSR_PAT[23:16]	RX fixed pattern bits 23:16

### 3.3.34 RX Path Fixed Pattern Control 3 (RXUSR\_PAT3: Address 0x129 - 0x629)

**Table 3-70. RX Path Fixed Pattern Control 3 (RXUSR\_PAT3: Address 0x129 - 0x629)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	RXUSR_PAT[31:24]	RX fixed pattern bits 31:24

### 3.3.35 RX Path Bit Error Counter State 0 (RXBECNT\_ST0: Address 0x12C - 0x62C)

**NOTE:**

To properly read the Bit Error and Bit counters, the RXBECNT\_ST0 at address offset 0xn30 must be read first. This will latch the remainder of the Bit counters and latch the Bit Error counters.

**Table 3-71. RX Path Bit Error Counter State 0 (RXBECNT\_ST0: Address 0x12C - 0x62C)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBECNT_ST[7:0]	Bit Error counter status bits 7:0

### 3.3.36 RX Path Bit Error Counter State 1 (RXBECNT\_ST1: Address 0x12D - 0x62D)

**Table 3-72. RX Path Bit Error Counter State 1 (RXBECNT\_ST1: Address 0x12D - 0x62D)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBECNT_ST[15:8]	Bit Error counter status bits 15:8

### 3.3.37 RX Path Bit Error Counter State 2 (RXBECNT\_ST2: Address 0x12E - 0x62E)

**Table 3-73. RX Path Bit Error Counter State 2 (RXBECNT\_ST2: Address 0x12E - 0x62E)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBECNT_ST[23:16]	Bit Error counter status bits 23:16

### 3.3.38 RX Path Bit Error Counter State 3 (RXBECNT\_ST3: Address 0x12F - 0x62F)

**Table 3-74. RX Path Bit Error Counter State 3 (RXBECNT\_ST3: Address 0x12F - 0x62F)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBECNT_ST[31:24]	Bit Error counter status bits 31:24

### 3.3.39 RX Path Bit Counter State 0 (RXBITCNT\_ST0: Address 0x130 - 0x630)

**Table 3-75. RX Path BIT Counter State 0 (RXBITCNT\_ST0: Address 0x130 - 0x630)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBITCNT_ST[7:0]	BIT counter status bits 7:0

### 3.3.40 RX Path Bit Counter State 1 (RXBITCNT\_ST1: Address 0x131 - 0x631)

**Table 3-76. RX Path BIT Counter State 1 (RXBITCNT\_ST1: Address 0x131 - 0x631)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBITCNT_ST[15:8]	BIT counter status bits 15:8

### 3.3.41 RX Path Bit Counter State 2 (RXBITCNT\_ST2: Address 0x132 - 0x632)

**Table 3-77. RX Path BIT Counter State 2 (RXBITCNT\_ST2: Address 0x132 - 0x632)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBITCNT_ST[23:16]	BIT counter status bits 23:16

### 3.3.42 RX Path Bit Counter State 3 (RXBITCNT\_ST3: Address 0x133 - 0x633)

**Table 3-78. X Path BIT Counter State 3 (RXBITCNT\_ST3: Address 0x133 - 0x633)**

Bits	Type	Default	Label	Description
7:0	RC	NA	RXBITCNT_ST[31:24]	BIT counter status bits 31:24

### 3.3.43 LCV Counter State 0 (LCVCNT1\_ST0: Address 0x134, 0x234, 0x334, 0x434, 0x534, 0x634)

**NOTE:**

To properly read the LCV counters, the LCVCNT1\_ST0 at address offset 0xn34 must be read first. This will latch the remainder of the LCV counters.

**Table 3-79. LCV Counter State 0 (LCVCNT1\_ST0: Address 0x134, 0x234, 0x334, 0x434, 0x534, 0x634)**

Bits	Type	Default	Label	Description
7:0	RC	NA	LCVCNT_ST[7:0]	LCV counter1 bits 7:0

### 3.3.44 LCV Counter State 1 (LCVCNT1\_ST1: Address 0x135 - 0x635)

**Table 3-80. LCV Counter State 1 (LCVCNT1\_ST1: Address 0x135 - 0x635)**

Bits	Type	Default	Label	Description
7:0	RC	NA	LCVCNT_ST[15:8]	LCV counter1 status bits 15:8

### 3.3.45 LCV Counter State 2 (LCVCNT1\_ST2: Address 0x136 - 0x636)

**Table 3-81. LCV Counter State 2 (LCVCNT1\_ST2: Address 0x136 - 0x636)**

Bits	Type	Default	Label	Description
7:0	RC	NA	LCVCNT_ST[23:16]	LCV counter1 bits 23:16

**NOTE:**

To properly read the BPV counters, the BPVCNT\_ST0 at address offset 0xn38 must be read first. This will latch the remainder of the BPV counters.

### 3.3.46 BPV Counter State 0 (BPVCNT\_ST0: Address 0x138 - 0x638)

**Table 3-82. BPV Counter State 0 (BPVCNT\_ST0: Address 0x138 - 0x638)**

Bits	Type	Default	Label	Description
7:0	RC	NA	BPVCNT_ST[7:0]	BPV counter bits 7:0

### 3.3.47 BPV Counter State 1 (BPVCNT\_ST1: Address 0x139 - 0x639)

**Table 3-83. BPV Counter State 1 (BPVCNT\_ST1: Address 0x139 - 0x639)**

Bits	Type	Default	Label	Description
7:0	RC	NA	BPVCNT_ST[15:8]	BPV counter status bits 15:8



### 3.3.48 BPV Counter State 2 (BPVCNT\_ST2: Address 0x13A - 0x63A)

**Table 3-84. BPV Counter State 2 (BPVCNT\_ST2: Address 0x13A - 0x63A)**

Bits	Type	Default	Label	Description
7:0	RC	NA	BPVCNT2_ST[23:16]	BPV counter bits 23:16

**NOTE:**

To properly read the EXZ counters, the EXZCNT\_ST0 at address offset 0xn3C must be read first. This will latch the remainder of the EXZ counters.

### 3.3.49 EXZ Counter State 0 (EXZCNT\_ST0: Address 0x13C - 0x63C)

**Table 3-85. EXZ Counter State 0 (EXZCNT\_ST0: Address 0x13C - 0x63C)**

Bits	Type	Default	Label	Description
7:0	RC	NA	EXZCNT_ST[7:0]	EXZ counter bits 7:0

### 3.3.50 EXZ Counter State 1 (EXZCNT\_ST1: Address 0x13D - 0x63D)

**Table 3-86. EXZ Counter State 1 (EXZCNT\_ST1: Address 0x13D - 0x63D)**

Bits	Type	Default	Label	Description
7:0	RC	NA	EXZCNT_ST[15:8]	EXZ counter status bits 15:8

### 3.3.51 EXZ Counter State 2 (EXZCNT\_ST2: Address 0x13E - 0x63E)

**Table 3-87. EXZ Counter State 2 (EXZCNT\_ST2: Address 0x13E - 0x63E)**

Bits	Type	Default	Label	Description
7:0	RC	NA	EXZCNT_ST[23:16]	EXZ counter bits 23:16

### 3.3.52 TX Path PRBS Control 0 (TXPRBS\_CTRL0: Address 0x140 - 0x640)

**Table 3-88. TX Path PRBS Control 0 (TXPRBS\_CTRL0: Address 0x140 - 0x640)**

Bits	Type	Default	Label	Description																																				
7:6		NA		Reserved																																				
5:3	RW	0x0	TXAER[2:0]	Auto Error insertion interval setting: <table><tr><th>[2]</th><th>[1]</th><th>[0]</th><th>Inserted Error Rate</th></tr><tr><td>0</td><td>0</td><td>0</td><td>No auto inserted errors</td></tr><tr><td>0</td><td>0</td><td>1</td><td>10<sup>-1</sup></td></tr><tr><td>0</td><td>1</td><td>0</td><td>10<sup>-2</sup></td></tr><tr><td>0</td><td>1</td><td>1</td><td>10<sup>-3</sup></td></tr><tr><td>1</td><td>0</td><td>0</td><td>10<sup>-4</sup></td></tr><tr><td>1</td><td>0</td><td>1</td><td>10<sup>-5</sup></td></tr><tr><td>1</td><td>1</td><td>0</td><td>10<sup>-6</sup></td></tr><tr><td>1</td><td>1</td><td>1</td><td>10<sup>-7</sup></td></tr></table>	[2]	[1]	[0]	Inserted Error Rate	0	0	0	No auto inserted errors	0	0	1	10 <sup>-1</sup>	0	1	0	10 <sup>-2</sup>	0	1	1	10 <sup>-3</sup>	1	0	0	10 <sup>-4</sup>	1	0	1	10 <sup>-5</sup>	1	1	0	10 <sup>-6</sup>	1	1	1	10 <sup>-7</sup>
[2]	[1]	[0]	Inserted Error Rate																																					
0	0	0	No auto inserted errors																																					
0	0	1	10 <sup>-1</sup>																																					
0	1	0	10 <sup>-2</sup>																																					
0	1	1	10 <sup>-3</sup>																																					
1	0	0	10 <sup>-4</sup>																																					
1	0	1	10 <sup>-5</sup>																																					
1	1	0	10 <sup>-6</sup>																																					
1	1	1	10 <sup>-7</sup>																																					
2	RW	0	TXAUTO_RSYNC	TX PRBS auto resync 0 = no resync 1 = resync automatically																																				
1		NA		Reserved																																				
0	RW	0	TXMAN_RSYNC	TX PRBS manual resync 0 = not resync 1 = manual resync																																				

### 3.3.53 TX Path PRBS Control 1 (TXPRBS\_CTRL1: Address 0x141 - 0x641)

**Table 3-89. TX Path PRBS Control 1 (TXPRBS\_CTRL1: Address 0x141 - 0x641)**

Bits	Type	Default	Label	Description
7	RW	0	TXOUT_CTRL	TXPRBS pattern control 0 = not inverted PRBS pattern 1 = inverted PRBS pattern
6:5	RW	0x0	TXMODE_SEL[1:0]	PRBS mode control 00 (11) = bypass mode 01 = generator mode 10 = detector
4	RW	0	TXERRIN	PRBS error insertion, cleared upon error insertion 0 = error insertion enabled 1 = insert an error
3	RW	0	TXFRAM_EN	PRBS framed pattern generation control 0 = generate unframed pattern 1 = generate framed pattern (for DS3 mode)
2	RW	0	TXZERO_LMT	PRBS zero limit control 0 = normal 1 = 14 consecutive zeros suppression mode
1	RW	1	TXPAT_CTRL	PRBS/fixed pattern control 0 = fixed pattern generator 1 = PRBS pattern generator
0	RW	0	TXPRBS_EN	PRBS block enable 0 = disable 1 = enable

### 3.3.54 TX Path PRBS Control 2 (TXPRBS\_CTRL2: Address 0x142 - 0x642)

**Table 3-90. TX Path PRBS Control 2 (TXPRBS\_CTRL2: Address 0x142 - 0x642)**

Bits	Type	Default	Label	Description
7:5		0		Unused
4:0	RW	0x16	TXTAPA[4:0]	Defines the first back stage in PRBS generation

### 3.3.55 TX Path PRBS Control 3 (TXPRBS\_CTRL3: Address 0x143 - 0x643)

**Table 3-91. TX Path PRBS Control 3 (TXPRBS\_CTRL3: Address 0x143 - 0x643)**

Bits	Type	Default	Label	Description
7:5		0		Unused
4:0	RW	0x11	TXTAPB[4:0]	Define the second back stage in PRBS generation

### 3.3.56 TX Path PRBS Control 4 (TXPRBS\_CTRL4: Address 0x144 - 0x644)

**Table 3-92. TX Path PRBS Control 4 (TXPRBS\_CTRL4: Address 0x144 - 0x644)**

Bits	Type	Default	Label	Description
7:3		0		Unused
2	RW	0	TXOVF_FREEZE	TX Bit Counter (TXBITCNT_STn) and Bit Error (RXBECNT_STn) saturation mode selection 0 = roll count to zero after saturation 1 = freeze count at saturation until register is read
1	RW	0	TXPRBS_ONESEC	TX Bit Counter (TXBITCNT_STn) and Bit Error (TXBECNT_STn) read mode selection 0 = live status value 1 = 1-sec value
0		NA		Reserved

### 3.3.57 TX PRBS Interrupt Status (CH\_INTST4: Address 0x145 - 0x645)

**Table 3-93. TX PRBS Interrupt Status (CH\_INTST4: Address 0x145 - 0x645)**

Bits	Type	Default	Label	Description
7:6		0		Unused
5	RC	0	TXALL_ONES_INT	PRBS detects 32 consecutive ones 0 = no interrupt 1 = interrupt
4	RC	0	TXALL_ZEROS_INT	PRBS detects 32 consecutive zeros 0 = no interrupt 1 = interrupt
3	RC	0	TXLOSS_PTRN_INT	PRBS detector received more than 6 errors in a 64 bit window (pattern sync is lost) 0 = no interrupt 1 = interrupt
2	RC	0	TXERRDET_INT	PRBS detects mismatch between incoming data and recovered data 0 = no interrupt 1 = interrupt
1:0		NA		Reserved

### 3.3.58 TX Path AIS Control (TXAIS\_CTRL: Address 0x147 - 0x647)

**Table 3-94. TX Path AIS Control (TXAIS\_CTRL: Address 0x147 - 0x647)**

Bits	Type	Default	Label	Description
7:1		0		Unused
0	RW	0	TXAIS_EN	<p>Enable bit for TX AIS.</p> <p>0: TX AIS disabled 1: TX AIS enabled</p> <p>When TAIS is asserted, an AIS replaces the transmit data at TPOS and TNEG. Along with the E3 type of AIS signal (all 1s), a framed DS3 AIS signal is supported. In three-level signal form, this is a continuously alternating positive and negative pulse stream, as if the transmit data were a continuous string of logical 1s.</p> <p>The TAIS pin has the same data latency as the TX data pins and can be used to replace single symbols within a data stream. When the encoder is disabled (TXENC_EN = 0), the TAIS mode maintains the proper phase, based on the polarity of the last 1 received.</p> <p>The AIS signal follows the same path as the TX data during line or source (local) loopback.</p>

### 3.3.59 TX Path Fixed Pattern Control 0 (TXUSR\_PAT0: Address 0x148 - 0x648)

**NOTE:**

Refer to product bulletin for -11 devices.  
The TXUSR\_PAT registers are big endian.

**Table 3-95. TX Path Fixed Pattern Control 0 (TXUSR\_PAT0: Address 0x148 - 0x648)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	TXUSR_PAT[7:0]	TX fixed pattern bits 7:0

### 3.3.60 TX Path Fixed Pattern Control 1 (TXUSR\_PAT1: Address 0x149 - 0x649)

**Table 3-96. TX Path Fixed Pattern Control 1 (TXUSR\_PAT1: Address 0x149 - 0x649)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	TXUSR_PAT[15:8]	TX fixed pattern bits 15:8

### 3.3.61 TX Path Fixed Pattern Control 2 (TXUSR\_PAT2: Address 0x14A - 0x24A)

**Table 3-97. TX Path Fixed Pattern Control 2 (TXUSR\_PAT2: Address 0x14A - 0x24A)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	TXUSR_PAT[23:16]	TX fixed pattern bits 23:16

### 3.3.62 TX Path Fixed Pattern Control 3 (TXUSR\_PAT3: Address 0x14B - 0x64B)

**Table 3-98. TX Path Fixed Pattern Control 3 (TXUSR\_PAT3: Address 0x14B - 0x64B)**

Bits	Type	Default	Label	Description
7:0	RW	0x00	TXUSR_PAT[31:24]	TX fixed pattern bits 31:24

**NOTE:**

To properly read the Bit Error and Bit counters, the TXBITCNT\_ST0 at address offset 0xn50 must be read first. This will latch the remainder of the Bit counters and latch the Bit Error counters.

### 3.3.63 TX Path Bit Error Counter State 0 (TXBECNT\_ST0: Address 0x14C - 0x64C)

**Table 3-99. TX Path Bit Error Counter State 0 (TXBECNT\_ST0: Address 0x14C - 0x64C)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBECNT_ST[7:0]	Bit Error counter status bits 7:0

### 3.3.64 TX Path Bit Error Counter State 1 (TXBECNT\_ST1: Address 0x14D - 0x64D)

**Table 3-100. TX Path Bit Error Counter State 1 (TXBECNT\_ST1: Address 0x14D - 0x64D)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBECNT_ST[15:8]	Bit Error counter status bits 15:8

### 3.3.65 TX Path Bit Error Counter State 2 (TXBECNT\_ST2: Address 0x14E - 0x64E)

**Table 3-101. TX Path Bit Error Counter State 2 (TXBECNT\_ST2: Address 0x14E - 0x64E)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBECNT_ST[23:16]	Bit Error counter status bits 23:16

### 3.3.66 TX Path Bit Error Counter State 3 (TXBECNT\_ST3: Address 0x14F - 0x64F)

**Table 3-102. TX Path Bit Error Counter State 3 (TXBECNT\_ST3: Address 0x14F - 0x64F)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBECNT_ST[31:24]	Bit Error counter status bits 31:24

### 3.3.67 TX Path Bit Counter State 0 (TXBITCNT\_ST0: Address 0x150 - 0x650)

**Table 3-103. TX Path BIT Counter State 0 (TXBITCNT\_ST0: Address 0x150 - 0x650)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBITCNT_ST[7:0]	BIT counter status bits 7:0

### 3.3.68 TX Path Bit Counter State 1 (TXBITCNT\_ST1: Address 0x151 - 0x651)

**Table 3-104. TX Path BIT Counter State 1 (TXBITCNT\_ST1: Address 0x151 - 0x651)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBITCNT_ST[15:8]	BIT counter status bits 15:8



### 3.3.69 TX Path Bit Counter State 2 (TXBITCNT\_ST2: Address 0x152 - 0x652)

**Table 3-105. TX Path BIT Counter State 2 (TXBITCNT\_ST2: Address 0x152 - 0x652)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBITCNT_ST[23:16]	BIT counter status bits 23:16

### 3.3.70 TX Path Bit Counter State 3 (TXBITCNT\_ST3: Address 0x153 - 0x653)

**Table 3-106. TX Path BIT Counter State 3 (TXBITCNT\_ST3: Address 0x153 - 0x653)**

Bits	Type	Default	Label	Description
7:0	RC	NA	TXBITCNT_ST[31:24]	BIT counter status bits 31:24

### 3.3.71 TX Path Encoder/Decoder Control (TXENDEC\_CTRL: Address 0x155 - 0x655)

**Table 3-107. TX Path Encoder/Decoder Control (TXENDEC\_CTRL: Address 0x155 - 0x655)**

Bits	Type	Default	Label	Description
7:3		NA		
2	RW	1	TXAMI_RAIL	TX Decoder and Encoder control 0 = normal mode 1 = substitute consecutive zeros depending on HDB3 or B3ZS encoding.
1				Reserved
0	RW	1	TXENC_EN	TX path encoder enable 0 = disable 1 = enable <b>Note:</b> The ENENCDEC pin must either be left unconnected or held high for this bit to usable while in the software mode. Also, when this bit is set, the ENENCDEC pin may be used to control this function.

### 3.3.72 RLOS Control (RLOS\_CTRL: Address 0x156, 0x256 - 0x656)

**Table 3-108. RLOS Control (RLOS\_CTRL: Address 0x156, 0x256 - 0x656)**

Bits	Type	Default	Label	Description
7:3		NA		
2	RW	0	P20_MODE	LOS defect clear 0 = 33% average pulse density clears defect 1 = 20% average pulse density clears defect
1		NA		Reserved
0	RW	0	LOSF_MODE	0 = RLOS defect mode 1 = RLOS failure mode enabled, defect integrated over time. 2.5 seconds to declare and 10 seconds w/o RLOS defect to clear failures Independent of line rate mode selected - DS3/E3/STS-1.

### 3.3.73 Clock Offset Indicator Control (COI\_CTRL: Address 0x157, 0x257 - 0x657)

**Table 3-109. Clock Offset Indicator Control (COI\_CTRL: Address 0x157, 0x257 - 0x657)**

Bits	Type	Default	Label	Description
7:1		NA		Reserved
0	RW	0	COI_EN	PPM Enable 0 = disabled 1 = enabled

### 3.3.74 Clock OFFSET Indicator(COI\_OFFSET1: Address 0x158 - 0x658)

**Table 3-110. Clock OFFSET Indicator (COI\_OFFSET1: Address 0x158 - 0x658)**

Bits	Type	Default	Label	Description
7	R	NA	COI_VALID	<u>PPM valid:</u> if '1' => indicates the PPM offset value is a valid value; if '0' => indicates that the offset is greater than 127 ppm and the value isn't valid.
6:0	R	NA	COI_OFFSET	PPM offset status [6:0] [6:0] <u>PPM offset:</u> value between the two clocks ranging from 0 to 127 ppm +/- 1 ppm

### 3.3.75 Clock OFFSET Indicator2(COI\_OFFSET2: Address 0x159 - 0x659)

**Table 3-111. Clock OFFSET Indicator2(COI\_OFFSET2: Address 0x159 - 0x659)**

Bits	Type	Default	Label	Description
7:1		0		Unused
0	R	NA	COI_POLARITY	<u>Polarity bit:</u> indicates which clock is running faster. '0' => clock A, '1' => clock B.

### 3.3.76 JAT Control (JATCTRL: Address 0x15B - 0x65B)

**Table 3-112. JAT Control (JATCTRL: Address 0x15B - 0x65B)**

Bits	Type	Default	Label	Description
7	RW	0	IN_SMP	Control bit selecting sampling edge for incoming data 0 = falling edge of DJAT input clock 1 = rising edge of DJAT input clock
6	RW	0	OUT_SMP	Control bit selecting edge for sending out outgoing data 0 = falling edge of DJAT output clock 1 = rising edge of DJAT output clock
5:4		NA		Reserved
3	RW	1	JAT_EN	Control Bit for enabling DJAT 0 = DJAT disabled 1 = DJAT enabled
2:1				Reserved
0	RW	1	PDB_JAT	Master Power-down and reset all digital DJAT logic except DJAT control bits 0 = DJAT powered down 1 = DJAT powered up

### 3.3.77 JAT Monitor2 (JATnMON2: Address 0x15F - 0x65F)

**Table 3-113. JAT Monitor2 (JATnMON2: Address 0x15F - 0x65F)**

Bits	Type	Default	Label	Description
7	R	NA	FNPLL_LD	Status bits of fractional N PLL (1= in lock, 0 = out of lock)
6:0		NA		Reserved

### 3.3.78 JAT Control (JATnCTRL1: Address 0x161 - 0x661)

**Table 3-114. JAT Control (JATnCTRL1: Address 0x161 - 0x661)**

Bits	Type	Default	Label	Description
7:2		0		Unused
1	RW	0	RX_EDGE	This bit controls the edge of RXCLK to the framer that is used to drive the RXDATA. It is only effective when the DJAT is not in the RX path. 1 = falling edge 0 = rising edge
0	RW	0	TX_EDGE	This bit controls the edge of TXCLK from the framer that is used to sample the TXDATA. It is only effective when the DJAT is not in the TX path. 1 = falling edge 0 = rising edge





## 4.0 Product Specification

### 4.1 Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
VDD	Power Supply	-0.25	4.6	V
V <sub>i</sub>	Voltage on any signal pin	-0.5	VDD + 0.5	V
T <sub>s</sub>	Storage temperature	-40	125	°C
T <sub>j</sub>	Junction temperature	—	125	°C
Θ <sub>ja</sub> (PBGA 452-pin)	Thermal resistance	—	20	°C/W
Θ <sub>ja</sub> (PBGA 280-pin)	Thermal resistance	—	24	°C/W
---	Static discharge voltage	TBD	TBD	V
---	Latch-up current	TBD	TBD	mA

### 4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions (1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
VDD33	3.3V Power supply	3.135	3.465	V
VDD18	1.8V Power supply	1.71	1.89	V
Tamb	Ambient operating temperature	-40	85	°C
V <sub>ih</sub>	Input high voltage, TTL	2.0	VDD + 0.25	V
V <sub>il</sub>	Input low voltage, TTL	-0.25	0.8	V
V <sub>h</sub>	Input hysteresis	0.3	—	V
V <sub>th</sub>	Input high threshold voltage, hysteresis	0.7 x VDD	VDD + 0.25	V

**Table 4-2. Recommended Operating Conditions (2 of 2)**

$V_{tl}$	Input low threshold voltage, hysteresis	0	$0.3 \times V_{DD}$	V
$T_{vsol}$	Vapor phase soldering temperature, 1 minute	—	220	°C
$T_{st}$	Storage temperature	-40	125	°C

## 4.3 DC Characteristics

**Table 4-3. DC Characteristics**

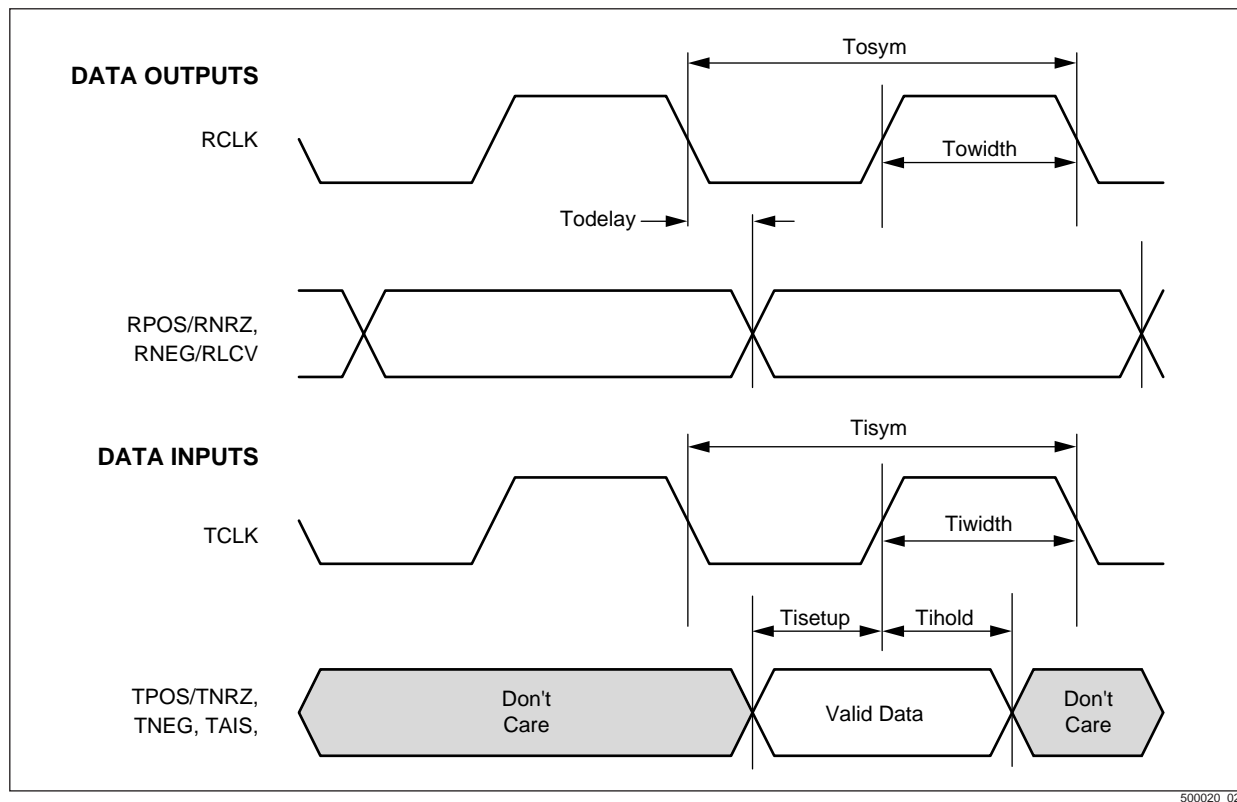
Parameter	Conditions	Min	Nom	Max	Units
$V_{ih}$ high threshold	Digital inputs	2.0		$1.8/3.3 + 0.3$	V
$V_{il}$ low threshold	Digital inputs	-0.3		0.8	V
$V_{oh}$ high threshold	Digital outputs, $I_{oh} = -4mA$	2.4		—	V
$V_{ol}$ low threshold	Digital outputs, $I_{ol} = 4mA$	—		0.4	V
$I_{Leak}$	0V = digital $V_{in} = V_{DD}$	-10		200	µA
Input Capacitance	—	—		10	pF
Load Capacitance	Digital outputs	—		15	pF

## 4.4 AC Characteristics - Logic Timing

**Table 4-4. AC Characteristics – Logic Timing**

Parameter	Conditions	Min	Nom	Max	Units
Tosym, Tisym RCLK and TCLK	E3 DS3 STS-1	—	29.10 22.35 19.29	—	ns
Clock duty cycle	Towidth / Tosym, RCLK Tiwidth / Tisym, TCLK Tiwidth / Tisym, REFCLK Tiwidth / Tisym 19.44 MHz +/- 20 ppm clock	45 30 40 45	—	55 70 60 55	%
Todelay	—	—	—	3	ns
Tisetaup	TPOS / TNRZ, TNEG, TAIS	4	—	—	ns
Tihold	TPOS / TNRZ, TNEG, TAIS	0	—	—	ns
General Notes: 1. The description applies to the E3, DS3, and STS-1 clock rates and other parameters such as pulse width, set-up time, hold time, and duty cycle. 2. The timing diagram, illustrated in Figure 4-1, describes the logical relationship between various clock, data signals, and parameter values. 3. AC timings are based on 80 pF load.					



**Figure 4-1. Timing Diagram**

## 4.5 External Reference Timing Sources

**Table 4-5. External Reference Timing Sources**

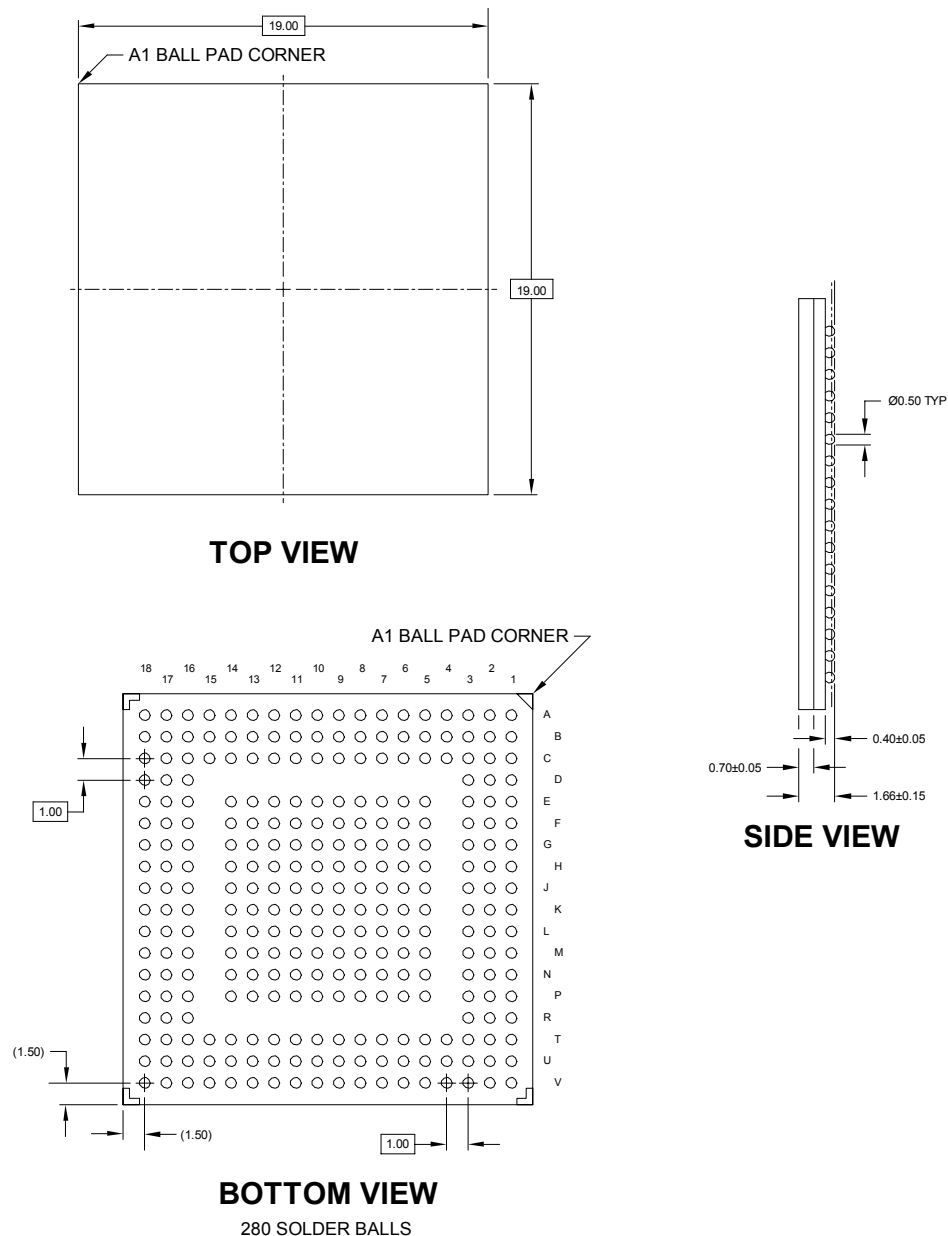
Interface Pins	Required External Timing Source	Specification		
		Frequency (1)	Jitter	
			Jitter Amplitude (2)	Jitter Measurement Frequency Bandwidth
XTAL_IN1, XTAL_IN2	19.44 MHz Crystal	19.44 MHz +/- 10 ppm	(3)	(3)
STS1_REFCLK (Input) (4)	STS-1 Reference Clock	51.84 MHz +/- 20 ppm	NA	NA
DS3_REFCLK (Input) (4)	DS3 Reference Clock	44.736 MHz +/- 20 ppm	0.005 UIpp 0.010 UIpp	30 kHz to 400 kHz 10 Hz to 400 kHz
E3_REFCLK (Input) (4)	E3 Reference Clock	34.368 MHz +/- 20 ppm	0.010 UIpp 0.060 UIpp	10 kHz to 800 kHz 10 Hz to 800 kHz
CLK19P44_IO (Input) (4)	19.44 MHz Reference Clock	19.44 MHz +/- 20 ppm	(3)	(3)
<p>Operation Notes:</p> <ol style="list-style-type: none"> <li>1. The specified frequency accuracy in parts per million (ppm) must not be exceeded over temperature, time (operating life), load, and vibration.</li> <li>2. The jitter amplitude requirements for all external timing sources must not be exceeded over temperature, time (operating life), load, and vibration; and the values specified in this table represent 20 percent of the intrinsic jitter allowed by the standard G.751 for E3 and the standard TR 54014 for DS3.</li> <li>3. The jitter component of the 19.44 MHz crystal or the external 19.44 MHz reference clock must be small enough to ensure that the CLAD will generate clocks on the STS1_REFCLK, DS3_REFCLK, and E3_REFCLK output pins that meet the same jitter requirements as the corresponding external reference clocks specified in this table.</li> <li>4. Do not connect these external timing sources to the indicated pins if these pins are configured as output pins.</li> </ol>				

## 4.6 Package Specification

### 4.6.1 M28352/M28353/M28354/M28356 (M2835x) Mechanical Description

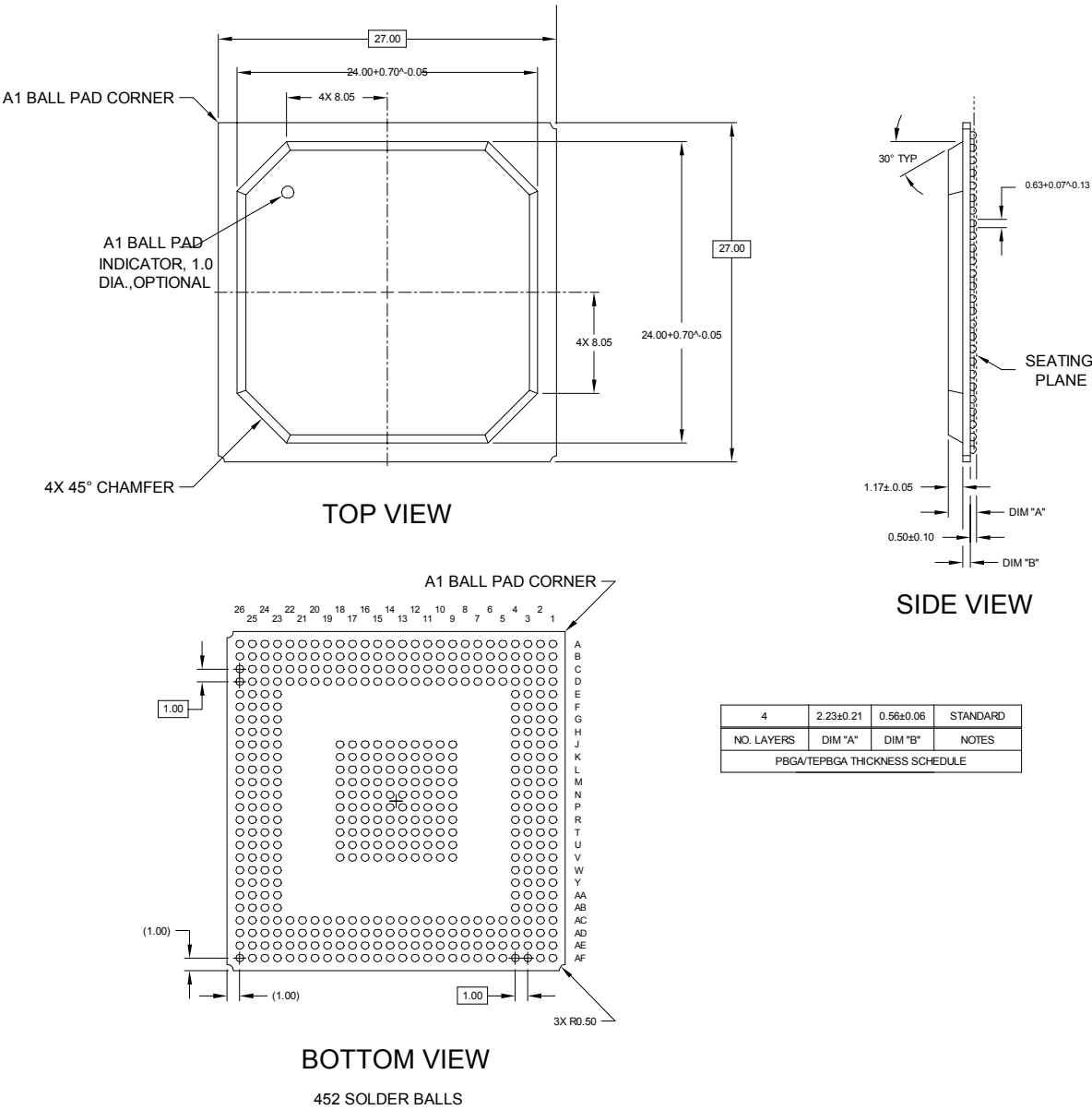
The package for the M28352/3/4 is a 280-ball 19 mm FPBGA as illustrated in [Figure 4-2](#).

**Figure 4-2. 280-ball 19 mm FPBGA**



The package for the M28356 is a 452-ball 27 mm PBGA as illustrated in [Figure 4-3](#).

Figure 4-3. 452-Ball 27 mm PBGA







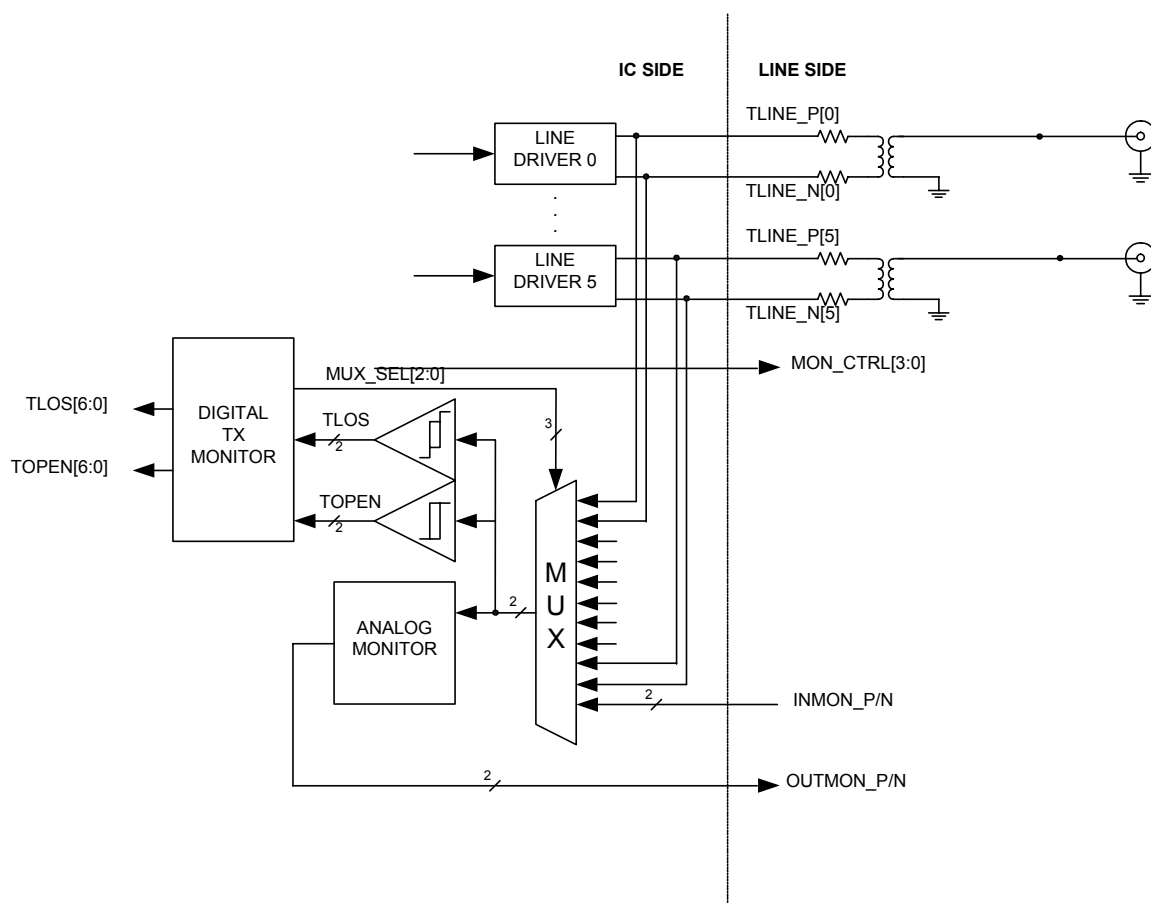


## 5.0 Appendices

### 5.1 Transmission Monitoring

#### 5.1.1 Internal

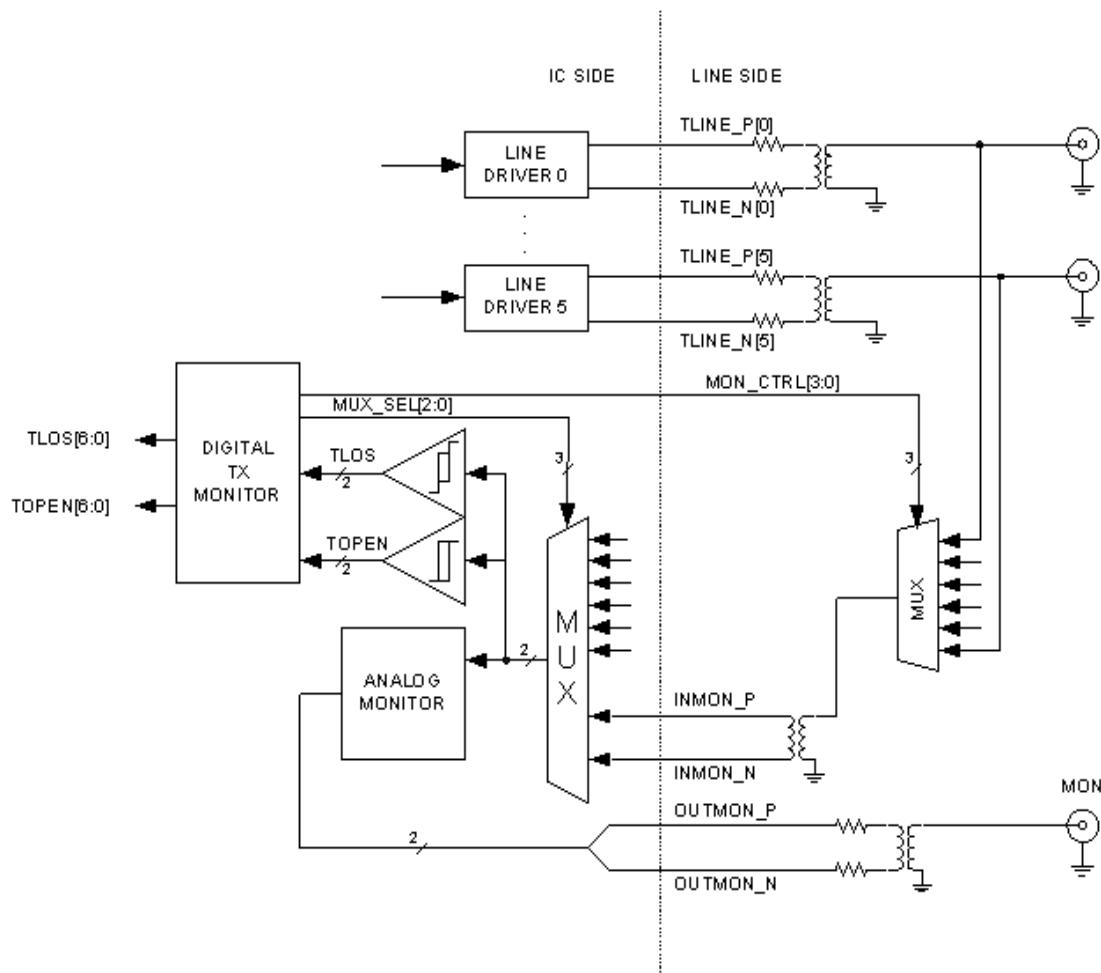
Figure 5-1. Internal Transmission Monitoring



## 5.1.2 External

TX monitor digital control (TLOS\_CONTROL: Address 0x00F)

**Figure 5-2. External Transmission Monitoring**









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