

Digital Step Attenuator

50Ω DC-2400 MHz

31 dB, 1 dB Step

5 Bit, Serial Control Interface, Single Positive Supply Voltage, +3V

Product Features

- Single positive supply voltage, +3V
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Serial control interface
- Low Insertion Loss
- High IP3, +52 dBm Typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm

Typical Applications

- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops



DAT-31-SP+
DAT-31-SP

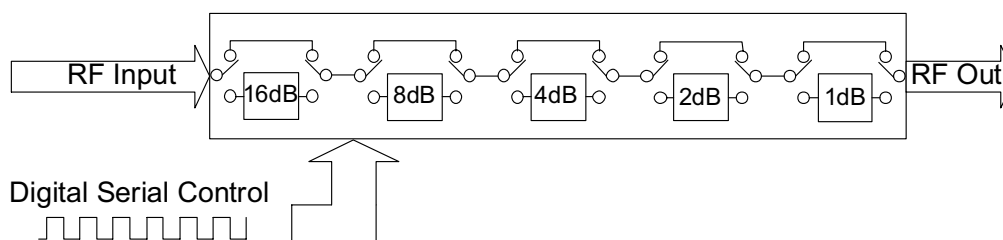
+ RoHS compliant in accordance
with EU Directive (2002/95/EC)

The +suffix identifies RoHS Compliance. See our web site for
RoHS Compliance methodologies and qualifications.

General Description

The DAT-31-SP is a 50Ω RF digital step attenuator that offers an attenuation range up to 31 dB in 1.0 dB steps. The control is a 5-bit serial interface, operating on a single +3 volt supply. The DAT-31-SP is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



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Rev.B
M106151
DAT-31-SP
060703
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RF Electrical Specifications, DC-2400 MHz, $T_{AMB}=25^{\circ}\text{C}$, $V_{DD}=+3\text{V}$

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Units
Accuracy @ 1 dB Attenuation Setting	DC-1	—	0.02	0.1	dB
	1-2.4	—	0.05	0.15	dB
Accuracy @ 2 dB Attenuation Setting	DC-1	—	0.05	0.15	dB
	1-2.4	—	0.15	0.25	dB
Accuracy @ 4 dB Attenuation Setting	DC-1	—	0.07	0.2	dB
	1-2.4	—	0.15	0.25	dB
Accuracy @ 8 dB Attenuation Setting	DC-1	—	0.03	0.2	dB
	1-2.4	—	0.15	0.25	dB
Accuracy @ 16 dB Attenuation Setting	DC-1	—	0.1	0.3	dB
	1-2.4	—	0.15	0.3	dB
Insertion Loss ^(note 1) @ all attenuator set to 0dB	DC-1	—	1.3	1.9	dB
	1-2.4	—	1.6	2.4	dB
Input IP3 ^(note 2) (at Min. and Max. Attenuation)	DC-2.4	—	+52	—	dBm
Input Power @ 0.2dB Compression ^(note 2) (at Min. and Max. Attenuation)	DC-2.4	—	+24	—	dBm
VSWR	DC-1	—	1.2	1.5	—
	1-2.4	—	1.2	1.5	—

Notes:

1. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.35dB @1000MHz, 0.60dB @2400MHz, 0.75dB @4000MHz)
2. Input IP3 and 1dB compression degrades below 1 MHz

DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
V_{DD} , Supply Voltage	2.7	3	3.3	V
I_{DD} , Supply Current	—	—	100	μA
Control Input Low	—	—	$0.3 \times V_{DD}$	V
Control Input High	$0.7 \times V_{DD}$	—	—	V
Control Current	—	—	1	μA

Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	μSec
Switching Control Frequency	—	—	25	KHz

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
V_{DD}	-0.3V Min., 4V Max.
Voltage on any input	-0.3V Min., $V_{DD}+0.3\text{V}$ Max.
ESD, HBM	500V
ESD, MM	100V
Input Power	+24dBm

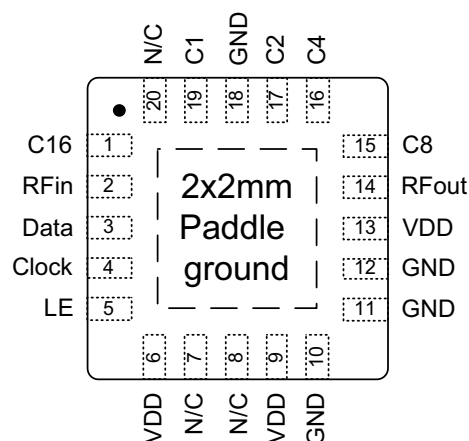
Pin Description

Function	Pin Number	Description
C16	1	Control for Attenuation bit, 16dB (Notes 3,4)
RF in	2	RF in port (Note 1)
Data	3	Serial Interface data input (Note 3)
Clock	4	Serial Interface clock input
LE	5	Latch Enable Input (Note 2)
V _{DD}	6	Power Supply
N/C	7	Not connected
N/C	8	Not connected
V _{DD}	9	Power Supply
GND	10	Ground connection
GND	11	Ground connection
GND	12	Ground connection
V _{DD}	13	Power Supply
RF out	14	RF out port (Note 1)
C8	15	Control for attenuation bit, 8 dB (Note 4)
C4	16	Control for attenuation bit, 4 dB (Note 4)
C2	17	Control for attenuation bit, 2 dB (Note 4)
GND	18	Ground Connection
C1	19	Control for attenuation bit, 1 dB (Note 4)
N/C	20	Not connected (Note 5)
GND	Paddle	Paddle ground (Note 6)

Notes:

- Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
- Latch Enable (LE) has an internal 100KΩ resistor to V_{DD}.
- Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance.
- Refer to Power-up Control Settings.
- Place a shunt 10KΩ resistor to GND
- The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation

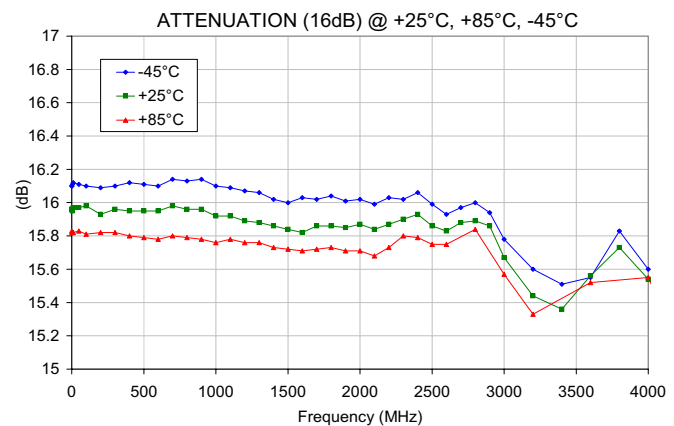
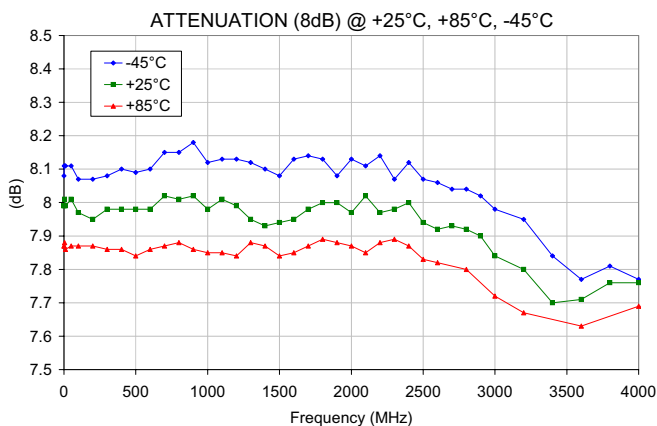
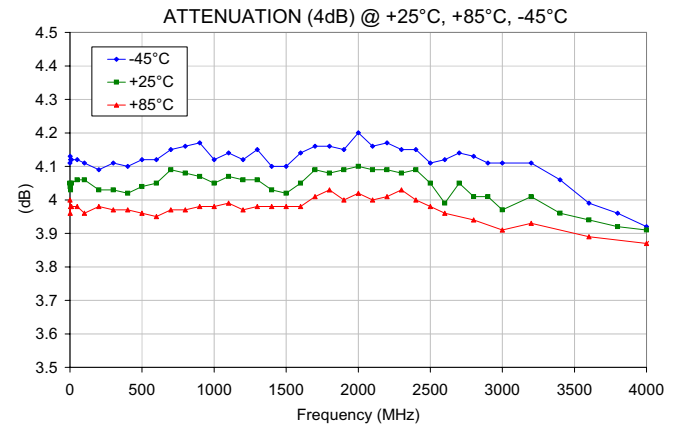
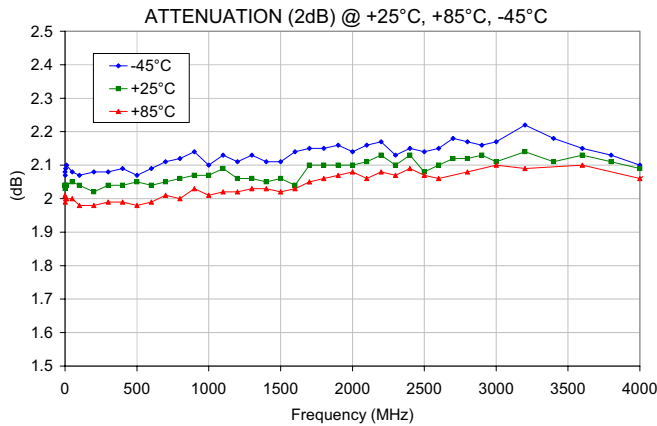
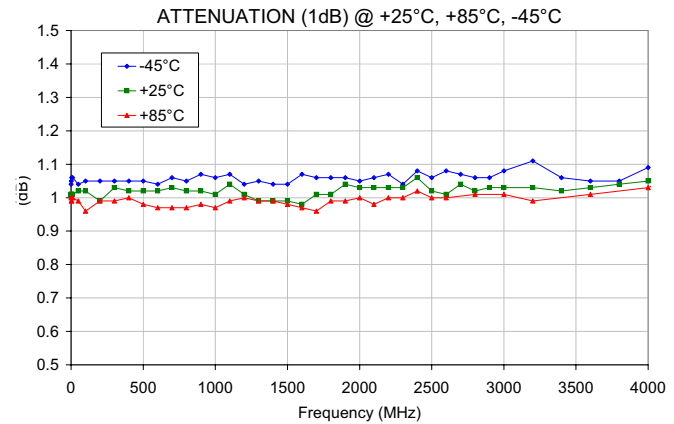
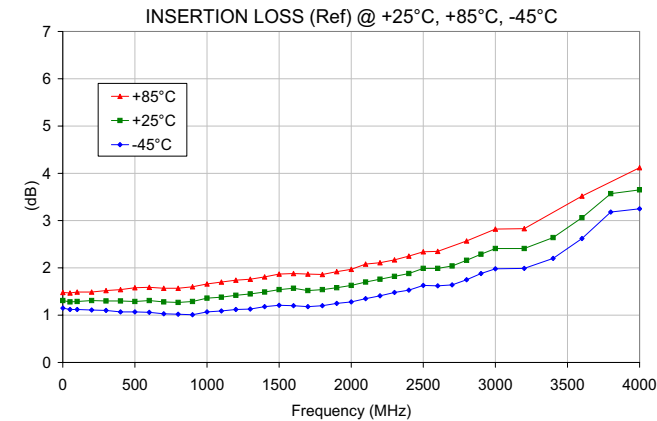
Pin Configuration (Top View)



Digital Step Attenuator

DAT-31-SP+
DAT-31-SP

Typical Performance Curves



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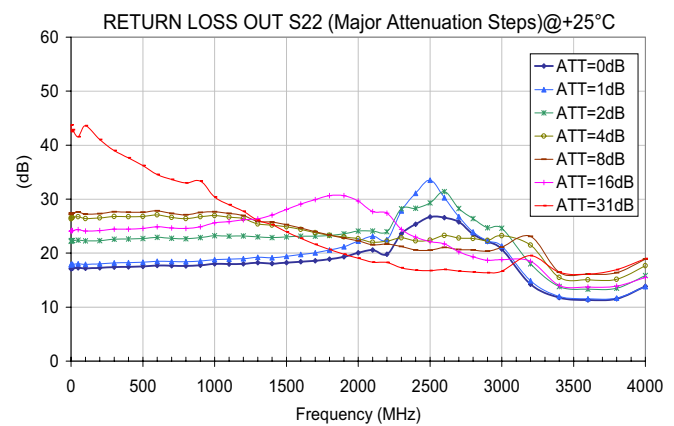
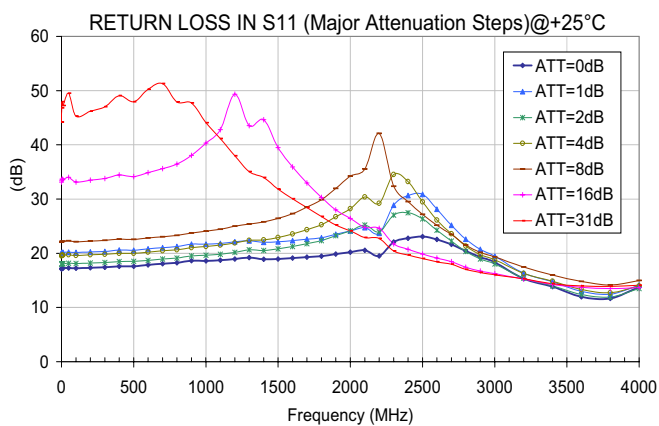
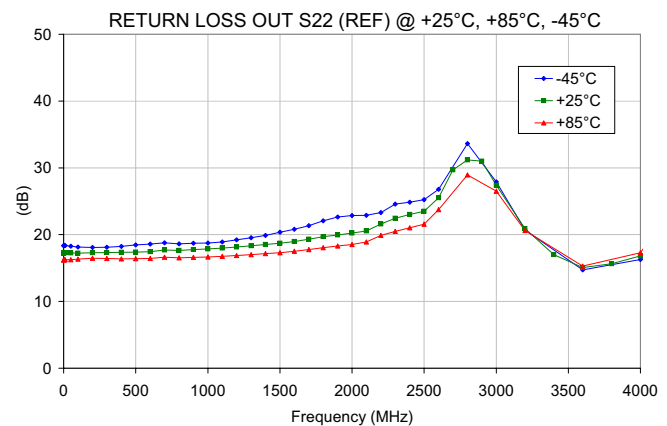
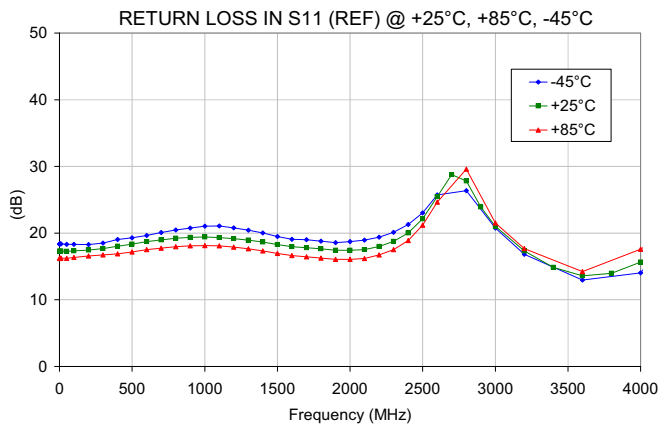
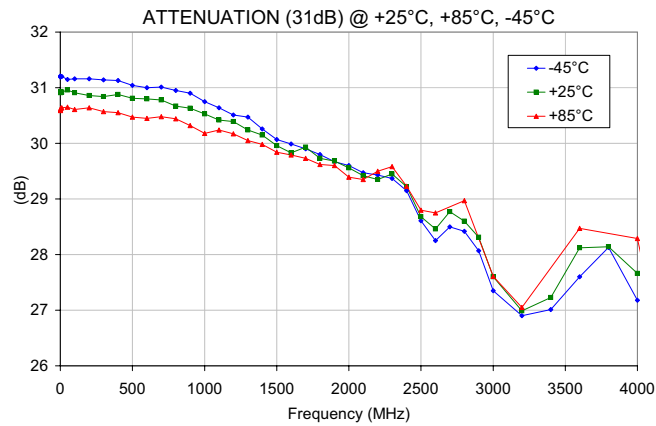
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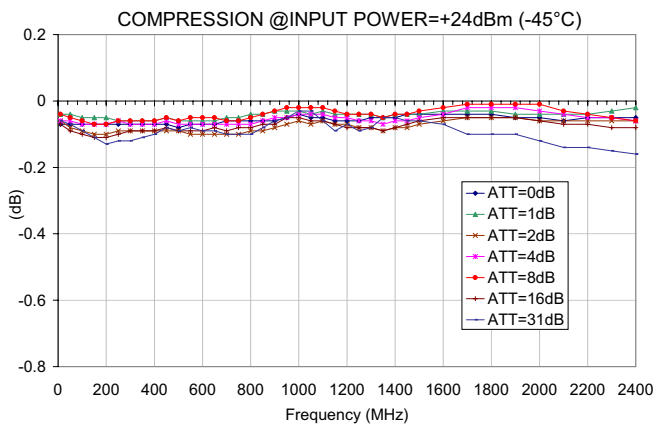
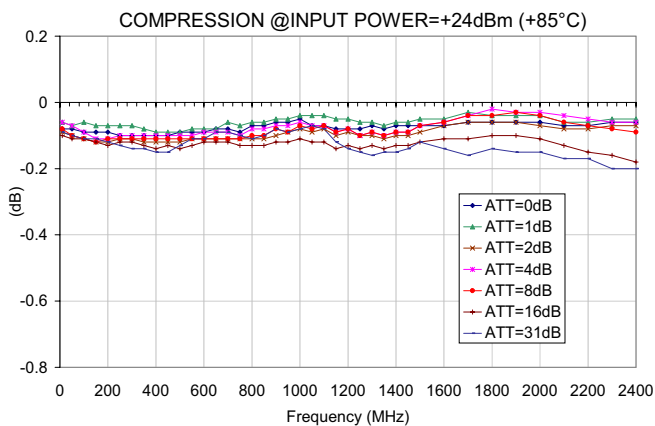
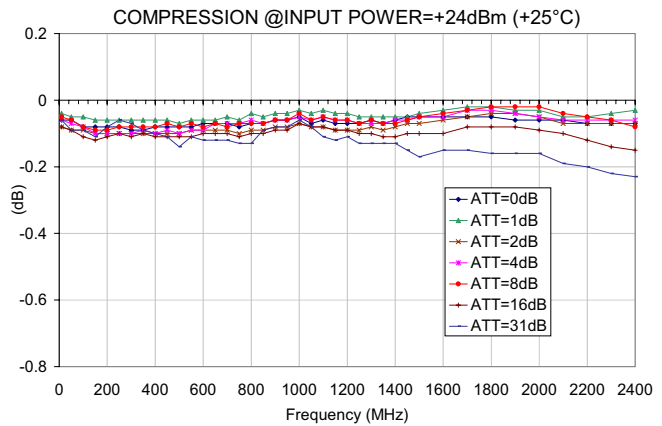
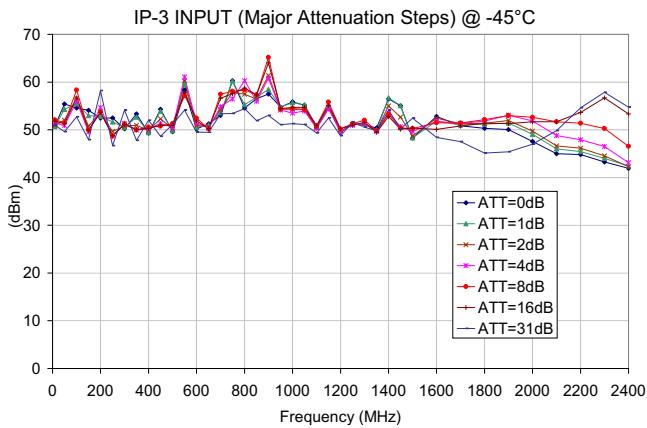
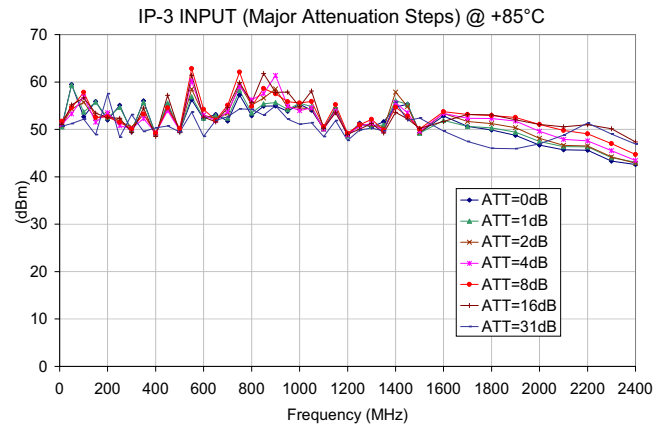
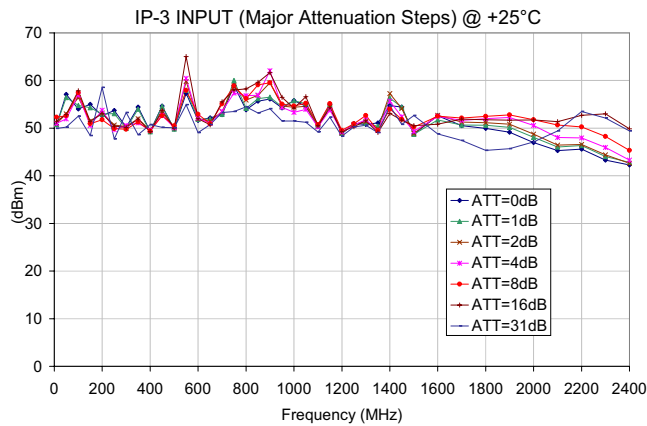
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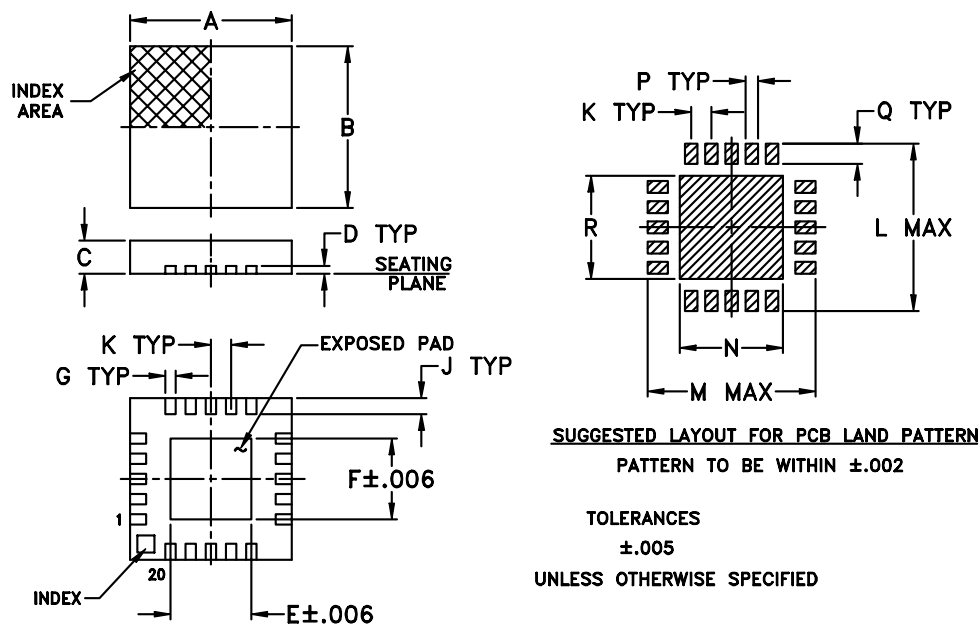
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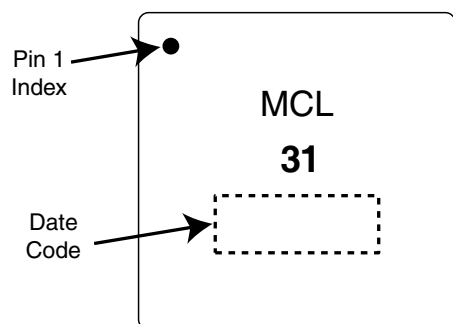
Typical Performance Curves



Outline Drawing (DG983-1)



Device Marking

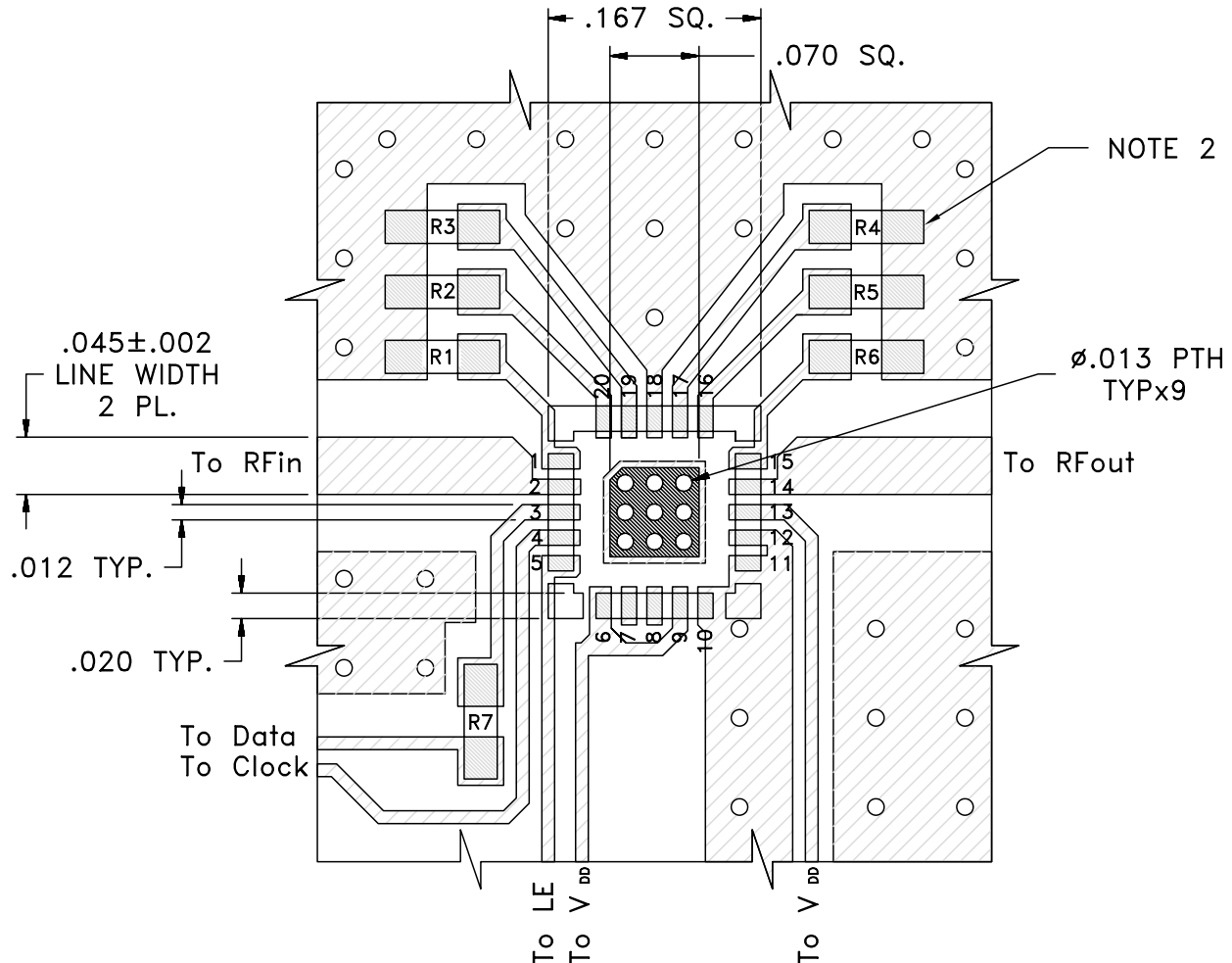


Outline Dimensions (inch/mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	WT. GRAMS
.157	.157	.035	.008	.081	.081	.010	—	.022	.020	.166	.166	.070	.012	.020	.070	.04
4.00	4.00	0.90	0.20	2.06	2.06	0.25	—	0.56	0.50	4.22	4.22	1.78	0.31	0.51	1.78	



Suggested Layout for PCB Design (PL-191)

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1-R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.



NOTE:

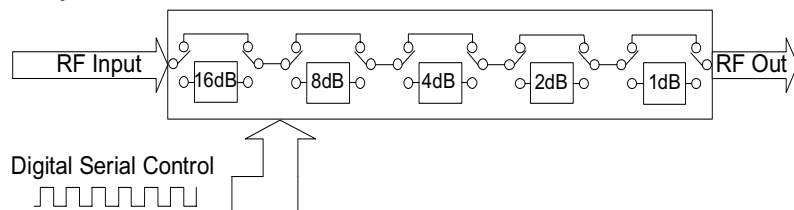
1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS. $.025" \pm .002"$. COPPER: 1/2 OZ. EACH SIDE.
FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603 SIZE CHIP FOOT PRINTS SHOWN FOR REFERENCE,
VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

-  DENOTES PCB COPPER LAYOUT WITH SOMBC
(SOLDER MASK OVER BARE COPPER)
-  DENOTES COPPER LAND PATTERN FREE OF SOLDERMASK

Digital Step Attenuator

DAT-31-SP+
DAT-31-SP

Simplified Schematic



The DAT-31-SP Serial interface consists of 5 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

Table 1. Truth Table					
Attenuation State	C16	C8	C4	C2	C1
Reference	0	0	0	0	0
1 (dB)	0	0	0	0	1
2 (dB)	0	0	0	1	0
4 (dB)	0	0	1	0	0
8 (dB)	0	1	0	0	0
16 (dB)	1	0	0	0	0
31 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C1 - C16 are shown in table

The serial interface is a 5-bit serial in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 1 (Serial Interface Timing Diagram) and Table 2 (Serial Interface AC Characteristics).

Figure 1: Serial Interface Timing Diagram

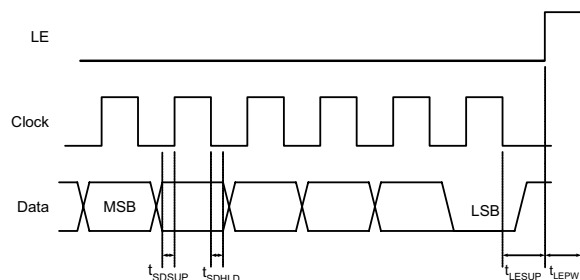


Table 2. Serial Interface AC Characteristics				
Symbol	Parameter	Min.	Max.	Units
f_{clk}	Serial data clock frequency (Note 1)		10	MHz
t_{clkH}	Serial clock HIGH time	30		ns
t_{clkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note 1. f_{clk} verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify f_{clk} specification.

The DAT-31-SP, uses a common 5-bit serial word format, as shown in Table 3: 5-Bit attenuator Serial Programming Register Map.

The first bit, the MSB, corresponds to the 16-dB Step and the B1 bit corresponds to the 1 dB step.

Table 3. 5-Bit attenuator Serial Programming Register Map					
B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	0

↑
MSB
(first in)

↑
LSB
(last in)

Note: The stop bit (B0) must always be low to prevent the attenuator from entering an unknown state.

Power-up Control Settings

The DAT-31-SP always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided.

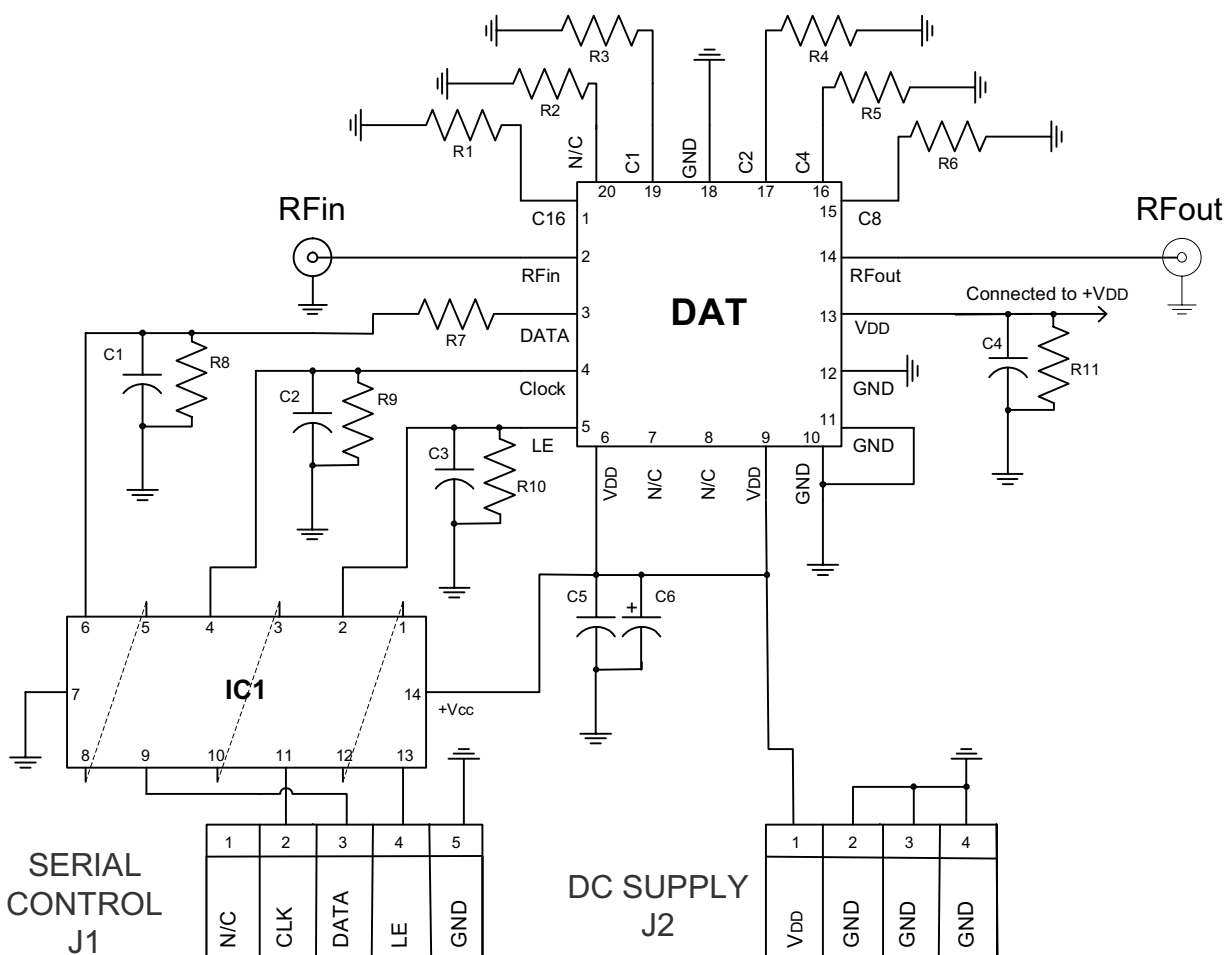
When the attenuator powers up, the five control bits are set to whatever data is present on the five data inputs (C1 to C16).

This allows any one of the 32 attenuation settings to be specified as the power-up state.

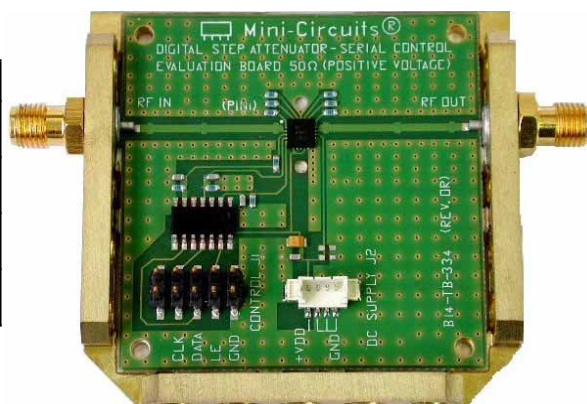
Digital Step Attenuator

DAT-31-SP+
DAT-31-SP

TB-334 Evaluation Board Schematic Diagram



Bill of Materials	
R1 - R11	Resistor 0603 10 KOhm +/- 1%
C1 - C5	NPO Capacitor 0603 100 pF +/-5%
C6	Tantalum Capacitor 100 nF +/-10%
IC1	Hex inverting Schmitt trigger MM74HC14



TB-334



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Table T&R

TR No.	No. of Devices	Designation Letter	Reel Size	Tape Width	Pitch	Unit Orientation
T-005	1000	K	7 inch	12 mm	8 mm	
	2000	T	13 inch			
		multiples of 10, less than full reel of 1K	PR	7 inch		
	multiples of 10, on tape only	E	not applicable			

Model No.	Description	Packaging Designation Letter (See Table T&R)	Quantity Min. No. of Units	Price \$ Ea.
DAT-31-SP (+)	Serial Interface, Single Positive Voltage	E	10	\$3.55
TB-334	Test Board Only	Not Applicable	1	\$79.95

1K DAT-31-SP+ T&R=K

Quantity Model No. T&R designation letter (see Table T&R)