

SDRAM (Rev.1.1)

Single Data Rate

**M2V56S20/ 30/ 40 ATP -5, -5L, -6, -6L, -7, -7L**

Aug '01

256M Synchronous DRAM

Some of contents are subject to change without notice.
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## DESCRIPTION

M2V56S20ATP is a 4-bank x 16777216-word x 4-bit,  
 M2V56S30ATP is a 4-bank x 8388608-word x 8-bit,  
 M2V56S40ATP is a 4-bank x 4194304-word x 16-bit,  
 synchronous DRAM, with LVTTL interface. All inputs and outputs are referenced to the rising edge of CLK. The M2V56S20/30/40ATP achieve very high speed data rate up to 100MHz (-7) , 133MHz (-6), 166MHz(-5) and are suitable for main memory or graphic memory in computer systems.

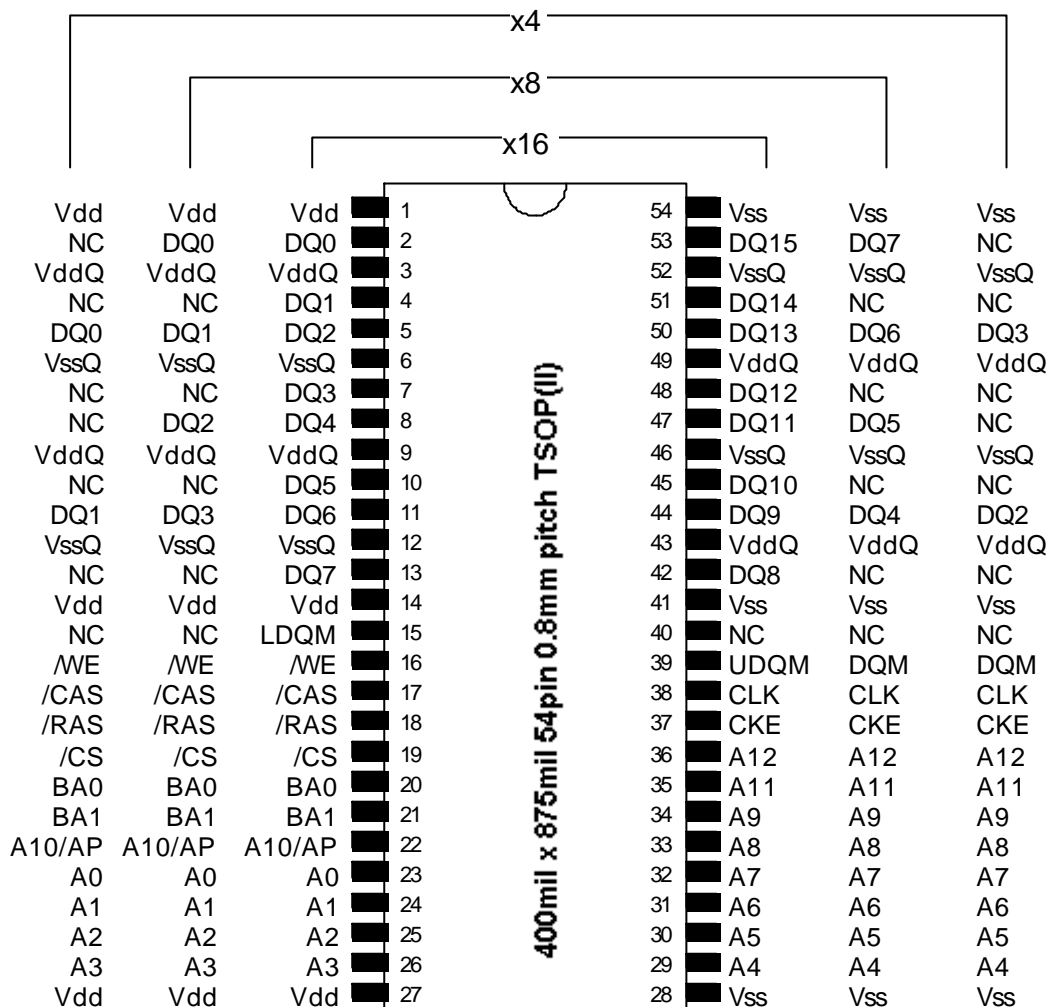
## FEATURES

- Single 3.3v±0.3V power supply
- Max. Clock frequency -5:PC166<3-3-3> / -6:PC133<3-3-3> / -7:PC100<2-2-2>
- Fully Synchronous operation referenced to clock rising edge
- Single Data Rate
- 4 bank operation controlled by BA0, BA1 (Bank Address)
- /CAS latency- 2/3 (programmable)
- Burst length- 1/2/4/8/full page (programmable)
- Burst type- sequential / interleave (programmable)
- Random column access
- Auto precharge / All bank precharge controlled by A10
- 8192 refresh cycles /64ms (4 banks concurrent refresh)
- Auto refresh and Self refresh
- Row address A0-12 / Column address A0-9,11(x4)/ A0-9(x8)/ A0-8(x16)
- LVTTL Interface
- 400-mil, 54-pin Thin Small Outline Package (TSOP II) with 0.8mm lead pitch

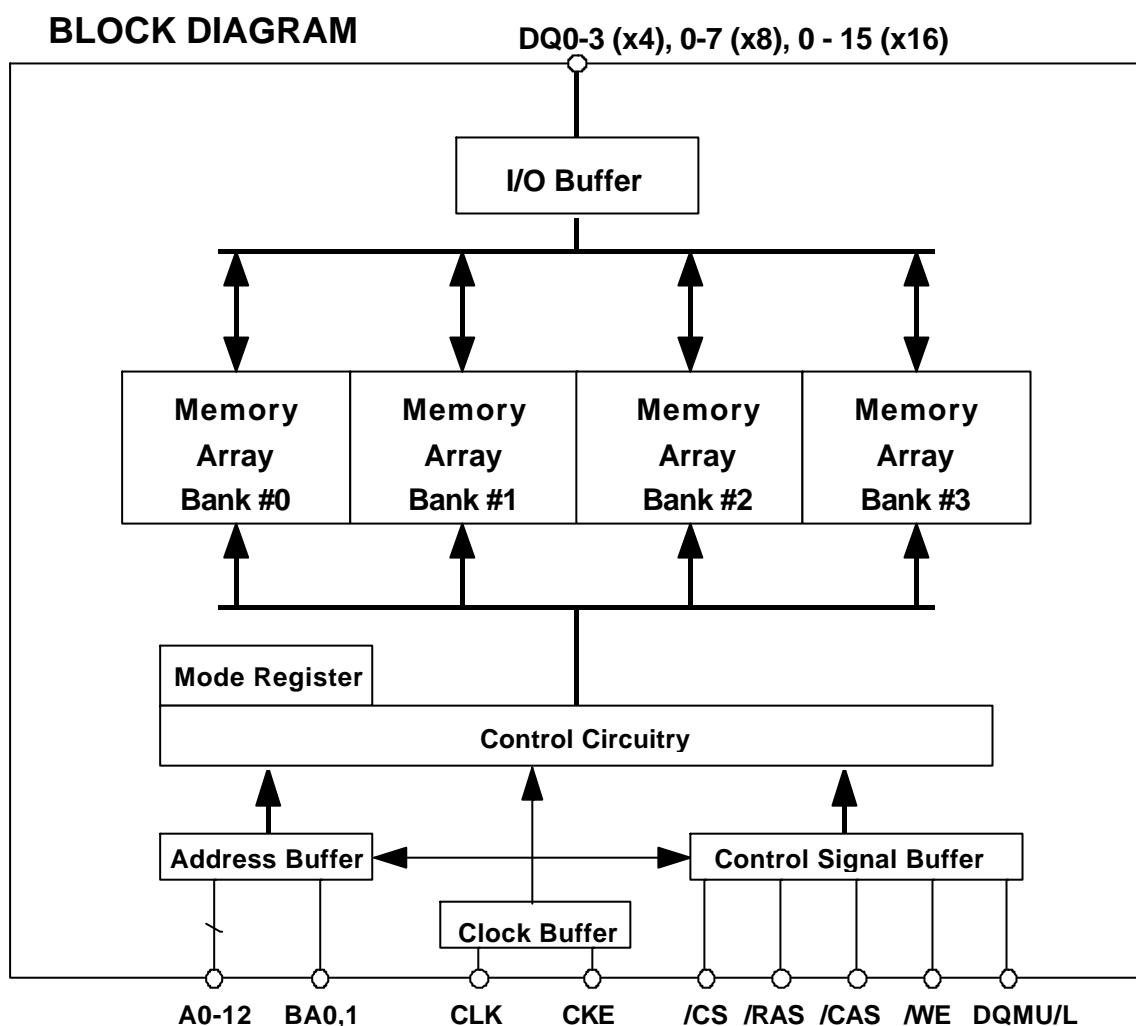
	Max. Frequency @CL2	Max. Frequency @CL3	Standard
M2V56S20/30/40ATP-5,-5L	133MHz	166MHz	PC133 (CL2)
M2V56S20/30/40ATP-6,-6L	100MHz	133MHz	PC133 (CL3)
M2V56S20/30/40ATP-7,-7L	100MHz	100MHz	PC100 (CL2)

**PIN CONFIGURATION**

**(TOP VIEW)**



- CLK** : Master Clock
- CKE** : Clock Enable
- /CS** : Chip Select
- /RAS** : Row Address Strobe
- /CAS** : Column Address Strobe
- /WE** : Write Enable
- DQ0-15** : Data I/O
- DQM, DQMU/L** : Output Disable / Write Mask
- A0-12** : Address Input
- BA0,1** : Bank Address Input
- Vdd** : Power Supply
- VddQ** : Power Supply for Output
- Vss** : Ground
- VssQ** : Ground for Output



### Type Designation Code

This rule is applied to only Synchronous DRAM family.

M 2 V 56 S 4 0 A TP - 5 L

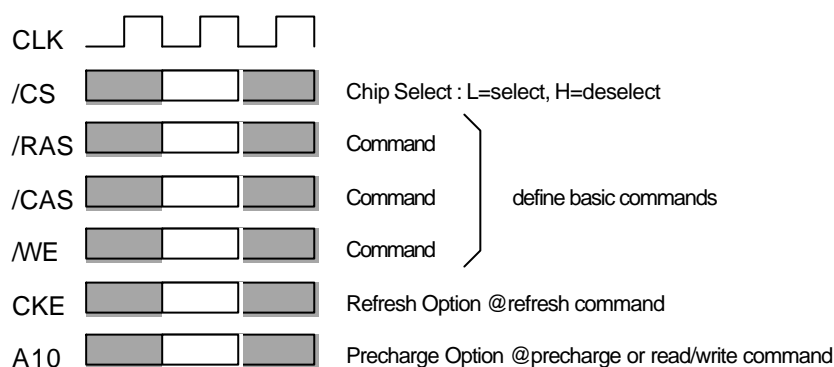
- Power Grade L:Low Power, Space:Standard
- Speed Grade 5: 166MHz@CL3, 133MHz@CL2  
6: 133MHz@CL3, 100MHz@CL2  
7: 100MHz@CL2
- Package Type TP: TSOP(II)
- Process Generation A:2nd. gen.
- Function Reserved for Future Use
- Organization 2<sup>n</sup> 2: x4, 3: x8, 4: x16
- SDRAM Data Rate Type S:Single Data Rate**
- Density 56: 256M bits
- Interface V:LVTTTL
- Memory Style (DRAM)
- Mitsubishi Main Designation

**PIN FUNCTION**

CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-12	Input	A0-12 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-12. The Column Address is specified by A0-9,11. A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
DQ0-15	Input / Output	Data In and Data out are referenced to the rising edge of CLK.
DQM DQMU/L	Input	Din Mask / Output Disable: When DQMU/L is high in burst write, Din for the current cycle is masked. When DQMU/L is high in burst read, Dout is disabled at the next but one cycle.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.

## BASIC FUNCTIONS

The M2V56S20/30/40ATP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS, CKE and A10 are used as chip select, refresh option, and precharge option, respectively. To know the detailed definition of commands, please see the command truth table.



### Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

### Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, **READA**)

### Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

### Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read /write operation. When A10 =H at this command, all banks are deactivated (precharge all, **PREA**).

### Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address are generated internally. After this command, the banks are precharged automatically.

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**COMMAND TRUTH TABLE**

COMMAND	MNEMONIC	CKE <sub>n-1</sub>	CKE <sub>n</sub>	/CS	/RAS	/CAS	/WE	BA0,1	A10 /AP	A0-9, 11-12	note
Deselect	DESEL	H	X	H	X	X	X	X	X	X	
No Operation	NOP	H	X	L	H	H	H	X	X	X	
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V	
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X	
Precharge All Banks	PREA	H	X	L	L	H	L	X	H	X	
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	L	V	
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V	
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V	
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	H	V	
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	
		L	H	L	H	H	H	X	X	X	
Burst Terminate	TBST	H	X	L	H	H	L	X	X	X	
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V	1

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. A7-9,11-12=L, A0-A6 =Mode  
Address

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**FUNCTION TRUTH TABLE**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE / PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	NOP
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto- Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

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**FUNCTION TRUTH TABLE (continued)**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL





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**FUNCTION TRUTH TABLE (continued)**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)
	L	H	H	H	X	NOP	NOP (Idle after tRP)
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	NOP*4 (Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RE- COVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

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**FUNCTION TRUTH TABLE (continued)**

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)
	L	H	H	H	X	NOP	NOP (Idle after tRC)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tRSC)
	L	H	H	H	X	NOP	NOP (Idle after tRSC)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

## ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

## NOTES:

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

## FUNCTION TRUTH TABLE for CKE

Current State	CKE <sub>n-1</sub>	CKE <sub>n</sub>	/CS	/RAS	/CAS	/WE	Add	Action
SELF-REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CLK Suspend

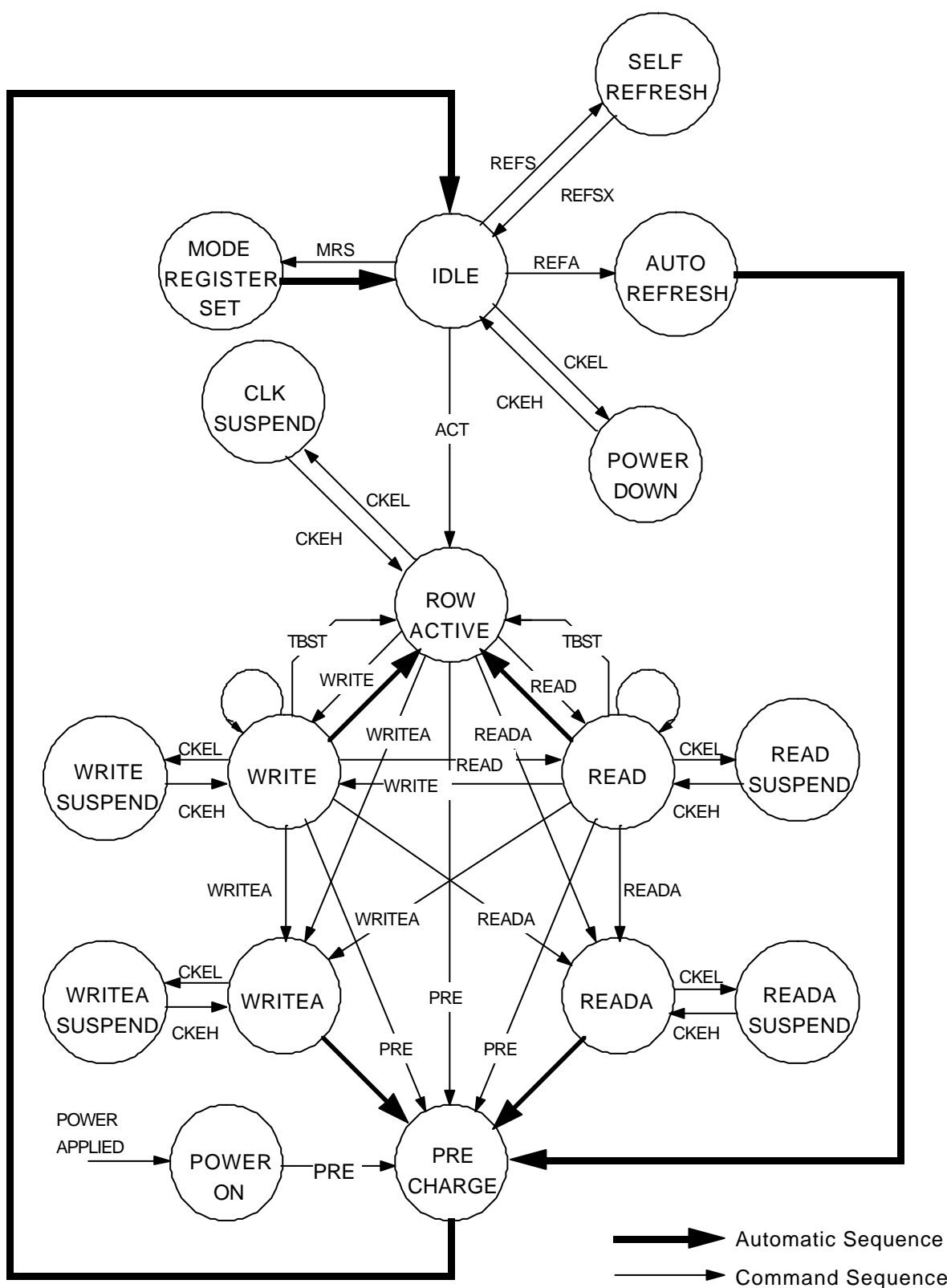
## ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

## NOTES:

1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously**.  
A minimum setup time must be satisfied before any command other than EXIT.
2. Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

# SIMPLIFIED STATE DIAGRAM



## POWER ON SEQUENCE

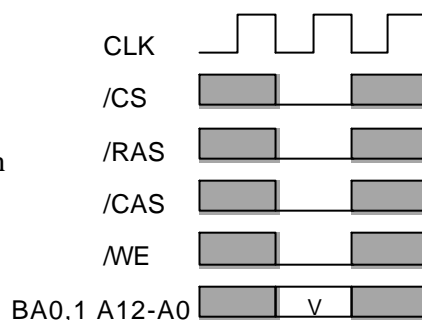
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 100μs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

## MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when all banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	SW	0	0	LTMODE			BT	BL		

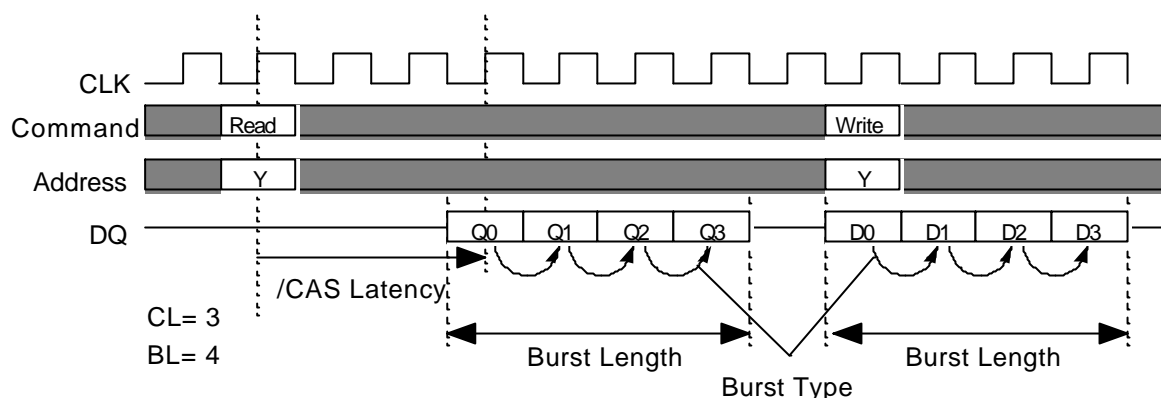
SW	0	Burst Write
	1	Single Write

LATENCY MODE	CL	/CAS LATENCY
	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	3
	1 0 0	R
	1 0 1	R
	1 1 0	R
	1 1 1	R

BURST LENGTH	BL	BT=0	BT=1
	0 0 0	1	1
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	Full Page	R

BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED

R: Reserved for Future Use



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

## OPERATIONAL DESCRIPTION

### BANK ACTIVATE

One of four banks is activated by an ACT command.

An bank is selected by BA0-1. A row is selected by A0-12.

Multiple banks can be active state concurrently by issuing multiple ACT commands.

Minimum activation interval between one bank and another bank is  $t_{RRD}$ .

### PRECHARGE

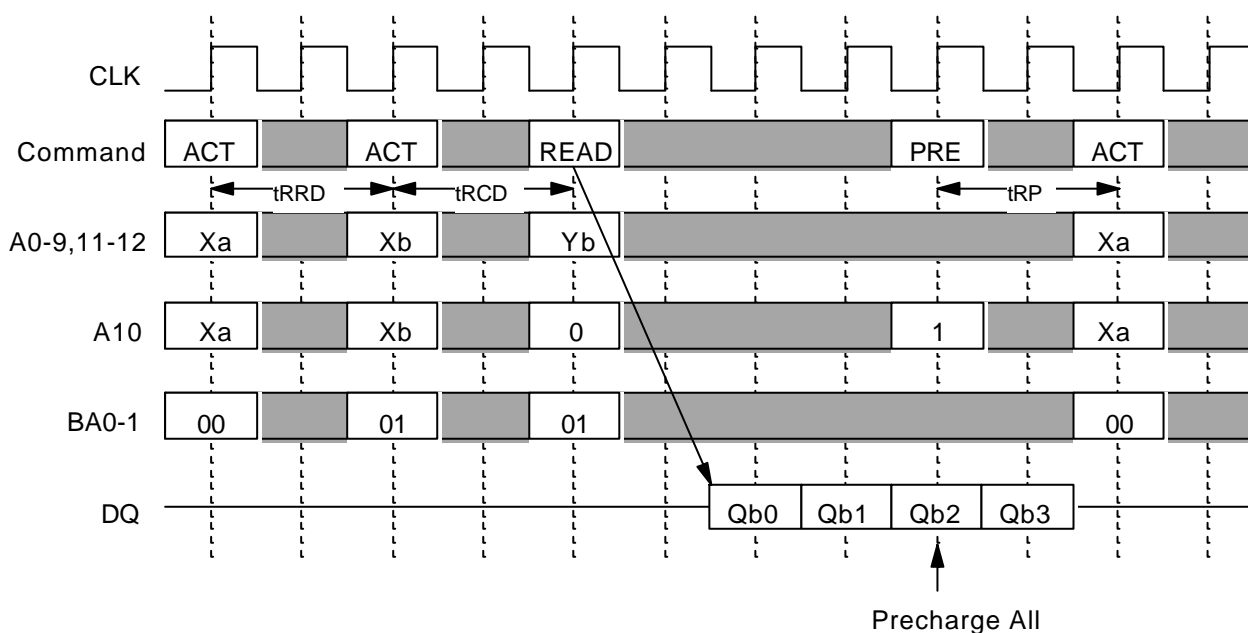
An open bank is deactivated by a PRE command.

A bank to be deactivated is designated by BA0-1.

When multiple banks are active, a precharge all command (PREA, PRE + A10=H) deactivates all of open banks at the same time. BA0-1 are "Don't Care" in this case.

Minimum delay time of an ACT command after a PRE command to the same bank is  $t_{RP}$ .

**Bank Activation and Precharge All (BL=4, CL=3)**

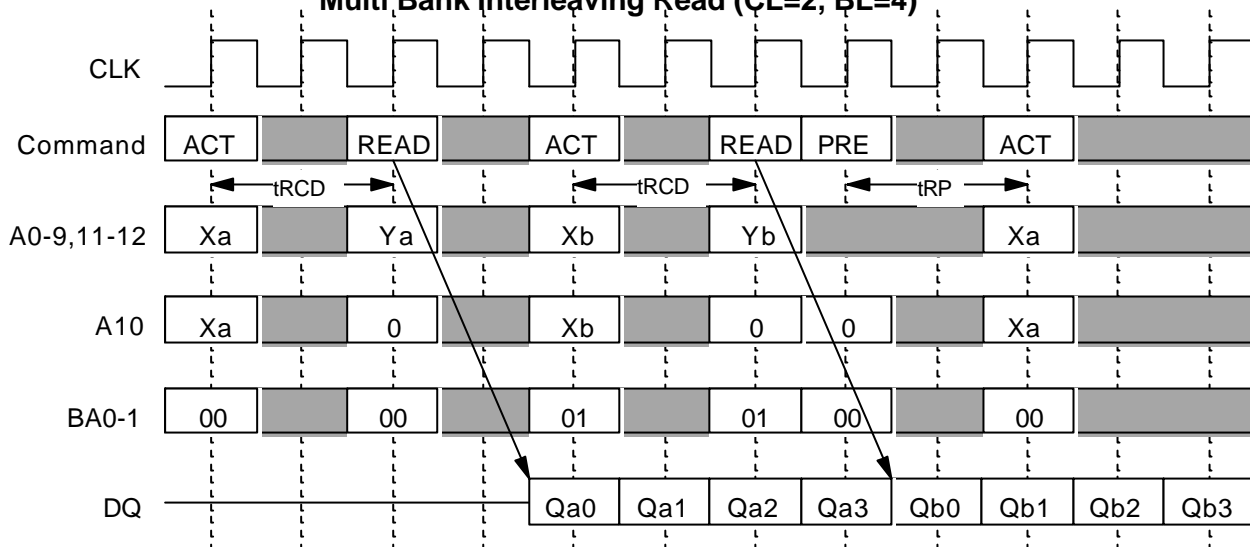


### READ

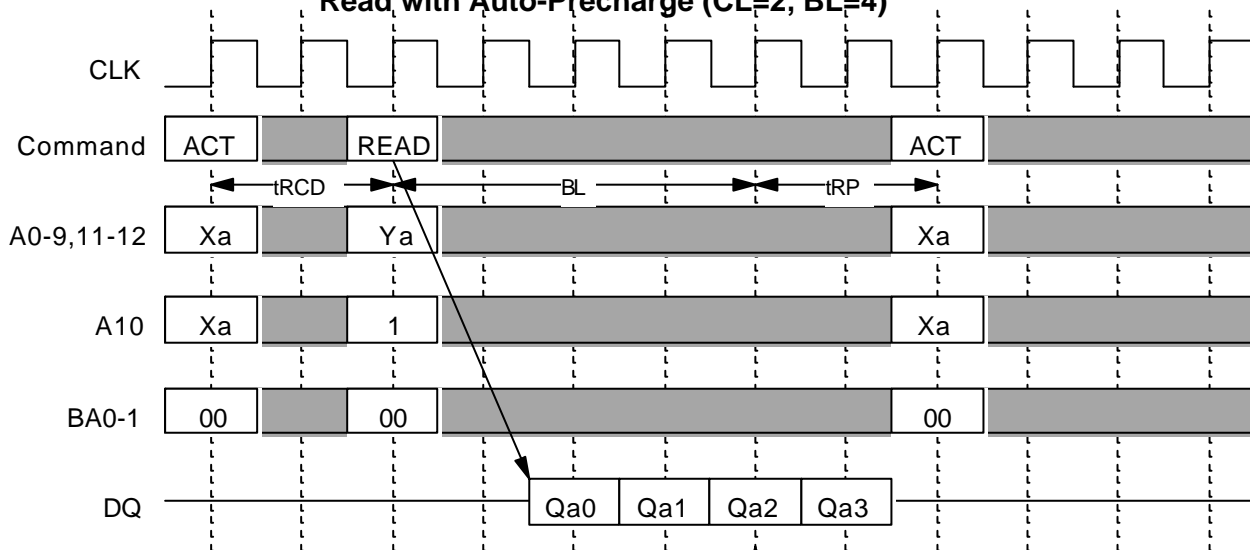
A READ command can be issued to any active bank. The start address is specified by A0-9,11(x4), A0-9 (x8), A0-8 (x16). 1st output data is available after the /CAS Latency from the READ. The consecutive data length is defined by the Burst Length. The address sequence of the burst data is defined by the Burst Type. Minimum delay time of a READ command after an ACT command to the same bank is  $t_{RCD}$ .

When A10 is high at a READ command, auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at the BL after READA. The next ACT command can be issued after  $(BL + t_{RP})$  from the previous READA. In any case,  $t_{RCD} + BL > t_{RASmin}$  must be met.

Multi Bank Interleaving Read (CL=2, BL=4)

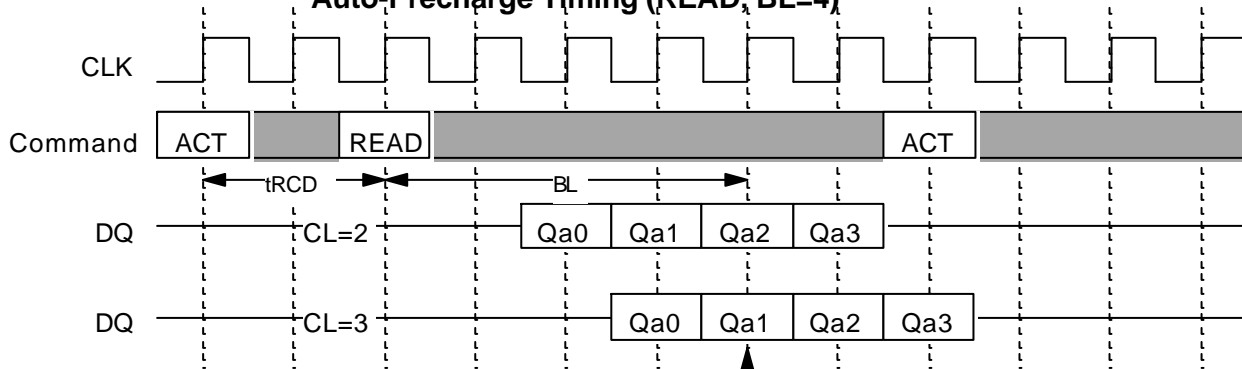


Read with Auto-Precharge (CL=2, BL=4)



internal precharge starts

Auto-Precharge Timing (READ, BL=4)

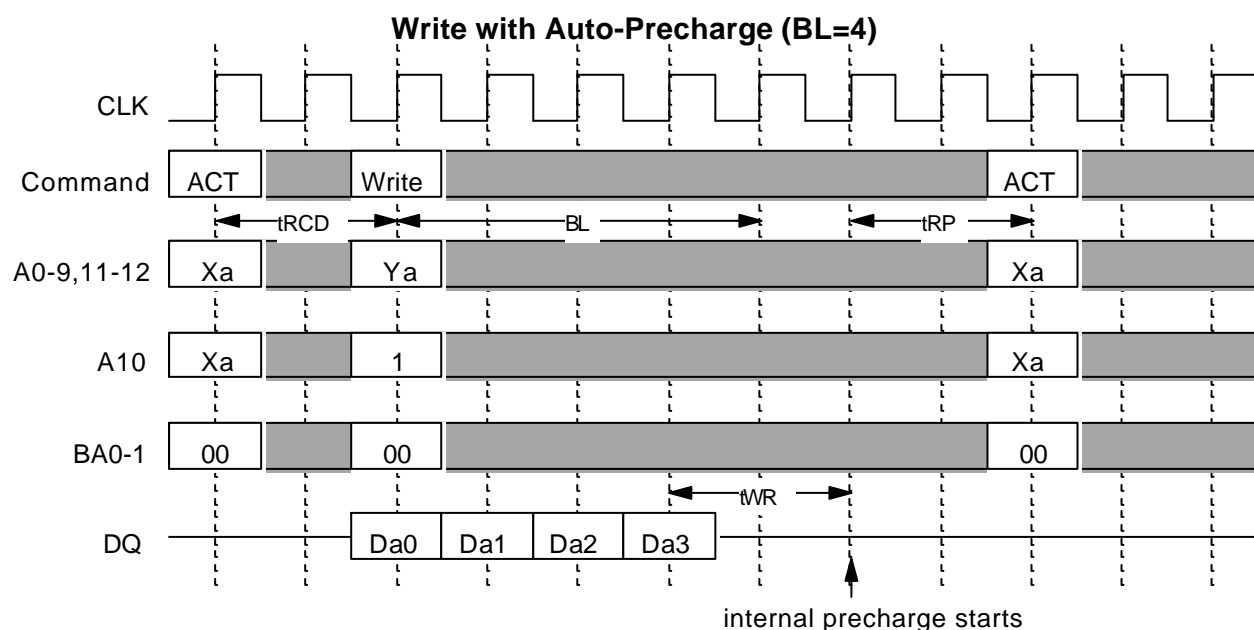
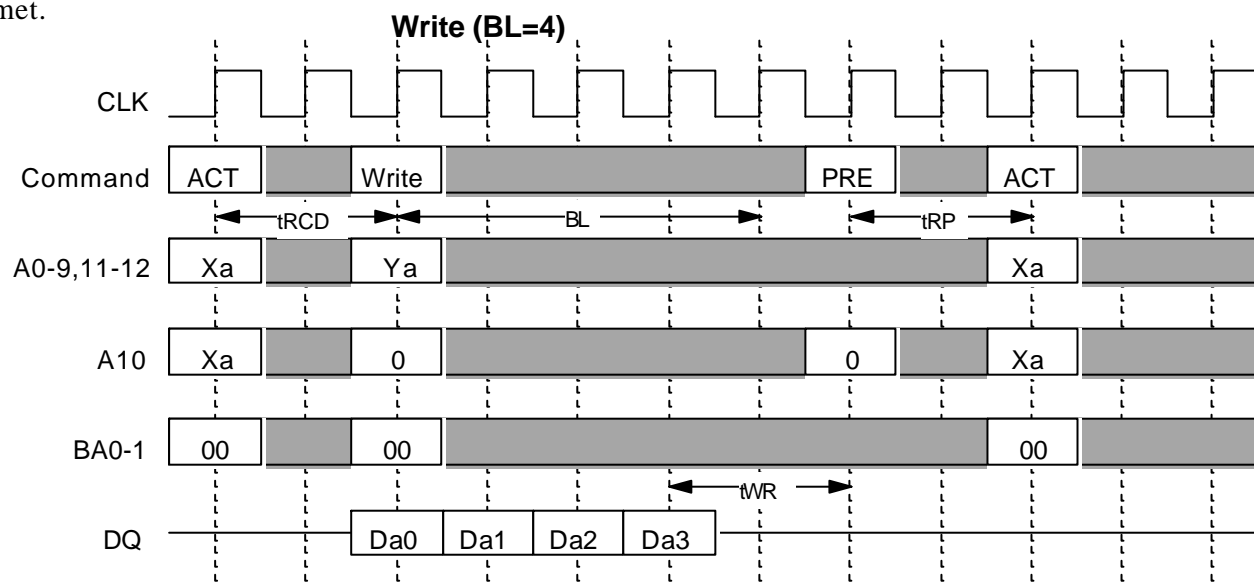


internal precharge starts



**WRITE**

A WRITE command can be issued to any active bank. The start address is specified by A0-9,11(x4), A0-9 (x8), A0-8 (x16). 1st input data is set at the same cycle as the WRITE. The consecutive data length to be written is defined by the Burst Length. The address sequence of burst data is defined by the Burst Type. Minimum delay time of a WRITE command after an ACT command to the same bank is  $t_{RCD}$ . From the last input data to the PRE command, the write recovery time ( $t_{WR}$ ) is required. When A10 is high at a WRITE command, auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at  $t_{WR}$  after the last input data cycle. The next ACT command can be issued after  $(BL + t_{WR} - 1 + t_{RP})$  from the previous WRITEA. In any case,  $t_{RCD} + BL + t_{WR} - 1 > t_{RASmin}$  must be met.

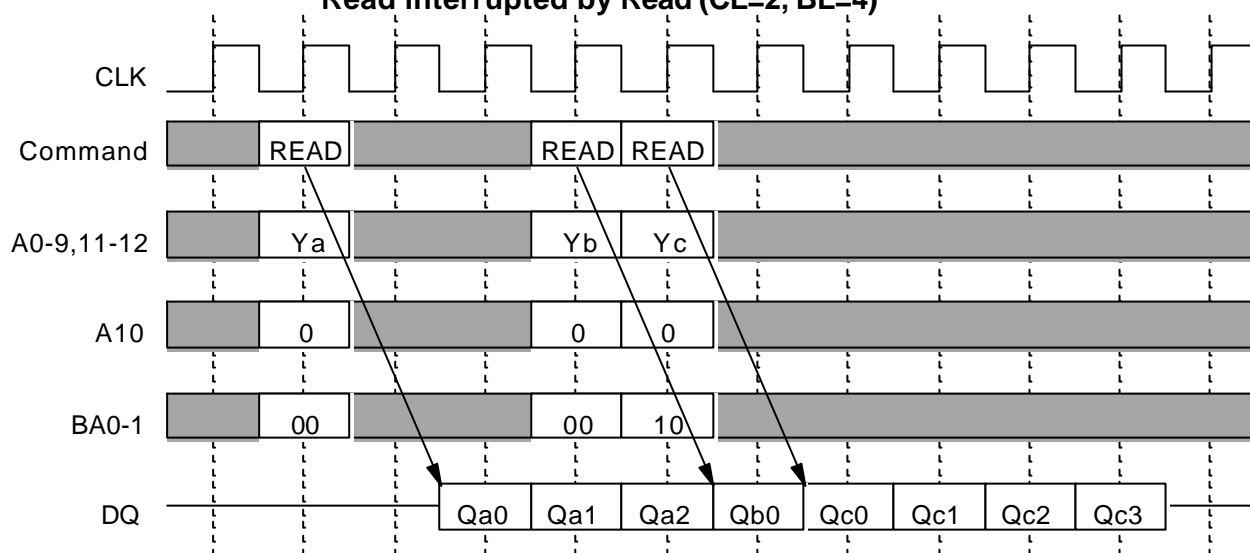


## BURST INTERRUPTION

### [ Read Interrupted by Read ]

Burst read operation can be interrupted by new read of any active bank. Random column access is allowed. READ to READ interval is minimum 1 CLK.

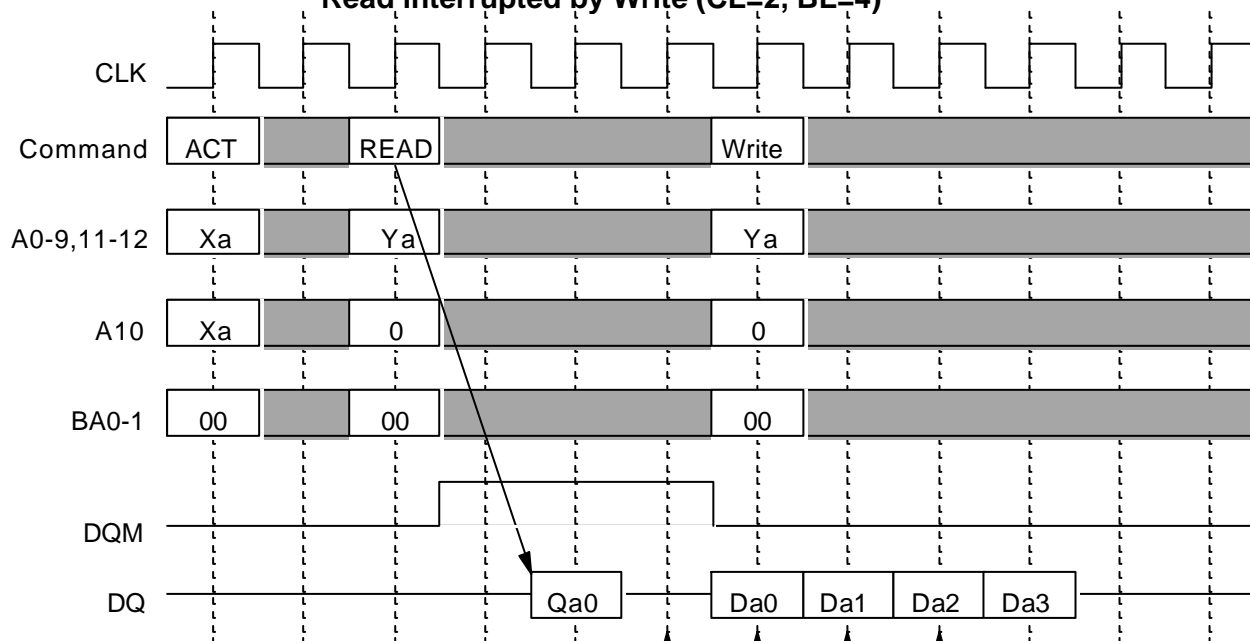
Read interrupted by Read (CL=2, BL=4)



### [ Read Interrupted by Write ]

Burst read operation can be interrupted by write of any active bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 2 cycle after WRITE assertion.

Read interrupted by Write (CL=2, BL=4)



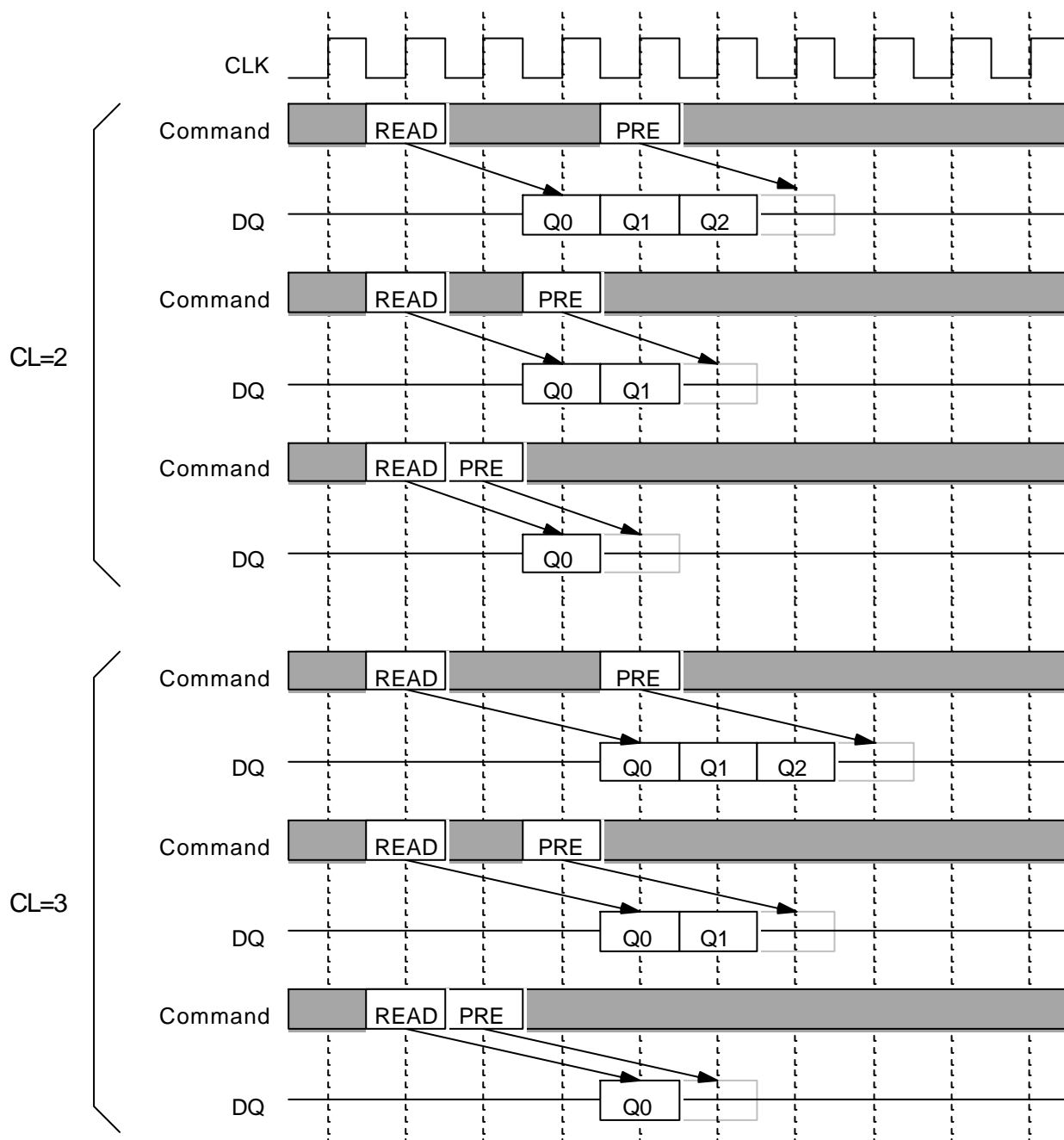
Output disable by DQM by WRITE

# [ Read Interrupted by Precharge ]

A burst read operation can be interrupted by a precharge of *the same bank*. READ to PRE interval is minimum 1 CLK.

A PRE command to output disable latency is equivalent to the /CAS Latency.

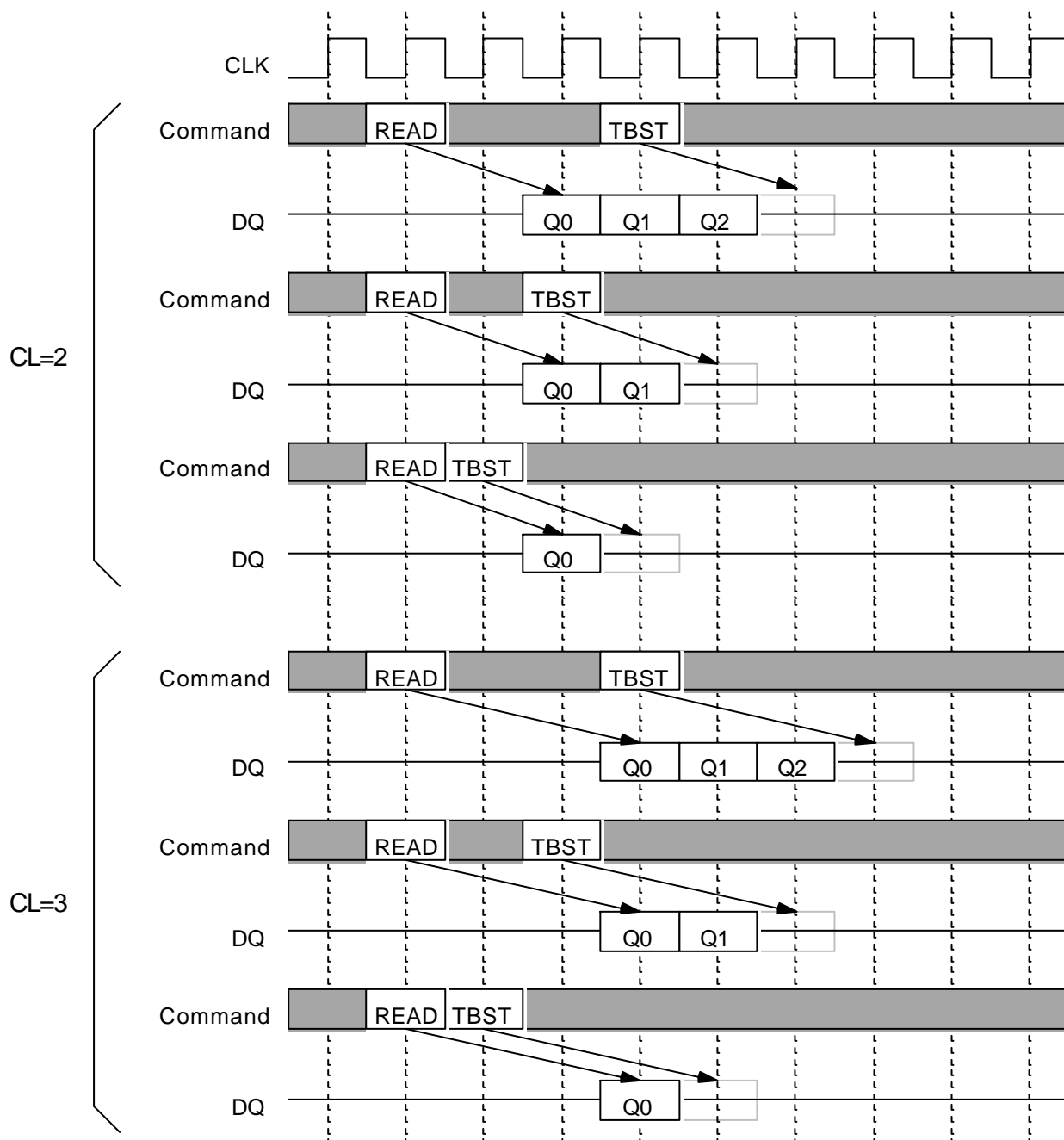
## Read interrupted by Precharge (BL=4)



**[ Read Interrupted by Burst Terminate ]**

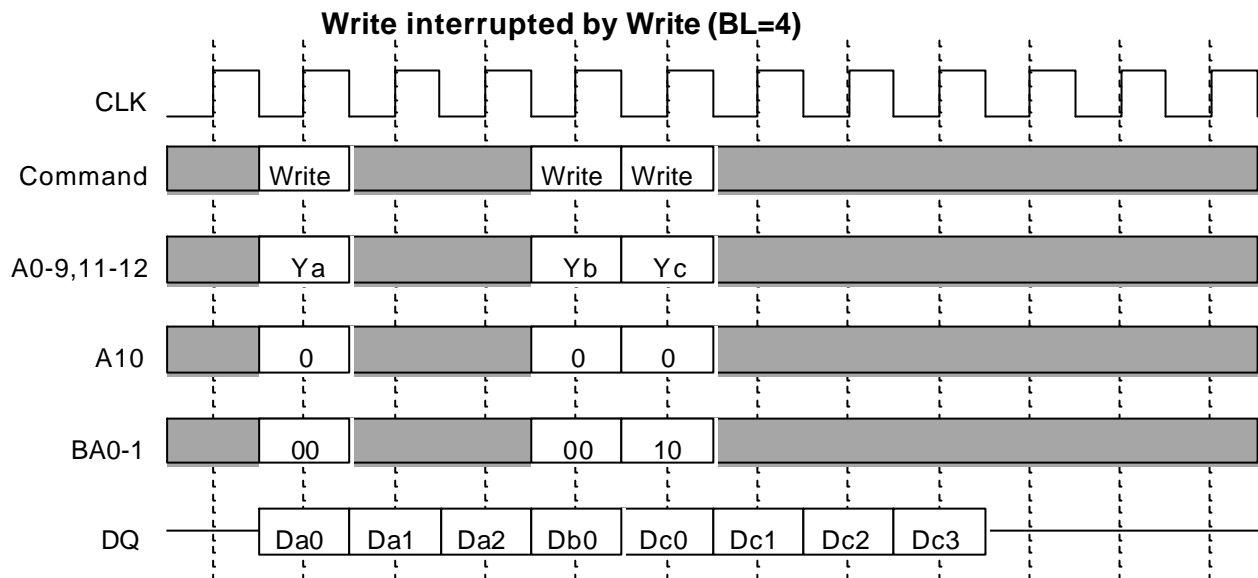
Similarly to the precharge, a burst terminate command can interrupt the burst read operation and disable the data output. The terminated bank remains active. READ to TBST interval is minimum 1 CLK. A TBST command to output disable latency is equivalent to the /CAS Latency.

**Read interrupted by Terminate (BL=4)**



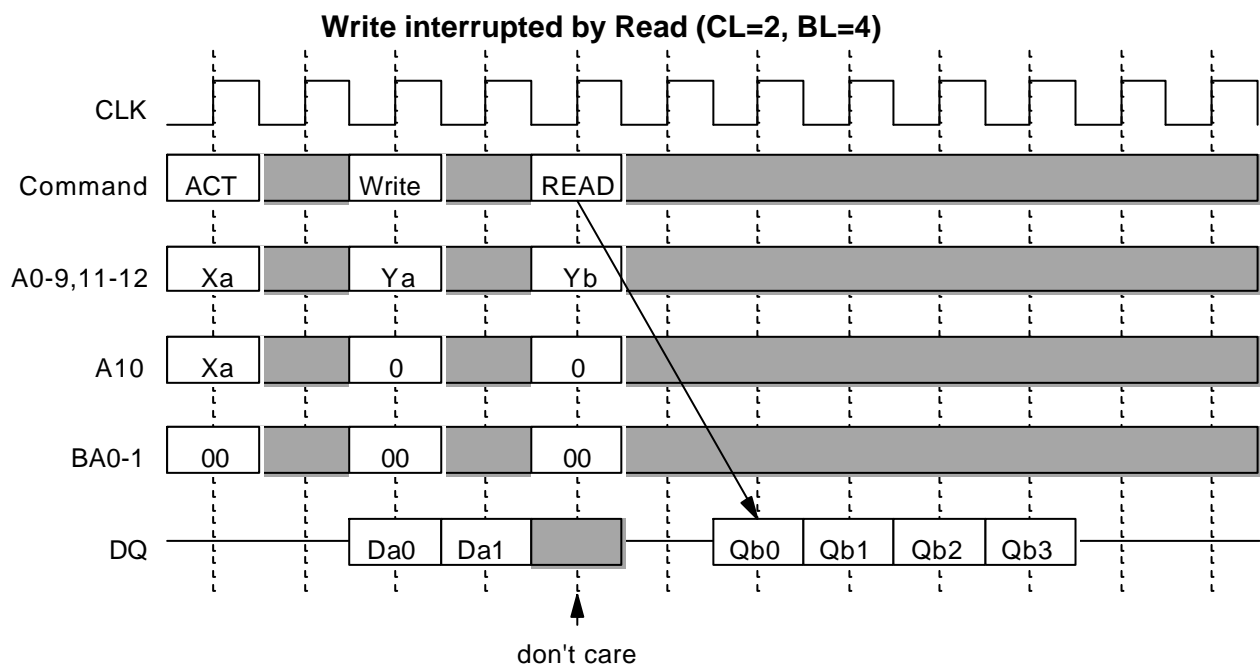
### [ Write Interrupted by Write ]

Burst write operation can be interrupted by new write of any active bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.



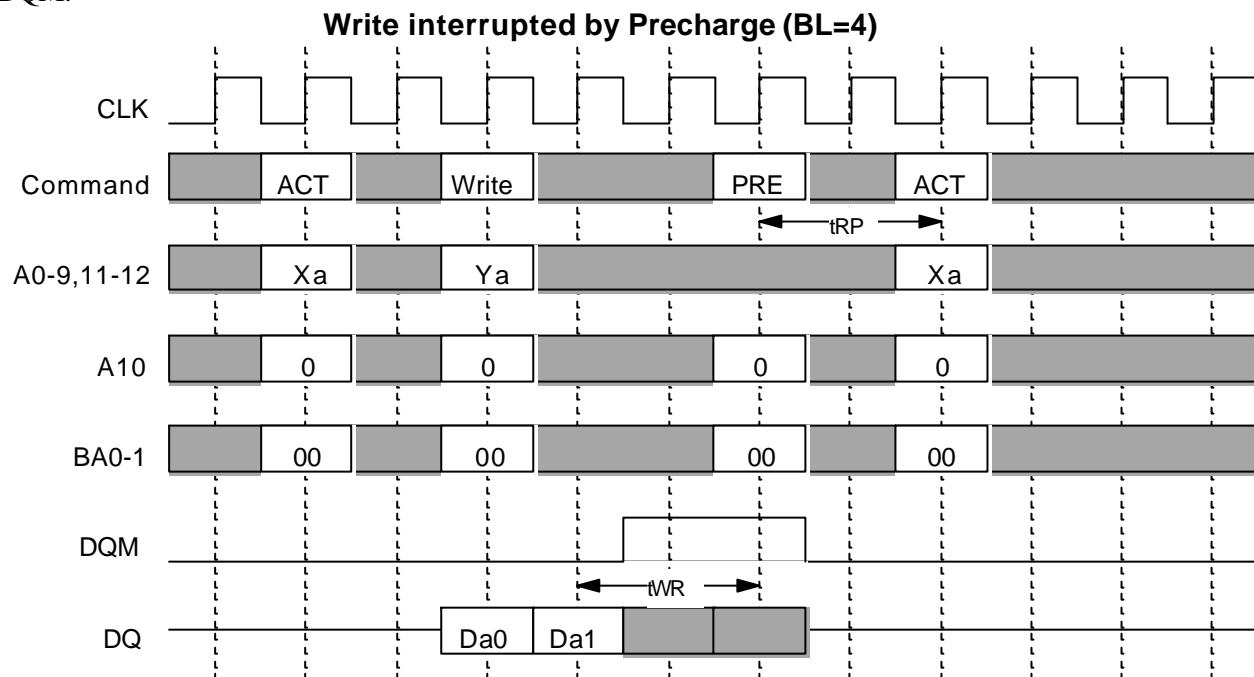
### [ Write Interrupted by Read ]

Burst write operation can be interrupted by read of any active bank. Random column access is allowed. WRITE to READ interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "Don't Care".

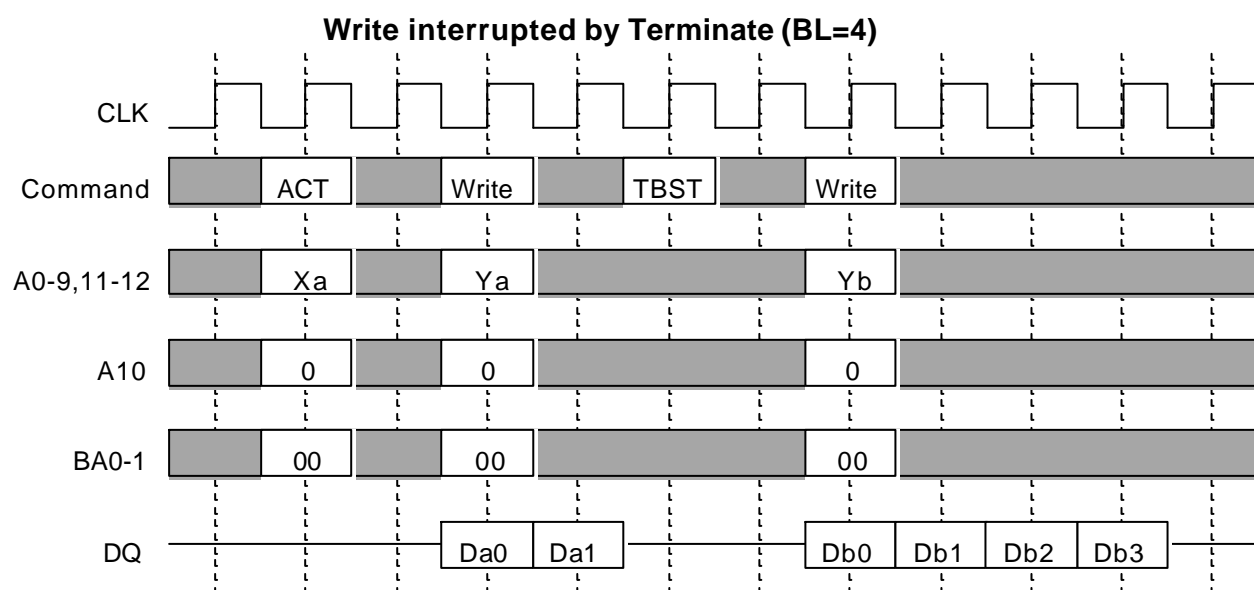


**[ Write Interrupted by Precharge ]**

Burst write operation can be interrupted by precharge of *the same bank*. Write recovery time ( $t_{WR}$ ) is required from the last data to PRE command. During write recovery, data inputs must be masked by DQM.

**[ Write Interrupted by Burst Terminate ]**

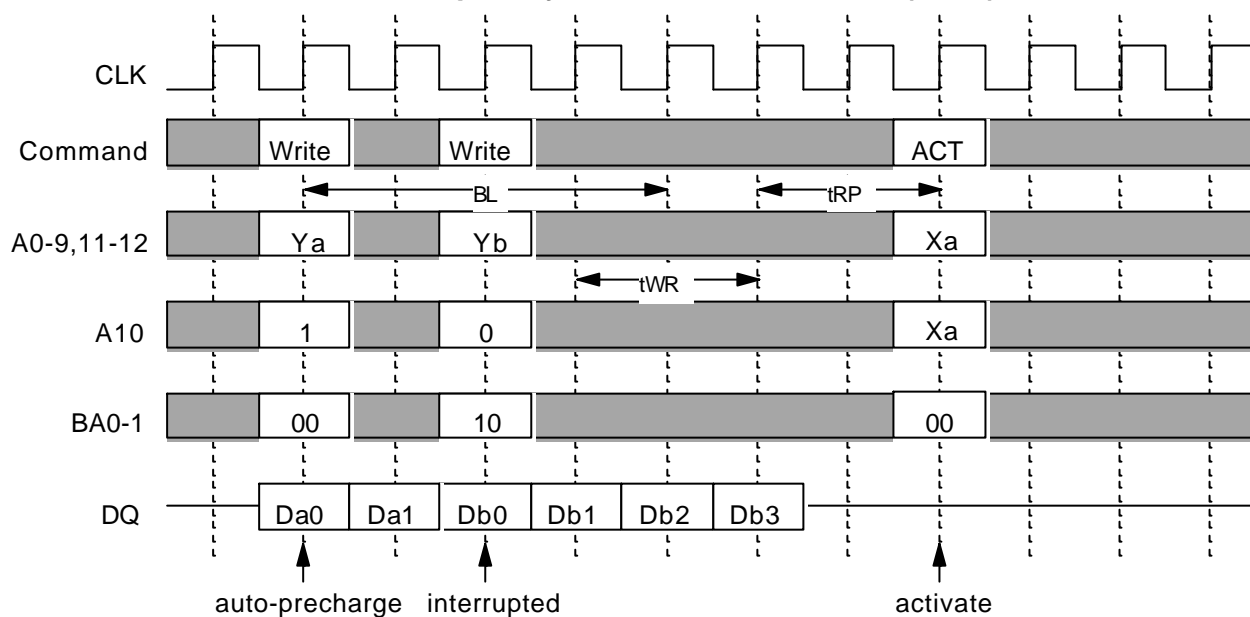
Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. WRITE to TBST interval is minimum 1 CLK.



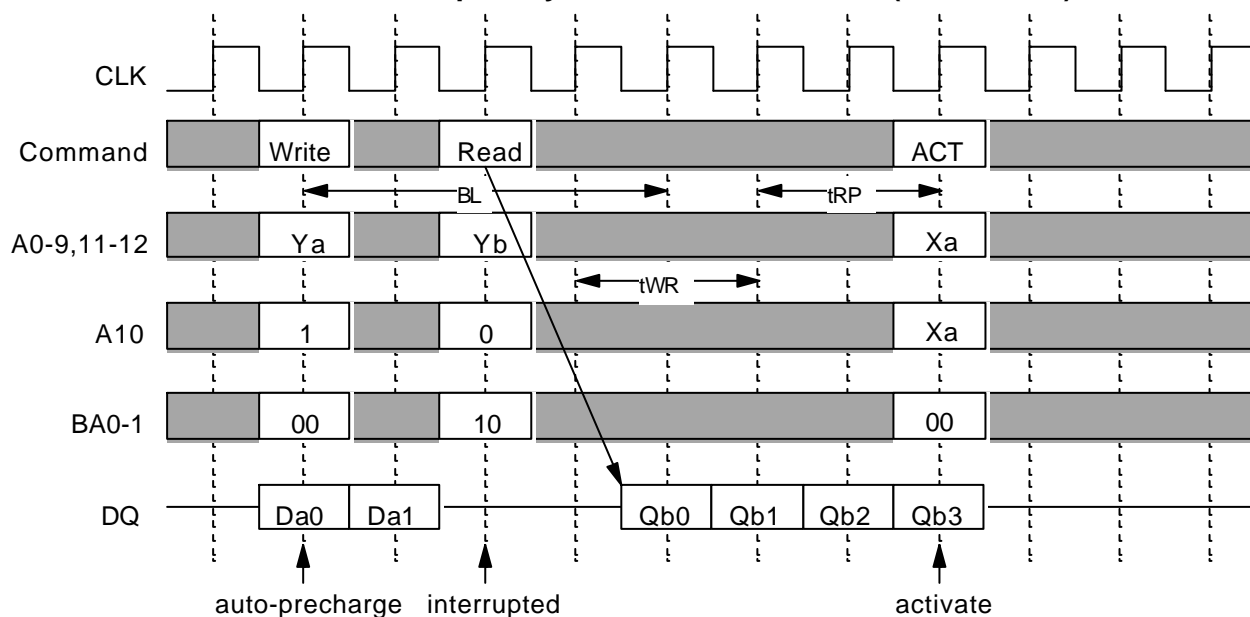
# [ Write with Auto-Precharge Interrupted by Write / Read to another Bank ]

Burst write with auto-precharge can be interrupted by write or read to **another** bank. Next ACT command can be issued after  $(BL+tWR-1+tRP)$  from the WRITEEA. Auto-precharge interruption by a command to the same bank is inhibited.

## WRITEEA interrupted by WRITE to another bank (BL=4)

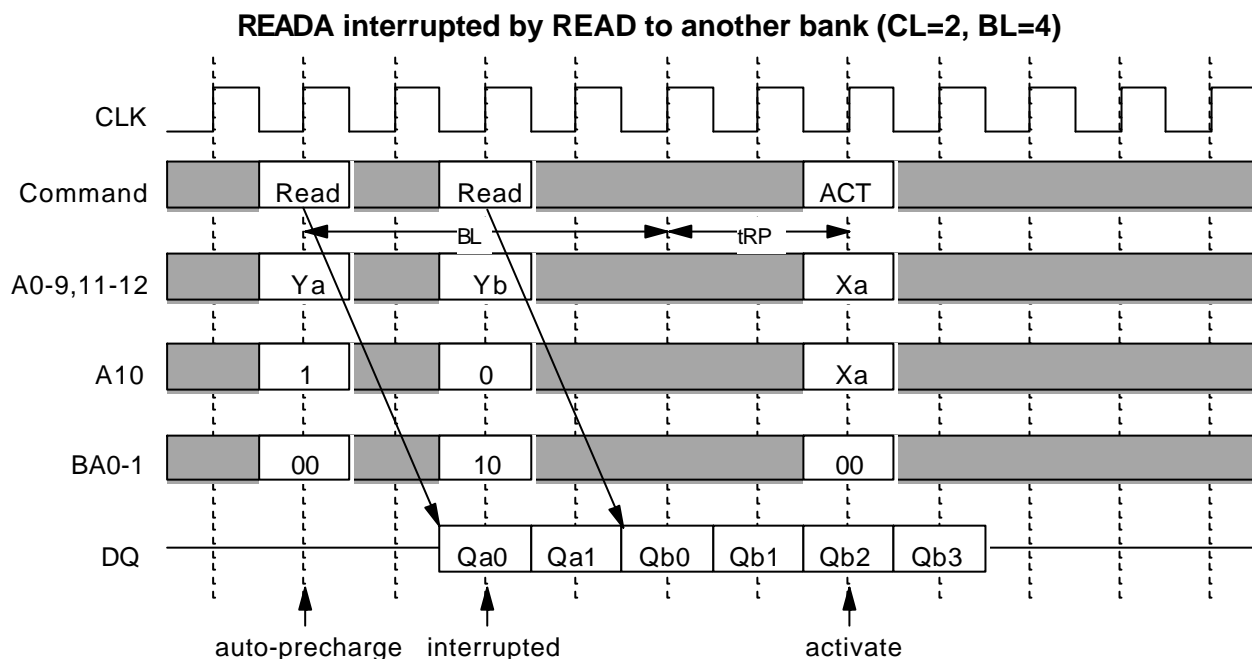


## WRITEEA interrupted by READ to another bank (CL=2, BL=4)



### [ Read with Auto-Precharge Interrupted by Read to another Bank ]

Burst read with auto-precharge can be interrupted by read to **another** bank. Next ACT comand can be issued after (BL+tRP) from the READA. Auto-precharge interruption by a command to the same bank is inhibited.



### Full Page Burst

Full page burst length is available for only the sequential burst type. Full page burst read / write is repeated until a Precharge or a Burst Terminate command is issued. In case of the full page burst, a read / write with auto-precharge command is illegal.

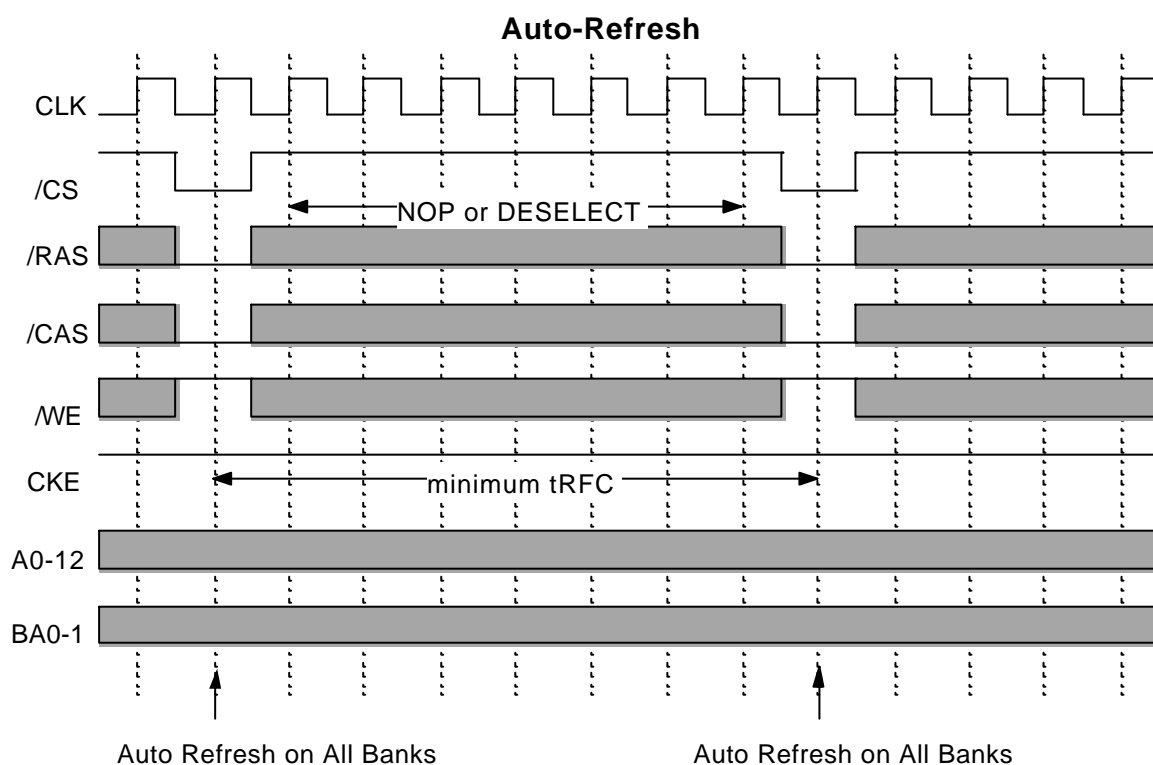
### Single Write

When single write mode is set, burst length for write is always one, independently of Burst Length defined by (A2-0).



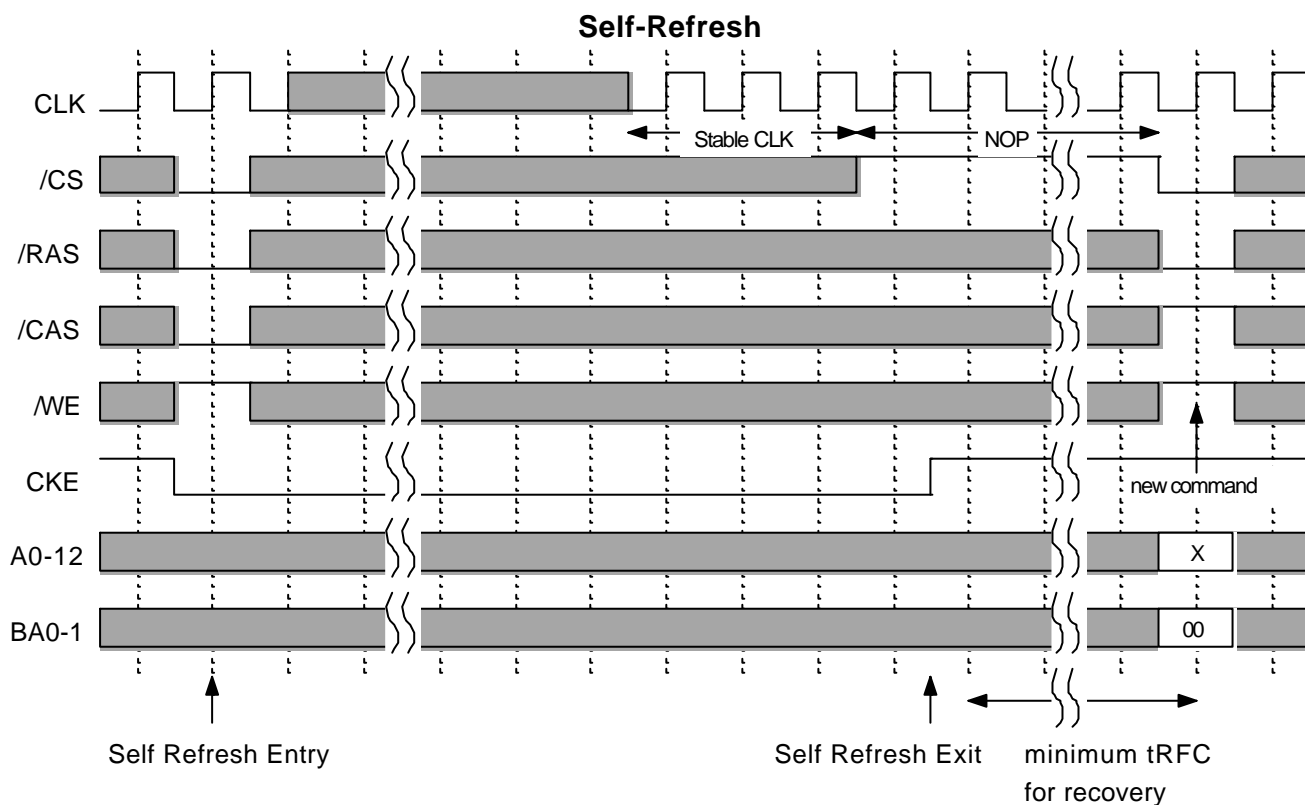
**AUTO REFRESH**

Single cycle of auto-refresh is initiated with a REFA (/CS= /RAS= /CAS= L, /WE= /CKE= H) command. The refresh address is generated internally. 8192 REFA cycles within 64ms refresh 256Mbit memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto-refresh, all banks must be in idle state. Auto-refresh to auto-refresh interval is minimum tRFC. Any command must not be issued before tRFC from the REFA command.



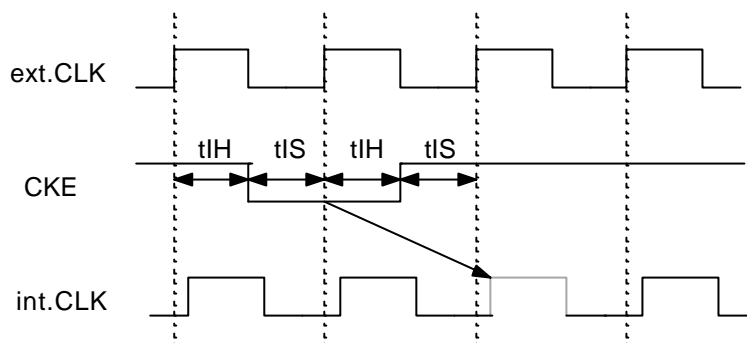
**SELF REFRESH**

Self-refresh mode is entered by issuing a REFS command (/CS= /RAS= /CAS= L, /WE= H, CKE= L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input. All other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE=H. After tRFC from the 1st CLK edge following CKE=H, all banks are in idle state and a new command can be issued, but DESEL or NOP commands must be asserted till then.

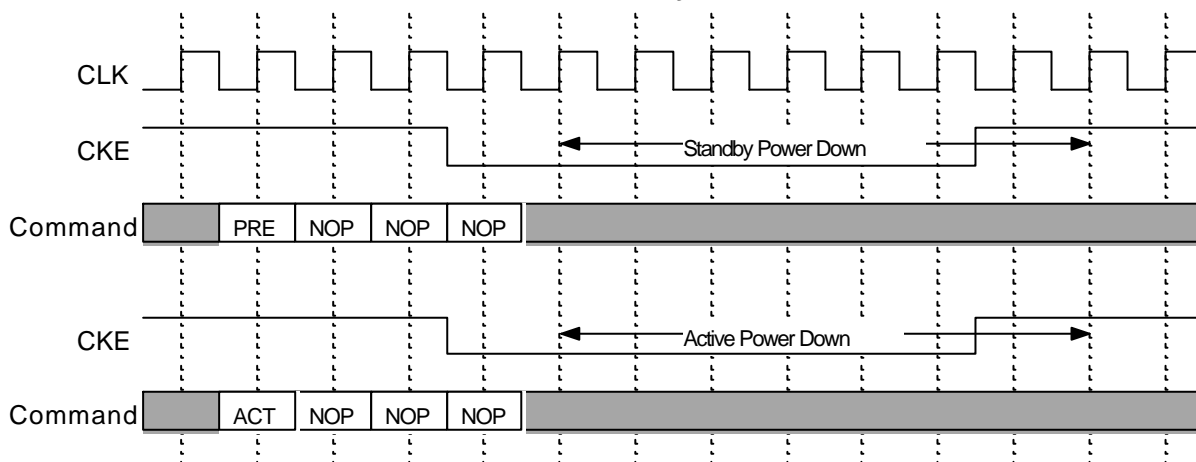


## CLK SUSPEND and POWER DOWN

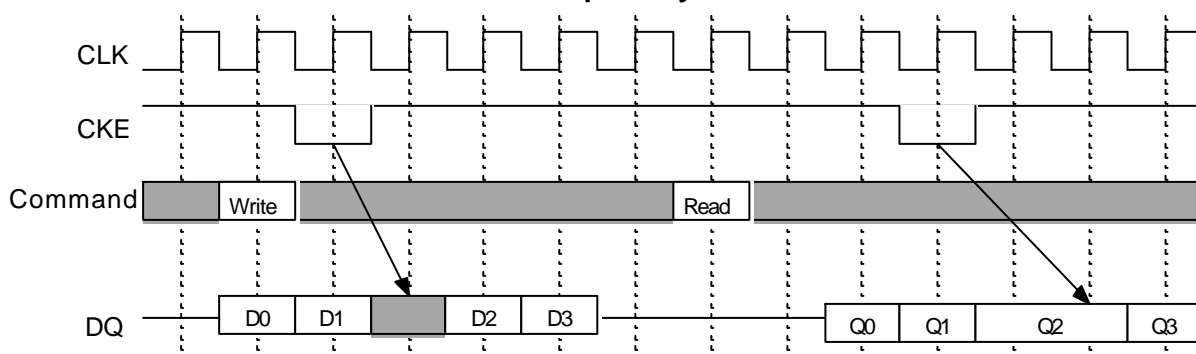
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.



### Power Down by CKE

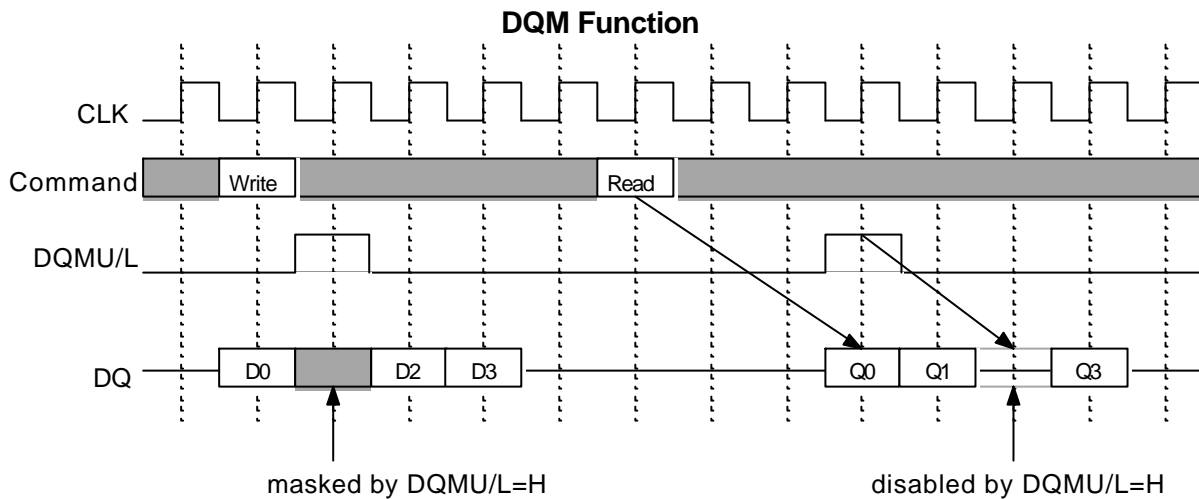


### DQ Suspend by CKE



**DQM CONTROL**

DQMU/L is a dual functional signal defined as the data mask for writes and the output disable for reads. During writes, DQMU/L masks input data word by word. DQMU/L to Data In latency is 0. During reads, DQMU/L forces output to Hi-Z word by word. DQMU/L to output Hi-Z latency is 2.



SDRAM (Rev.1.1)

Single Data Rate

**M2V56S20/ 30/ 40 ATP -5, -5L, -6, -6L, -7, -7L**

Aug '01

256M Synchronous DRAM

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>dd</sub>	Supply Voltage	with respect to V <sub>ss</sub>	-0.5 ~ 4.6	V
V <sub>ddQ</sub>	Supply Voltage for Output	with respect to V <sub>ssQ</sub>	-0.5 ~ 4.6	V
V <sub>I</sub>	Input Voltage	with respect to V <sub>ss</sub>	-0.5 ~ V <sub>dd</sub> +0.5	V
V <sub>O</sub>	Output Voltage	with respect to V <sub>ssQ</sub>	-0.5 ~ V <sub>ddQ</sub> +0.5	V
I <sub>O</sub>	Output Current		50	mA
P <sub>d</sub>	Power Dissipation	T <sub>a</sub> =25°C	1000	mW
T <sub>opr</sub>	Operating Temperature		0 ~ 70	°C
T <sub>stg</sub>	Storage Temperature		-65 ~ 150	°C

**RECOMMENDED OPERATING CONDITIONS**(T<sub>a</sub>=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>dd</sub>	Supply Voltage	3.0	3.3	3.6	V
V <sub>ss</sub>	Supply Voltage	0	0	0	V
V <sub>ddQ</sub>	Supply Voltage for Output	3.0	3.3	3.6	V
V <sub>ssQ</sub>	Supply Voltage for Output	0	0	0	V
V <sub>IH</sub>	High-Level Input Voltage all inputs	2.0		V <sub>dd</sub> +0.3	V
V <sub>IL</sub>	Low-Level Input Voltage all inputs	-0.3		0.8	V

**CAPACITANCE**(T<sub>a</sub>=0 ~ 70°C, V<sub>dd</sub> = V<sub>ddQ</sub> = 3.3 ± 0.3V, V<sub>ss</sub> = V<sub>ssQ</sub> = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Unit
			Min.	Max.	
C <sub>I(A)</sub>	Input Capacitance, address pin	V <sub>I</sub> =1.4V f=1MHz V <sub>I</sub> =25mVrms	2.5	3.8	pF
C <sub>I(C)</sub>	Input Capacitance, control pin		2.5	3.8	pF
C <sub>I(K)</sub>	Input Capacitance, CLK pin		2.5	3.5	pF
C <sub>I/O</sub>	Input Capacitance, I/O pin		4.0	6.5	pF

SDRAM (Rev.1.1)

Single Data Rate

**M2V56S20/ 30/ 40 ATP -5, -5L, -6, -6L, -7, -7L**

Aug '01

256M Synchronous DRAM

**AVERAGE SUPPLY CURRENT from Vdd**

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3V, Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter	Test Conditions	Organi- zation	Limits(max)			Unit	Note
				-5	-6	-7		
Icc1	Operating Current (1bank)	tCLK=min, tRC=min, BL=1	x4	110	90	80	mA	1
			x8	115	95	85		
			x16	120	100	90		
Icc2P	Idle Standby Current	tCLK=min, CKE<VILmax		2	1.5	1	mA	2
Icc2PS	in Power Down Mode	tCLK=L, CKE<VILmax		1	1	1		
Icc2N	Idle Standby Current	tCLK=min, CKE>VIHmin, /CS>VIHmin		30	25	20	mA	2,3
Icc2NS	in Normal Mode	tCLK=L, CKE>VIHmin		6	6	6		
Icc3N	Active Standby Current	tCLK=min, CKE>VIHmin, /CS> VIHmin		35	30	25	mA	3,5
Icc3NS	in Normal Mode	tCLK=L, CKE>VIHmin		15	15	15		
Icc4	Burst Operating Current	tCLK=min, BL=4, gapless data	x4	140	110	90	mA	5
			x8	140	110	90		
			x16	150	120	100		
Icc5	Auto-Refresh Current	tCLK=min, tRFC=min		220	180	170	mA	
Icc6	Self-Refresh Current	CKE<0.2v	-5/-6/-7	3	3	3		
			-5L/-6L/-7L	2	2	2		

## Notes

- addresses are changed 3 times during tRC, only 1 bank is active & all other banks are idle
- all banks are idle
- input signals are changed one time during 3xtCLK
- input signals are stable
- all banks are active
- Low Power Version (-5L/-6L/-7L)

**AC OPERATING CONDITIONS AND CHARACTERISTICS**

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min.	Max.	
VOH(DC)	High-Level Output Voltage (DC)	IOH=-2mA	2.4		V
VOL(DC)	Low-Level Output Voltage (DC)	IOL= 2mA		0.4	V
IOZ	Off-state Output Current	Q floating Vo=0 ~ VddQ	-10	10	μA
II	Input Current	VIH=0 ~ VddQ+0.3V, other input pins=0V	-10	10	μA

SDRAM (Rev.1.1)

Single Data Rate

**M2V56S20/ 30/ 40 ATP -5, -5L, -6, -6L, -7, -7L**

Aug '01

256M Synchronous DRAM

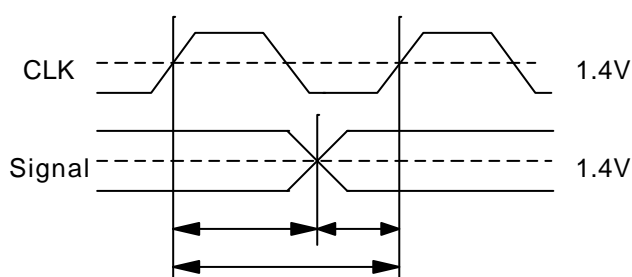
**AC TIMING REQUIREMENTS**

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3V, Vss = VssQ = 0V, unless otherwise noted)

Input Pulse Levels: 0.8V to 2.0V

Input Timing Measurement Level: 1.4V

Symbol	Parameter		Limits						Unit	Note
			-5		-6		-7			
			Min.	Max.	Min.	Max.	Min.	Max.		
tCLK	CLK cycle time	CL=2	7.5		10		10		ns	
		CL=3	6		7.5		10		ns	
tCH	CLK High pulse width		2.5		2.5		3		ns	
tCL	CLK Low pulse width		2.5		2.5		3		ns	
tT	Transition time of CLK		1	10	1	10	1	10	ns	
tIS	Input Setup time (all inputs)		1.5		1.5		2		ns	
tIH	Input Hold time (all inputs)		0.8		0.8		1		ns	
tRC	Row Cycle time		60		67.5		70		ns	
tRFC	Refresh Cycle time		60		75		80		ns	
tRCD	Row to Column Delay		15		20		20		ns	
tRAS	Row Active time		42	120000	45	120000	50	120000	ns	
tRP	Row Precharge time		15		20		20		ns	
tWR	Write Recovery time		12		15		20		ns	
tRRD	ACT to ACT Delay time		12		15		20		ns	
tRSC	Mode Register Set Cycle time		12		15		20		ns	
tREF	Average Refresh Interval			7.8		7.8		7.8	μs	



AC timing is referenced to the input signal crossing through 1.4V.

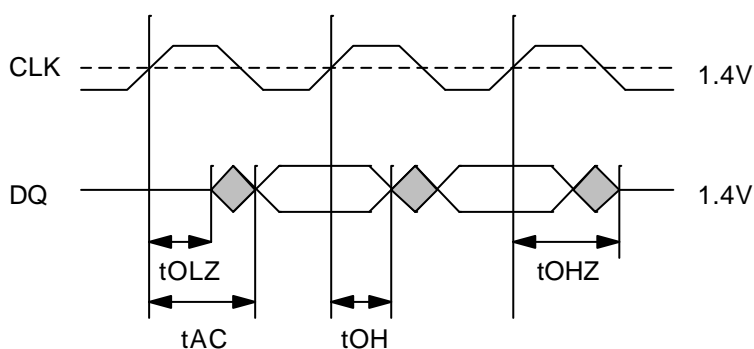
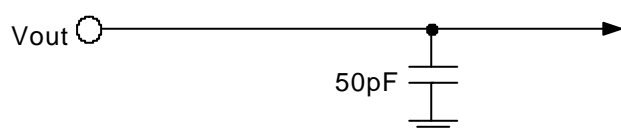
## SWITCHING CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter		Limits						Unit
			-5		-6		-7		
			Min.	Max	Min.	Max	Min.	Max	
tAC	Access Time from CLK	CL=2		5.4		6		6	ns
		CL=3		5.4		5.4		6	ns
tOH	Output Hold Time from CLK	CL=2	3		3		3		ns
		CL=3	3		3		3		ns
tOLZ	Delay Time, Output Low impedance from CLK		0		0		0		ns
tOHZ	Delay Time, Output High impedannce from CLK	CL=2	3	5.4	3	6	3	6	ns
		CL=3	3	5.4	3	5.4	3	6	ns

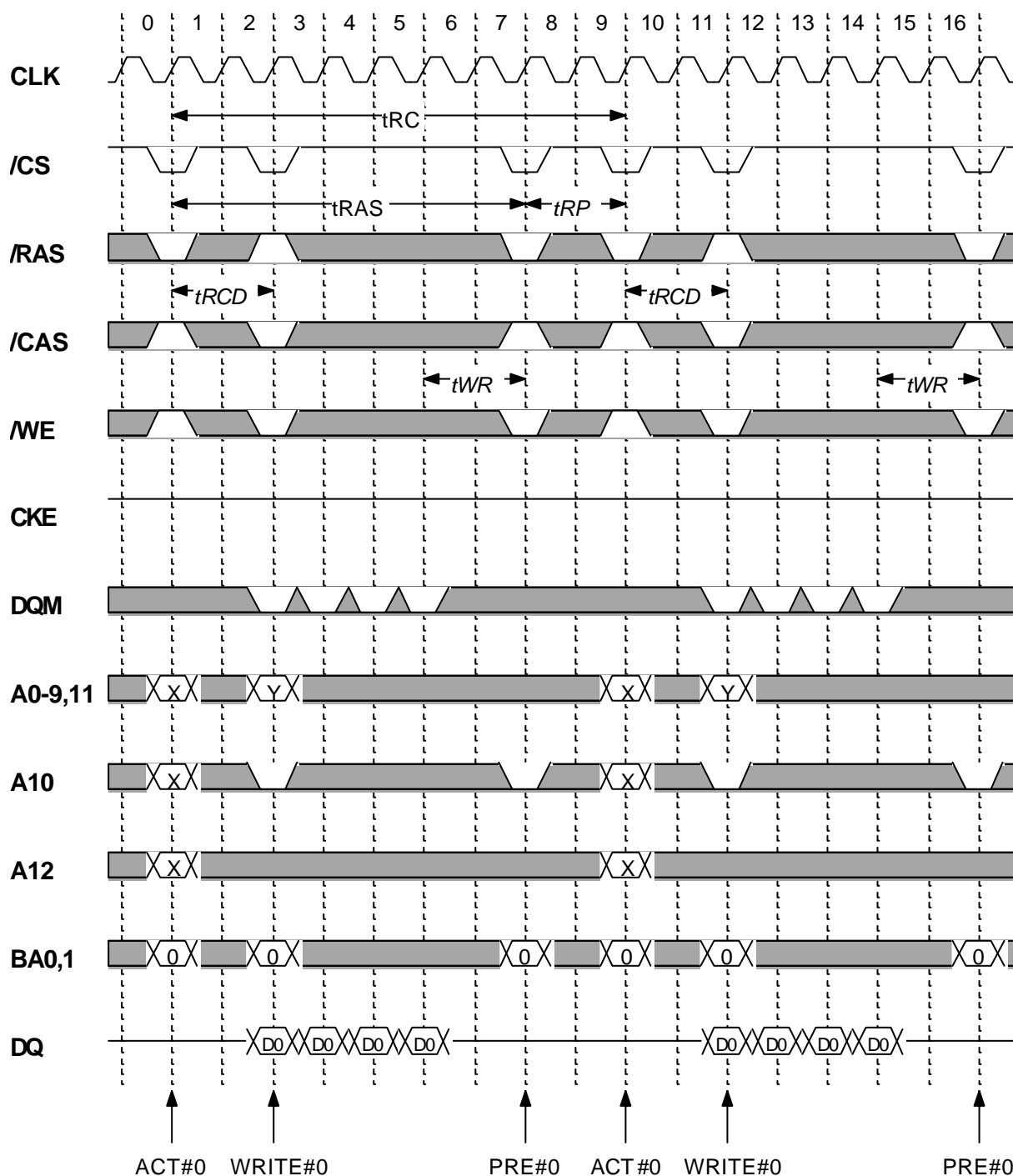
Note. If tr (CLK rising time) is > 1ns, (tr/2 - 0.5ns) should be added to the parameters.

### Output Load Condition



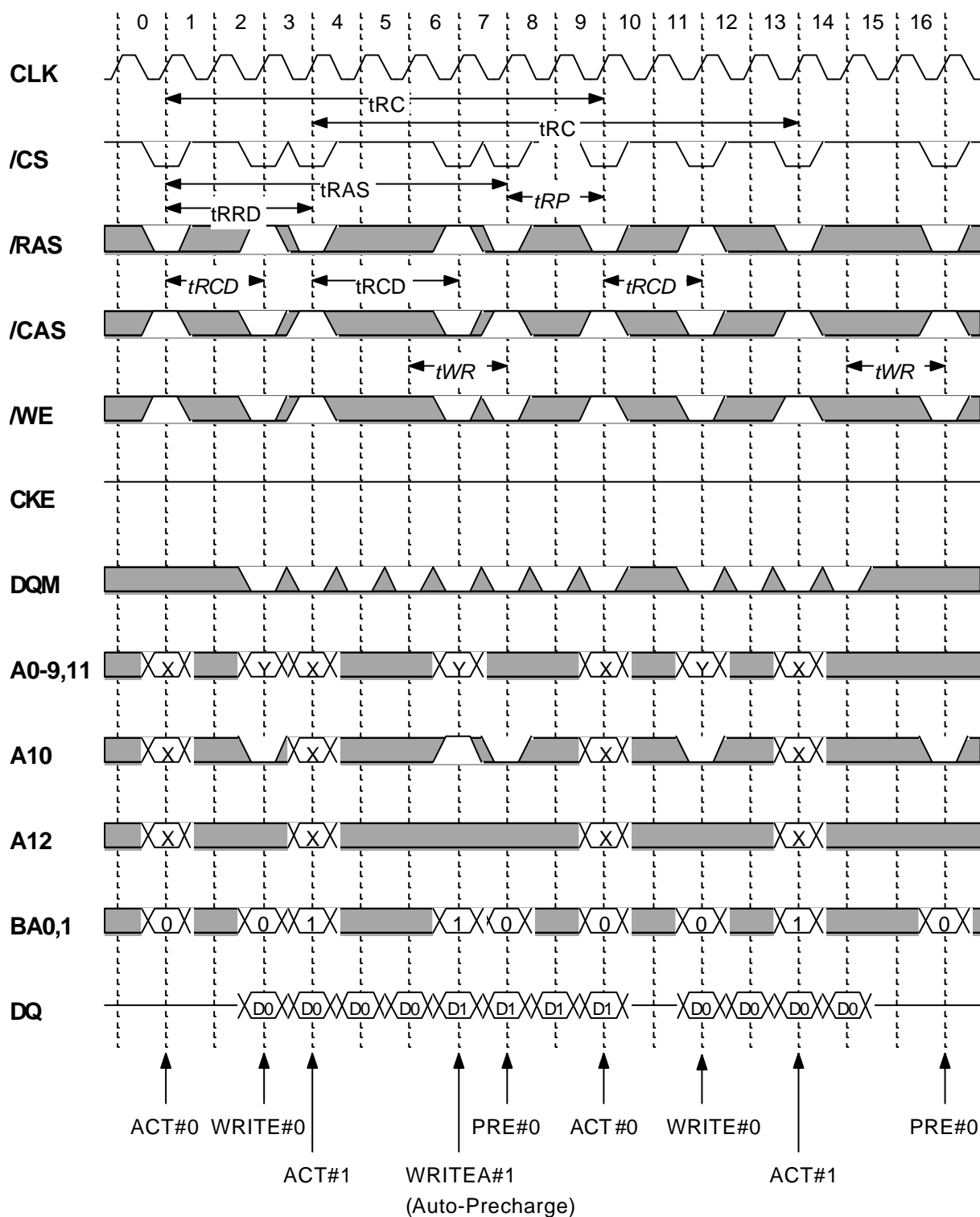


**Burst Write (Single Bank) [BL=4]**



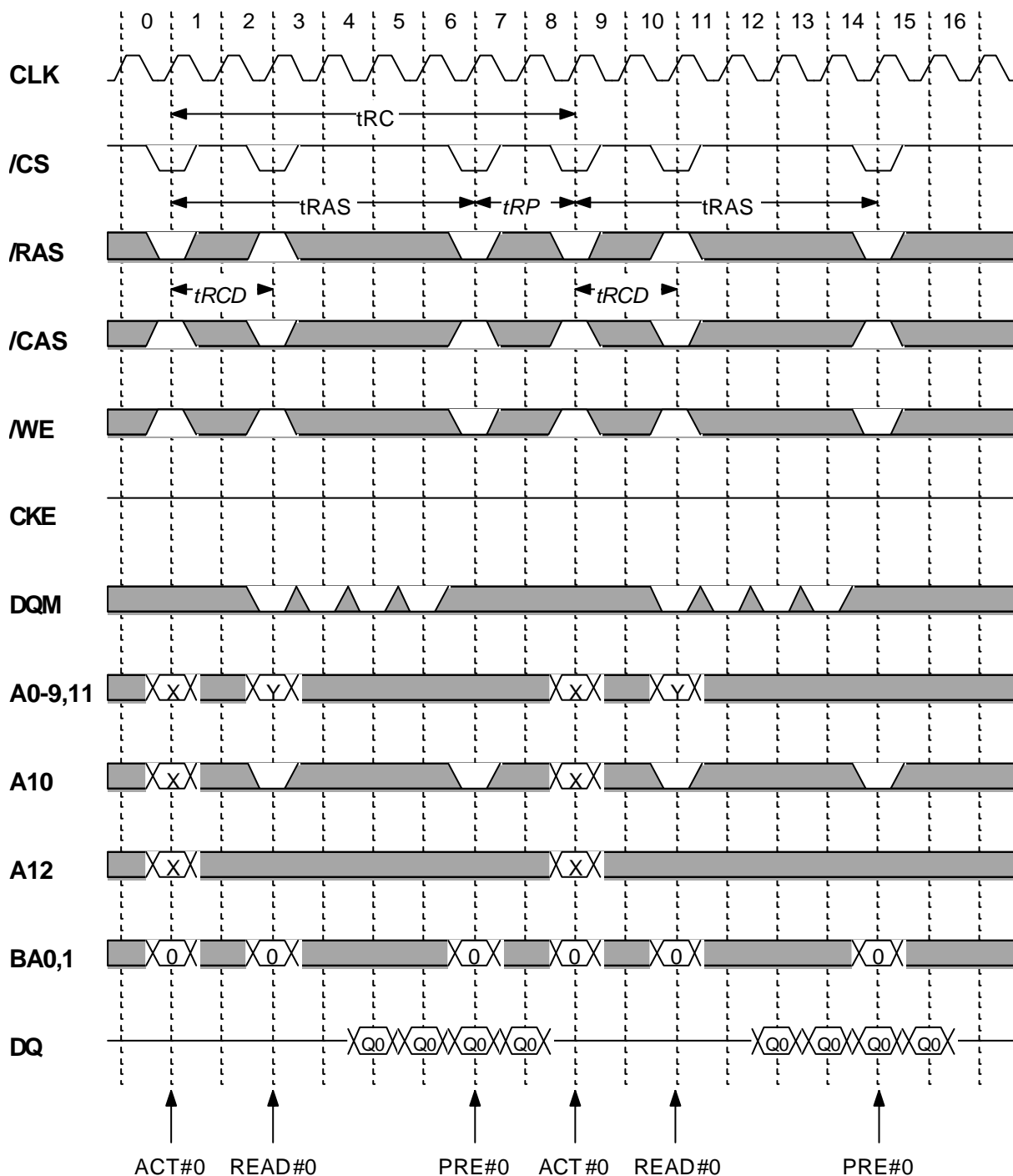
*Italic parameter* shows minimum case

Burst Write (Multi Bank) [BL=4]



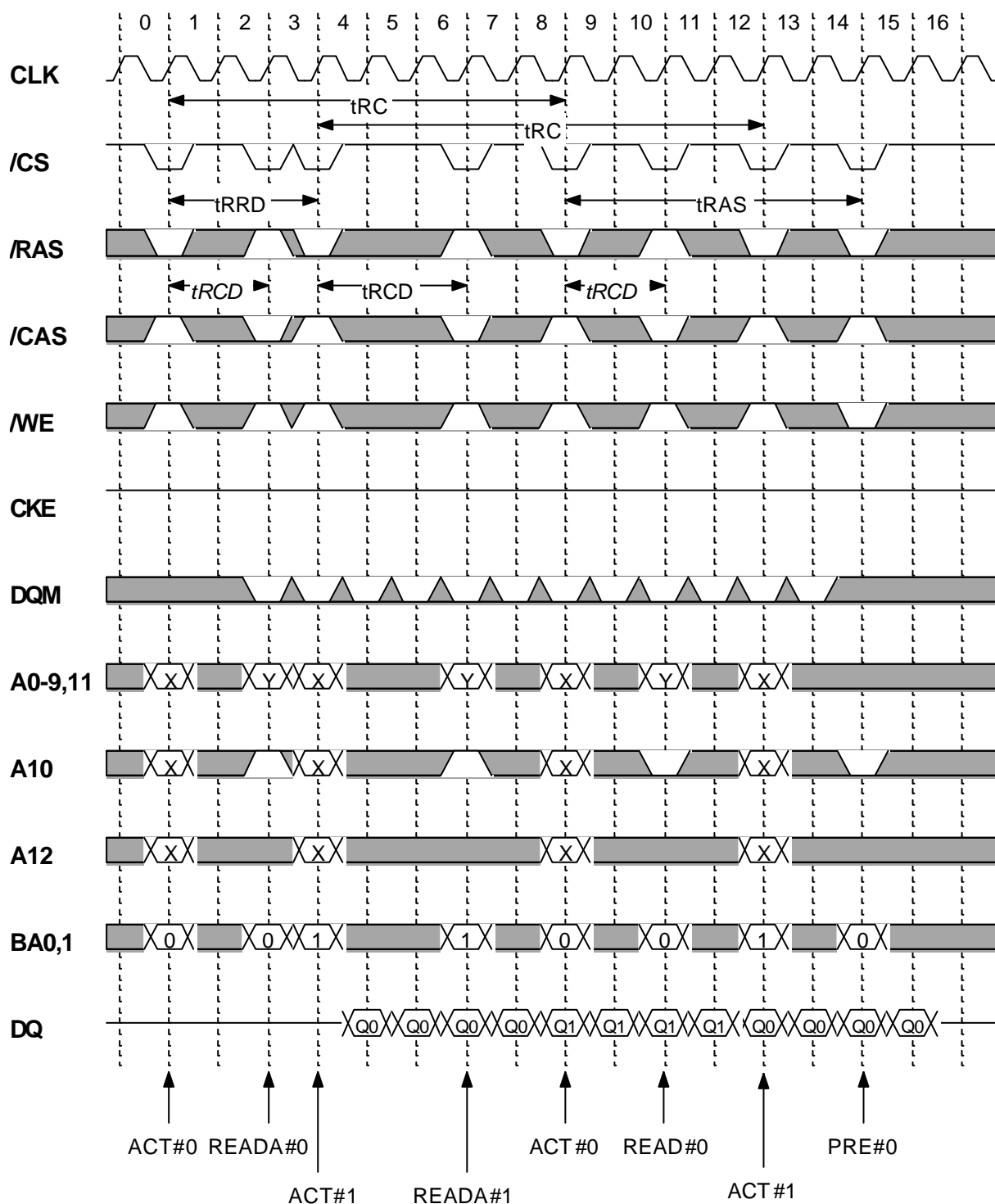
*Italic parameter* shows minimum case

Burst Read (Single Bank) [CL=2, BL=4]



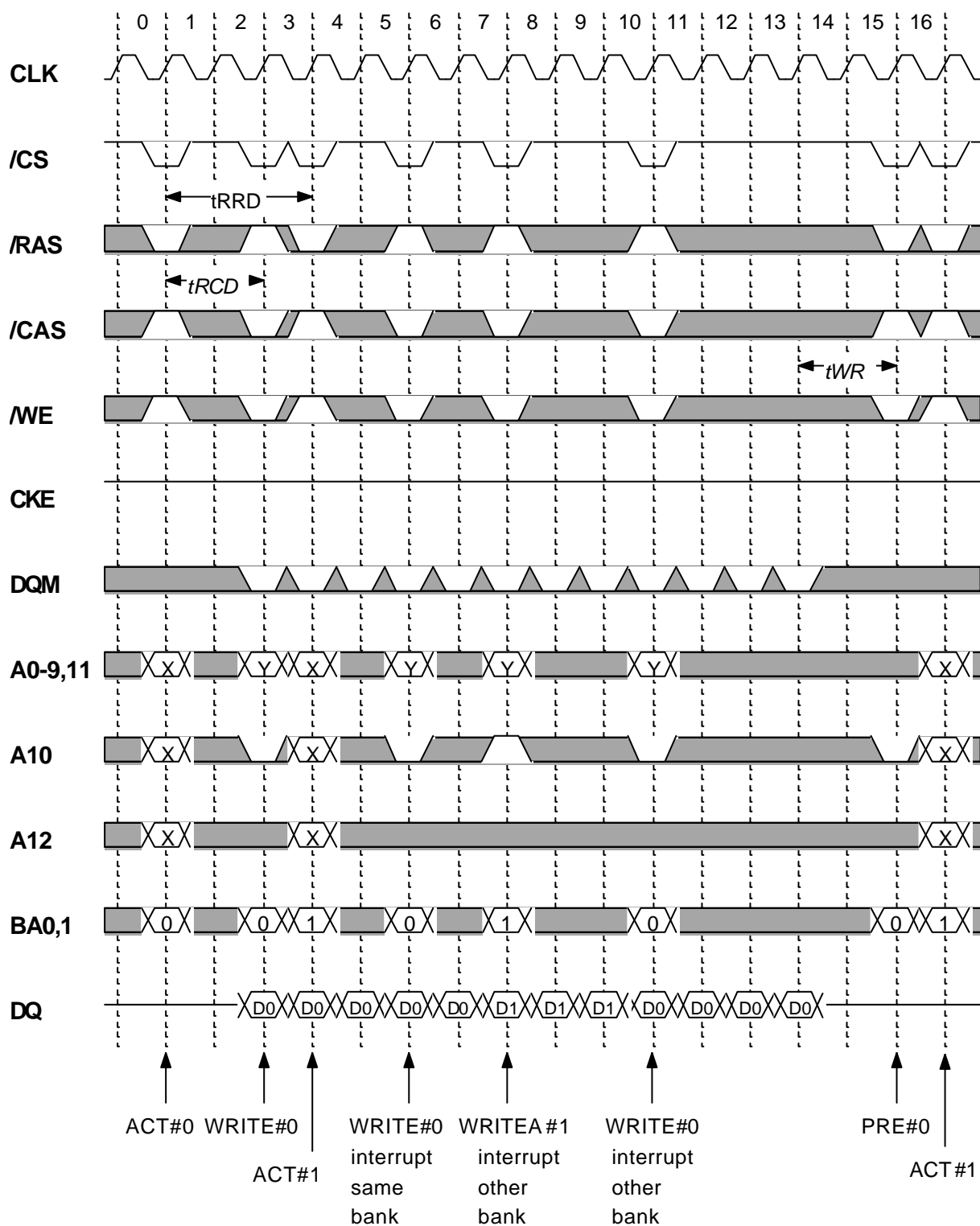
*Italic parameter* shows minimum case

**Burst Read (Multi Bank) [CL=2, BL=4]**



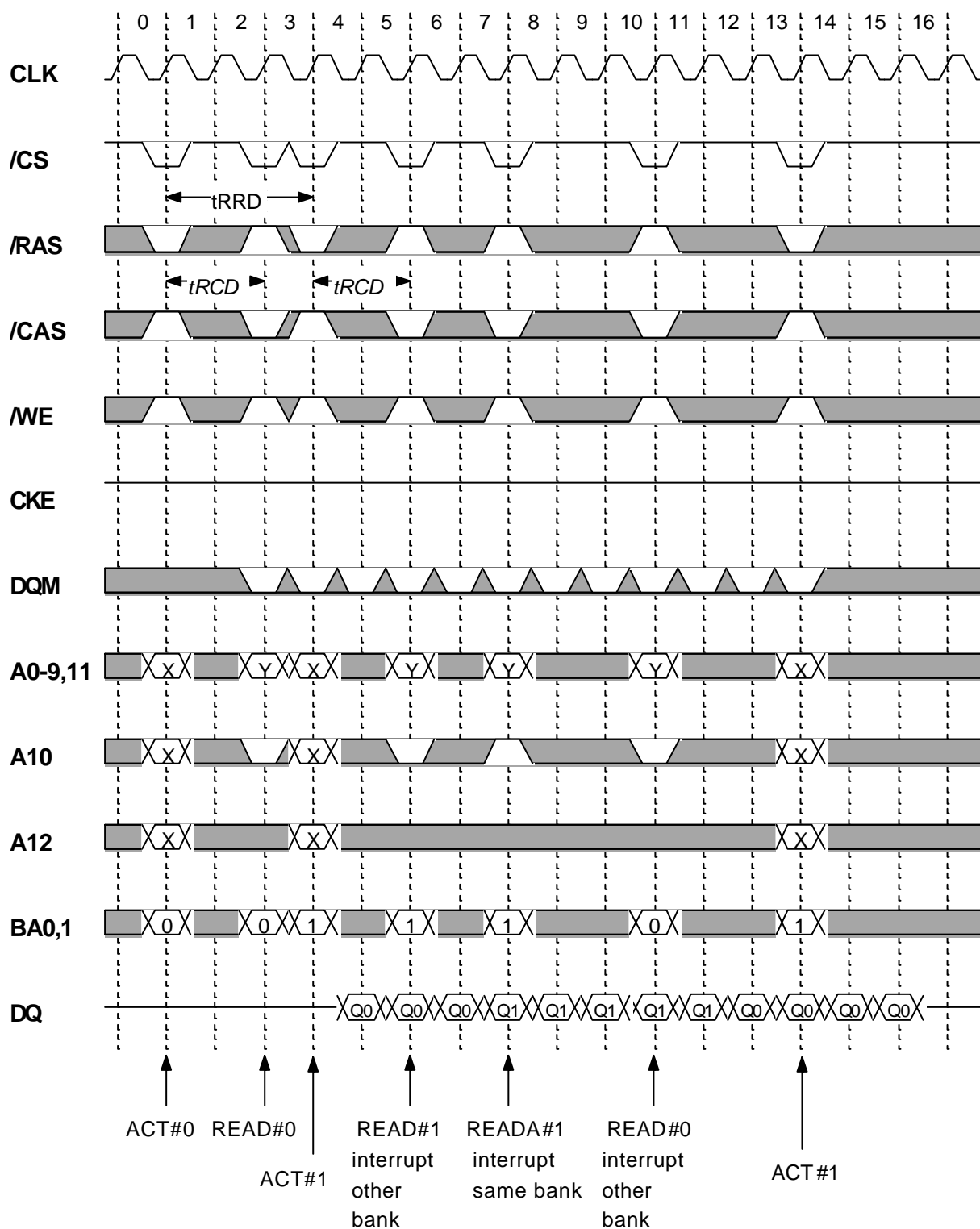
*Italic parameter* shows minimum case

Write Interrupted by Write [BL=4]



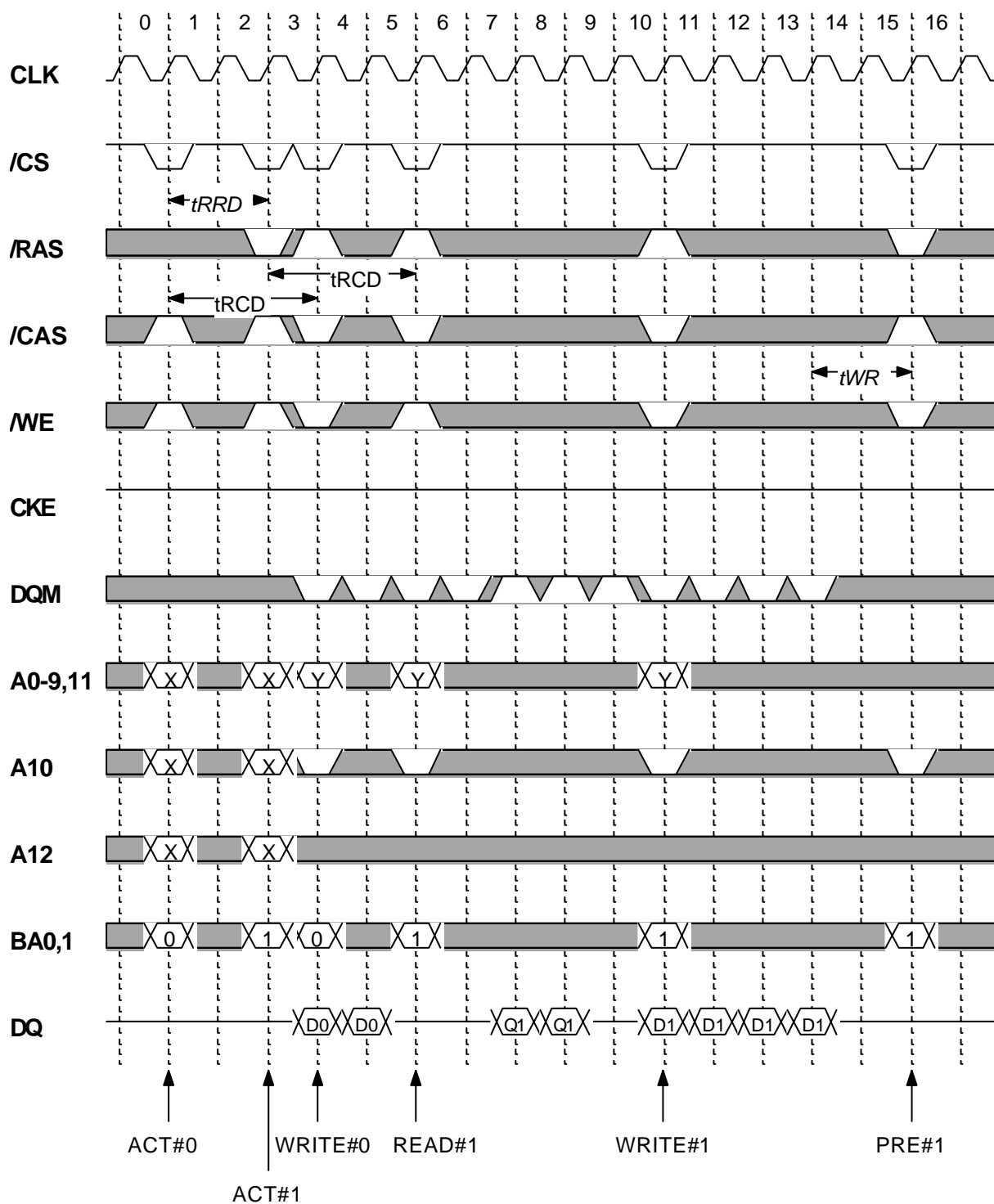
*Italic parameter* shows minimum case

Read Interrupted by Read [CL=2, BL=4]



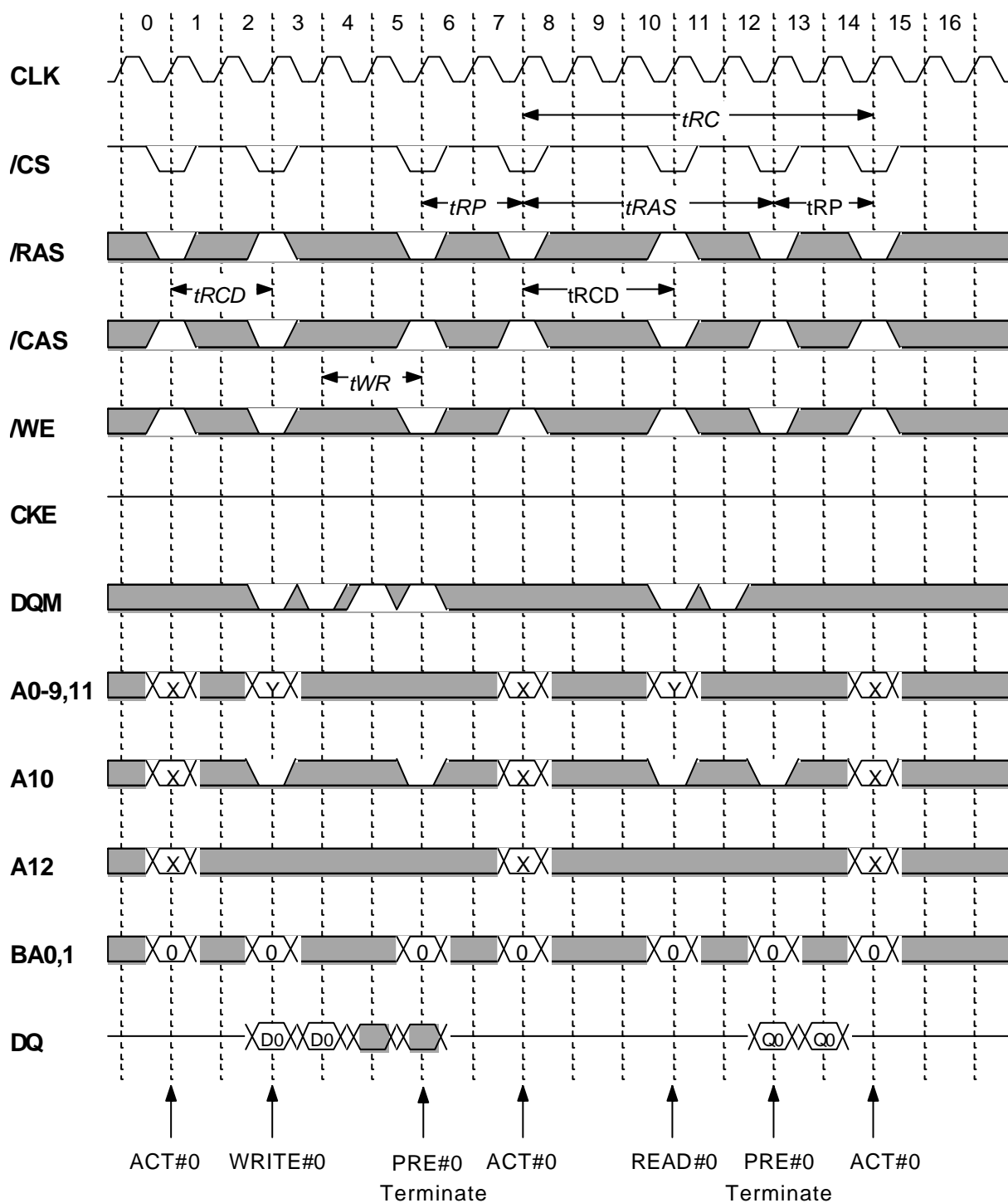
*Italic parameter* shows minimum case

Write Interrupted by Read, Read Interrupted by Write [CL=2, BL=4]



*Italic parameter* shows minimum case

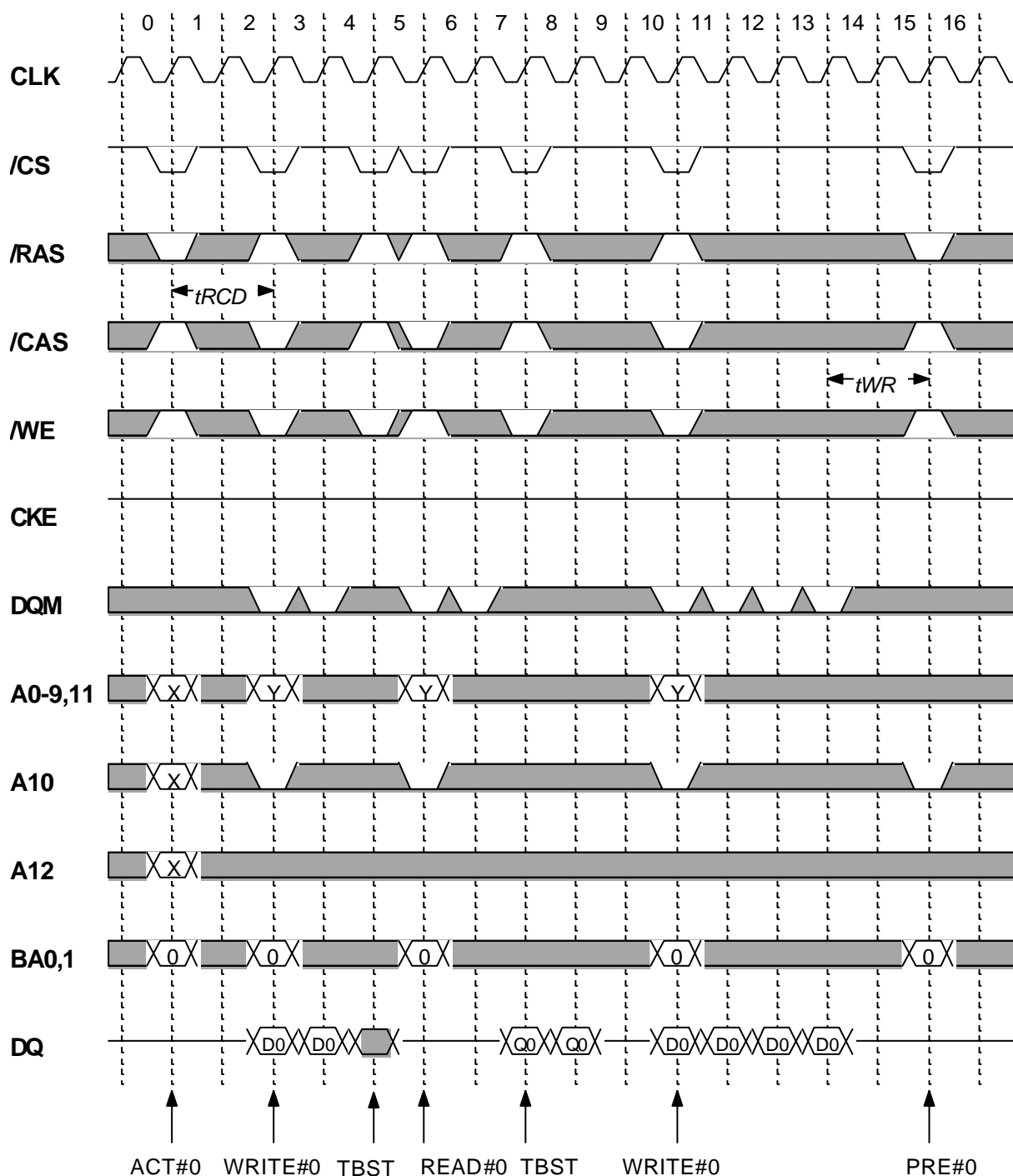
Write / Read Terminated by Precharge [CL=2, BL=4]



*Italic parameter* shows minimum case

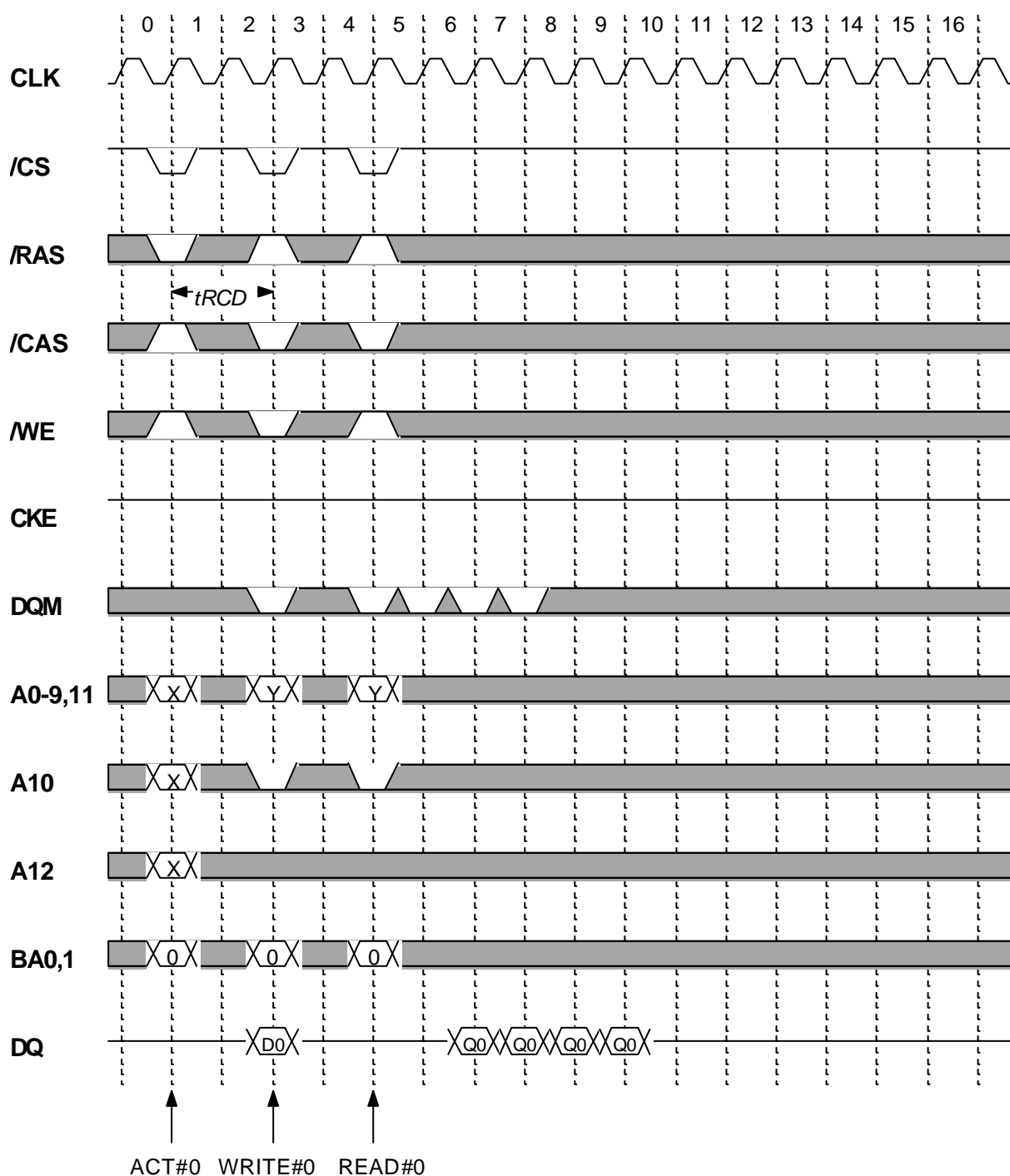


Write / Read Terminated by Burst Terminate [CL=2, BL=4]



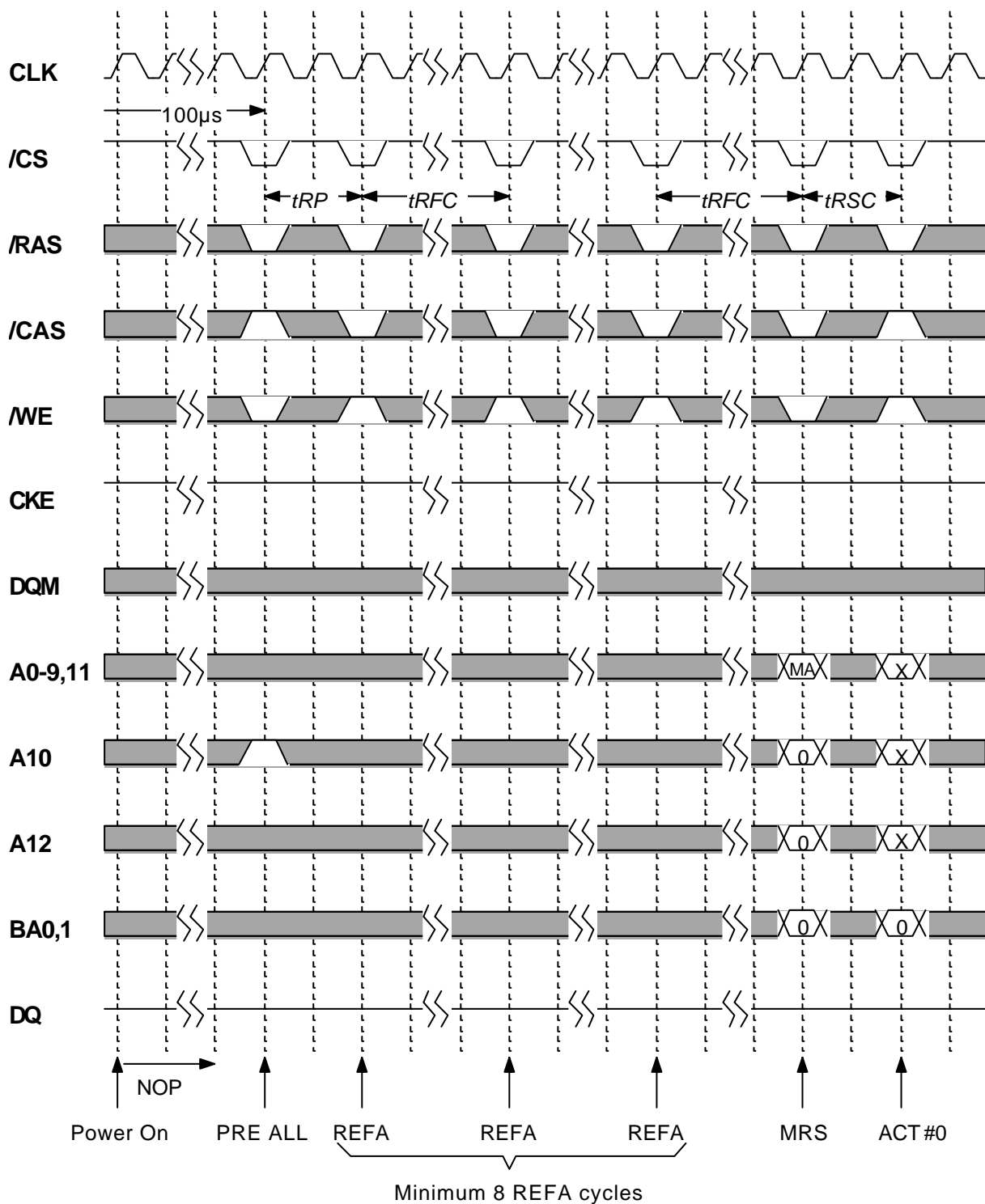
*Italic parameter* shows minimum case

### Single Write Burst Read [CL=2, BL=4]



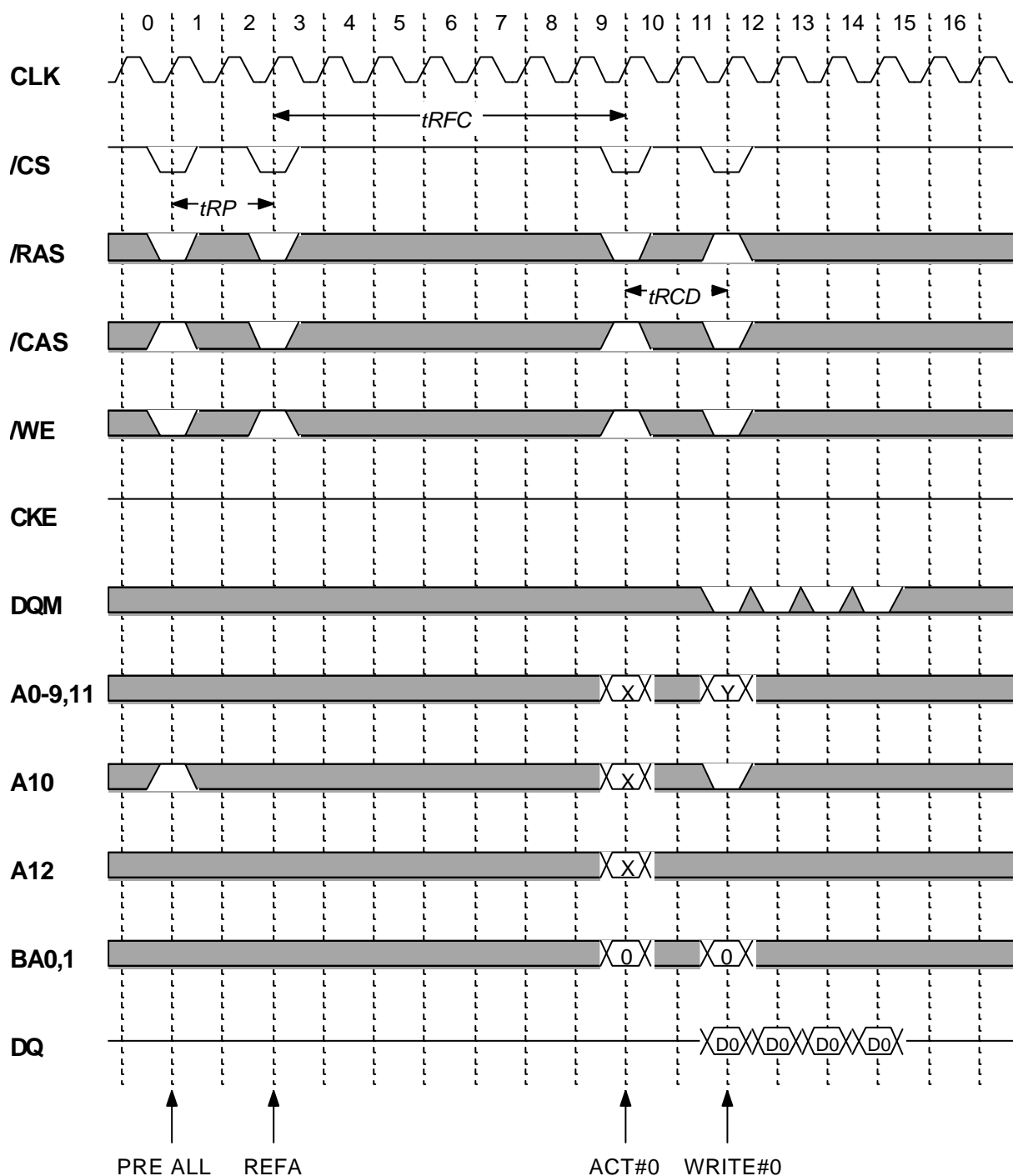
***Italic paramater*** shows minimum case

**Power-Up Sequence and Intialize**



*Italic paramater* shows minimum case

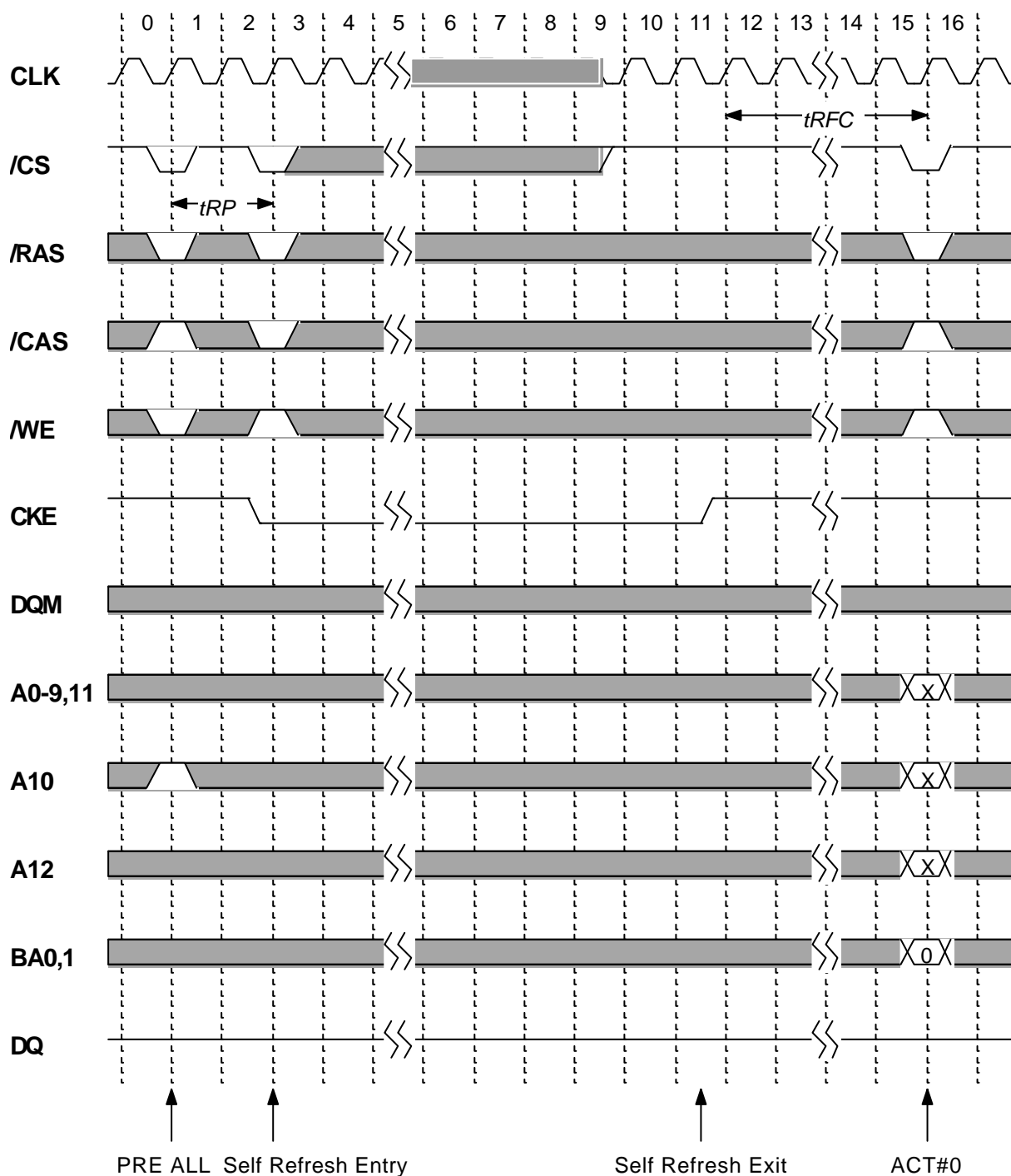
### Auto Refresh



All banks must be idle before REFA is issued.

*Italic parameter* shows minimum case

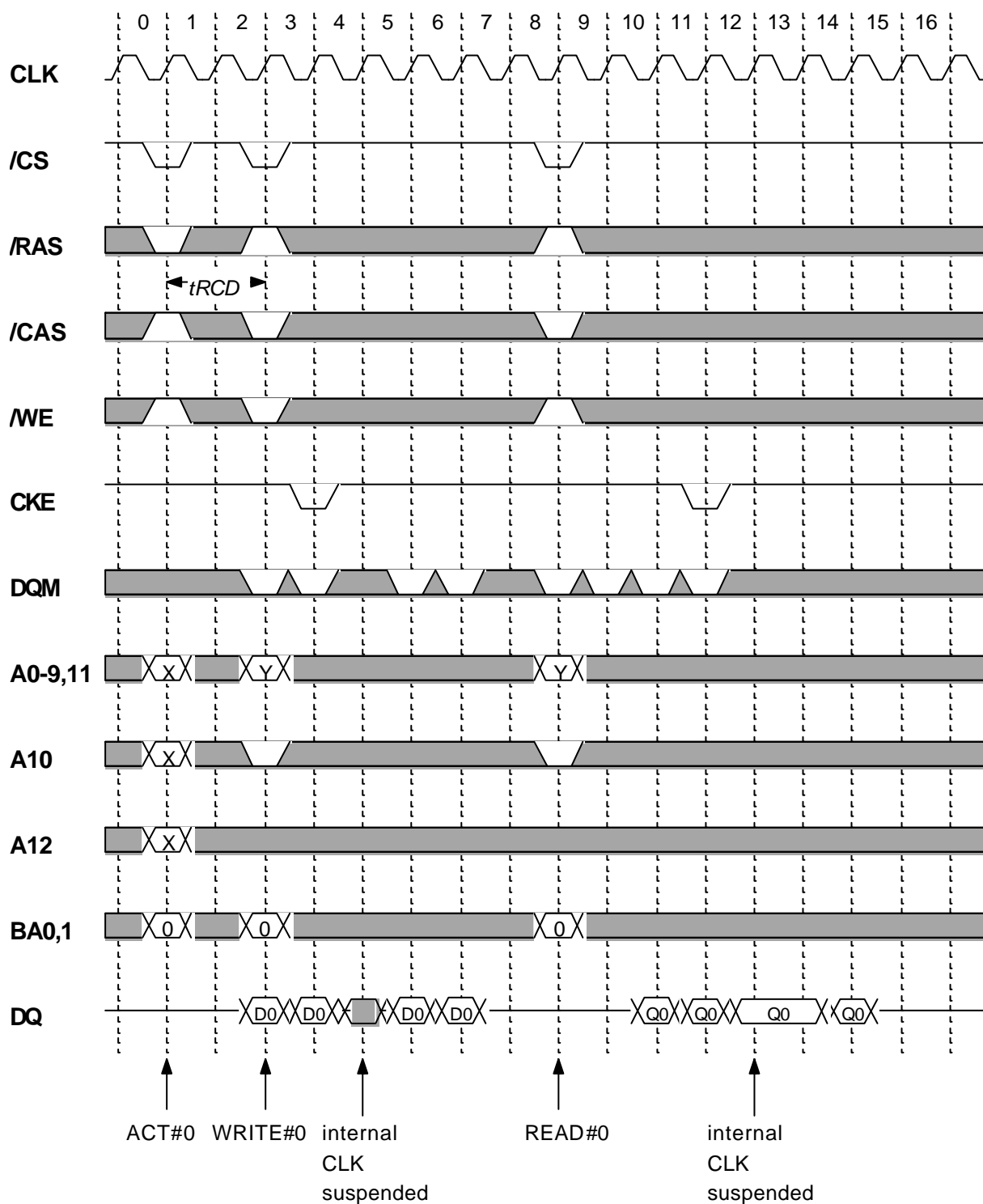
# Self Refresh



All banks must be idle before REFS is issued.

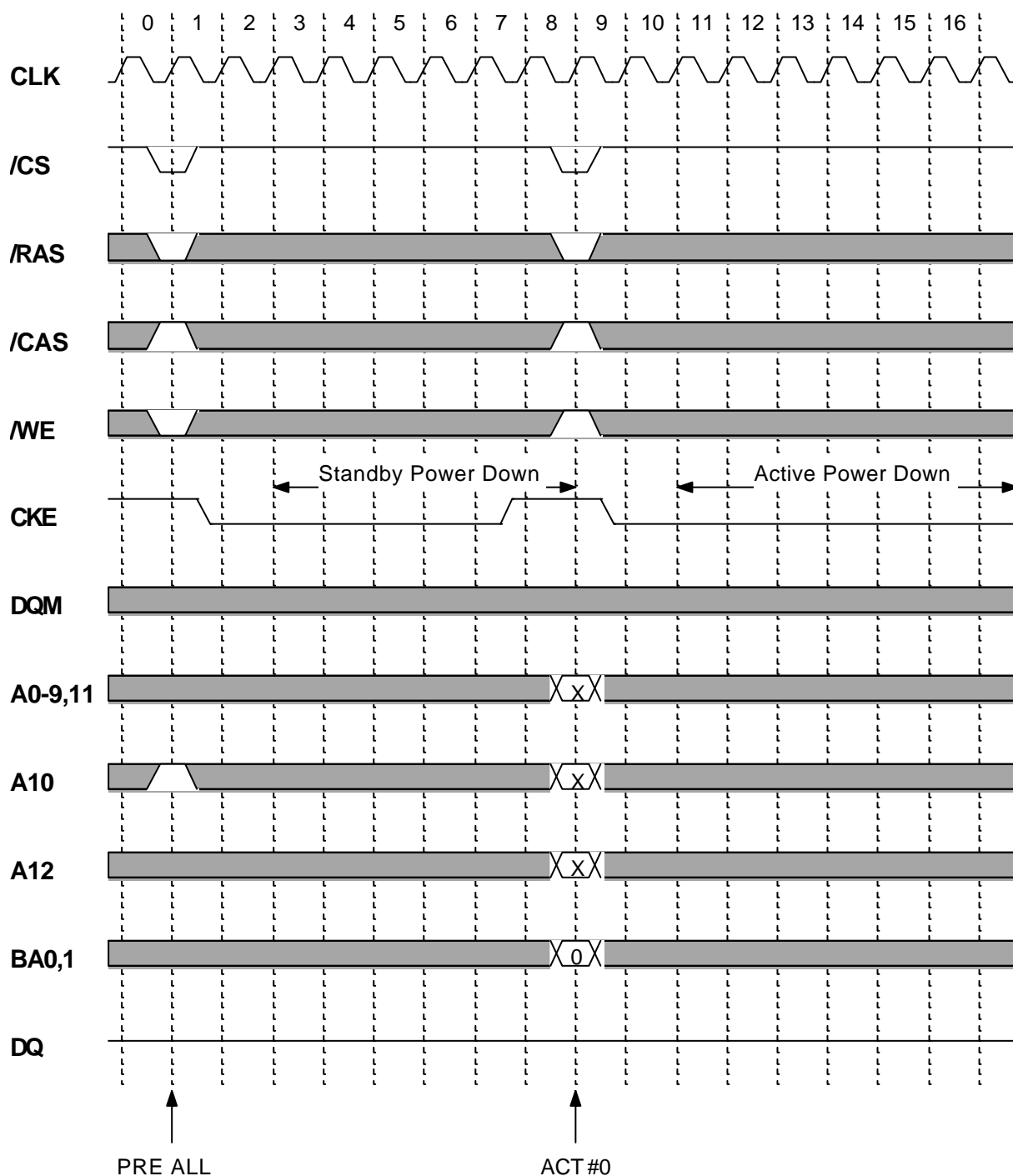
*Italic parameter* shows minimum case

**CLK Suspension [CL=2, BL=4]**



*Italic parameter* shows minimum case

**Power Down**



*Italic parameter* shows minimum case

SDRAM (Rev.1.1)

Single Data Rate

**M2V56S20/ 30/ 40 ATP -5, -5L, -6, -6L, -7, -7L**

Aug '01

256M Synchronous DRAM

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**Preliminary**

**MITSUBISHI LSIs**

**SDRAM (Rev.1.1)**

**Single Data Rate**

**M2V56S20/ 30/ 40 ATP -5, -5L, -6, -6L, -7, -7L**

**Aug '01**

**256M Synchronous DRAM**

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**Revision History**

Rev.	Date	Description
1.01	July / '01	1st edition
1.1	Aug./'01	-Add -5L/-6L/-7L spec. forM2V56S20ATP/30ATP/40ATP