

3819 Group

SINGLE-CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

The 3819 group is a 8-bit microcomputer based on the 740 family core technology.

The 3819 group has a fluorescent display automatic display circuit and an 16-channel 8-bit A-D converter as additional functions.

The various microcomputers in the 3819 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3819 group, refer to the section on group expansion.

FEATURES

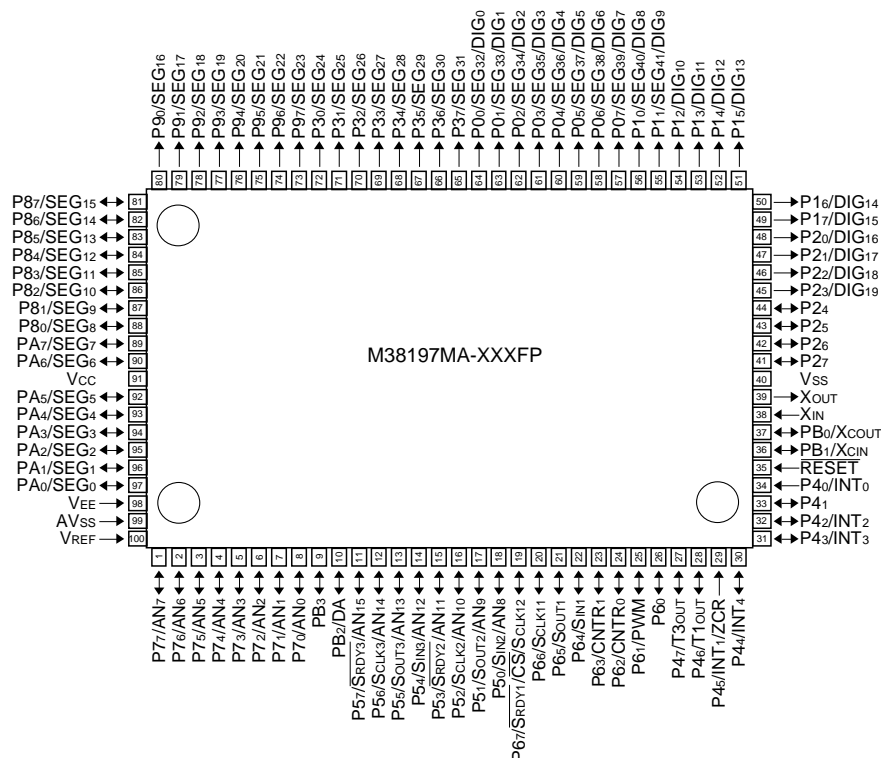
- Basic machine-language instructions 71
- The minimum instruction execution time 0.48 μ s
(at 8.4 MHz oscillation frequency)
- Memory size
ROM 4K to 60 K bytes
RAM 192 to 2048 bytes
- Programmable input/output ports 54
- High-breakdown-voltage output ports 52
- Interrupts 20 sources, 16 vectors
- Timers 8-bit X 6
- Serial I/O (Serial I/O1 has an automatic transfer function)
..... 8-bit X 3(clock-synchronized)
- PWM output circuit 8-bit X 1(also functions as timer 6)
- A-D converter 8-bit X 16 channels

- D-A converter 8-bit X 1 channels
- Zero cross detection input 1 channel
- Fluorescent display function
Segments 16 to 42
Digits 6 to 16
- 2 Clock generating circuit
Clock (XIN-XOUT) Internal feedback resistor
Sub-clock (XCIN-XCOUT) Without internal feedback resistor
(connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
In high-speed mode 4.0 to 5.5 V
(at 8.4 MHz oscillation frequency and high-speed selected)
In middle-speed mode 2.8 to 5.5 V
(at 8.4 MHz oscillation frequency)
In low-speed mode 2.8 to 5.5 V
(at 32 kHz oscillation frequency)
- Power dissipation
In high-speed mode 35 mW
(at 8.4 MHz oscillation frequency)
In low-speed mode 60 μ W
(at 3 V power source voltage and 32 kHz oscillation frequency)
- Operating temperature range -10 to 85°C

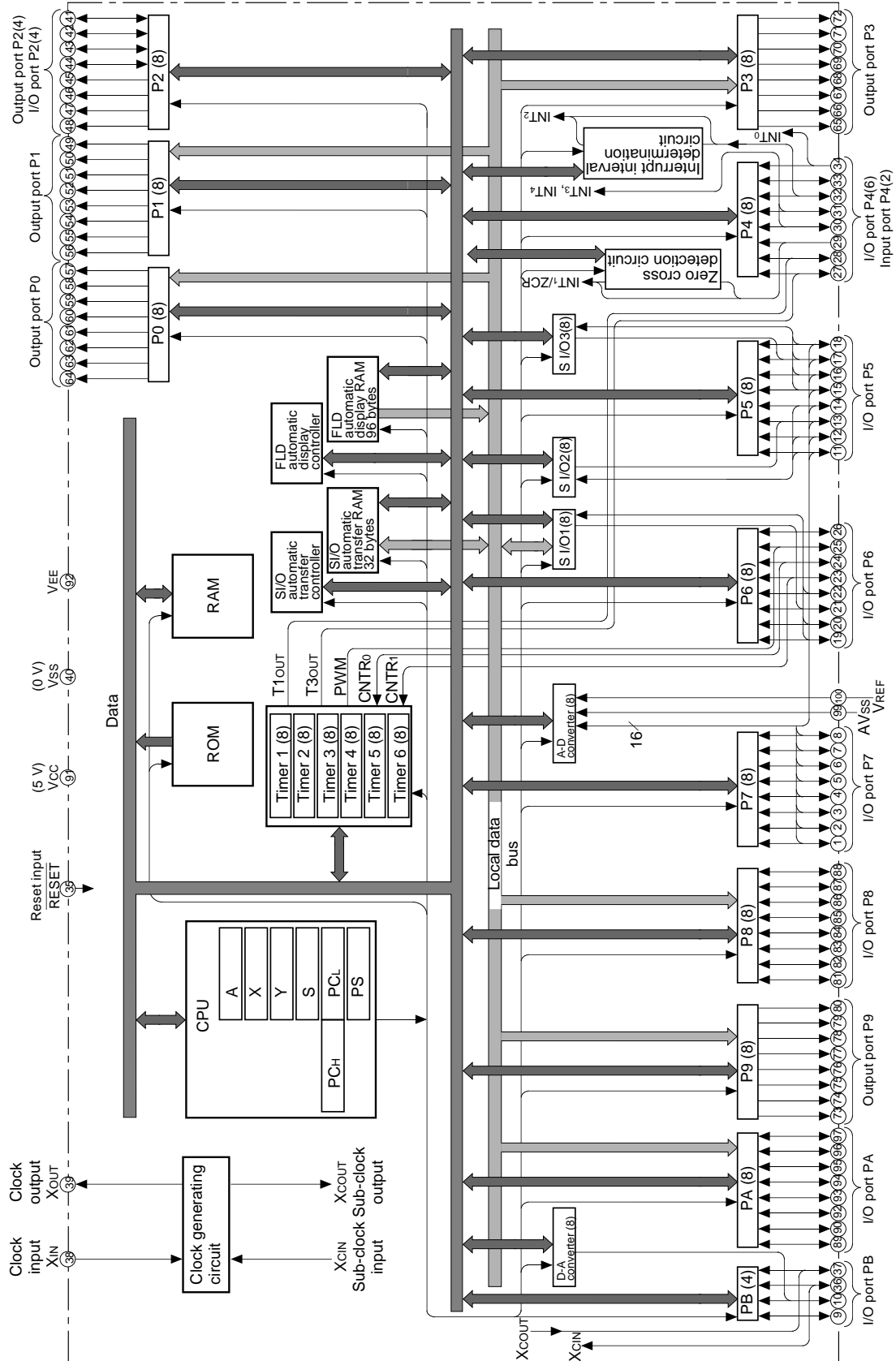
APPLICATION

Musical Instruments, household appliance, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 100P6S-A
100-pin plastic-molded QFP



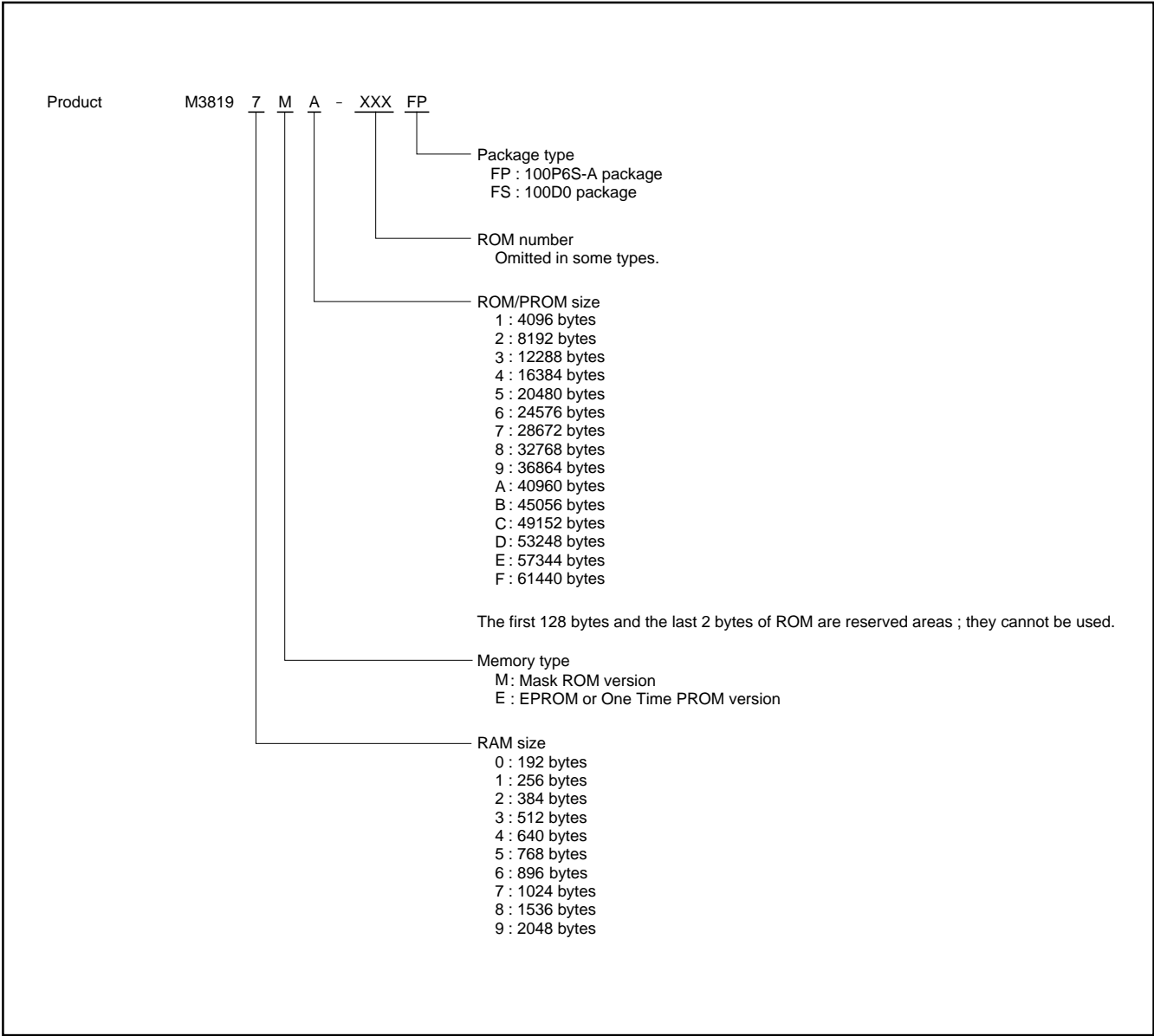
PIN DESCRIPTION

Pin	Name	Function	Function except a port function
VCC, VSS	Power source	•Apply voltage of 4.0 to 5.5 V to Vcc, and 0 V to VSS.	
VEE	Pull-down Power source	•Applies voltage supplied to pull-down resistors of ports P0, P1, P20–P23, P3, and P9.	
VREF	Analog reference voltage	•Reference voltage input pin for A-D converter and D-A converter	
AVSS	Analog power source	•GND input pin for A-D converter and D-A converter •Connect AVSS to Vss.	
RESET	Reset input	•Reset input pin for active “L”	
XIN	Clock input	•Input and output pins for the main clock generating circuit •Feedback resistor is built in between XIN pin and XOUT pin. •Connect a ceramic resonator or a quartz-crystal oscillator between the XIN pin and XOUT pin to set oscillation frequency. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. •This clock is used as the oscillating source of system clock.	
XOUT	Clock output		
P00/SEG32/ DIG0–P07/ SEG39/DIG7	Output port P0	•8-bit output port •This port builds in pull-down resistor between port P0 and the VEE pin. •At reset this port is set to VEE level. •The high-breakdown-voltage P-channel open-drain	FLD automatic display pins
P10/SEG40/ DIG8–P17/ DIG15	Output port P1	•8-bit output port with the same function as port P0	FLD automatic display pins
P20/DIG16– P23/DIG19	Output port P2	•4-bit output port with the same function as port P0	FLD automatic display pins
P24–P27	I/O port P2	•4-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •At reset this port is set to input mode. •TTL input level •CMOS 3-state output	
P30/SEG24– P37/SEG31	Output port P3	•8-bit output port with the same function as port P0	FLD automatic display pins
P40/INT0, P45/INT1/ ZCR	Input port P4	•2-bit input port •CMOS compatible input level	External interrupt input pins A zero cross detection circuit input pin (P45)
P42/INT2– P44/INT4	I/O port P4	•6-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level	
P41			
P46/T1OUT, P47/T3OUT			•CMOS 3-state output

PIN DESCRIPTION (Continued)

Pin	Name	Function	Function except a port function
P50/SIN2/AN8, P51/SOUT2/AN9, P52/SCLK2/AN10, P53/SRDY2/AN11	I/O port P5	<ul style="list-style-type: none"> •8-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level •CMOS 3-state output 	Serial I/O2 function pins A-D conversion input pins
P54/SIN3/AN12, P55/SOUT3/AN13, P56/SCLK3/AN14, P57/SRDY3/AN15			Serial I/O3 function pins A-D conversion input pins
P60	I/O port P6	<ul style="list-style-type: none"> •8-bit CMOS I/O port with the same function as ports P24–P47 •CMOS compatible input level •CMOS 3-state output 	
P61/PWM			PWM output pin (Timer output pin)
P62/CNTR0, P63/CNTR1			Timer input pins
P64/SIN1, P65/SOUT1, P66/SCLK11, P67/SRDY1/CS/ SCLK12			Serial I/O1 function pins
P70/AN0– P77/AN7	I/O port P7	<ul style="list-style-type: none"> •8-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level •CMOS 3-state output 	A-D conversion input pins
P80/SEG8– P87/SEG15	I/O port P8	<ul style="list-style-type: none"> •8-bit I/O port with the same function as ports P24–P27 •CMOS compatible input level •The high-breakdown-voltage P-channel open-drain 	FLD automatic display pins
P90/SEG16– P97/SEG23	Output port P9	•8-bit output port with the same function as port P0	
PA0/SEG0– PA7/SEG7	I/O port PA	<ul style="list-style-type: none"> •8-bit I/O port with the same function as ports P24–P27 •CMOS compatible input level •The high-breakdown voltage P-channel open-drain 	
PB0/XCOUT, PB1/XCIN	I/O port PB	<ul style="list-style-type: none"> •4-bit CMOS I/O port with the same function as ports P24–P27 •CMOS compatible input level •CMOS 3-state output 	I/O pins for sub-clock generating circuit (connect a ceramic resonator or a quartz-crystal oscillator)
PB2/DA			D-A conversion output pin
PB3			

PART NUMBERING



GROUP EXPANSION

Mitsubishi plans to expand the 3819 group as follows:

(1) Support for mask ROM, One Time PROM, and EPROM versions

ROM/PROM capacity 40 K to 60 K bytes

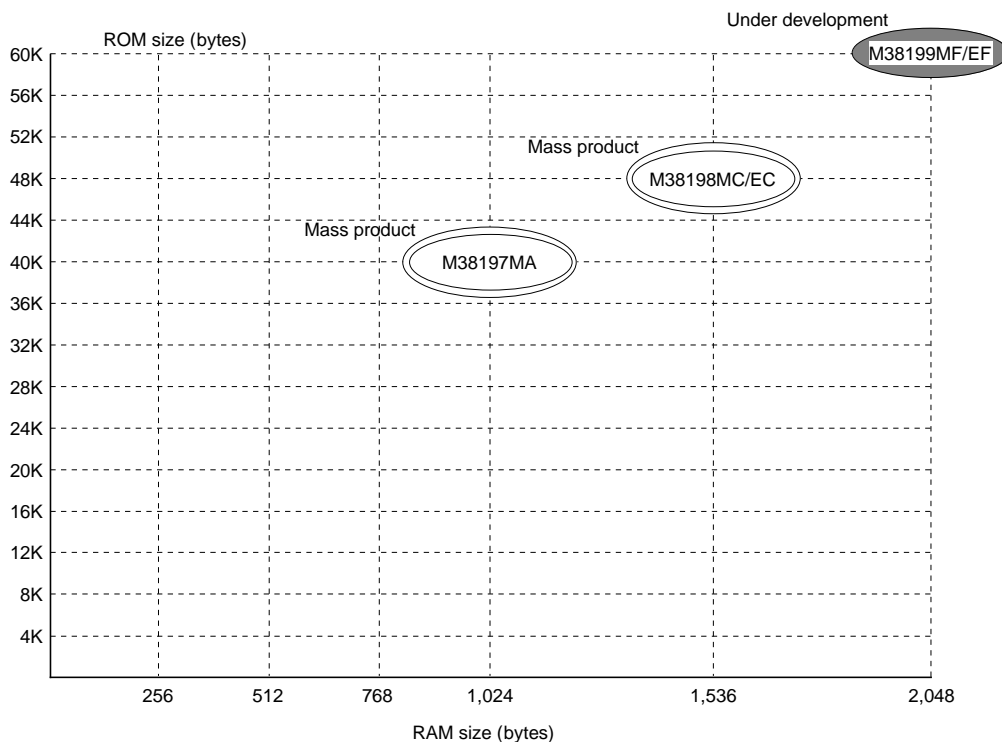
RAM capacity 1024 to 2048 bytes

(2) Packages

100P6S-A 0.65 mm-pitch plastic molded QFP

100D0 Ceramic LCC(built-in EPROM version)

Memory Expansion Plan



Products under development : the development schedule and specifications may be revised without notice.

Currently supported products are listed below.

As of May 1996

Product	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38197MA-XXXFP	40960 (40830)	1024	100P6S-A	Mask ROM version
M38197MA-XXXKP			100P6P-E	Mask ROM version
M38198MC-XXXKP				Mask ROM version
M38199MF-XXXKP				Mask ROM version
M38198MC-XXXFP	49152 (49022)	1536	100P6S-A	Mask ROM version
M38198EC-XXXFP				One Time PROM version
M38198ECFP				One Time PROM version (blank)
M38198ECFS			100D0	EPROM version
M38199MF-XXXFP	61440 (61310)	2048	100P6S-A	Mask ROM version
M38199EF-XXXFP				One Time PROM version
M38199EFP				One Time PROM version (blank)
M38199EFP			100D0	EPROM version

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 3819 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address 003B₁₆. The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

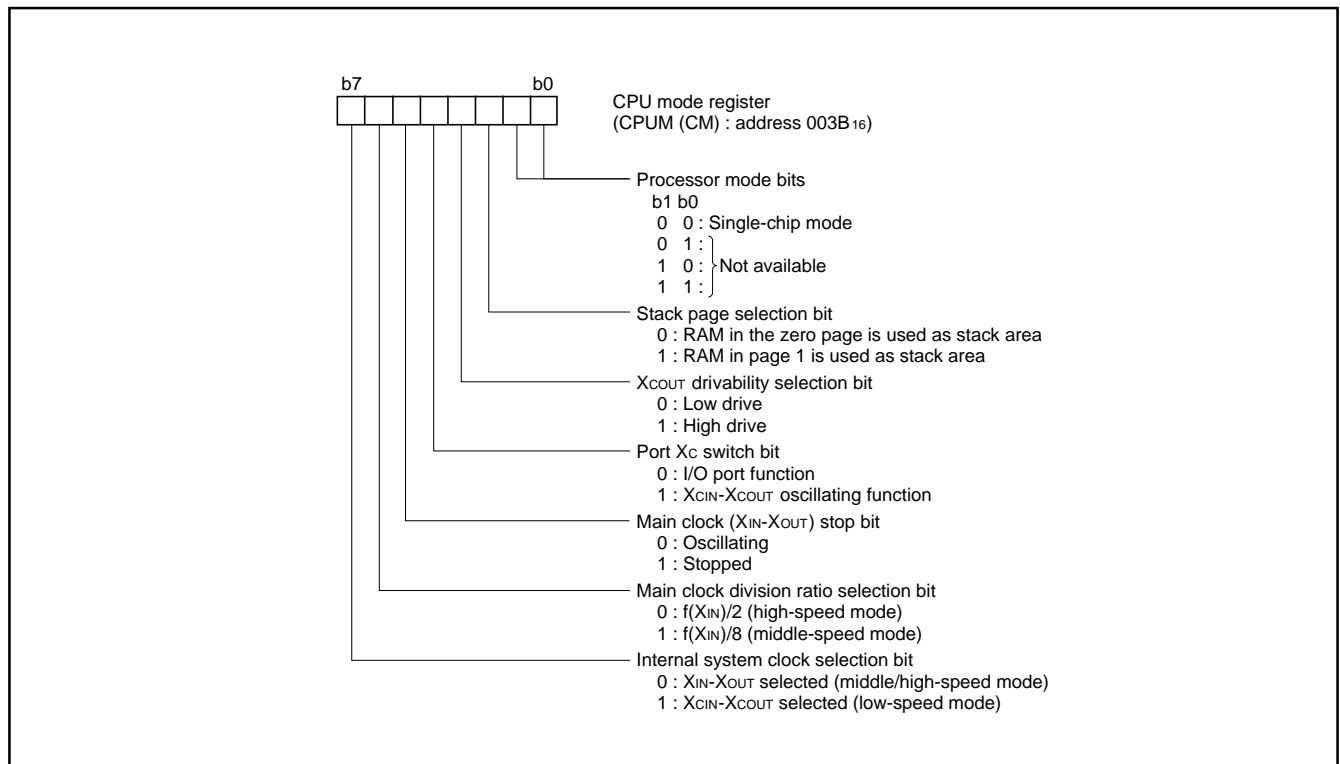


Fig. BA-1 Structure of CPU mode register

Memory

Special function register (SFR) area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the reset is user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM capacity (bytes)	Address XXXX ₁₆
192	00FF ₁₆
256	013F ₁₆
384	01BF ₁₆
512	023F ₁₆
640	02BF ₁₆
768	033F ₁₆
896	03BF ₁₆
1024	043F ₁₆
1536	063F ₁₆
2048	083F ₁₆

ROM area

ROM capacity (bytes)	Address YYYY ₁₆	Address ZZZZ ₁₆
4096	F000 ₁₆	F080 ₁₆
8192	E000 ₁₆	E080 ₁₆
12288	D000 ₁₆	D080 ₁₆
16384	C000 ₁₆	C080 ₁₆
20480	B000 ₁₆	B080 ₁₆
24576	A000 ₁₆	A080 ₁₆
28672	9000 ₁₆	9080 ₁₆
32768	8000 ₁₆	8080 ₁₆
36864	7000 ₁₆	7080 ₁₆
40960	6000 ₁₆	6080 ₁₆
45056	5000 ₁₆	5080 ₁₆
49152	4000 ₁₆	4080 ₁₆
53248	3000 ₁₆	3080 ₁₆
57344	2000 ₁₆	2080 ₁₆
61440	1000 ₁₆	1080 ₁₆

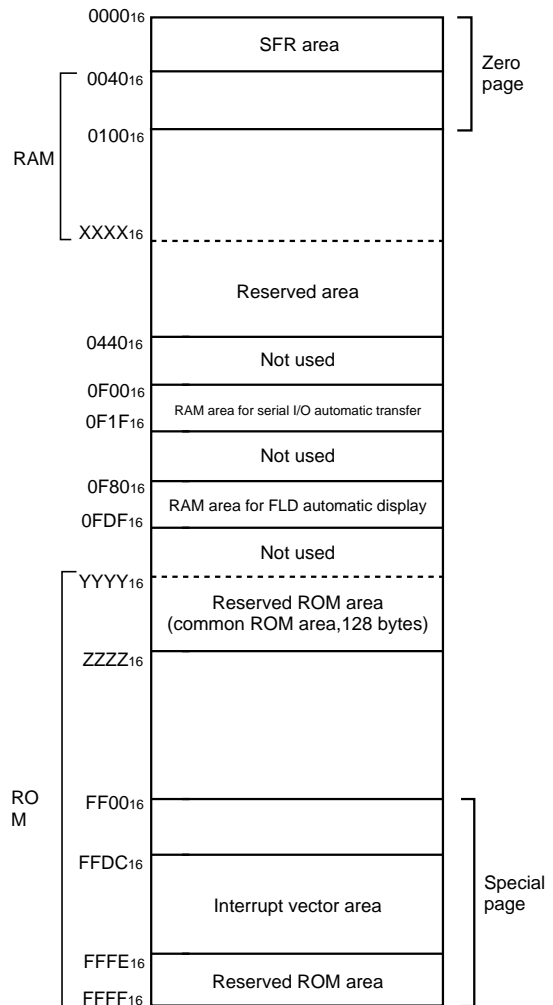


Fig. CA-1 Memory map

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer 1 (T1)
0001 ₁₆		0021 ₁₆	Timer 2 (T2)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 3 (T3)
0003 ₁₆		0023 ₁₆	Timer 4 (T4)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 5 (T5)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 6 (T6)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Serial I/O3 register (SIO3)
0007 ₁₆		0027 ₁₆	Timer 6 PWM register (T6PWM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer 12 mode register (T12M)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 34 mode register (T34M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Timer 56 mode register (T56M)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	D-A conversion register (DA)
000C ₁₆	Port P6 (P6)	002C ₁₆	AD-DA control register (ADCON)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	A-D conversion register (AD)
000E ₁₆	Port P7 (P7)	002E ₁₆	
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	
0010 ₁₆	Port P8 (P8)	0030 ₁₆	Interrupt interval determination register (IID)
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	Interrupt interval determination control register (IIDCON)
0012 ₁₆	Port P9 (P9)	0032 ₁₆	Port P0 segment/digit switch register (P0SDR)
0013 ₁₆		0033 ₁₆	Port P2 digit/port switch register (P2DPR)
0014 ₁₆	Port PA (PA)	0034 ₁₆	Port P8 segment/port switch register (P8SPR)
0015 ₁₆	Port PA direction register (PAD)	0035 ₁₆	Port PA segment/port switch register (PASPR)
0016 ₁₆	Port PB (PB)	0036 ₁₆	FLDC mode register 1 (FLDM1)
0017 ₁₆	Port PB direction register (PBD)	0037 ₁₆	FLDC mode register 2 (FLDM2)
0018 ₁₆	Serial I/O automatic transfer data pointer (SIODP)	0038 ₁₆	FLD data pointer (FLDDP)
0019 ₁₆	Serial I/O1 control register (SIO1CON)	0039 ₁₆	Zero cross detection control register (ZCRCON)
001A ₁₆	Serial I/O automatic transfer control register (SIOAC)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	Serial I/O1 register (SIO1)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Serial I/O automatic transfer interval register (SIOAI)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Serial I/O2 control register (SIO2CON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆	Serial I/O3 control register (SIO3CON)	003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Serial I/O2 register (SIO2)	003F ₁₆	Interrupt control register 2 (ICON2)

Fig. CA-2 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The 3819 group has 54 programmable I/O pins arranged in 8 I/O ports (ports P24–P27, P41–P44, P46, P47, P5–P8, PA, and PB). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set for output, the value of the port latch is read, not the value of the pin itself. A pin which is set for input the value of the pin itself is read because the pin is in floating state. If a pin set for input is written to, only the port latch is written to and the pin remains floating.

High-Breakdown-Voltage Output Ports

The 3819 group microprocessors have 7 ports with high-breakdown-voltage pins (ports P0, P1, P20–P23, P3, P8, P9, PA). The high-breakdown-voltage ports have P-channel open-drain output with V_{CC} –40 V of breakdown voltage.

Each pin in ports P0, P1, P20–P23, P3, and P9 has an internal pull-down resistor connected to V_{EE}. Ports P8 and PA have no internal pull-down resistors, so that connect an external resistor to each port. At reset, the P-channel output transistor of each port latch is turned off, so it becomes V_{EE} level (“L”) by the pull-down resistor.

Writing “1” (weak drivability) to bit 7 of the FLDC mode register 1 (address 003616) shows the rising transition of the output transistors for reducing transient noise. At reset, bit 7 of the FLDC mode register 1 is set to “0” (strong drivability).

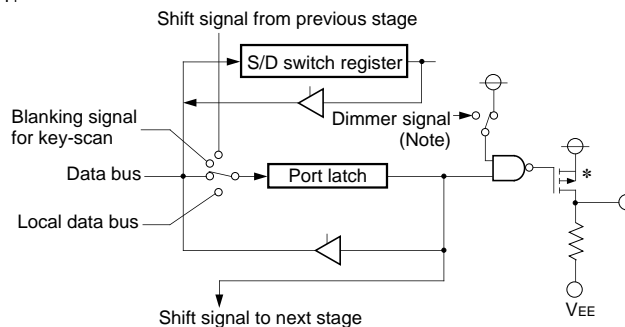
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P00/SEG32/ DIG0– P07/SEG39/ DIG7	Port P0	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2 Port P0 segment/digit switch register	(1)
P10/SEG40/ DIG8– P17/DIG15	Port P1	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2	(1) (2)
P20/DIG16– P23/DIG19	Port P2	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2 Port P2 digit/port switch register	(3)
P24–P27		Input/output, individual bits	TTL level input CMOS 3-state output			(4)
P30/SEG24– P37/SEG31	Port P3	Output	High-breakdown-voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register 1 FLDC mode register 2	(5)
P40/INT0 P45/INT1/ ZCR	Port P4	Input	CMOS compatible input level	External interrupt input Zero cross detection circuit input (P45)	Interrupt edge selection register Zero cross detection control register	(6)
P42/INT2– P44/INT4		Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(7)
P41						(4)
P46/T1OUT, P47/T3OUT				Timer output	Timer 12 mode register Timer 34 mode register	(8)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

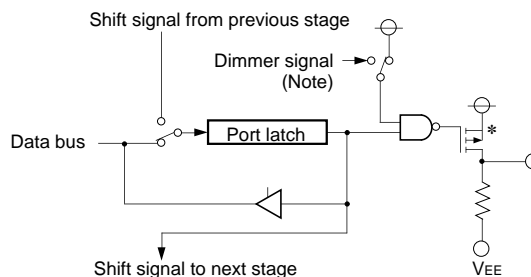
Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P50/SIN2/ AN8	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 func- tion I/O A-D conversion in- put	Serial I/O2 control register AD/DA control regis- ter	(9)
P51/SOUT2/ AN9, P52/SCLK2/ AN10						(10)
P53/SRDY2/ AN11						(11)
P54/SIN3/ AN12				Serial I/O3 func- tion I/O A-D conversion in- put	Serial I/O3 control register AD/DA control regis- ter	(9)
P55/SOUT3/ AN13, P56/SCLK3/ AN14						(10)
P57/SRDY3/ AN15						(11)
P60	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(4)
P61/PWM				PWM (timer) out- put	Timer 56 mode regis- ter	(8)
P62/CNTR0, P63/CNTR1				Timer input	Interrupt edge selec- tion register	(7)
P64/SIN1				Serial I/O1 func- tion I/O	Serial I/O1 control register Serial I/O automatic transfer control regis- ter	(9)
P65/SOUT1, P66/SCLK11						(10)
P67/SRDY1/ CS/SCLK12						(11)
P70/AN0– P77/AN7	Port P7		CMOS compatible input level CMOS 3-state output	A-D conversion in- put	AD/DA control regis- ter	(12)
P80/SEG8– P87/SEG15	Port P8		CMOS compatible input level High-breakdown- voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register Segment/port switch register	(13)
P90/SEG16– P97/SEG23	Port P9	Output	High-breakdown- voltage P-channel open-drain output with pull-down resistor		FLDC mode register	(5)
PA0/SEG0– PA7/SEG7	Port PA	Input/output, individual bits	CMOS compatible input level High-breakdown- voltage P-channel open-drain output		FLDC mode register Segment/port switch register	(13)
PB0/XCOUT, PB1/XCIN	Port PB	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	I/O for sub-clock generating circuit	CPU mode register	(14) (15)
PB2/DA				D-A conversion output	AD/DA control regis- ter	(16)
PB3						(4)

Note : Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

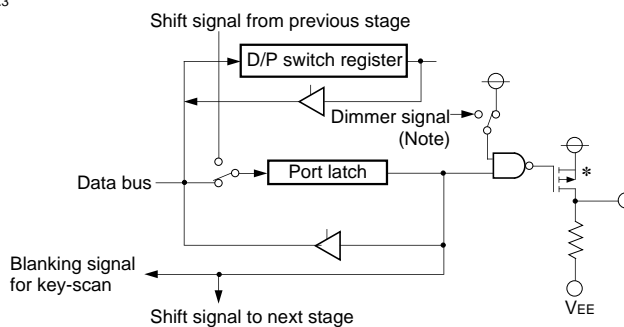
(1) Ports P0, P10, P11



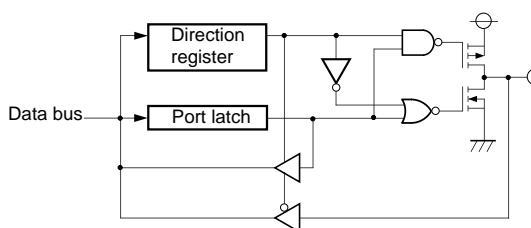
(2) Ports P12–P17



(3) Ports P20–P23



(4) Ports P24–P27, P41, P60, PB3

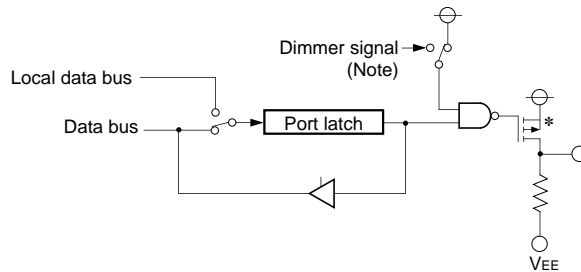


* : High-breakdown-voltage P-channel transistor

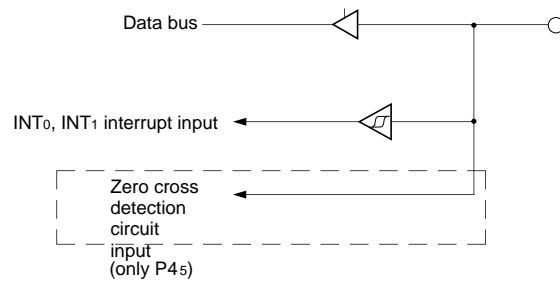
Note: The dimmer signal sets the Toff timing.

Fig. UA-2 Port block diagram (1)

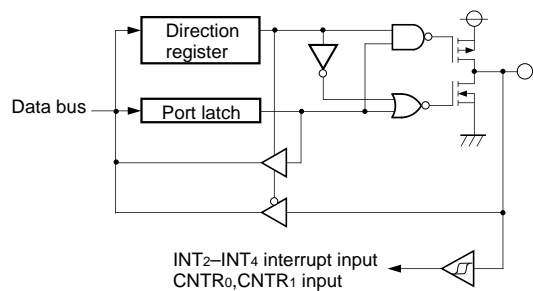
(5) Ports P3, P9



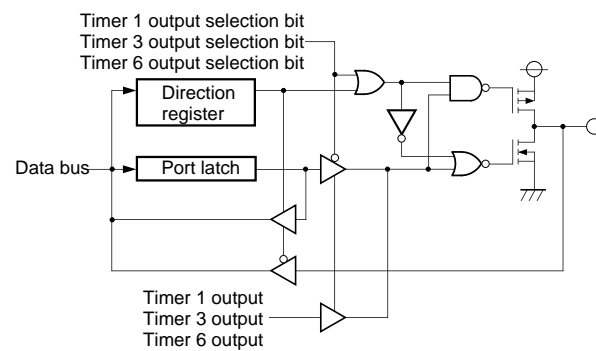
(6) Ports P40, P45



(7) Ports P42-P44, P62, P63



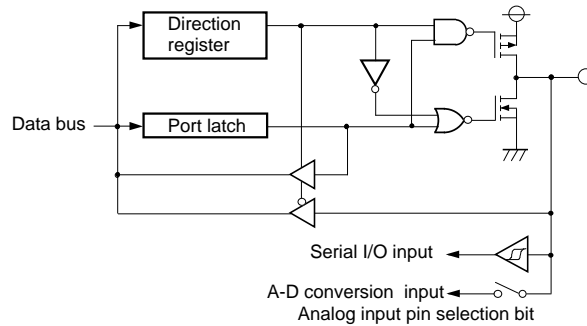
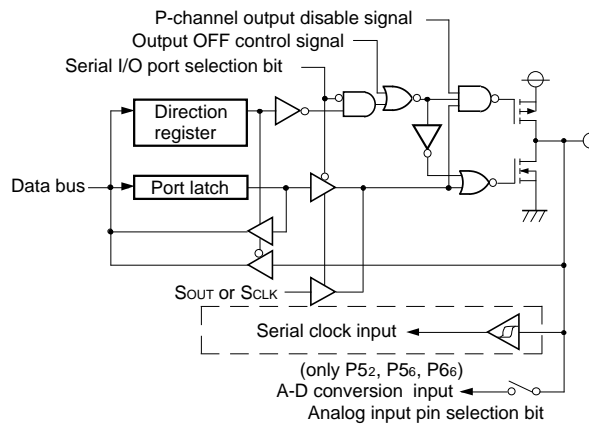
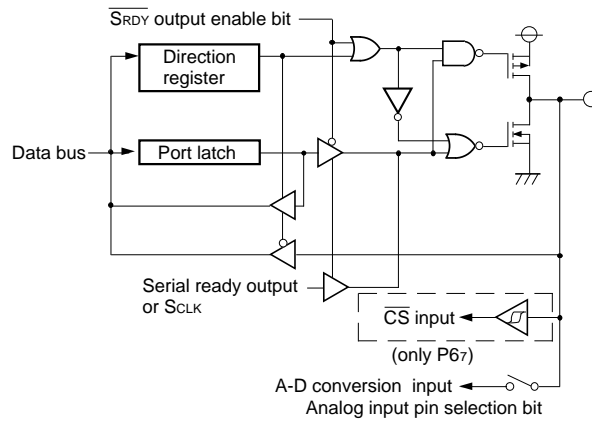
(8) Ports P46, P47, P61



* : High-breakdown-voltage P-channel transistor

Note: The dimmer signal sets the Toff timing.

Fig. UA-3 Port block diagram (2)

(9) Ports P5₀, P5₄, P6₄(10) Ports P5₁, P5₂, P5₅, P5₆, P6₅, P6₆(11) Ports P5₃, P5₇, P6₇

(12) Port P7

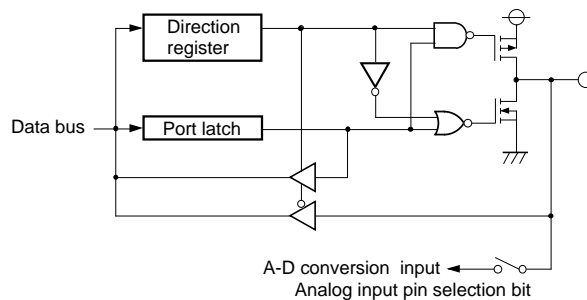
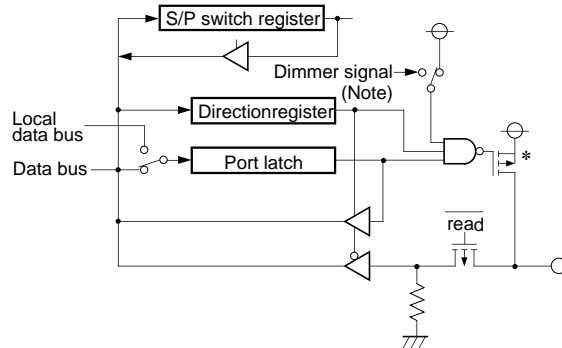
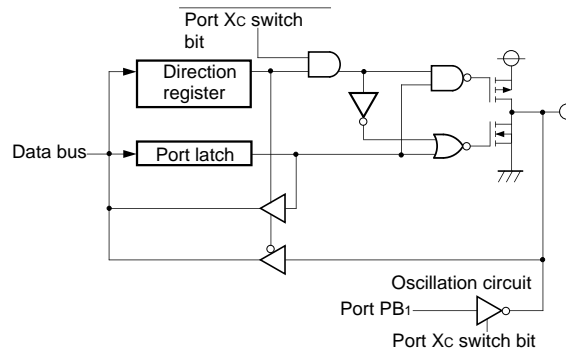


Fig. UA-4 Port block diagram (3)

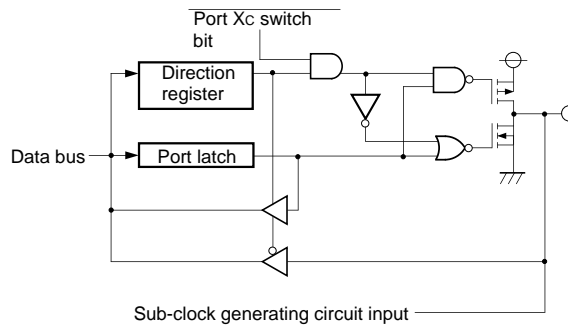
(13) Ports P8, PA



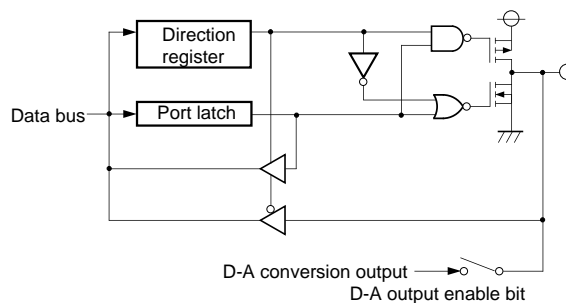
(14) Port PB₀



(15) Port PB₁



(16) Port PB₂



* : High-breakdown-voltage P-channel transistor

Note: The dimmer signal sets the Toff timing.

Fig. UA-5 Port block diagram (4)

INTERRUPTS

Interrupts occur by 20 sources: 5 external, 14 internal, and 1 software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit.

The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

Interrupt Operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

Notes on Use

When the active edge of an external interrupt (INT0 to INT4) is changed or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge.
- (3) Clear the interrupt request bit which is selected to "0".
- (4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT0	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1/ZCR	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT1/ZCR input	External interrupt (active edge selectable)
INT2	4	FFF7 ₁₆	FFF6 ₁₆	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
Remote control/counter overflow				At 8-bit counter overflow	Valid when interrupt interval determination is operating
Serial I/O1	5	FFF5 ₁₆	FFF4 ₁₆	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O automatic transfer				At completion of the last data transfer	Valid when serial I/O automatic transfer mode is selected
Serial I/O2	6	FFF3 ₁₆	FFF2 ₁₆	At completion of data transfer	Valid when serial I/O2 is selected
Serial I/O3	7	FFF1 ₁₆	FFF0 ₁₆	At completion of data transfer	Valid when serial I/O3 is selected
Timer 1	8	FFEF ₁₆	FFEE ₁₆	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED ₁₆	FFEC ₁₆	At timer 2 underflow	
Timer 3	10	FFEB ₁₆	FFEA ₁₆	At timer 3 underflow	
Timer 4	11	FFE9 ₁₆	FFE8 ₁₆	At timer 4 underflow	
Timer 5	12	FFE7 ₁₆	FFE6 ₁₆	At timer 5 underflow	
Timer 6	13	FFE5 ₁₆	FFE4 ₁₆	At timer 6 underflow	
INT3	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
INT4	15	FFE1 ₁₆	FFE0 ₁₆	At detection of either rising or falling edge of INT4 input	Valid when INT4 interrupt is selected External interrupt (active edge selectable)
A-D conversion				At completion of A-D conversion	Valid when A-D conversion interrupt is selected
FLD blanking	16	FFDF ₁₆	FFDE ₁₆	At falling edge of the last digit immediately before blanking period starts	Valid when FLD blanking interrupt is selected
FLD digit				At rising edge of each digit	Valid when FLD digit interrupt is selected
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.

2 : Reset function in the same way as an interrupt with the highest priority.

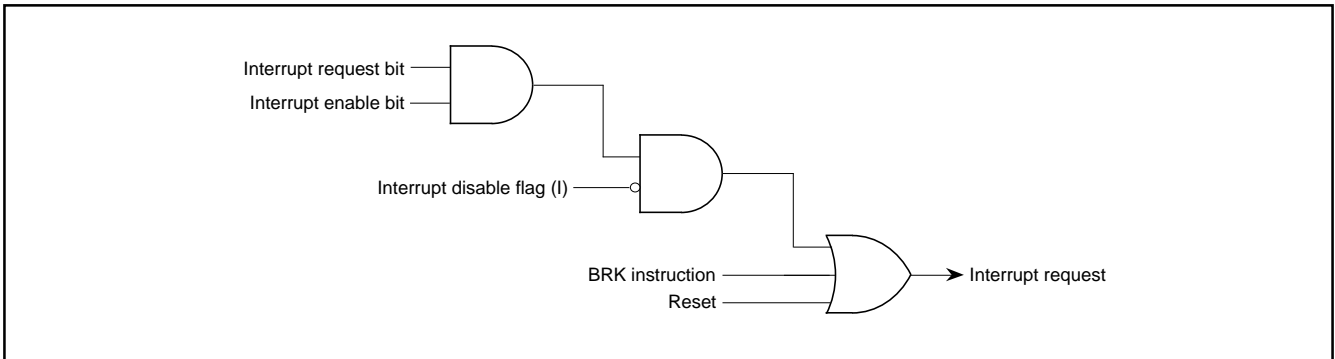


Fig. DD-1 Interrupt control

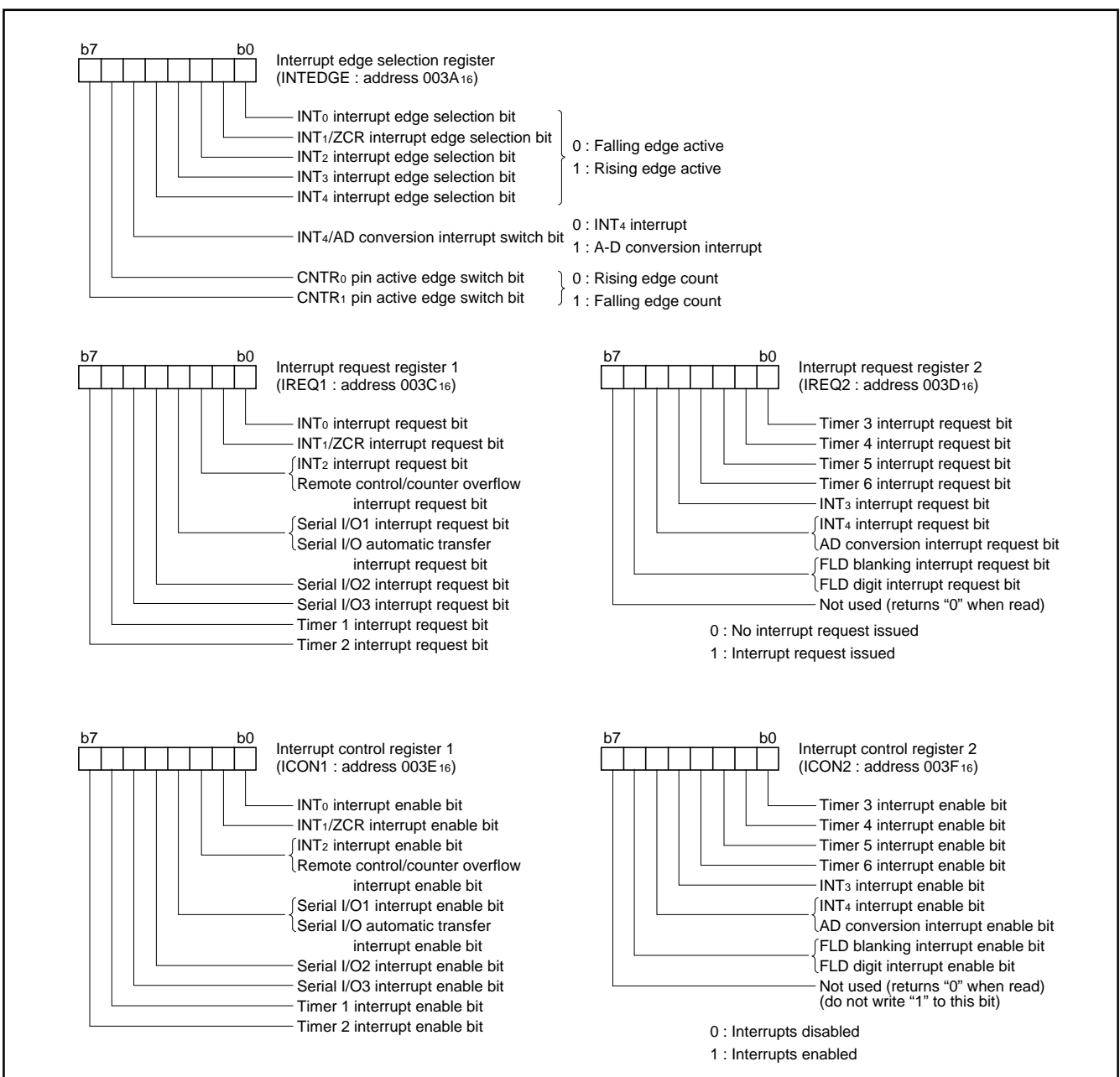


Fig. DD-2 Structure of interrupt-related registers

TIMERS

The 3819 group has 6 built-in timers: timer 1, timer 2, timer 3, timer 4, timer 5, and timer 6.

Each timer has the 8-bit timer latch. The timers count down.

Once a timer reaches 00₁₆, at the next count pulse the contents of each timer latch is loaded into the corresponding timer, and sets the corresponding interrupt request bit to "1".

The count can be stopped by setting the stop bit of each timer to "1". The internal clock ϕ can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, timer internal count source is switched to either $f(XIN)$ or $f(XCIN)$.

Timer 1 and Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 is output from the P46/T1OUT pin. The waveform polarity changes each time timer 1 overflows. The active edge of the external clock CNTR₀ can be switched with the bit 6 of the interrupt edge selection register.

At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0", timer 1 is set to "FF₁₆", and timer 2 is set to "01₁₆".

Timer 3 and Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 is output from the P47/T3OUT pin. The waveform polarity changes each time timer 3 overflows.

The active edge of the external clock CNTR₁ can be switched with the bit 7 of the interrupt edge selection register.

Timer 5 and Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register.

A rectangular waveform of timer 6 underflow signal divided by 2 is output from the P61/PWM pin. The waveform polarity changes each time timer 6 overflows.

Timer 6 PWM Mode

Timer 6 can output a rectangular waveform with duty cycle $n/(n + m)$ from the P61/PWM pin by setting the timer 56 mode register (refer to fig. FB-3). The n is the value set in timer 6 latch (address 0025₁₆) and m is the value in the timer 6 PWM register (address 0027₁₆). If n is "0", the PWM output is "L", if m is "0", the PWM output is "H" ($n=0$ is prior than $m=0$). In the PWM mode, interrupts occur at the rising edge of the PWM output.

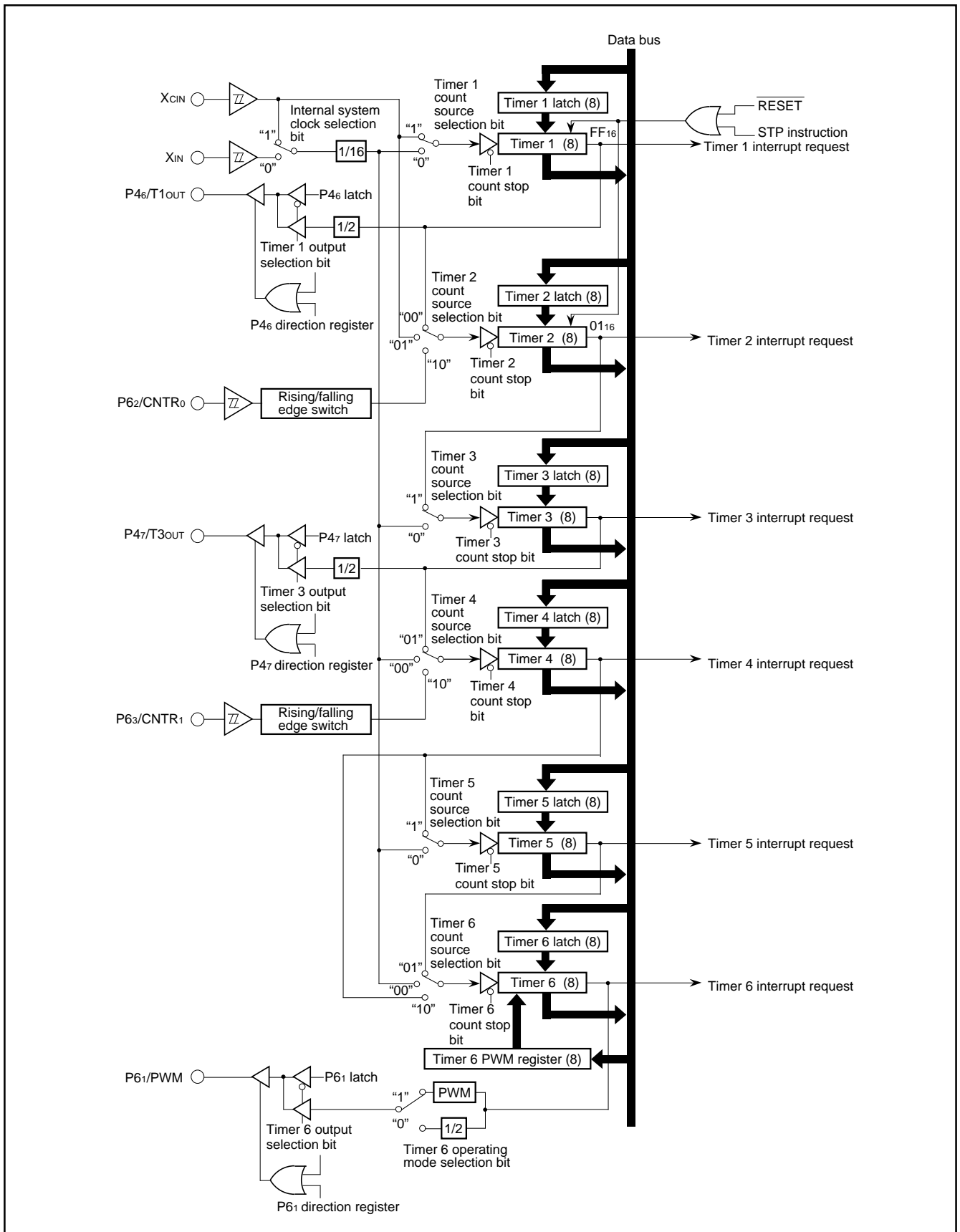


Fig. FB-1 Timer block diagram

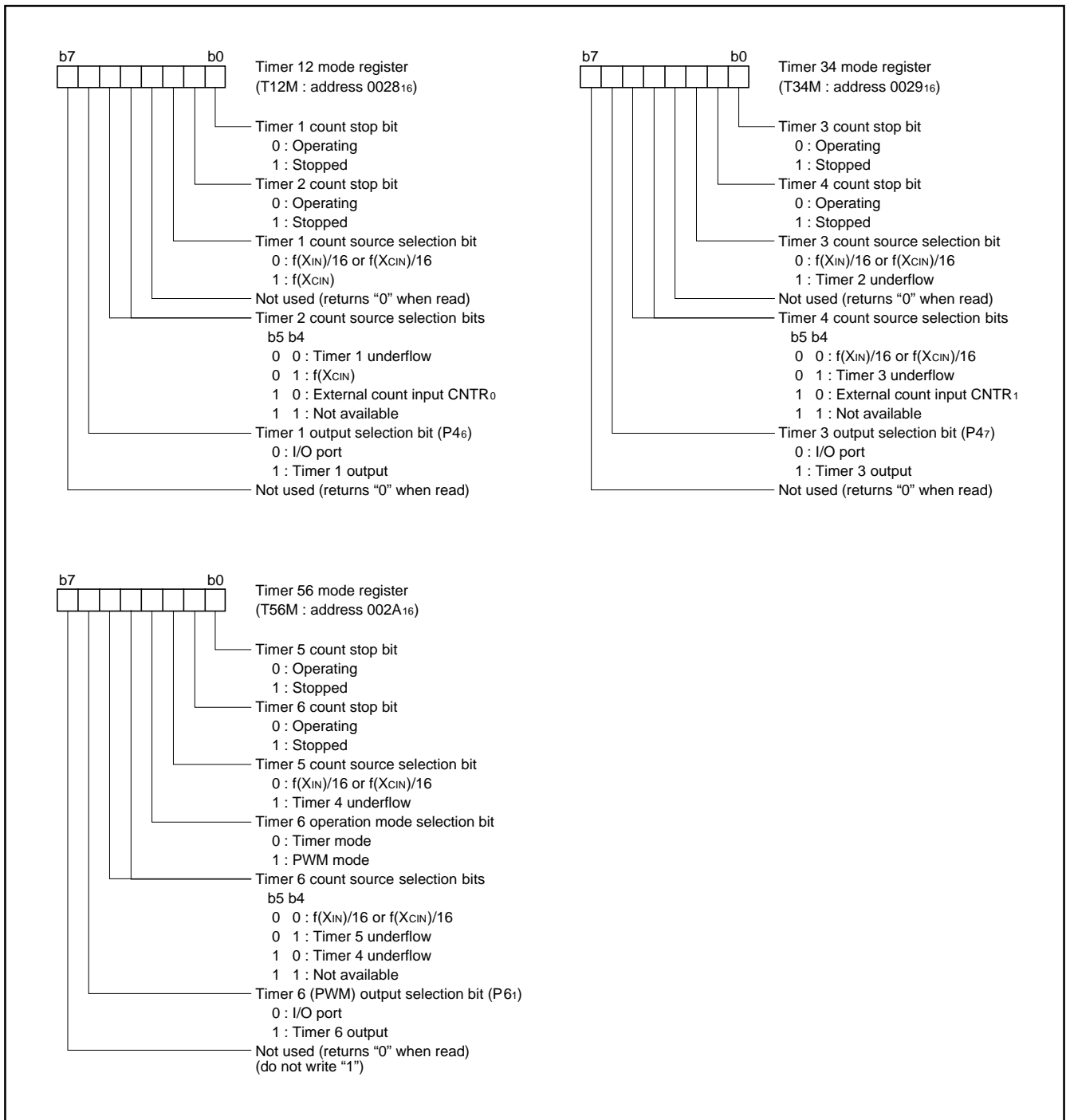


Fig. FB-2 Structure of timer-related registers

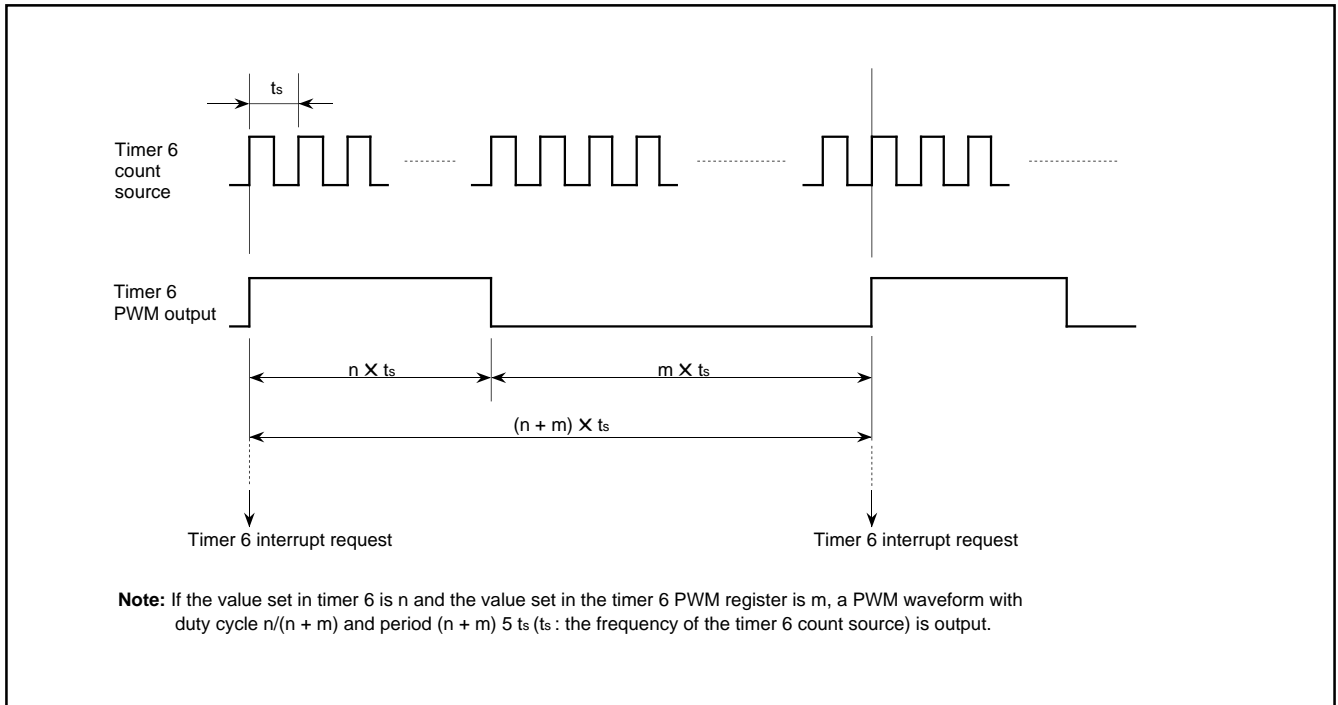


Fig. FB-3 Timing in timer 6 PWM mode

SERIAL I/O

The 3819 group has built-in 8-bit clock synchronized serial I/O × 3 channels (serial I/O1, serial I/O2, and serial I/O3).

Serial I/O1 builds in the automatic transfer function. The function can be switched to the serial I/O ordinary mode with the serial I/O automatic transfer control register (address 001A₁₆).

Serial I/O2 and Serial I/O3 can be used only in the serial I/O ordinary mode.

The I/O pins of the serial I/O function are also used as I/O ports P5 and P64–P67, and their operation is selected with the serial I/O control registers (addresses 0019₁₆, 001D₁₆, and 001E₁₆).

Serial I/O Control Registers (SIO1CON, SIO2CON, SIO3CON) 0019₁₆, 001D₁₆, 001E₁₆

Each of the serial I/O control registers (addresses 0019₁₆, 001D₁₆, and 001E₁₆) consists of 8 selection bits which control the serial I/O function.

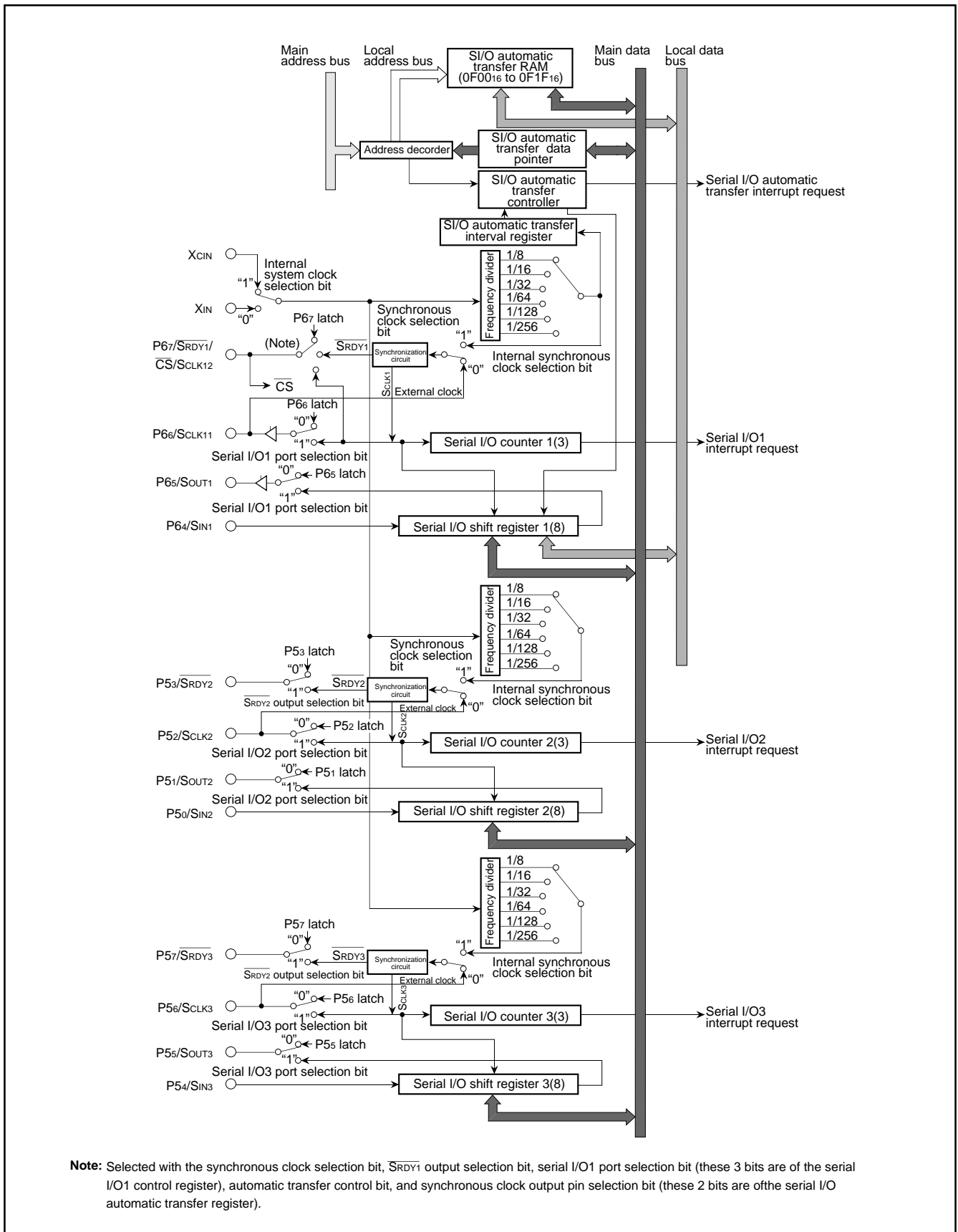


Fig. GA-1 Serial I/O block diagram

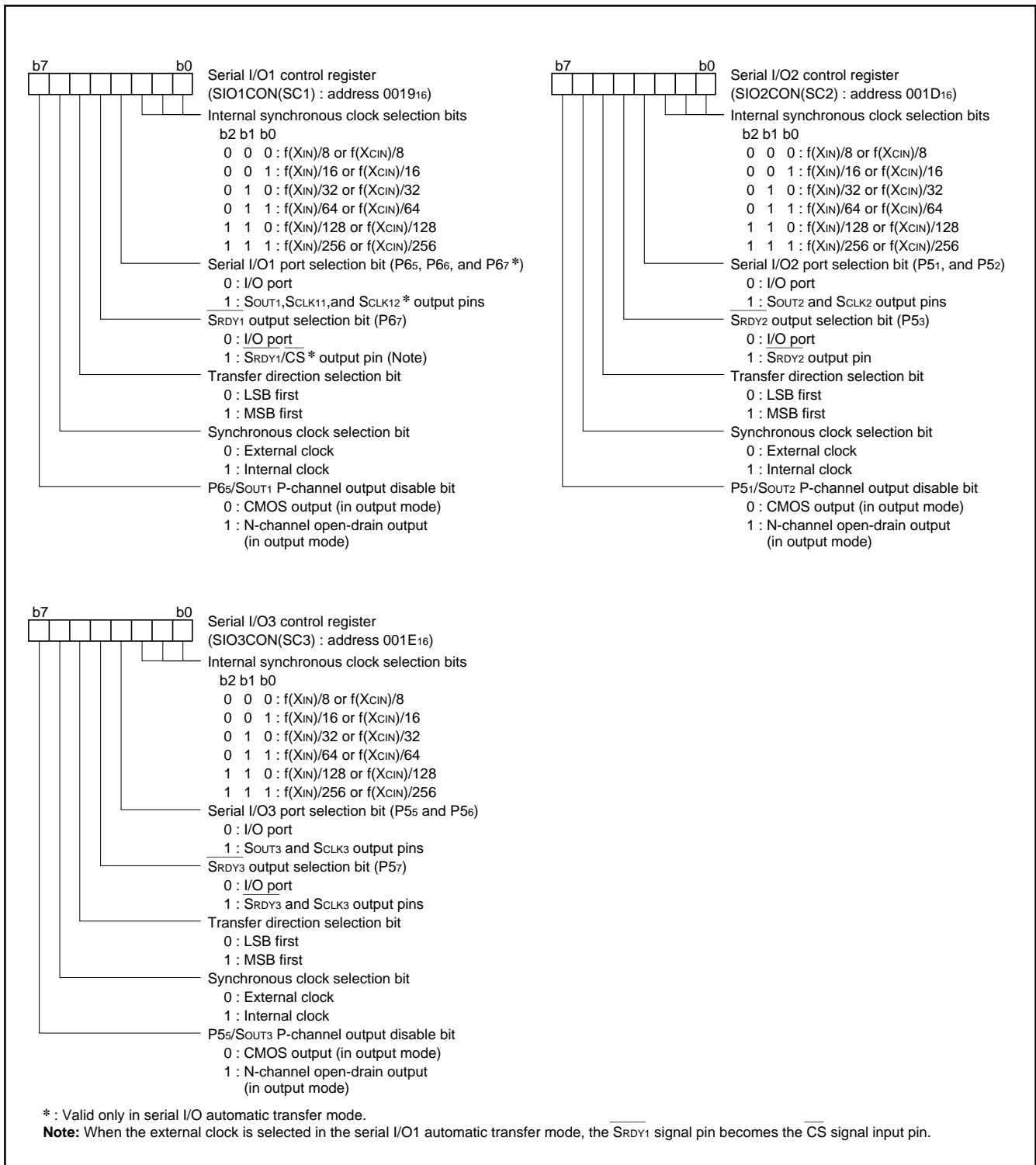


Fig. GA-2 Structure of serial I/O control registers

(1) Serial I/O Ordinary Mode

Either an internal clock or an external clock can be selected as the synchronous clock for serial I/O transfer. A dedicated divider is built in as the internal clock for selecting of 6 clocks. If internal clock is selected, transfer starts with a write signal to a serial I/O register (addresses 001B₁₆, 001F₁₆, or 0026₁₆). After 8 bits have been transferred, the SOUT pin goes to high impedance state.

If external clock is selected, control the clock externally because the contents of the serial I/O register continue to shift during inputting the transfer clock. In this case, note that the SOUT pin does not go to high impedance state at the completion of data transfer.

The interrupt request bit is set at the completion of the transfer of 8 bits, regardless of whether the internal or external clock is selected.

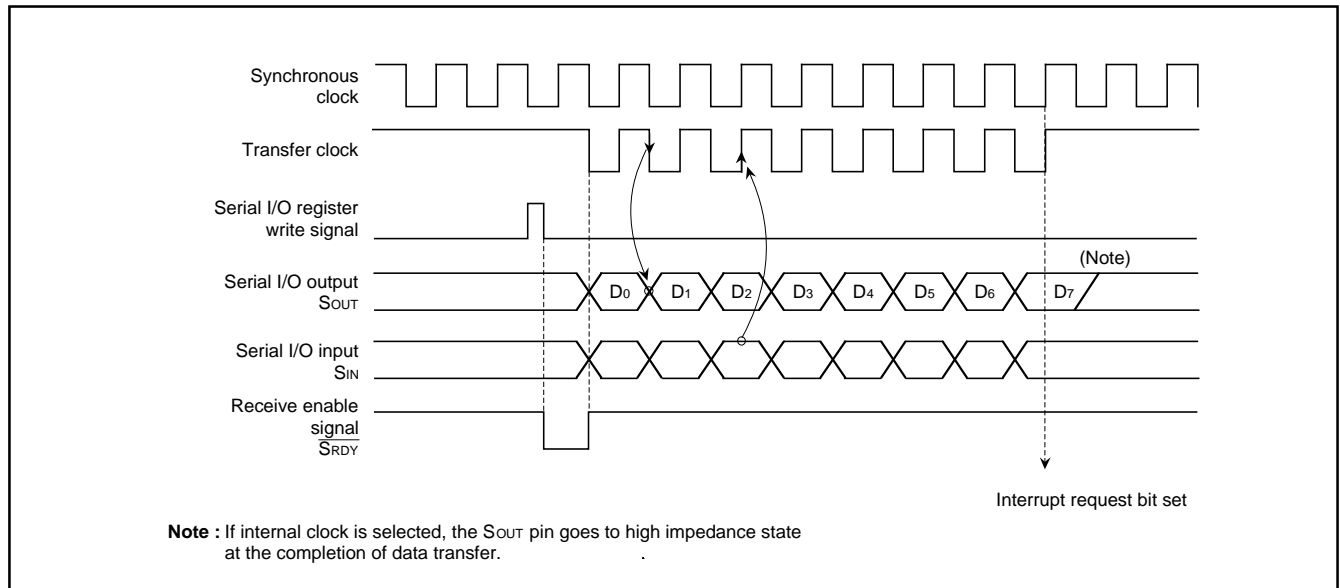


Fig. GA-3 Serial I/O timing in the serial I/O ordinary mode (for LSB first)

(2) Serial I/O Automatic Transfer Mode

The serial I/O1 has the automatic transfer function. For automatic transfer, switch to the automatic transfer mode by setting the serial I/O automatic transfer control register (address 001A₁₆).

The following memory spaces and registers used to enable automatic transfer mode:

- 32-byte serial I/O automatic transfer RAM
- A serial I/O automatic transfer control register
- A serial I/O automatic transfer interval register
- A serial I/O automatic transfer data pointer

When using serial I/O automatic transfer, set the serial I/O1 control register (address 0019₁₆) in the same way as the serial I/O ordinary mode. However, note that when external clock is selected, port P67 becomes the \overline{CS} input pin by setting the bit 4 (the \overline{SRDY} output selection bit) of the serial I/O1 control register to "1".

Serial I/O Automatic Transfer Control Register (SIOAC) 001A₁₆

The serial I/O automatic transfer control register (address 001A₁₆) consists of 4 bits which control automatic transfer.

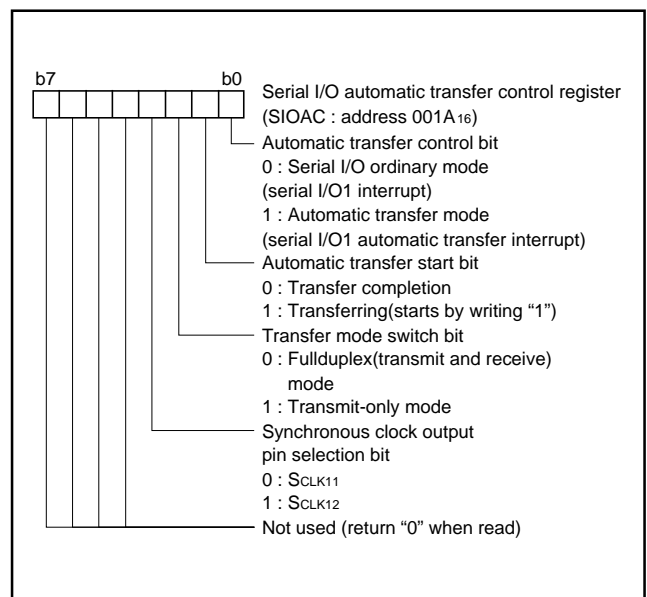


Fig. GA-4 Structure of serial I/O automatic transfer control register

**Serial I/O Automatic Transfer Data Pointer
(SIODP) 0018₁₆**

The serial I/O automatic transfer data pointer (address 0018₁₆) consists of 5 bits which indicate addresses in serial I/O automatic transfer RAM (the value which adds 0F00₁₆ to the serial I/O automatic transfer data pointer is actual address in memory). Set the value (the number of transfer data-1) to the serial I/O automatic transfer data pointer for specifying the storage address of first data.

● **Serial I/O Automatic Transfer RAM**

The serial I/O automatic transfer RAM is the 32 bytes from address 0F00₁₆ to address 0F1F₁₆.

Address \ Bit	7	6	5	4	3	2	1	0
0F00 ₁₆								
0F01 ₁₆								
0F02 ₁₆								
⋮								
0F1D ₁₆								
0F1E ₁₆								
0F1F ₁₆								

Fig. GA-5 Bit allocation of serial I/O automatic transfer RAM

● **Setting of Serial I/O Automatic Transfer Data**

When data is stored in the serial I/O automatic transfer RAM, store the first data at the address set with the serial I/O automatic transfer data pointer so that the last data can be stored at address 0F00₁₆.

**Serial I/O Automatic Transfer Interval Register
(SIOAI) 001C₁₆**

The serial I/O automatic transfer interval register (address 001C₁₆) consists of a 5-bit counter that determines the transfer interval T_i during automatic transfer.

When writing the value n to the serial I/O automatic transfer interval register, $T_i = (n+2) \times T_c$ (T_c : the length of one bit of the transfer clock) occurs. However, note that this transfer interval setting is valid only when selecting the internal clock as the clock source.

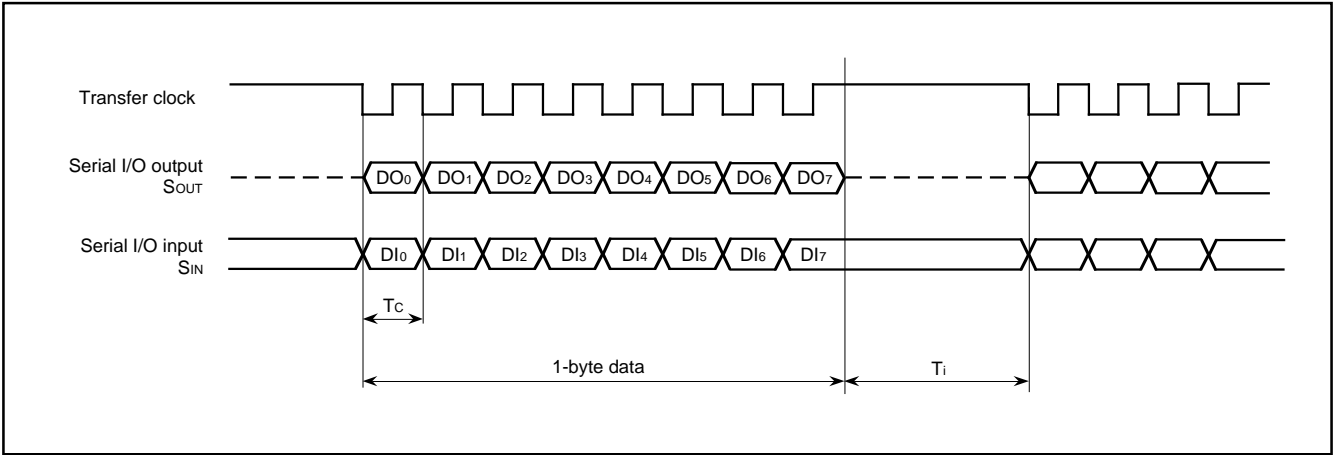


Fig. GA-6 Serial I/O automatic transfer interval timing

● Setting of Serial I/O Automatic Transfer Timing

The timing of serial I/O automatic transfer is set with the serial I/O1 control register (address 0019₁₆) and the serial I/O automatic transfer interval register (address 001C₁₆).

The serial I/O1 control register sets the transfer clock speed, and the serial I/O automatic transfer interval register sets the serial I/O automatic transfer interval. This setting of transfer interval is valid only when selecting the internal clock as the clock source.

● Start of Serial I/O Automatic Transfer

Automatic transfer mode is set by writing "1" to the bit 0 of the serial I/O automatic transfer control register (address 001A₁₆), then automatic transfer starts by writing "1" to the bit 1.

The bit 1 of the serial I/O automatic transfer control register is always "1" during automatic transfer; writing "0" can complete the serial I/O automatic transfer.

● Operation in Serial I/O Automatic Transfer Modes

There are two modes for serial I/O automatic transfer: full duplex mode and transmit-only mode. Either internal or external clock can be selected for each of these modes.

(2.1) Operation in Full Duplex Mode

In full duplex mode, data can be transmitted and received at the same time. Data in the automatic transfer RAM is transmitted in sequence in accordance with the serial I/O automatic transfer data pointer and simultaneously reception data is written to the automatic transfer RAM.

The transfer timing of each bit is the same as that in ordinary operation mode, and the transfer clock stops at "H" after eight transfer clocks are counted.

When selecting the internal clock, the transfer clock remains at "H" for the time set with the serial I/O automatic transfer interval register, then the data at the next address (the address is indicated with the serial I/O automatic transfer data pointer) are transferred.

If when selecting the external clock, the setting of the automatic transfer interval register is invalid, so control the transfer clock externally.

The last data transfer completes when the contents of the serial I/O automatic transfer pointer reach "001₆". At that point, the serial I/O automatic transfer interrupt request bit is set to "1" and the bit 1 of the serial I/O automatic transfer control register is cleared to "0" to complete the serial I/O automatic transfer.

(2.2) Operation in Transmit-Only Mode

The operation in transmit-only mode is the same as that in full duplex mode, except for that data is not transferred from the serial I/O1 register to the serial I/O automatic transfer RAM.

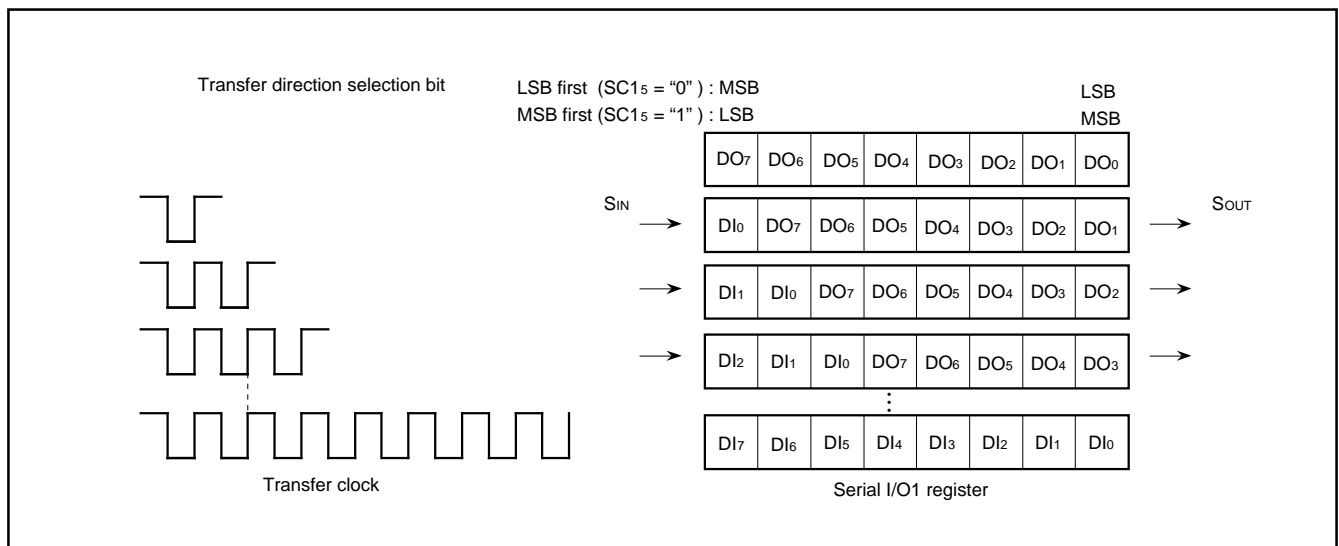


Fig. GA-7 Serial I/O1 register transfer operation in full duplex mode

(2.3) When Selecting the Internal Clock

When selecting the internal clock, the P67/ $\overline{\text{SRDY}}$ /CS/SCLK12 pin can be used as the $\overline{\text{SRDY}}$ pin by setting SC14 to "1".

When selecting the internal clock, the P67 pin can be used as the synchronous clock output pin SCLK12 by setting SIOAC3 to "1". In this case, the SCLK11 pin goes to high impedance state.

Select the function of the P67/ $\overline{\text{SRDY}}$ /CS/SCLK12 and P66/SCLK11 with the following registers (refer to Table GA-1):

- the bit 3 (SC13), the bit 4(SC14), and the bit 6(SC16) of the serial I/O1 control register
- the bit 3 (SIOAC3) of the serial I/O automatic transfer control register

When using both the SCLK11 and SCLK12 by switching, switch the P67/ $\overline{\text{SRDY}}$ /CS/SCLK12 to the P67 (SC14=0) and set the P67 direction register to input mode. Note that switch SIOAC3 during "H" of transfer clock at the completion of automatic transfer.

Table GA-1. SCLK11 and SCLK12 selection

SC16	SC14	SC33	SIOAC3	P66/SCLK11	P67/SCLK12
1	0	1	0	SCLK11	P67
			1	High impedance	SCLK12

Note : SC13: Serial I/O1 port selection bit
SC14: $\overline{\text{SRDY}}$ output selection bit
SC16: Synchronous clock selection bit
SIOAC3: Synchronous clock output pin selection bit

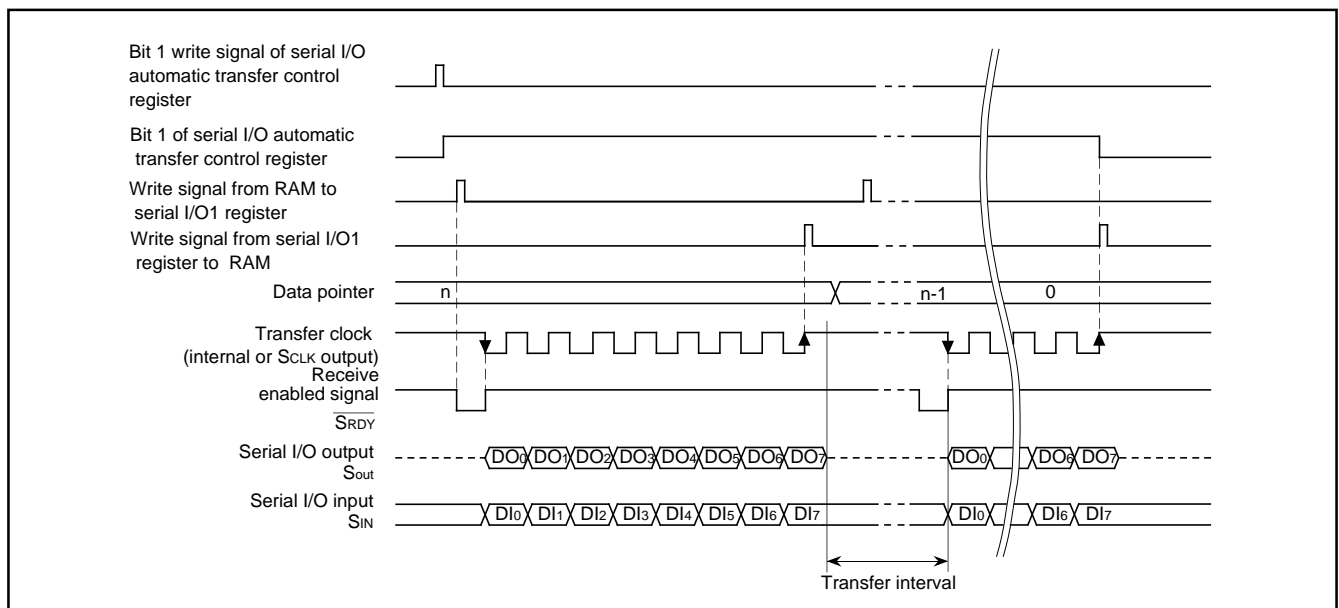


Fig. GA-8 Timing diagram during serial I/O automatic transfer (internal clock selected, $\overline{\text{SRDY}}$ used)

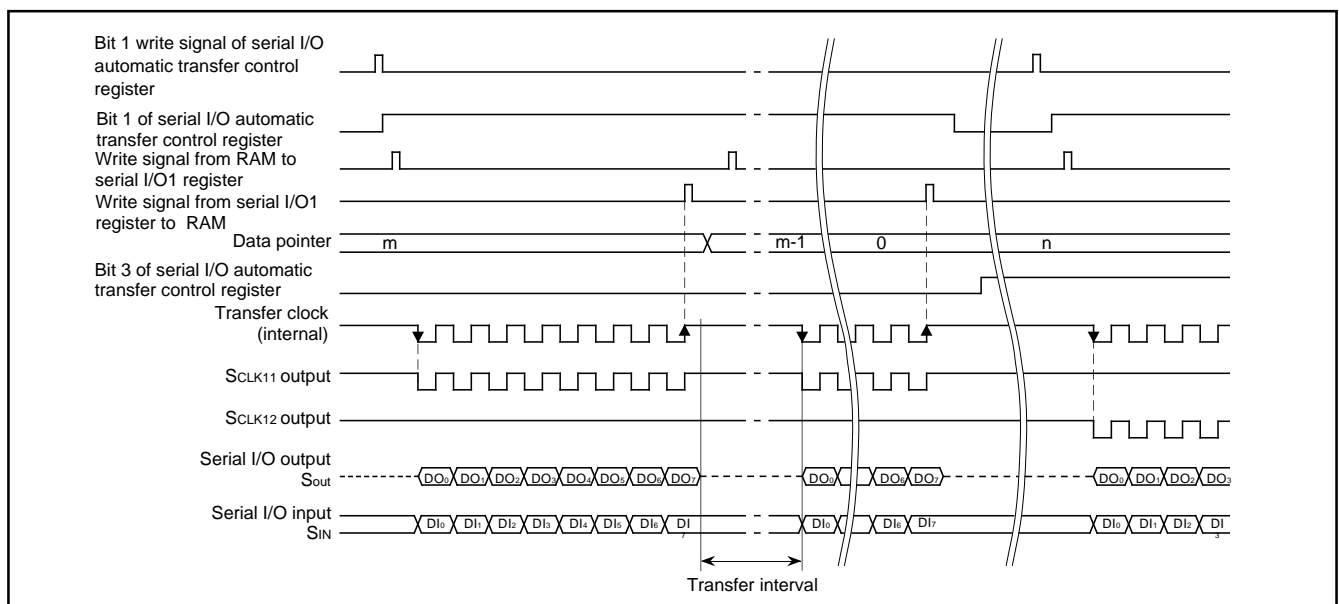


Fig. GA-9 Timing during serial I/O automatic transfer (internal clock selected, SCLK11 and SCLK12 used)

(2.4) When Selecting the External Clock

When selecting the external clock, the internal clock and the setting of transfer interval with the serial I/O automatic transfer interval register are invalid, but the serial I/O output pin SOUT1 and the internal transfer clock can be controlled from the outside by setting the SRDY1 pin to the CS (input) pin.

When the CS input is "L", the SOUT1 pin and the internal transfer clock are enabled.

When the CS input is "H", the SOUT1 pin goes to high impedance state and the internal transfer clock goes to "H".

Select the function of the P67/SRDY1/CS/SCLK12 with the following registers (refer to Table GA-2):

- the bit 4 (SC14) and the bit 6 (SC16) of the serial I/O1 control register
- the bit 0 (SIOAC0) of the serial I/O automatic transfer control register

Switch the CS pin from "L" to "H" or from "H" to "L" during "H" of the transfer clock (SCLK11 input) after transferring 1-byte data.

When selecting the external clock, set the external clock to "L" after 9 cycles or more of the internal clock ϕ after setting the start bit. After transferring 1-byte data, leave 11 cycles or more of the internal clock ϕ free for the transfer interval.

When not using the CS input, note that the SOUT pin will not go to high impedance state, even after transfer is completed.

When not using the CS input, or when CS is "L", control the external clock because the data in the serial I/O register will continue to shift while the external clock is input, even after the completion of automatic transfer (Note that the automatic transfer interrupt request bit is set and the bit 1 of the serial I/O automatic transfer register is cleared at the point when the specified number of bytes of data have been transferred.)

Table GA-2. P67/SRDY1/CS selection

SC16	SC14	SIOAC0	P67/SRDY1/CS
0	0	X	P67
	1	0	SRDY1
		1	CS

Note : SC14: SRDY1 output selection bit
SC16: Synchronous clock selection bit
SIOAC0: Automatic transfer control bit

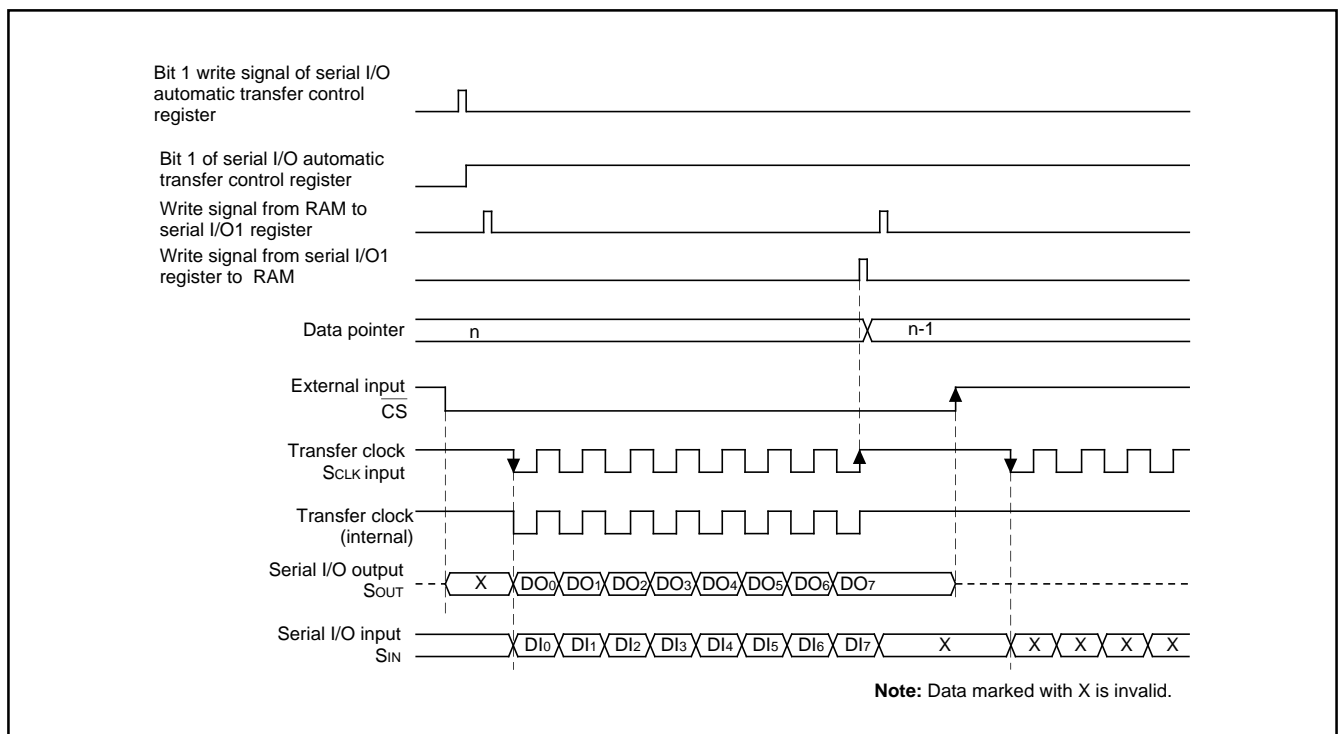


Fig. GA-10 Timing during serial I/O automatic transfer (external clock selected)

A-D CONVERTER

The functional blocks of the A-D converter are described below.

A-D Conversion Register (AD) 002D16

The A-D conversion register is a read-only register that stores the result of an A-D conversion. This register should not be read during A-D conversion.

AD/DA Control Register (ADCON) 002C16

The AD/DA control register controls the A-D and the D-A conversion process. Bits 0 to 3 of this register select analog input pins. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed.

The A-D conversion starts by writing "0" to this bit. Bit 6 controls the output of D-A converter.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports P77/AN7–P70/AN0, P57/SRDY3/AN15–P50/SIN2/AN8, and inputs to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to 500 kHz or more during A-D conversion.

Note : When using the A-D conversion interrupt, set the INT4/AD conversion interrupt switch bit (the bit 5 of the interrupt selection register) to "1".

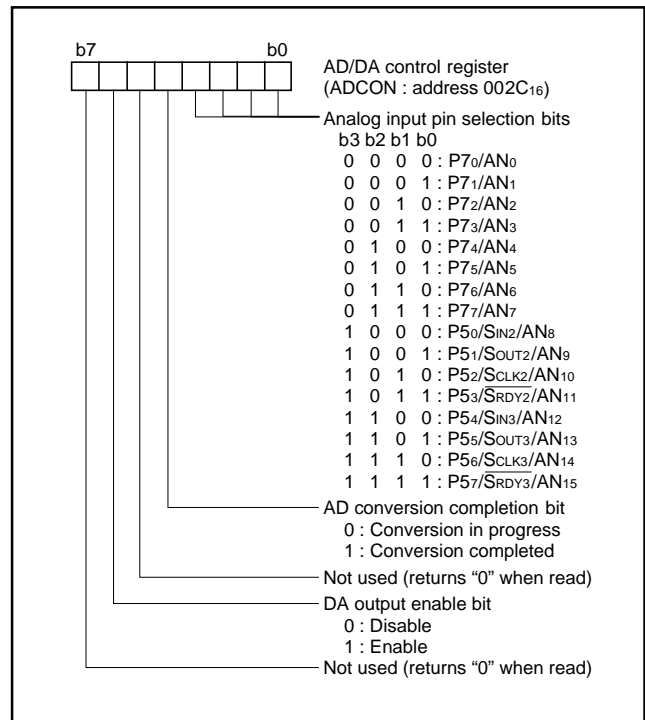


Fig. JA-1 Structure of A-D control register

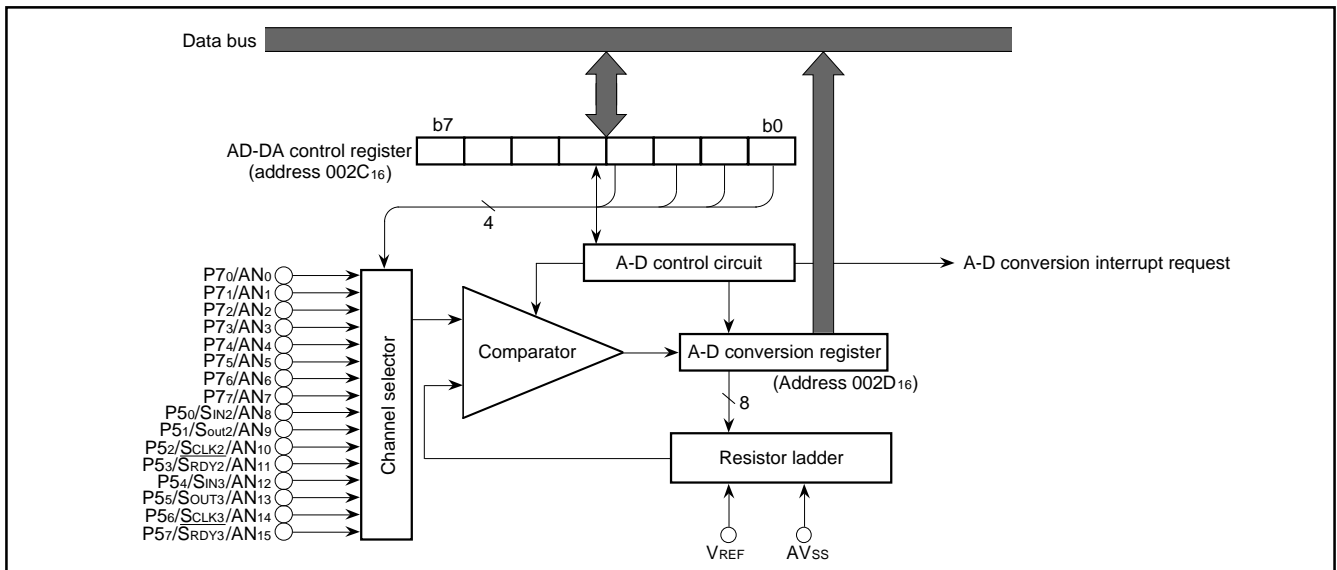


Fig. JA-2 A-D converter block diagram

D-A CONVERTER

The 3819 group has internal D-A converter with 8-bit resolutions X 1 channel.

D-A conversion is performed by setting the value in the D-A conversion register. The result of D-A conversion is output from the DA pin by setting the DA output enable bit to "1". At this time, the corresponding bit (PB2/DA) of the port PB direction register should be set to "0" (input status).

The output analog voltage V is determined with the value n (n : decimal number) in the D-A conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n=0 \text{ to } 255)$$

* V_{REF} : the reference voltage

At reset, the D-A conversion register is cleared to "0016", the DA output enable bits are cleared to "0", and the PB2/DA pin goes to high impedance state. The D-A output does not build in a buffer, so connect an external buffer when driving a low-impedance load. Set V_{CC} to 3.0 V or more when using the D-A converter.

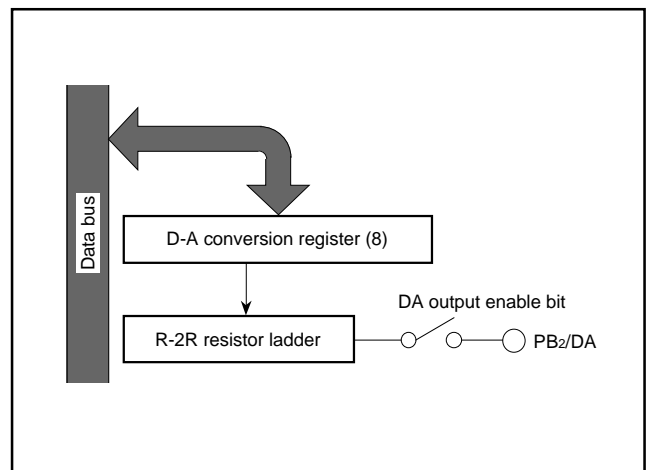


Fig. JB-1 D-A converter block diagram

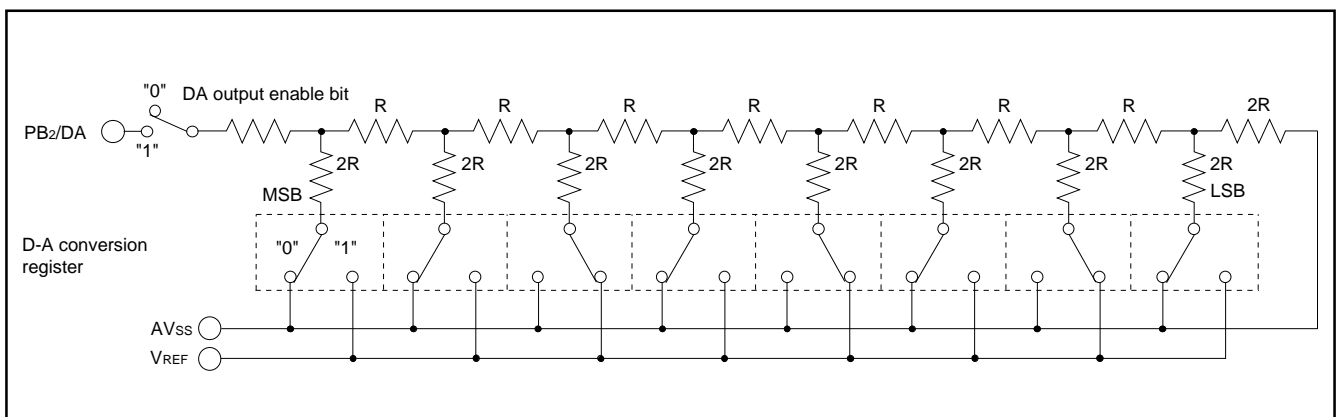


Fig. JB-2 Equivalent connection circuit of D-A converter

FLD CONTROLLER

The 3819 group has fluorescent display (FLD) drive and control circuits.

The FLD controller consists of the following components:

- 42 pins for segments
- 20 pins for digits
- FLDC mode register 1
- FLDC mode register 2
- FLD data pointer
- FLD data pointer reload register

- Port P0 segment/digit switch register
- Port P2 digit/port switch register
- Port PA segment/port switch register
- Port P8 segment/port switch register
- 96-byte FLD automatic display RAM

The segment pins can be used from 16 up to 42 pins (maximum) and the digit pins can be used from 6 up to 16 pins (maximum). The segment and the digit pins can be used up to 52 pins (maximum) in total.

In the FLD automatic display mode ports P12 to P17 become digit pins DIG10 to DIG15 automatically.

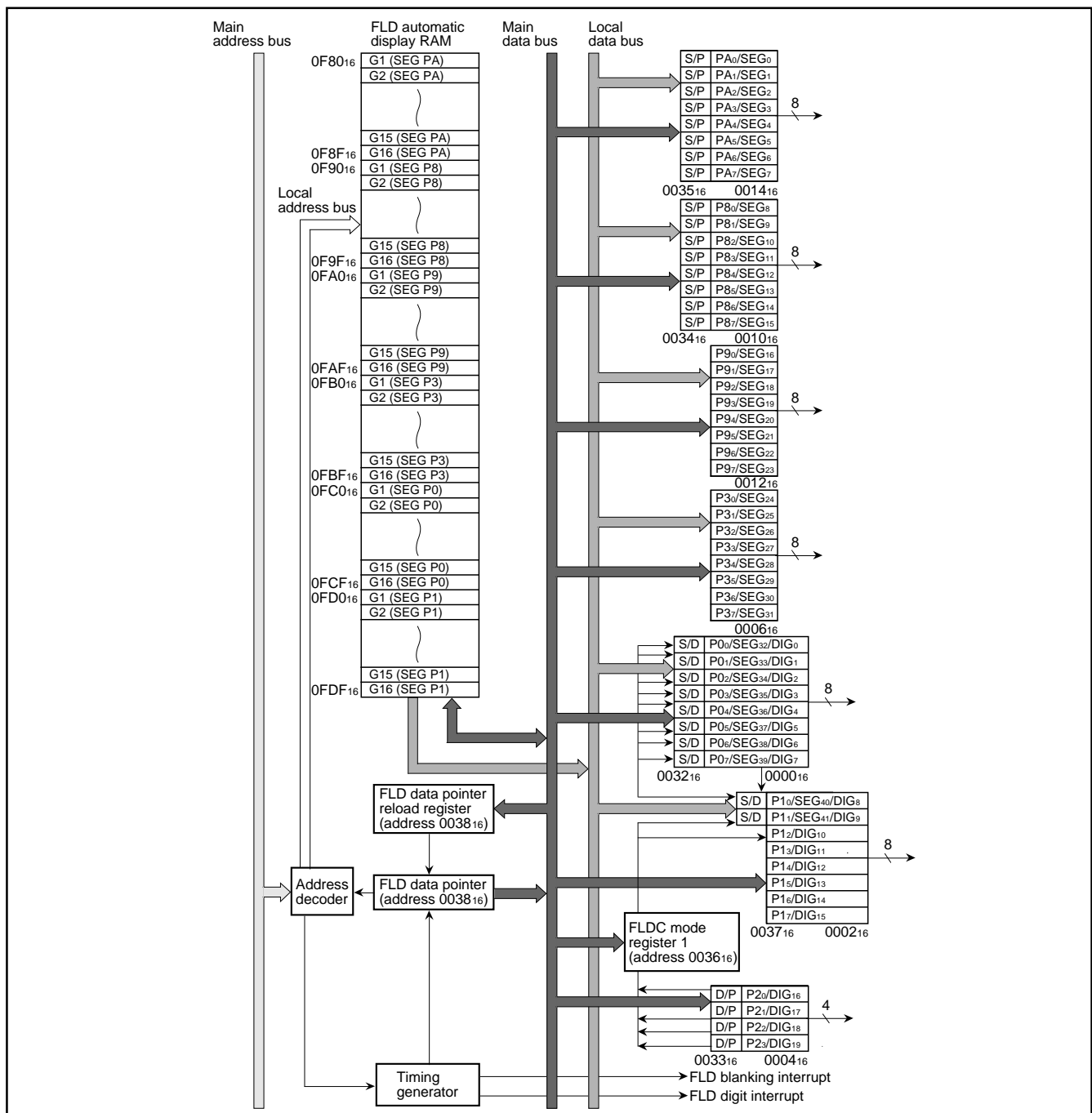


Fig. KA-1 FLD control circuit block diagram

FLDC Mode Registers (FLDM 1, FLDM 2) 0036₁₆, 0037₁₆

The FLDC mode register 1 (address 0036₁₆) and FLDC mode register 2 (address 0037₁₆) are a seven bit register and an eight bit

register respectively which are used to control the FLD automatic display and set the blanking time T_{scan} for key-scan.

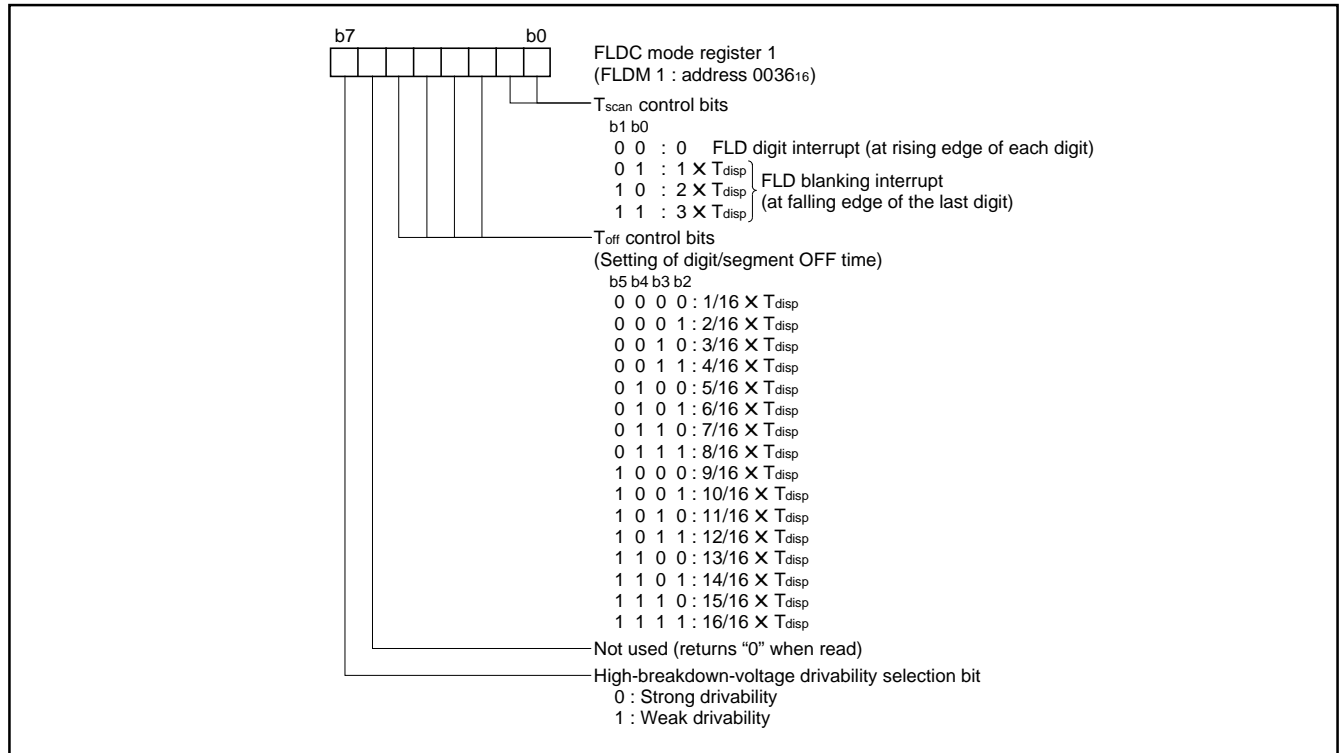


Fig. KA-2 Structure of FLDC mode register 1

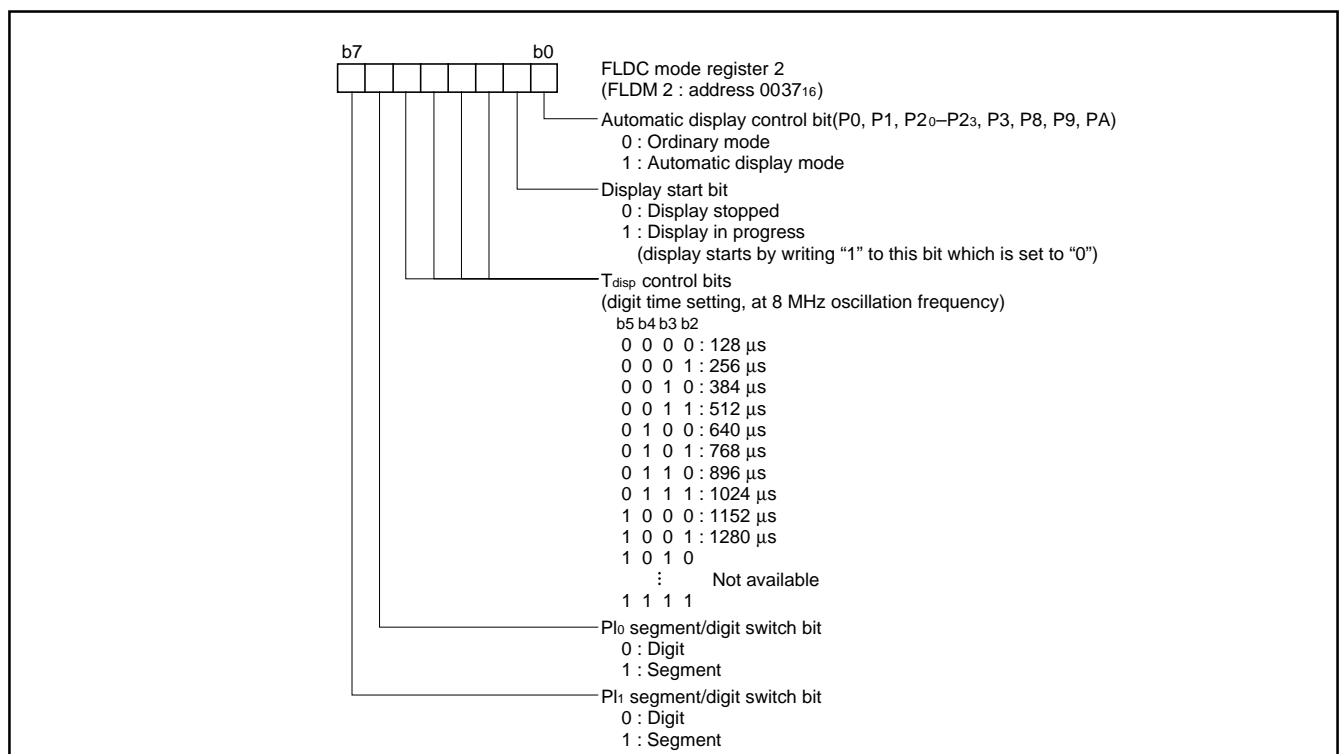


Fig. KA-3 Structure of FLDC mode register 2

● Pins for FLD Automatic Display

Ports P0, P1, P20–P23, P3, P8, P9, and PA is selected for the FLD automatic display function by setting the automatic display control bit of the FLDC mode register 2 (address 003716) to “1”.

When using the FLD automatic display mode, set the number of segments and digits for each port.

Table L-1. Pins in FLD automatic display mode

Port Name	Automatic Display Pins	Setting Method
PA0–PA7	SEG0–SEG7 or PA0–PA7	The individual bits of the segment/port switch register (address 003516) can be set each pin to either segment (“1”) or general-purpose I/O port (“0”).
P80–P87	SEG8–SEG15 or P80–P87	The individual bits of the segment/port switch register (address 003416) can be used to set each pin to either segment (“1”) or general-purpose I/O port (“0”).
P90–P97	SEG16–SEG23	None (segment only)
P30–P37	SEG24–SEG31	None (segment only)
P00–P07 P10, P11	SEG32–SEG41 or DIG0–DIG9	The individual bits of the segment/digit switch register (address 003216) and the bit 6, 7 of the FLDC mode register 2 can be used to set each pin to segment (“1”) or digit (“0”). (Note)
P12–P17	DIG10–DIG15	None (digit only)
P20–P23	DIG16–DIG19 or P20–P23	The individual bits of the digit/port switch register (address 003316) can be used to set each pin to digit (“1”) or general-purpose output port (“0”). (Note)

Note : Be sure to set digits in sequence.

Number of segments Number of digits				Number of segments Number of digits																											
24 8				30 10				36 16				24 8				30 10				36 16											
Port PA (has the segment/port switch register)				0 PA ₀ 0 PA ₁ 0 PA ₂ 0 PA ₃ 0 PA ₄ 0 PA ₅ 0 PA ₆ 0 PA ₇				0 PA ₀ 0 PA ₁ 0 PA ₂ 0 PA ₃ 0 PA ₄ 0 PA ₅ 0 PA ₆ 0 PA ₇				1 SEG ₀ 1 SEG ₁ 1 SEG ₂ 1 SEG ₃ 1 SEG ₄ 1 SEG ₅ 1 SEG ₆ 1 SEG ₇				Port P3 (segment only)				SEG ₂₄ SEG ₂₅ SEG ₂₆ SEG ₂₇ SEG ₂₈ SEG ₂₉ SEG ₃₀ SEG ₃₁				SEG ₂₄ SEG ₂₅ SEG ₂₆ SEG ₂₇ SEG ₂₈ SEG ₂₉ SEG ₃₀ SEG ₃₁				SEG ₂₄ SEG ₂₅ SEG ₂₆ SEG ₂₇ SEG ₂₈ SEG ₂₉ SEG ₃₀ SEG ₃₁			
Port P8 (has the segment/port switch register)				0 P8 ₀ 0 P8 ₁ 0 P8 ₂ 0 P8 ₃ 0 P8 ₄ 0 P8 ₅ 0 P8 ₆ 0 P8 ₇				0 P8 ₀ 0 P8 ₁ 0 P8 ₂ 0 P8 ₃ 1 SEG ₁₂ 1 SEG ₁₃ 1 SEG ₁₄ 1 SEG ₁₅				1 SEG ₈ 1 SEG ₉ 1 SEG ₁₀ 1 SEG ₁₁ 1 SEG ₁₂ 1 SEG ₁₃ 1 SEG ₁₄ 1 SEG ₁₅				Port P0 (has the segment/digit switch register)				1 SEG ₃₂ 1 SEG ₃₃ 1 SEG ₃₄ 1 SEG ₃₅ 1 SEG ₃₆ 1 SEG ₃₇ 1 SEG ₃₈ 1 SEG ₃₉				1 SEG ₃₂ 1 SEG ₃₃ 1 SEG ₃₄ 1 SEG ₃₅ 1 SEG ₃₆ 1 SEG ₃₇ 1 SEG ₃₈ 1 SEG ₃₉				1 SEG ₃₂ 1 SEG ₃₃ 1 SEG ₃₄ 1 SEG ₃₅ 0 DIG ₄ →G ₁₆ 0 DIG ₅ →G ₁₅ 0 DIG ₆ →G ₁₄ 0 DIG ₇ →G ₁₃			
Port P9 (segment only)				SEG ₁₆ SEG ₁₇ SEG ₁₈ SEG ₁₉ SEG ₂₀ SEG ₂₁ SEG ₂₂ SEG ₂₃				SEG ₁₆ SEG ₁₇ SEG ₁₈ SEG ₁₉ SEG ₂₀ SEG ₂₁ SEG ₂₂ SEG ₂₃				SEG ₁₆ SEG ₁₇ SEG ₁₈ SEG ₁₉ SEG ₂₀ SEG ₂₁ SEG ₂₂ SEG ₂₃				Port P1 (has the segment/digit switch register)				0 DIG ₈ →G ₈ 0 DIG ₉ →G ₇ DIG ₁₀ →G ₆ DIG ₁₁ →G ₅ DIG ₁₂ →G ₄ DIG ₁₃ →G ₃ DIG ₁₄ →G ₂ DIG ₁₅ →G ₁				1 SEG ₄₀ 1 SEG ₄₁ DIG ₁₀ →G ₁₀ DIG ₁₁ →G ₉ DIG ₁₂ →G ₈ DIG ₁₃ →G ₇ DIG ₁₄ →G ₆ DIG ₁₅ →G ₅				0 DIG ₈ →G ₁₂ 0 DIG ₉ →G ₁₁ DIG ₁₀ →G ₁₀ DIG ₁₁ →G ₉ DIG ₁₂ →G ₈ DIG ₁₃ →G ₇ DIG ₁₄ →G ₆ DIG ₁₅ →G ₅			
												Port P2 (has the digit/port switch register)				0 P2 ₀ 0 P2 ₁ 0 P2 ₂ 0 P2 ₃				1 DIG ₁₆ →G ₄ 1 DIG ₁₇ →G ₃ 1 DIG ₁₈ →G ₂ 1 DIG ₁₉ →G ₁				1 DIG ₁₆ →G ₄ 1 DIG ₁₇ →G ₃ 1 DIG ₁₈ →G ₂ 1 DIG ₁₉ →G ₁							

Fig. KA-4 Segment/digit setting example

● FLD Automatic Display RAM

The FLD automatic display RAM area is the 96 bytes from addresses 0F80₁₆ to 0FDF₁₆. The FLD automatic display RAM area can store 6-byte segment data up to 16 digits (maximum). Addresses 0F80₁₆ to 0F8F₁₆ are used for PA segment data, addresses 0F90₁₆ to 0F9F₁₆ are used for P8 segment data, addresses 0FA0₁₆ to 0FAF₁₆ are used for P9 segment data, addresses 0FB0₁₆ to 0FBF₁₆ are used for P3 segment data, addresses 0FC0₁₆ to 0FCF₁₆ are used for P0 segment data, and addresses 0FD0 to 0FDF₁₆ are used for P1 segment data.

FLD Data Pointer and FLD Data Pointer Reload Register

(FLDDP) 0038₁₆

Both the FLD data pointer and FLD data pointer reload register are 7-bit registers allocated at address 0038₁₆. When writing data to this address, the data is written to the FLD data pointer reload register, when reading data from this address, the value in the FLD data pointer is read.

The FLD data pointer indicates the data address in the FLD automatic display RAM to be transferred to a segment. The FLD data pointer reload register indicates the first digit address of the most significant segment.

The value which adds 0F80₁₆ to these data is actual address in memory.

The contents of the FLD data pointer indicate the first address of segment P1 (the contents of the FLD data pointer reload register) at the start of automatic display. The FLDC data pointer content changes repeatedly as follows: when transferring the segment P1 data to the segment, the content decreases by -16; when transferring the segment P0 data, it decreases by -16; when transferring the segment P3 data, it decreases by -16; when transferring the segment P9 data, it decreases by -16; when transferring the segment P8 data, it decreases by -16; when transferring the segment PA data, it increases by +79. Once it reaches "00", at the next timing the value in the FLD data pointer reload register is transferred to the FLD data pointer. In this way, the 6-byte data of P1, P0, P3, P9, P8 and PA segments for 1 digit are transferred.

Address \ Bit	7	6	5	4	3	2	1	0	
0F80 ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	← The last digit (The last data of segment PA)
0F81 ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Segment PA data area
0F8E ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	
0F8F ₁₆	SEG ₇	SEG ₆	SEG ₅	SEG ₄	SEG ₃	SEG ₂	SEG ₁	SEG ₀	← The last digit (The last data of segment P8)
0F90 ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	
0F91 ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	Segment P8 data area
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0F9E ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	← The last digit (The last data of segment P9)
0F9F ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	SEG ₈	
0FA0 ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	← The last digit (The last data of segment P9)
0FA1 ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Segment P9 data area
0FAE ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	
0FAF ₁₆	SEG ₂₃	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	SEG ₁₆	← The last digit (The last data of segment P3)
0FB0 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	
0FB1 ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	Segment P3 data area
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0FBE ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	← The last digit (The last data of segment P0)
0FBF ₁₆	SEG ₃₁	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	SEG ₂₄	
0FC0 ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	← The last digit (The last data of segment P0)
0FC1 ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	Segment P0 data area
0FCE ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	
0FCF ₁₆	SEG ₃₉	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	SEG ₃₂	← The last digit (The last data of segment P1)
0FD0 ₁₆							SEG ₄₁	SEG ₄₀	
0FD1 ₁₆							SEG ₄₁	SEG ₄₀	Segment P1 data area
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
0FDE ₁₆							SEG ₄₁	SEG ₄₀	
0FDF ₁₆							SEG ₄₁	SEG ₄₀	

Fig. KA-5 FLD automatic display RAM and bit allocation

Data Setup


When data is stored in the FLD automatic display RAM, the last data of segment PA is stored at address 0F80₁₆, the last data of segment P8 is stored at address 0F90₁₆, the last data of segment P9 is stored at address 0FA0₁₆, the last data of segment P3 is stored at address 0FB0₁₆, the last data of segment P0 is stored at address 0FC0₁₆, and the last data of segment P1 is stored at address 0FD0₁₆ to allocate in se-

quence from the last data respectively. The first data of the segment PA, P8, P9, P3, P0, and P1 is stored at an address which adds the value of (the digit number-1) to the corresponding address 0F80₁₆, 0F90₁₆, 0FA0₁₆, 0FB0₁₆, 0FC0₁₆, and 0FD0₁₆.

Set the low-order 4 bits of the FLD data pointer reload register to the value given by the number of digits-1. "1" is always written to bit 6 and bit 4, and "0" is always written to bit 5. Note that "0" is always read from bits 6, 5 and 4 when reading.

For 30 segments and 15 digits
(FLD data pointer reload register = 14)

Bit	7	6	5	4	3	2	1	0
Address								
0F80 ₁₆								
0F81 ₁₆								
0F82 ₁₆								
0F83 ₁₆								
0F84 ₁₆								
0F85 ₁₆								
0F86 ₁₆								
0F87 ₁₆								
0F88 ₁₆								
0F89 ₁₆								
0F8A ₁₆								
0F8B ₁₆								
0F8C ₁₆								
0F8D ₁₆								
0F8E ₁₆								
0F8F ₁₆								
0F90 ₁₆								
0F91 ₁₆								
0F92 ₁₆								
0F93 ₁₆								
0F94 ₁₆								
0F95 ₁₆								
0F96 ₁₆								
0F97 ₁₆								
0F98 ₁₆								
0F99 ₁₆								
0F9A ₁₆								
0F9B ₁₆								
0F9C ₁₆								
0F9D ₁₆								
0F9E ₁₆								
0F9F ₁₆								
0FA0 ₁₆								
0FA1 ₁₆								
0FA2 ₁₆								
0FA3 ₁₆								
0FA4 ₁₆								
0FA5 ₁₆								
0FA6 ₁₆								
0FA7 ₁₆								
0FA8 ₁₆								
0FA9 ₁₆								
0FAA ₁₆								
0FAB ₁₆								
0FAC ₁₆								
0FAD ₁₆								
0FAE ₁₆								
0FAF ₁₆								

Note :  Shaded areas are used.

For 30 segments and 15 digits
(FLD data pointer reload register = 14)

Bit	7	6	5	4	3	2	1	0
Address								
0FB0 ₁₆								
0FB1 ₁₆								
0FB2 ₁₆								
0FB3 ₁₆								
0FB4 ₁₆								
0FB5 ₁₆								
0FB6 ₁₆								
0FB7 ₁₆								
0FB8 ₁₆								
0FB9 ₁₆								
0FBA ₁₆								
0FBB ₁₆								
0FBC ₁₆								
0FBD ₁₆								
0FBE ₁₆								
0FBF ₁₆								
0FC0 ₁₆								
0FC1 ₁₆								
0FC2 ₁₆								
0FC3 ₁₆								
0FC4 ₁₆								
0FC5 ₁₆								
0FC6 ₁₆								
0FC7 ₁₆								
0FC8 ₁₆								
0FC9 ₁₆								
0FCA ₁₆								
0FCB ₁₆								
0FCC ₁₆								
0FCD ₁₆								
0FCE ₁₆								
0FCF ₁₆								
0FD0 ₁₆								
0FD1 ₁₆								
0FD2 ₁₆								
0FD3 ₁₆								
0FD4 ₁₆								
0FD5 ₁₆								
0FD6 ₁₆								
0FD7 ₁₆								
0FD8 ₁₆								
0FD9 ₁₆								
0FDA ₁₆								
0FDB ₁₆								
0FDC ₁₆								
0FDD ₁₆								
0FDE ₁₆								
0FDF ₁₆								

Fig. KA-6 Example of using the FLD automatic display RAM (1)

For 42 segments and 8 digits
(FLD data pointer reload register = 7)

Bit	7	6	5	4	3	2	1	0
Address								
0F80 ₁₆								
0F81 ₁₆								
0F82 ₁₆								
0F83 ₁₆								
0F84 ₁₆								
0F85 ₁₆								
0F86 ₁₆								
0F87 ₁₆								
0F88 ₁₆								
0F89 ₁₆								
0F8A ₁₆								
0F8B ₁₆								
0F8C ₁₆								
0F8D ₁₆								
0F8E ₁₆								
0F8F ₁₆								
0F90 ₁₆								
0F91 ₁₆								
0F92 ₁₆								
0F93 ₁₆								
0F94 ₁₆								
0F95 ₁₆								
0F96 ₁₆								
0F97 ₁₆								
0F98 ₁₆								
0F99 ₁₆								
0F9A ₁₆								
0F9B ₁₆								
0F9C ₁₆								
0F9D ₁₆								
0F9E ₁₆								
0F9F ₁₆								
0FA0 ₁₆								
0FA1 ₁₆								
0FA2 ₁₆								
0FA3 ₁₆								
0FA4 ₁₆								
0FA5 ₁₆								
0FA6 ₁₆								
0FA7 ₁₆								
0FA8 ₁₆								
0FA9 ₁₆								
0FAA ₁₆								
0FAB ₁₆								
0FAC ₁₆								
0FAD ₁₆								
0FAE ₁₆								
0FAF ₁₆								

Note :  Shaded areas are used.

For 42 segments and 8 digits
(FLD data pointer reload register = 7)

Bit	7	6	5	4	3	2	1	0
Address								
0FB0 ₁₆								
0FB1 ₁₆								
0FB2 ₁₆								
0FB3 ₁₆								
0FB4 ₁₆								
0FB5 ₁₆								
0FB6 ₁₆								
0FB7 ₁₆								
0FB8 ₁₆								
0FB9 ₁₆								
0FBA ₁₆								
0FBB ₁₆								
0FBC ₁₆								
0FBD ₁₆								
0FBE ₁₆								
0FBF ₁₆								
0FC0 ₁₆								
0FC1 ₁₆								
0FC2 ₁₆								
0FC3 ₁₆								
0FC4 ₁₆								
0FC5 ₁₆								
0FC6 ₁₆								
0FC7 ₁₆								
0FC8 ₁₆								
0FC9 ₁₆								
0FCA ₁₆								
0FCB ₁₆								
0FCC ₁₆								
0FCD ₁₆								
0FCE ₁₆								
0FCF ₁₆								
0FD0 ₁₆								
0FD1 ₁₆								
0FD2 ₁₆								
0FD3 ₁₆								
0FD4 ₁₆								
0FD5 ₁₆								
0FD6 ₁₆								
0FD7 ₁₆								
0FD8 ₁₆								
0FD9 ₁₆								
0FDA ₁₆								
0FDB ₁₆								
0FDC ₁₆								
0FDD ₁₆								
0FDE ₁₆								
0FDF ₁₆								

Fig. KA-6 Example of using the FLD automatic display RAM (2) (continued)

● Timing Setting

The digit time (T_{disp}) can be set with the FLDC mode register 2 (address 0037₁₆). The T_{scan} and digit/segment OFF time (T_{off}) can be set with the FLDC mode register 1 (address 0036₁₆). Note that flickering will occur if the repetition frequency ($1/(T_{\text{disp}} \times \text{number of digits} + T_{\text{scan}})$) is an integral multiple of the digit timing T_{disp} .

● FLD Automatic Display Start

To perform FLD automatic display, set the following registers.

- Port P0 segment/digit switch register
- Port P2 digit/port switch register
- Port P8 segment/port switch register
- Port PA segment/port switch register
- FLDC mode register 1
- FLDC mode register 2
- FLD data pointer

Automatic display mode is selected by writing "1" to the bit 0 of the FLDC mode register 2 (address 0037₁₆), and the automatic display is started by writing "1" to the bit 1.

During automatic display bit 1 of the FLDC mode register 2 always keeps "1", automatic display can be interrupted by writing "0" to the bit 1.

● Key-scan

If key-scan is performed with the segment during the key-scan blanking period T_{scan} , take the following sequence:

1. Write "0" to the bit 0 (automatic display control bit) of the FLDC mode register 2 (address 0037₁₆).
2. Set the port corresponding to the segment for key-scan to the output port.
3. Perform the key-scan.
4. After the key-scan is performed, write "1" (automatic display mode) to the bit 0 of FLDC mode register 2 (address 0037₁₆).

Note on performance of key-scan in the above 1 to 4 sequence.

1. Do not write "0" to the bit 1 of FLDC mode register 2 (address 0037₁₆).
2. Do not write "1" to the port corresponding to the digit.

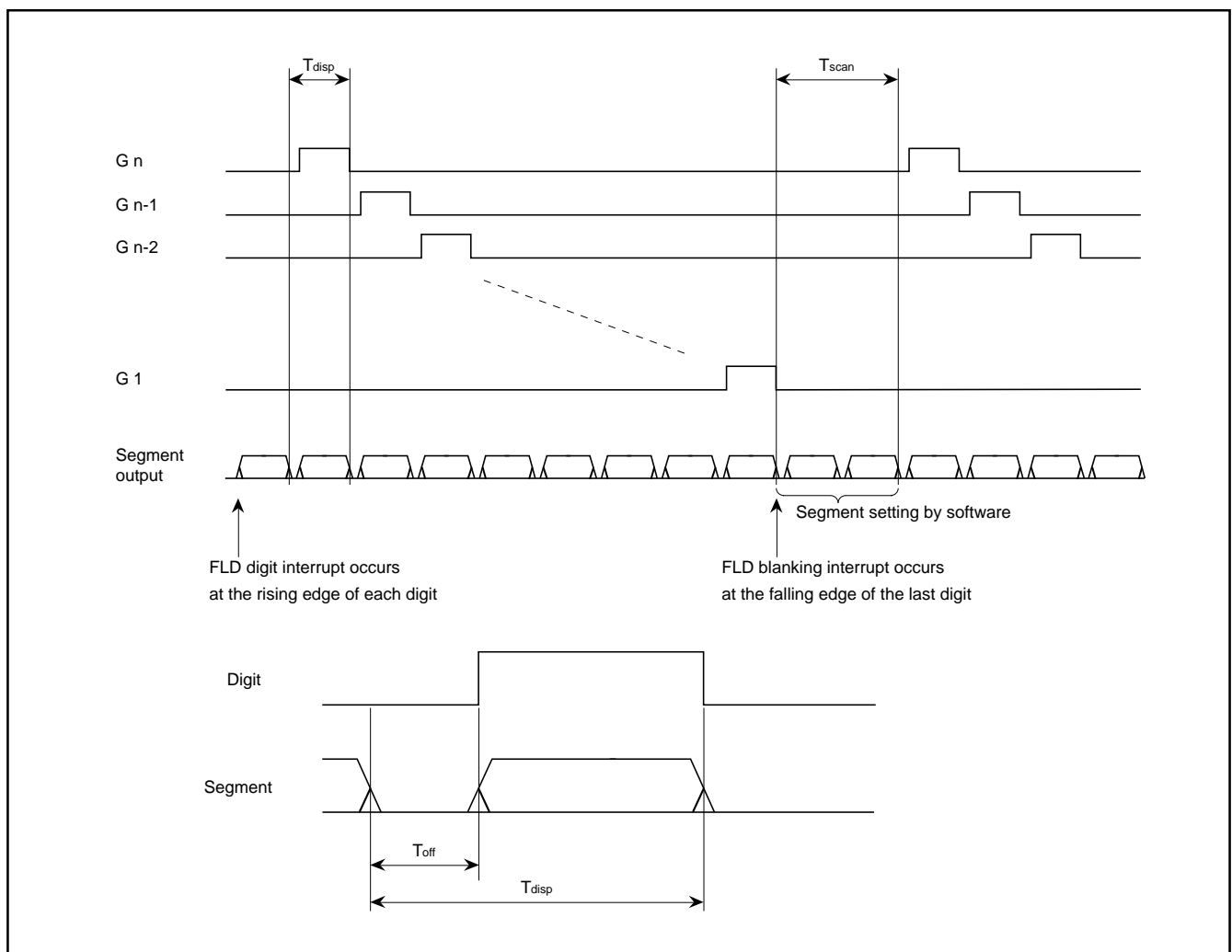


Fig. KA-7 FLDC timing

INTERRUPT INTERVAL DETERMINATION FUNCTION

The 3819 group builds in an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary up counter. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the P42/INT2 pin to the rising transition (falling transition) of the signal pulse that is input next.

How to determine the interrupt interval is described below.

- ① Enable the INT2 interrupt by setting the bit 2 of the interrupt control register 1 (address 003E₁₆). Select the rising interval or falling interval by setting the bit 2 of the interrupt edge selection register (address 003A₁₆).
- ② Set the bit 0 of the interrupt interval determination control register (address 0031₁₆) to "1" (interrupt interval determination operating).
- ③ Select the sampling clock of 8-bit binary up counter by setting the bit 1 of the interrupt interval determination control register. When writing "0", $f(X_{IN})/256$ is selected (the sampling interval: 32 μ s at $f(X_{IN}) = 8.38$ MHz) ; when "1", $f(X_{IN})/512$ is selected (the sampling interval: 64 μ s at $f(X_{IN}) = 8.38$ MHz).
- ④ When the signal of polarity which is set on the INT2 pin (rising or falling transition) is input, the 8-bit binary up counter starts counting up of the selected counter sampling clock.
- ⑤ When the signal of polarity above ④ is input again, the value of the 8-bit binary up counter is transferred to the interrupt interval

determination register (address 0030₁₆), and the remote control interrupt request occurs. Immediately after that, the 8-bit binary up counter is cleared to "00₁₆". The 8-bit binary up counter continues to count up again from "00₁₆".

- ⑥ When count value reaches "FF₁₆", the 8-bit binary up counter stops counting up. Then, simultaneously when the next counter sampling clock is input, the counter sets value "FF₁₆" to the interrupt interval determination register to generate the counter overflow interrupt request.

Noise filter

The P42/INT2 pin builds in the noise filter.

The noise filter operation is described below.

- ① Select the sampling clock of the input signal with the bits 2 and 3 of the interrupt interval determination control register. When not using the noise filter, set "00₂".
- ② The P42/INT2 input signal is sampled in synchronization with the selected clock. When sampling the same level signal in series, the signal is recognized as the interrupt signal, and the interrupt request occurs.

When setting the bit 4 of interrupt interval determination control register to "1", the interrupt request can occur at both rising and falling edges.

When using the noise filter, set the minimum pulse width of the INT2 input signal to 2 cycles or more.

Note : In the low-speed mode (CM7=1), the interrupt interval determination function can not operate.

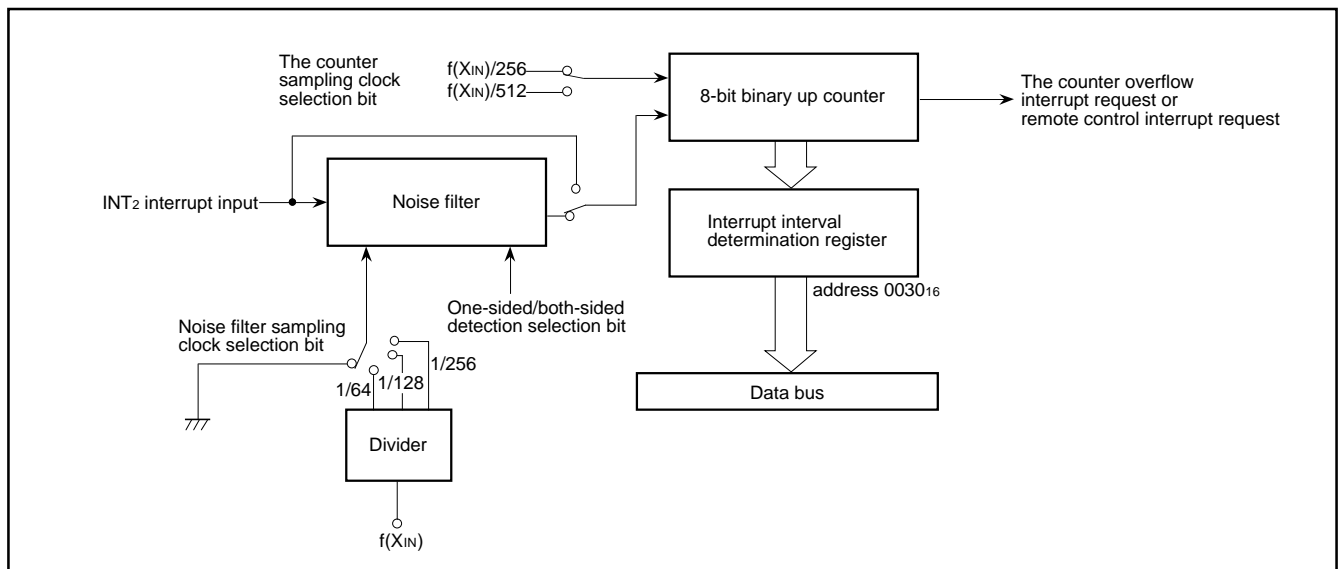


Fig. DE-1 Block diagram of interrupt interval datermination circuit

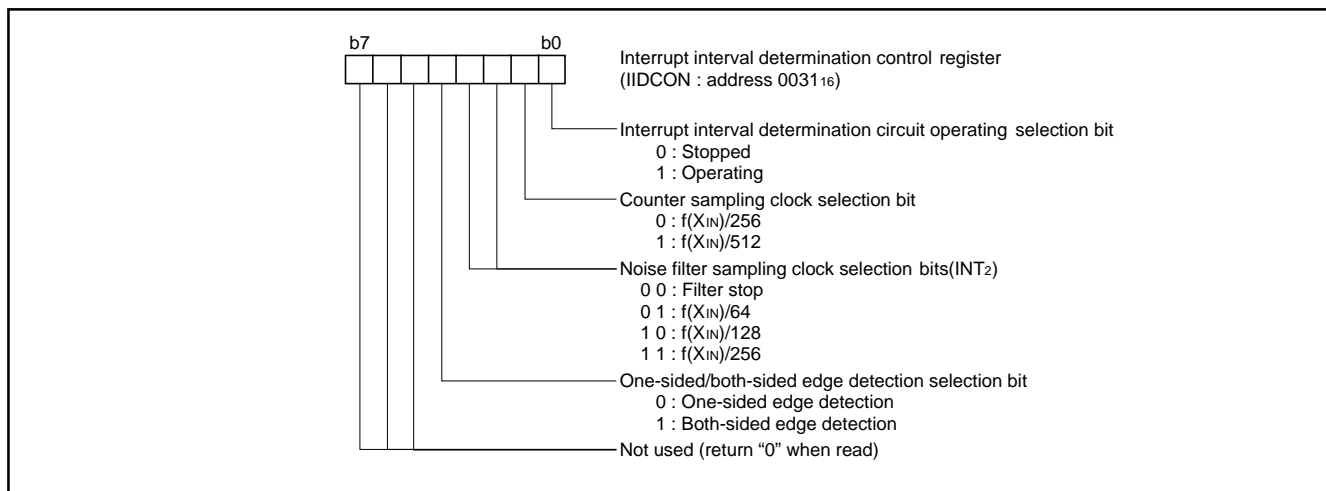


Fig. DE-2 Structure of interrupt interval determination control register

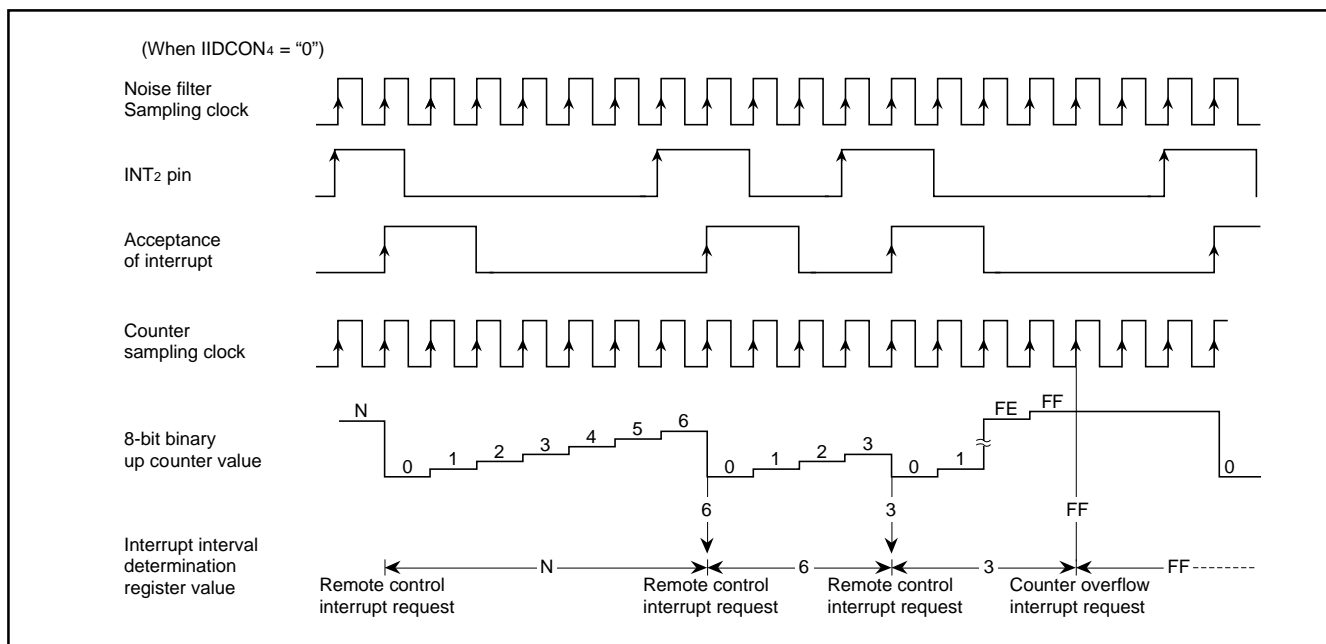


Fig. DE-3 Interrupt interval determination operation example (at rising edge active)

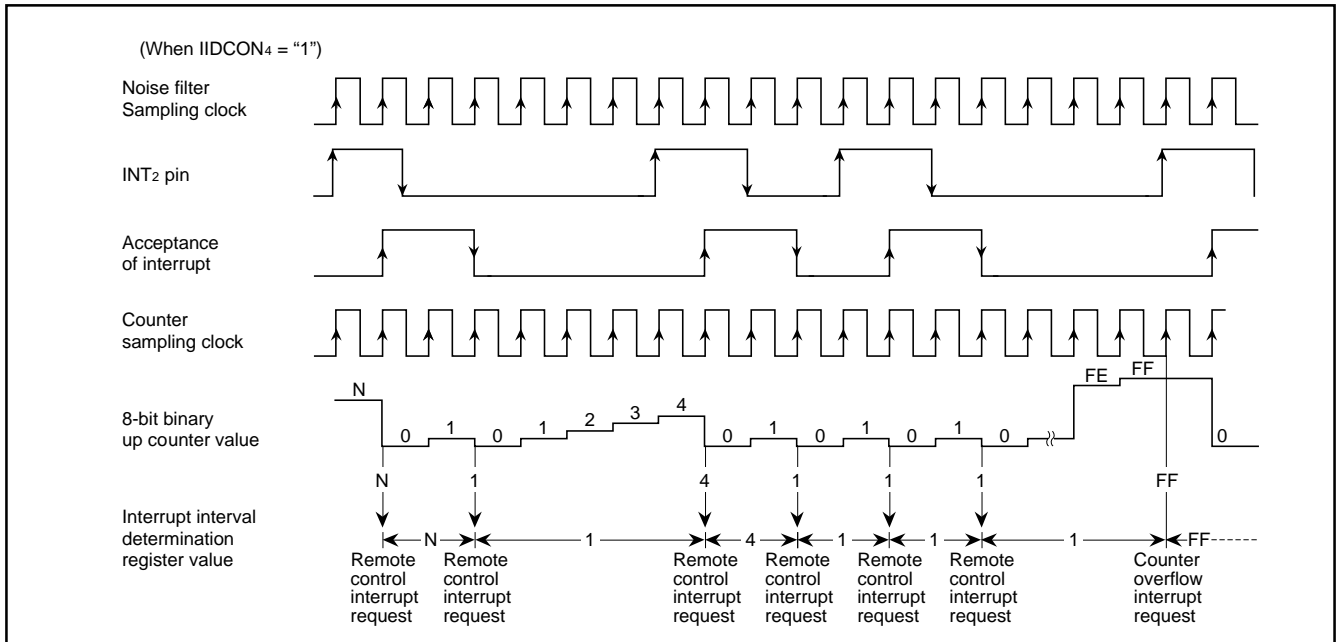


Fig. DE-4 Interrupt interval determination operation example (at both-sided edge active)

ZERO CROSS DETECTION CIRCUIT

The zero cross detection circuit compares the voltage applied to P45/INT1/ZCR pin and Vss. The result can be read from the zero cross detection circuit input bit (bit 7) of the zero cross detection control register. It is set to "1" when the input voltage is higher than Vss and to "0" when it is lower than Vss. The input signal to P45/INT1/ZCR pin can select to either pass through the zero cross detection comparator or not to do.

When using 100 V AC as input signal, insert an external circuit between it and P45/INT1/ZCR pin. Set the input current limiting resistors used in the external circuit to a value which satisfies the absolute maximum rating of port P45.

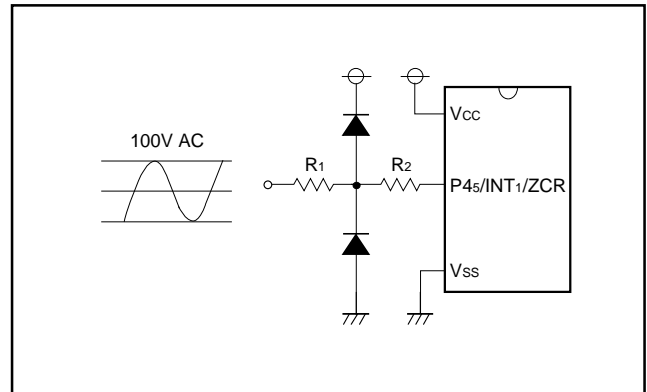


Fig. JE-1 External circuit example for zero cross detection

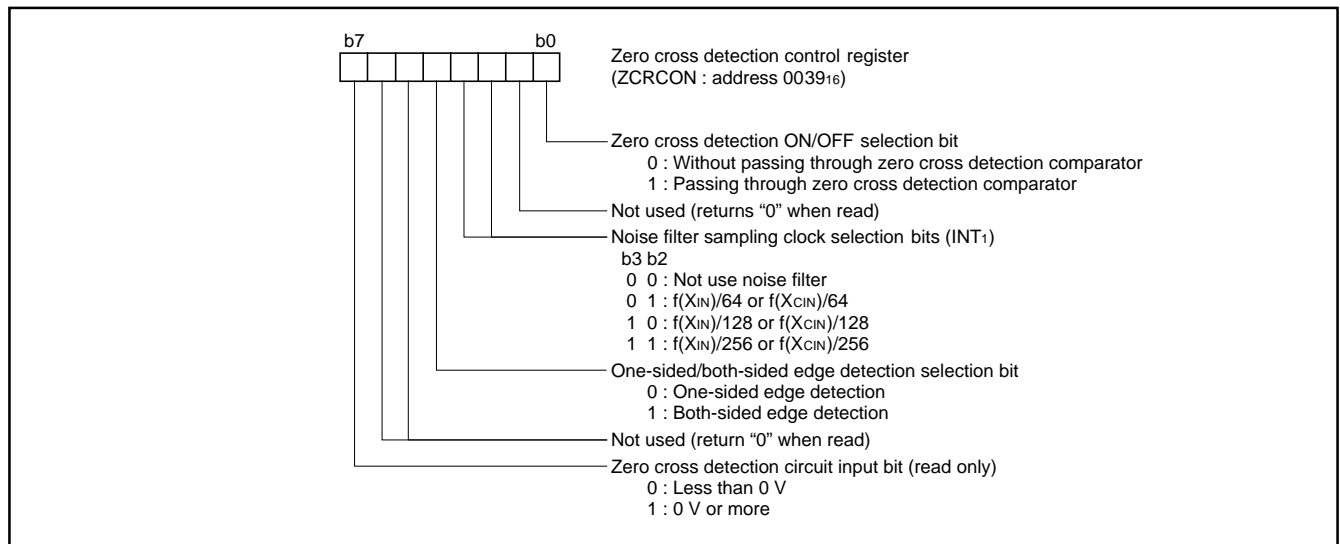


Fig. JE-2 Structure of zero cross detection control register

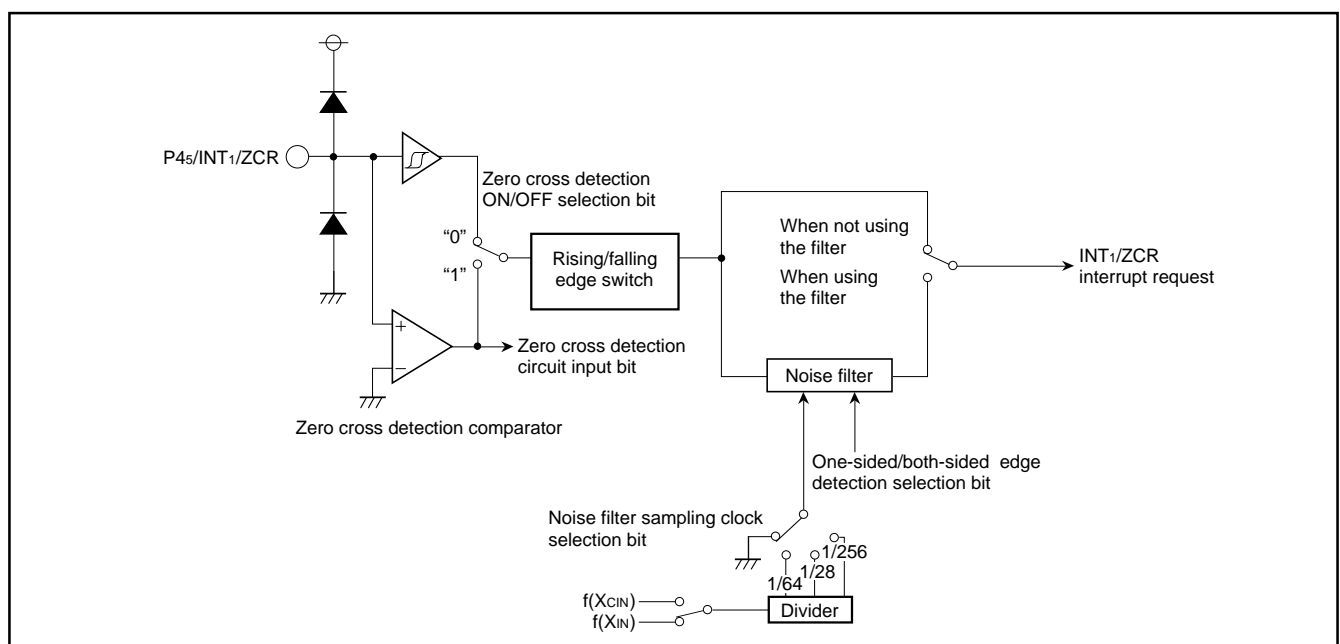


Fig. JE-3 Block diagram of zero cross detection circuit

NOISE FILTER

The noise filter uses a sampling clock to remove the noise component digitally from the input signal of P45/INT1/ZCR pin. The sampling clock can be selected from 8 μ s, 16 μ s, or 32 μ s (at $f(X_{IN}) = 8.38$ MHz) and this is used to change the noise component to be removed. It is also possible to generate an internal trigger and INT1/ZCR interrupt request directly without passing through

the noise filter. When passing through the noise filter, either both-sided edge detection or one-sided edge detection can be selected as the interrupt request generating source. The zero cross detection control register is used for this selection. Furthermore, switch between rising edge and falling edge is performed with the bit 1 of the interrupt edge selection register (address 003A16).

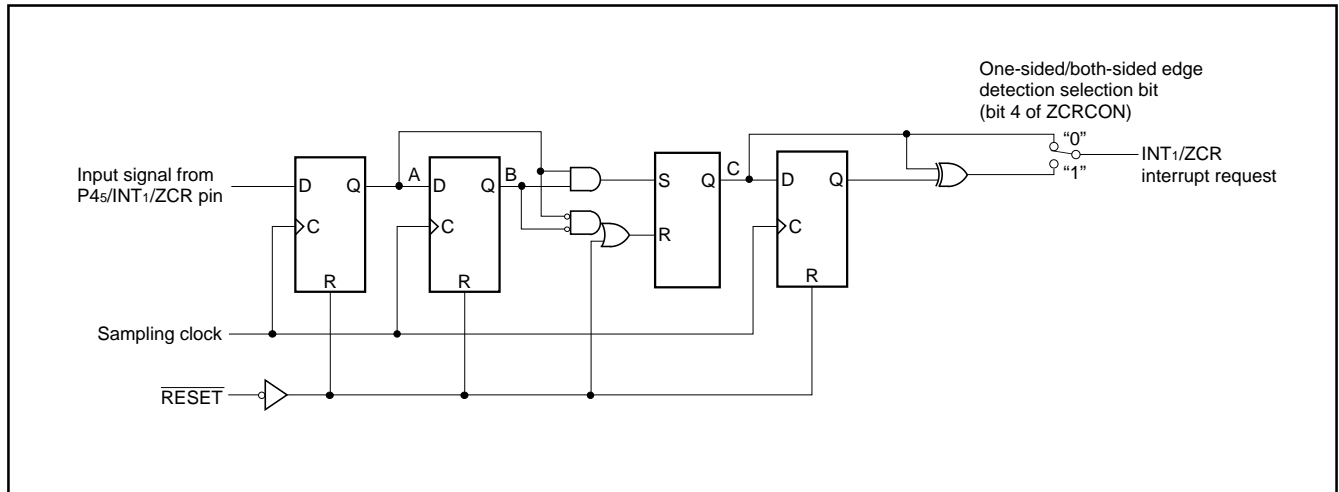


Fig. JE-4 Noise filter circuit diagram

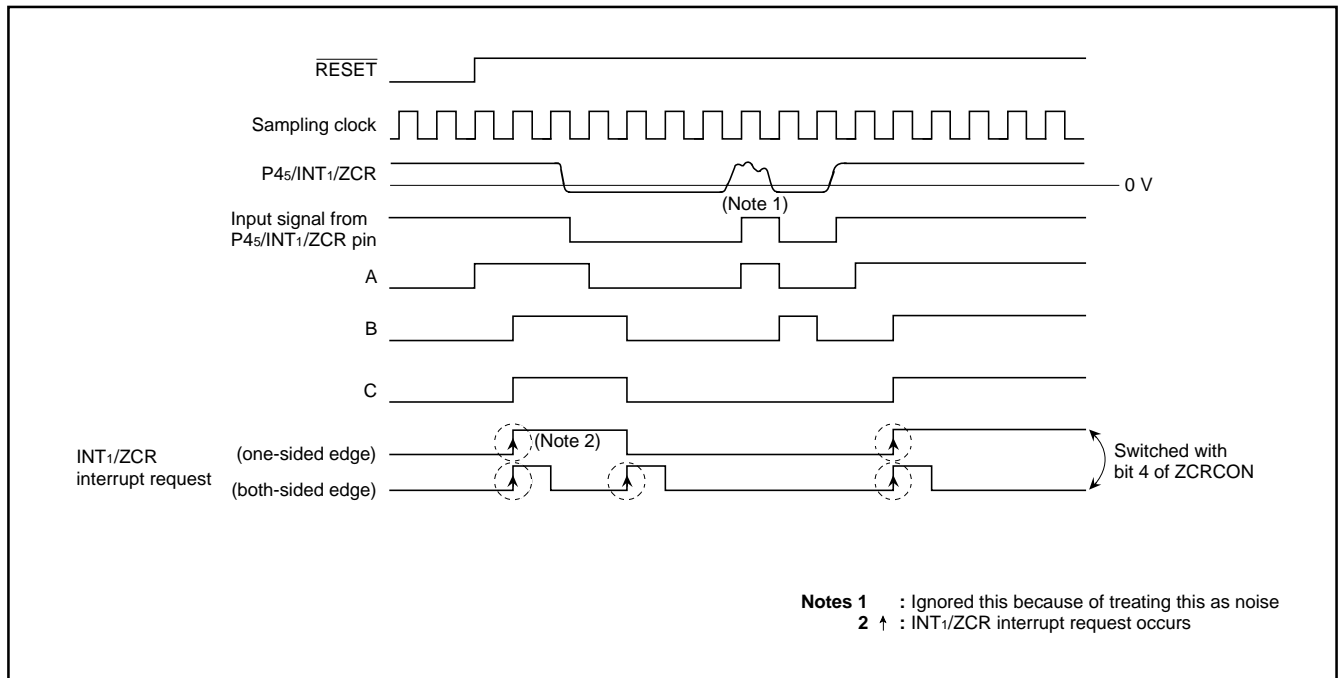


Fig. JE-5 Timing of noise filter circuit

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage should be between 2.8 V and 5.5 V, and X_{IN} oscillation is stable), reset is released. In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after about 4000 X_{IN} clock cycles (256 cycles of $f(X_{\text{IN}})/16$) are completed. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order) and address FFFC_{16} (low-order). Make sure that the reset input voltage is 0.5 V or less for 2.8 V of V_{CC} .

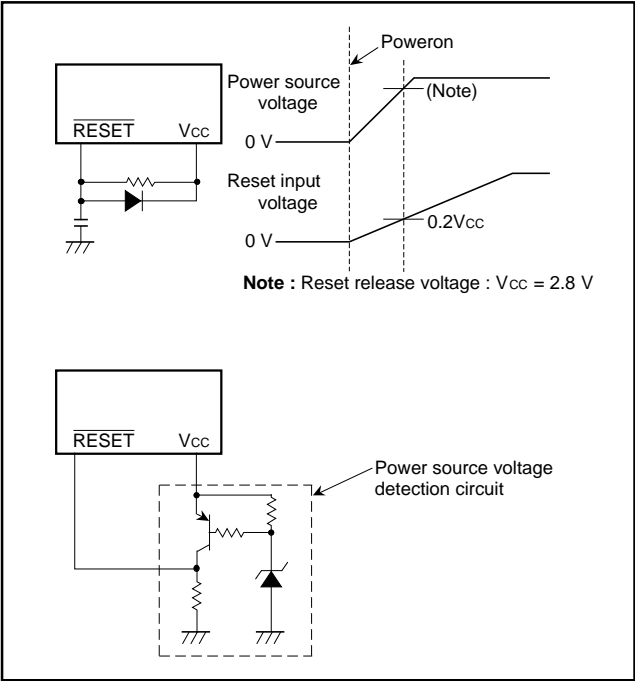


Fig. VB-2 Example of reset circuit

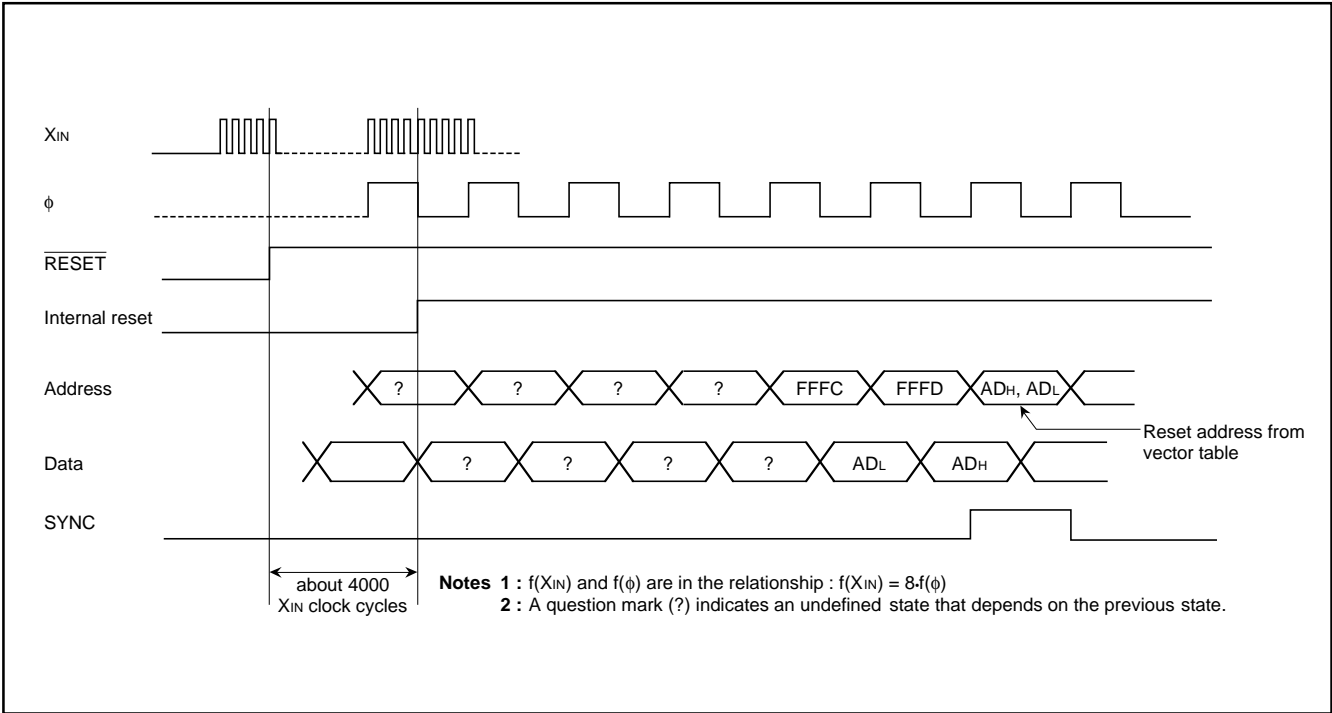


Fig. VB-2 Reset sequence

	Address	Register contents		Address	Register contents
(1) Port P0	(0000 ₁₆)...	00 ₁₆	(31) Timer 6	(0025 ₁₆)...	FF ₁₆
(2) Port P1	(0002 ₁₆)...	00 ₁₆	(32) Timer 12 mode register	(0028 ₁₆)...	00 ₁₆
(3) Port P2	(0004 ₁₆)...	00 ₁₆	(33) Timer 34 mode register	(0029 ₁₆)...	00 ₁₆
(4) Port P2 direction register	(0005 ₁₆)...	0F ₁₆	(34) Timer 56 mode register	(002A ₁₆)...	00 ₁₆
(5) Port P3	(0006 ₁₆)...	00 ₁₆	(35) D-A conversion register	(002B ₁₆)...	00 ₁₆
(6) Port P4	(0008 ₁₆)...	00 ₁₆	(36) AD/DA control register	(002C ₁₆)...	10 ₁₆
(7) Port P4 direction register	(0009 ₁₆)...	00 ₁₆	(37) Interrupt interval determination	(0031 ₁₆)...	00 ₁₆
(8) Port P5	(000A ₁₆)...	00 ₁₆	control register		
(9) Port P5 direction register	(000B ₁₆)...	00 ₁₆	(38) Port P0 segment/digit	(0032 ₁₆)...	00 ₁₆
(10) Port P6	(000C ₁₆)...	00 ₁₆	switch register		
(11) Port P6 direction register	(000D ₁₆)...	00 ₁₆	(39) Port P2 digit/port switching	(0033 ₁₆)...	00 ₁₆
(12) Port P7	(000E ₁₆)...	00 ₁₆	register		
(13) Port P7 direction register	(000F ₁₆)...	00 ₁₆	(40) Port P8 segment/port	(0034 ₁₆)...	00 ₁₆
(14) Port P8	(0010 ₁₆)...	00 ₁₆	switch register		
(15) Port P8 direction register	(0011 ₁₆)...	00 ₁₆	(41) Port PA segment/port switch	(0035 ₁₆)...	00 ₁₆
(16) Port P9	(0012 ₁₆)...	00 ₁₆	(42) FLDC mode register 1	(0036 ₁₆)...	00 ₁₆
(17) Port PA	(0014 ₁₆)...	00 ₁₆	(43) FLDC mode register 2	(0037 ₁₆)...	00 ₁₆
(18) Port PA direction register	(0015 ₁₆)...	00 ₁₆	(44) Zero cross detection control	(0039 ₁₆)...	00 ₁₆
(19) Port PB	(0016 ₁₆)...	00 ₁₆	register		
(20) Port PB direction register	(0017 ₁₆)...	00 ₁₆	(45) Interrupt edge selection register	(003A ₁₆)...	00 ₁₆
(21) Serial I/O1 control register	(0019 ₁₆)...	00 ₁₆	(46) CPU mode register	(003B ₁₆)...	0 1 0 0 1 0 0 0
(22) Serial I/O automatic transfer	(001A ₁₆)...	00 ₁₆	(47) Interrupt request register 1	(003C ₁₆)...	00 ₁₆
control register			(48) Interrupt request register 2	(003D ₁₆)...	00 ₁₆
(23) Serial I/O automatic transfer	(001C ₁₆)...	00 ₁₆	(49) Interrupt control register 1	(003E ₁₆)...	00 ₁₆
interval register			(50) Interrupt control register 2	(003F ₁₆)...	00 ₁₆
(24) Serial I/O2 control register	(001D ₁₆)...	00 ₁₆	(51) Processor status register	(PS)...	X X X X X 1 X X
(25) Serial I/O3 control register	(001E ₁₆)...	00 ₁₆	(52) Program counter	(PC _H)...	Contents of address FFFD ₁₆
(26) Timer 1	(0020 ₁₆)...	FF ₁₆		(PC _L)...	Contents of address FFFC ₁₆
(27) Timer 2	(0021 ₁₆)...	01 ₁₆			
(28) Timer 3	(0022 ₁₆)...	FF ₁₆			
(29) Timer 4	(0023 ₁₆)...	FF ₁₆			
(30) Timer 5	(0024 ₁₆)...	FF ₁₆			

Note : X : Undefined
The contents of all other registers and RAM are undefined at reset, so set their initial values.

Fig. VB-3 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3819 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

Immediately after poweron, only the XIN oscillation circuit starts oscillation, and XCIN and XCOUT pins function as I/O ports.

Frequency Control

Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

High-speed mode

The internal clock ϕ is half the frequency of XIN.

Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

Note : If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the XCIN oscillation to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(XIN) > 3 \cdot f(XCIN)$.

Low-power dissipation mode

When stopping the main clock XIN in the low-speed mode, the low-power dissipation operation starts. To stop the main clock, set the bit 5 of the CPU mode register to "1". When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

The low-power dissipation operation 200 μ A or less (at $f(XIN) = 32$ kHz) can be realized by reducing the XCIN–XCOUT drivability. To reduce the XCIN–XCOUT drivability, clear the bit 3 of the CPU mode register to "0". At reset or when executing the STP instruction, this bit is set to "1" and strong drivability is selected to help the oscillation to start.

Oscillation Control

Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116". Either XIN or XCIN divided by 16 is input to timer 1, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction.

Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 1 underflows. When using an external resonator, it is necessary for oscillating to stabilize.

Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

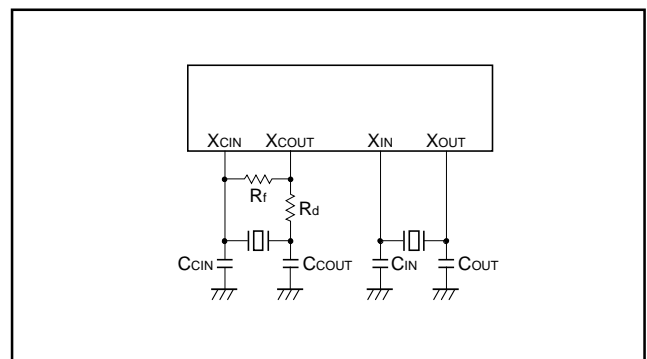


Fig. WA-1 Ceramic resonator external circuit

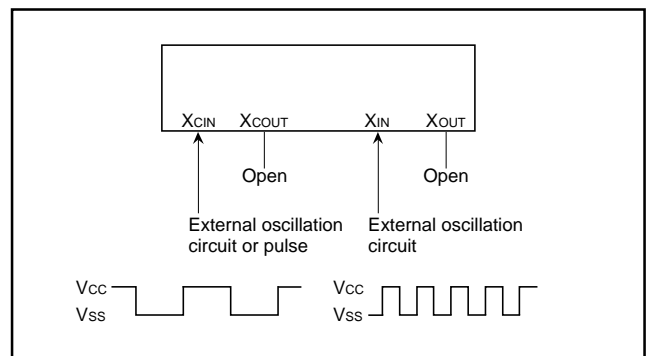
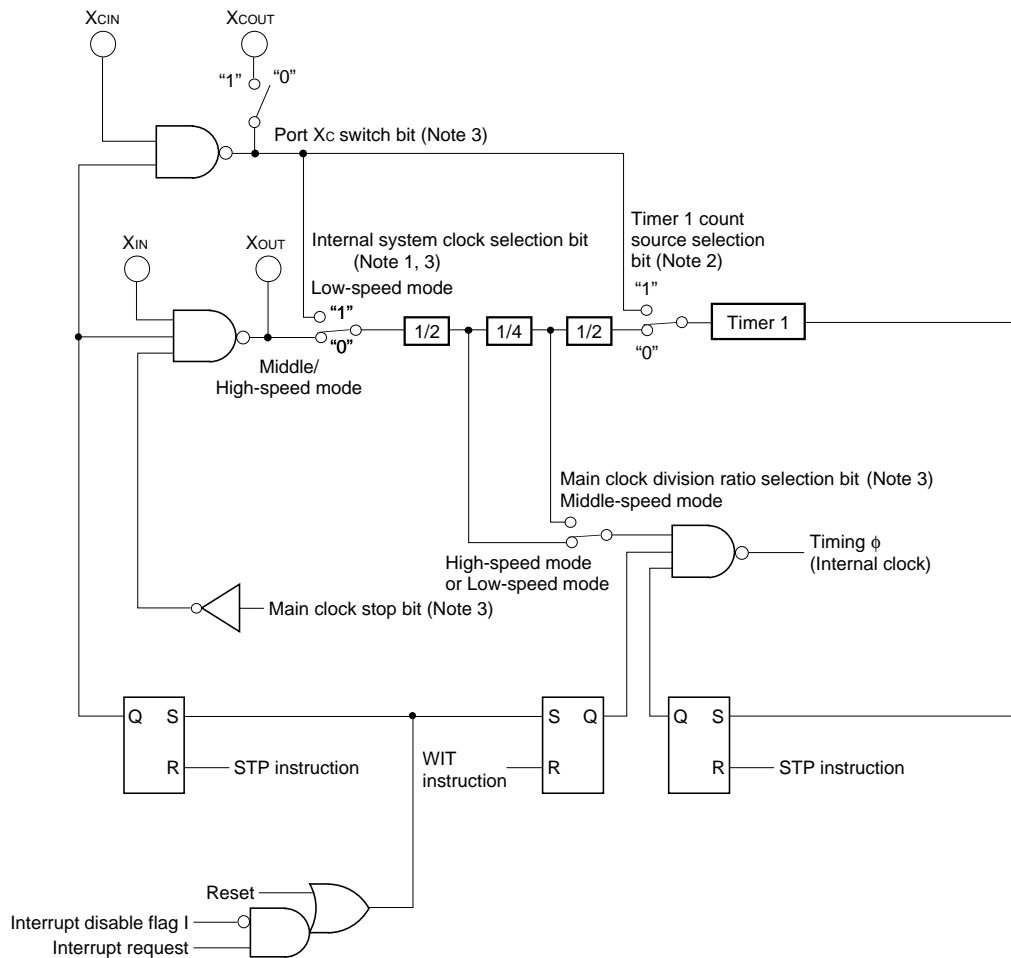


Fig. WA-2 External clock input circuit



Notes 1 : When selecting the low-speed mode, set the port Xc switch bit to "1".
 2 : Refer to the structure of timer 12 mode register.
 3 : Refer to the structure of CPU mode register (next page).

Fig. WA-3 Clock generating circuit block diagram

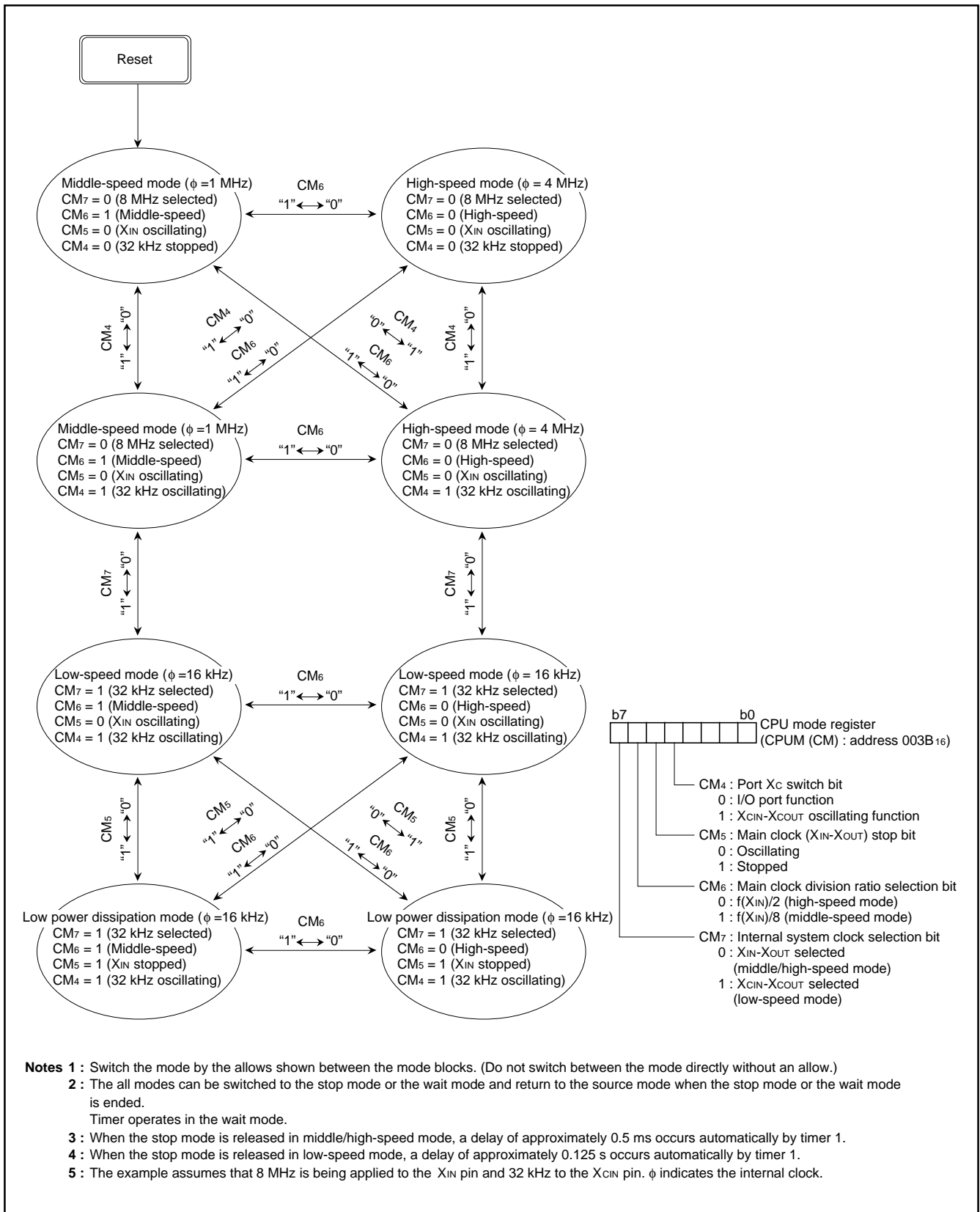


Fig. WA-4 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flag are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- the data transfer instruction (LDA, etc.)
- the operation instruction when the index X mode flag (T) is "1"
- the addressing mode which uses the value of a direction register as an index
- the bit-test instruction (BBC or BBS, etc.) to a direction register
- the read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.

When using the internal clock, set the synchronous clock to internal clock, then clear the serial I/O interrupt request bit before executing a serial I/O transfer and serial I/O automatic transfer.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(XIN)$ is 500 kHz or more during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions. The frequency of the internal clock ϕ is half of the XIN or $XCIN$ frequency.

At the STP Instruction Release

At the STP instruction release, all bits of the timer 12 mode register are cleared.

The XCOUT drivability selection bit (the CPU mode register) is set to "1" (high drive) in order to start oscillating.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mask Specification Form
- (3) Data to be written to ROM, in EPROM form (three identical copies)

PROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Package	Name of Programming Adapter
100P6S-A	PCA4738F-100A
100D0	PCA4738L-100A

Set the address of PROM programmer in the user ROM area. The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after writing, the procedure shown in Figure XC-1 is recommended to verify programming.

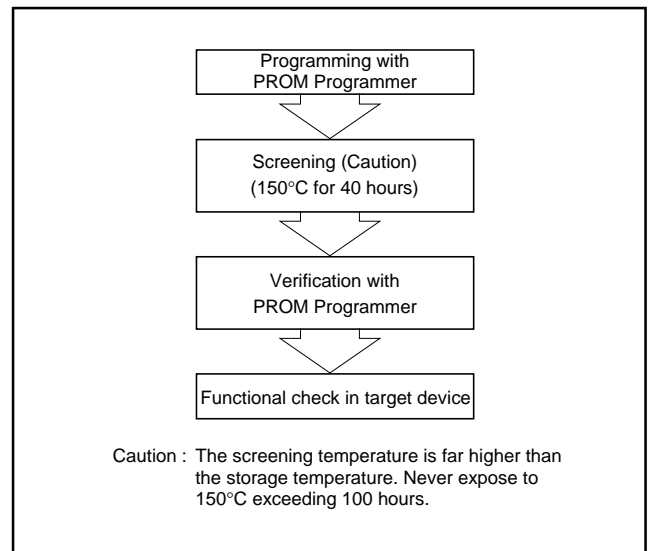


Fig. XC-1 Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	All voltages are based on VSS. Output transistors are cut off.	−0.3 to 7.0	V
VEE	Pull-down power source voltage		VCC−40 to VCC+0.3	V
VI	Input voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3		−0.3 to VCC +0.3	V
VI	Input voltage P40, P45		−0.3 to VCC +0.3	V
VI	Input voltage P80–P87, PA0–PA7		VCC−40 to VCC+0.3	V
VI	Input voltage RESET, XIN		−0.3 to VCC +0.3	V
VI	Input voltage XCIN		−0.3 to VCC +0.3	V
VO	Output voltage P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7		VCC−40 to VCC+0.3	V
VO	Output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3, XOUT, XCOUT		−0.3 to VCC +0.3	V
Pd	Power dissipation	Ta = 25°C	600	mW
Topr	Operating temperature		−10 to 85	°C
Tstg	Storage temperature		−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (VCC = 4.0 to 5.5 V, Ta = −10 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage	High-speed mode	4.0	5.0	5.5	V
		Middle/Low-speed mode	2.8	5.0	5.5	V
VSS	Power source voltage			0		V
VEE	Pull-down power source voltage		VCC−38		VCC	V
VREF	Analog reference voltage (when using A-D converter)		2.0		VCC	V
	Analog reference voltage (when using D-A converter)		3.0		VCC	V
AVSS	Analog power source voltage			0		V
VIA	Analog input voltage AN0–AN15		0		VCC	V
VIH	"H" input voltage	P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	0.75VCC		VCC	V
VIH	"H" input voltage	P24–P27	0.4VCC		VCC	V
VIH	"H" input voltage	P80–P87, PA0–PA7	0.8VCC		VCC	V
VIH	"H" input voltage	RESET	0.8VCC		VCC	V
VIH	"H" input voltage	XIN, XCIN	0.8VCC		VCC	V
VIL	"L" input voltage	P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	0		0.25VCC	V
VIL	"L" input voltage	P24–P27	0		0.16VCC	V
VIL	"L" input voltage	P80–P87, PA0–PA7	0		0.2VCC	V
VIL	"L" input voltage	RESET	0		0.2VCC	V
VIL	"L" input voltage	XIN, XCIN	0		0.2VCC	V

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH}(\text{peak})$	"H" total peak output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37, P80–P87, P90–P97, PA6, PA7			–240	mA
	"H" total peak output current (Note 1) P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PA0–PA5, PB0–PB3			–60	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			100	mA
$\Sigma I_{OH}(\text{avg})$	"H" total average output current (Note 1) P00–P07, P10–P17, P20–P27, P30–P37, P80–P87, P90–P97, PA6, PA7			–120	mA
	"H" total average output current (Note 1) P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PA0–PA5, PB0–PB3			–30	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			50	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7			–40	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			–10	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 3) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			10	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7			–18	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			–5.0	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3			5.0	mA
$f(\text{CNTR}0)$ $f(\text{CNTR}1)$	Clock input frequency for timers 2 and 4 (duty cycle 50%)			250	kHz
$f(\text{XIN})$	Main clock input oscillation frequency (Note 4)			8.4	MHz
$f(\text{XCIN})$	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Notes 1 : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2 : The peak output current is the peak current flowing in each port.

3 : The average output current is an average value measured over 100 ms.

4 : When the oscillation frequency has a 50% duty cycle.

5 : When using the microcomputer in low-speed operation mode, set the sub-clock input oscillation frequency on condition that $f(\text{XCIN}) < f(\text{XIN})/3$.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7	$I_{OH} = -18$ mA	$V_{CC} - 2.0$			V
V_{OH}	"H" output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$I_{OH} = -10$ mA	$V_{CC} - 2.0$			V
V_{OL}	"L" output voltage P24–P27, P41–P44, P46, P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$I_{OL} = 10$ mA			2.0	V
$V_{T+} - V_{T-}$	Hysteresis $\overline{INT0} - \overline{INT4}$, SIN1, SIN2, SIN3, SCLK11, SCLK2, SCLK3, CS, CNTR0, CNTR1	When using a non-port function		0.4		V
$V_{T+} - V_{T-}$	Hysteresis \overline{RESET} , XIN			0.5		V
$V_{T+} - V_{T-}$	Hysteresis XCIN			0.5		V
I_H	"H" input current P24–P27, P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$V_i = V_{CC}$			5.0	μA
I_H	"H" input current P80–P87, PA0–PA7 (Note)	$V_i = V_{CC}$			5.0	μA
I_H	"H" input current \overline{RESET} , XCIN	$V_i = V_{CC}$			5.0	μA
I_H	"H" input current XIN	$V_i = V_{CC}$		4.0		μA
I_L	"L" input current P24–P27, P40–P47, P50–P57, P60–P67, P70–P77, PB0–PB3	$V_i = V_{SS}$			-5.0	μA
I_L	"L" input current P80–P87, PA0–PA7 (Note)	$V_i = V_{SS}$			-5.0	μA
I_L	"L" input current \overline{RESET} , XCIN	$V_i = V_{SS}$			-5.0	μA
I_L	"L" input current XIN	$V_i = V_{SS}$		-4.0		μA
I_{LOAD}	Output load current P00–P07, P10–P17, P20–P23, P30–P37, P90–P97	$V_{EE} = V_{CC} - 36$ V, $V_{OL} = V_{CC}$, Output transistors "off"	150	500	900	μA
I_{LEAK}	Output leakage current P00–P07, P10–P17, P20–P23, P30–P37, P80–P87, P90–P97, PA0–PA7	$V_{EE} = V_{CC} - 38$ V, $V_{OL} = V_{CC} - 38$ V, Output transistors "off"			-10	μA
VRAM	RAM hold voltage	When clock is stopped	2		5.5	V

Note : Except when reading ports P8 or PA.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC}	Power source current	<ul style="list-style-type: none"> High-speed mode f(X_{IN}) = 8.4 MHz f(X_{CIN}) = 32 kHz Output transistors "off" 		7.5	15	mA
		<ul style="list-style-type: none"> High-speed mode f(X_{IN}) = 8.4 MHz (in WIT state) f(X_{CIN}) = 32 kHz Output transistors "off" 		1		mA
		<ul style="list-style-type: none"> Middle-speed mode f(X_{IN}) = 8.4 MHz f(X_{CIN}) = stopped Output transistors "off" 		3		mA
		<ul style="list-style-type: none"> Middle-speed mode f(X_{IN}) = 8.4 MHz (in WIT state) f(X_{CIN}) = stopped Output transistors "off" 		1		mA
		<ul style="list-style-type: none"> Low-speed mode f(X_{IN}) = stopped, f(X_{CIN}) = 32 kHz Low-power dissipation mode set (CM₃) = 0 Output transistors "off" 		60	200	μA
		<ul style="list-style-type: none"> Low-speed mode f(X_{IN}) = stopped f(X_{CIN}) = 32 kHz (in WIT state) Low-power dissipation mode set (CM₃) = 0 Output transistors "off" 		20	40	μA
		Increase at A-D converter operating f(X _{IN}) = 8.4 MHz		0.6		mA
		Increase at zero cross detection (P ₄₅ = V _{CC})		1		mA
		All oscillation stopped (in STP state)	T _a = 25°C	0.1	1	μA
		Output transistors "off"	T _a = 85°C		10	

ZERO CROSS DETECTION INPUT CHARACTERISTICS

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
fZCR	Input frequency of zero cross detection			50, 60	1000	Hz
ΔVT	Voltage error of zero cross detection distinction	50 Hz or 60 Hz	-100	0	100	mV

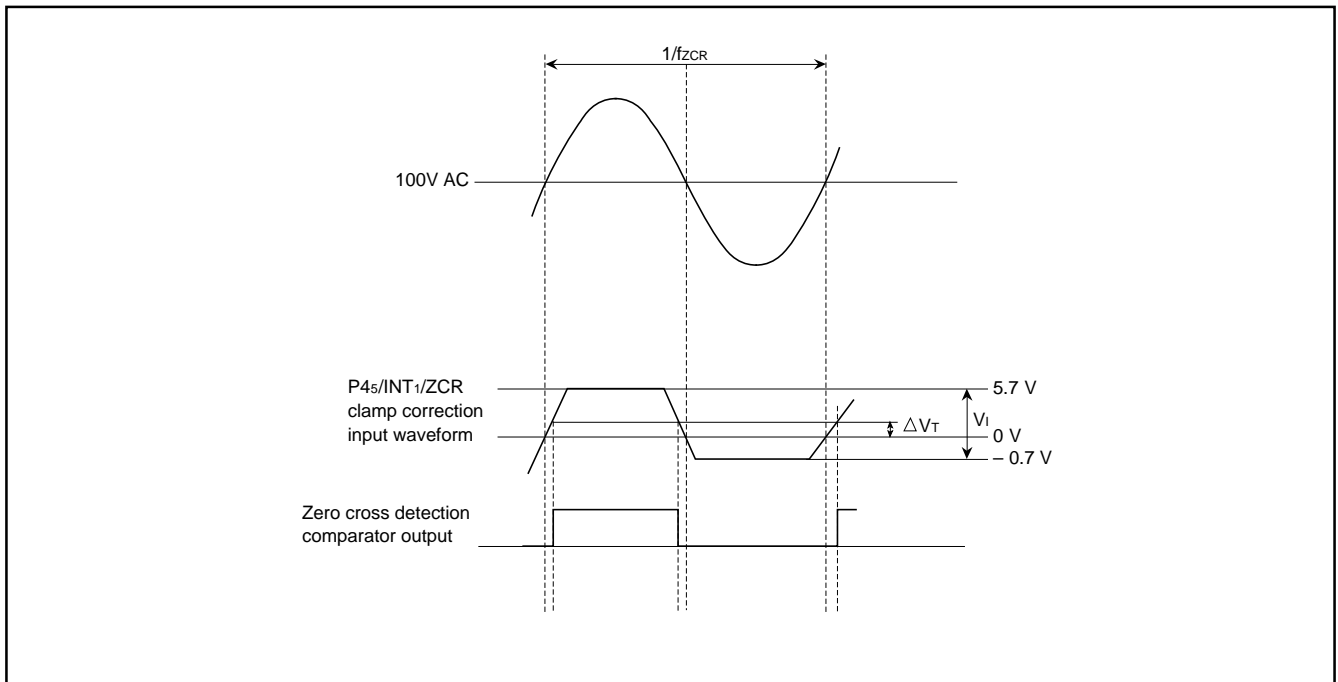


Fig. ZA-1 Zero cross detection input characteristics

A-D CONVERTER CHARACTERISTICS

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -10 to 85°C, high-speed operation mode f(XIN) = 500 kHz to 8.4 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	VCC = VREF = 5.12 V		±1	±2.5	LSB
TCONV	Conversion time		49		50	tc (φ)
IVREF	Reference power source input current	VREF = 5 V	50	150	200	μA
IIA	Analog port input current			0.5	5.0	μA
RLADDER	Ladder resistor			35		kΩ

D-A CONVERTER CHARACTERISTICS

(VCC = 4.0 to 5.5 V, VSS = AVSS = 0 V, VREF = 3.0 to VCC, Ta = -10 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	VCC = 4.0 to 5.5 V			1.0	%
		VCC = 3.0 to 5.5 V			2.5	%
Tsu	Setting time				3	μs
Ro	Output resistor		1	2.5	4	kΩ
IVREF	Reference power source input current (Note)				3.2	mA

Note : Exclude currents flowing through the A-D converter ladder resistor

TIMING REQUIREMENTS ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\text{RESET})$	Reset input "L" pulse width	2.0			μs
$t_C(X_{IN})$	Main clock input cycle time (X_{IN} input)	119			ns
$t_{WH}(X_{IN})$	Main clock input "H" pulse width	30			ns
$t_{WL}(X_{IN})$	Main clock input "L" pulse width	30			ns
$t_C(X_{CIN})$	Sub-clock input cycle time (X_{CIN} input)	20			μs
$t_{WH}(X_{CIN})$	Sub-clock input "H" pulse width	5.0			μs
$t_{WL}(X_{CIN})$	Sub-clock input "L" pulse width	5.0			μs
$t_C(\text{CNTR})$	CNTR0, CNTR1 input cycle time	4.0			μs
$t_{WH}(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	1.6			μs
$t_{WL}(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	1.6			μs
$t_{WH}(\text{INT})$	INT0–INT4 input "H" pulse width	80			ns
$t_{WL}(\text{INT})$	INT0–INT4 input "L" pulse width	80			ns
$t_C(\text{SCLK})$	Serial I/O clock input cycle time	1.0			μs
$t_{WH}(\text{SCLK})$	Serial I/O clock input "H" pulse width	400			ns
$t_{WL}(\text{SCLK})$	Serial I/O clock input "L" pulse width	400			ns
$t_{su}(\text{SCLK} \rightarrow \text{SIN})$	Serial I/O input setup time	200			ns
$t_h(\text{SCLK} \rightarrow \text{SIN})$	Serial I/O input hold time	200			ns

SWITCHING CHARACTERISTICS ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -10$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$C_L = 100$ pF	$t_C(\text{SCLK}) / 2 \sim 160$			ns
$t_{WL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$C_L = 100$ pF	$t_C(\text{SCLK}) / 2 \sim 160$			ns
$t_d(\text{SCLK} \rightarrow \text{SOUT})$	Serial I/O output delay time				$0.2t_C(\text{SCLK})$	ns
$t_v(\text{SCLK} \rightarrow \text{SOUT})$	Serial I/O output hold time		0			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time	$C_L = 100$ pF			40	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time	$C_L = 100$ pF			40	ns
$t_r(\text{Pch-strg})$	High-breakdown-voltage P-channel open-drain output rising time (Note 1)	$C_L = 100$ pF $V_{EE} = V_{CC} - 36$ V		55		ns
$t_f(\text{Pch-weak})$	High-breakdown-voltage P-channel open-drain output falling time (Note 2)	$C_L = 100$ pF $V_{EE} = V_{CC} - 36$ V		1.8		μs

Notes 1: When the bit 7 of the FLDC mode register 1 (address 003616) is at "0".

2: When the bit 7 of the FLDC mode register 1 (address 003616) is at "1".

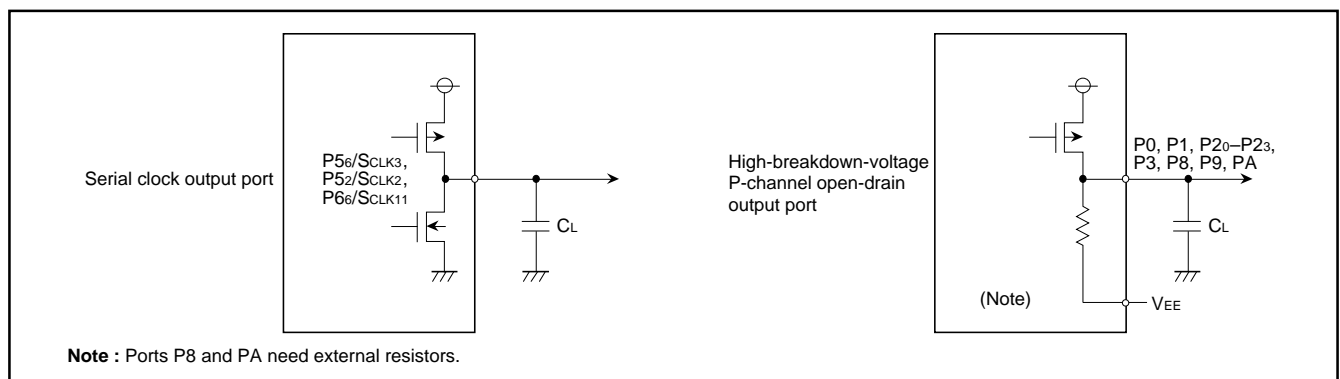
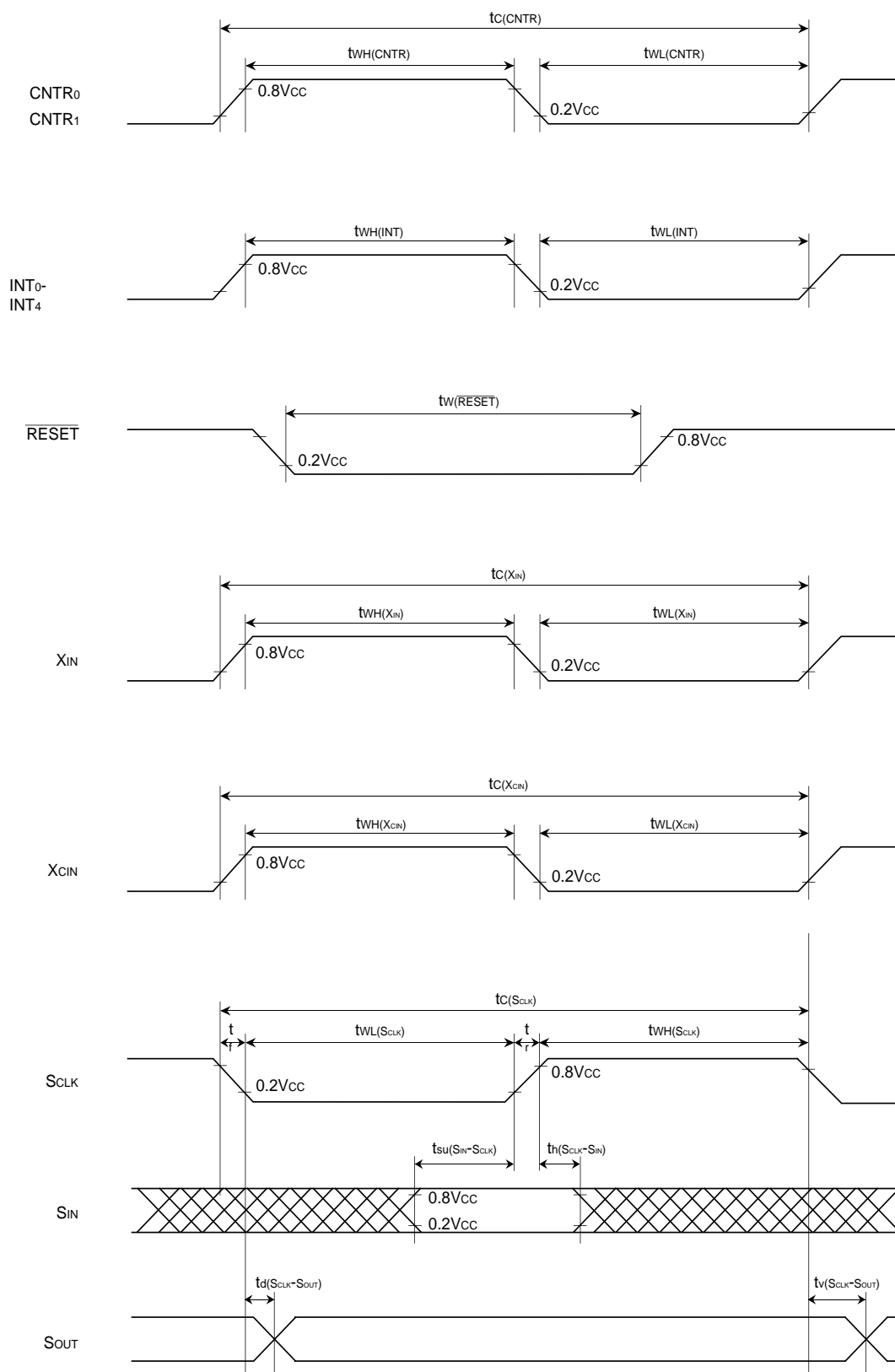


Fig. ZA-2 Circuit for measuring output switching characteristics

TIMING DIAGRAM



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