

<b>HIGH PERFORMANCE</b>	<b>50</b>	<b>60</b>	<b>70</b>
Max. $\overline{\text{RAS}}$ Access Time, ( $t_{\text{RAC}}$ )	50 ns	60 ns	70 ns
Max. Column Address Access Time, ( $t_{\text{CAA}}$ )	25 ns	30 ns	35 ns
Min. Extended Data Out Page Mode Cycle Time, ( $t_{\text{PC}}$ )	20 ns	25 ns	30 ns
Min. Read/Write Cycle Time, ( $t_{\text{RC}}$ )	84 ns	104 ns	124 ns

**Features**

- 1M x 16-bit organization
- EDO Page Mode for a sustained data rate of 50 MHz
- $\overline{\text{RAS}}$  access time: 50, 60, 70 ns
- Dual  $\overline{\text{CAS}}$  Inputs
- Low power dissipation
- Read-Modify-Write,  $\overline{\text{RAS}}$ -Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh, Hidden Refresh, and Self Refresh.
- Refresh Interval: 1024 cycles/16 ms
- Available in 42-pin 400 mil SOJ and 50/44-pin 400 mil TSOP-II
- Single +3.3 V  $\pm 0.3$  V Power Supply
- TTL Interface

**Description**

The V53C318165A is a 1048576 x 16 bit high-performance CMOS dynamic random access memory. The V53C318165A offers Page mode operation with Extended Data Output. The V53C318165A has an symmetric address, 10-bit row and 10-bit column.

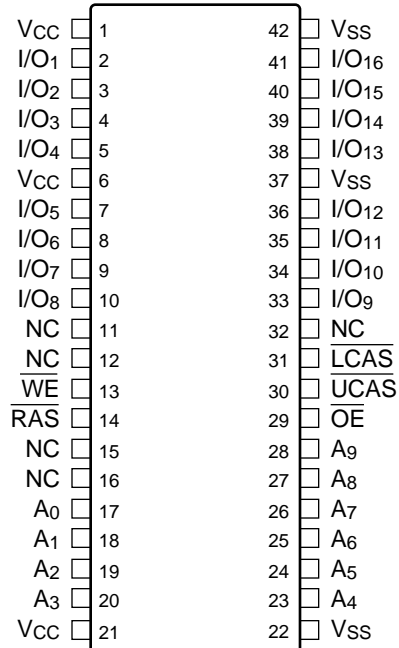
All inputs are TTL compatible. EDO Page Mode operation allows random access up to 1024 x 16 bits, within a page, with cycle times as short as 20ns.

These features make the V53C318165A ideally suited for a wide variety of high performance computer systems and peripheral applications.

**Device Usage Chart**

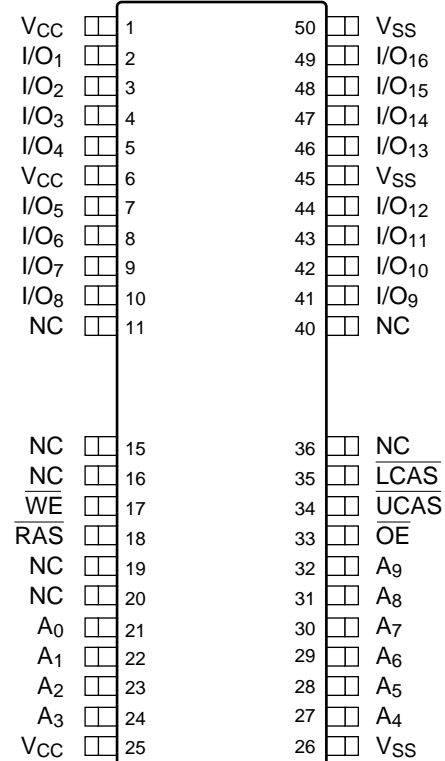
Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	K	T	50	60	70	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank

**42-Pin Plastic SOJ  
PIN CONFIGURATION  
Top View**



311816500-02

**50/44-Pin Plastic TSOP-II  
PIN CONFIGURATION  
Top View**



311816500-03

**Pin Names**

A <sub>0</sub> –A <sub>9</sub>	Row, Column Address Inputs
RAS	Row Address Strobe
UCAS	Column Address Strobe/Upper Byte Control
LCAS	Column Address Strobe/Lower Byte Control
WE	Write Enable
OE	Output Enable
I/O <sub>1</sub> –I/O <sub>16</sub>	Data Input, Output
V <sub>CC</sub>	+3.3V Supply
V <sub>SS</sub>	0V Supply
NC	No Connect

Description	Pkg.	Pin Count
SOJ	K	42
TSOP-II	T	50

**Absolute Maximum Ratings\***

Operating temperature range ..... 0 to 70 °C  
 Storage temperature range ..... -55 to 150 °C  
 Soldering temperature ..... 260 °C  
 Soldering time ..... 10 s  
 Input/output voltage .... -0.5 to min ( $V_{CC}+0.5$ , 4.6) V  
 Power supply voltage ..... -0.5V to 4.6 V  
 Power dissipation ..... 0.5 W  
 Data out current (short circuit) ..... 50 mA

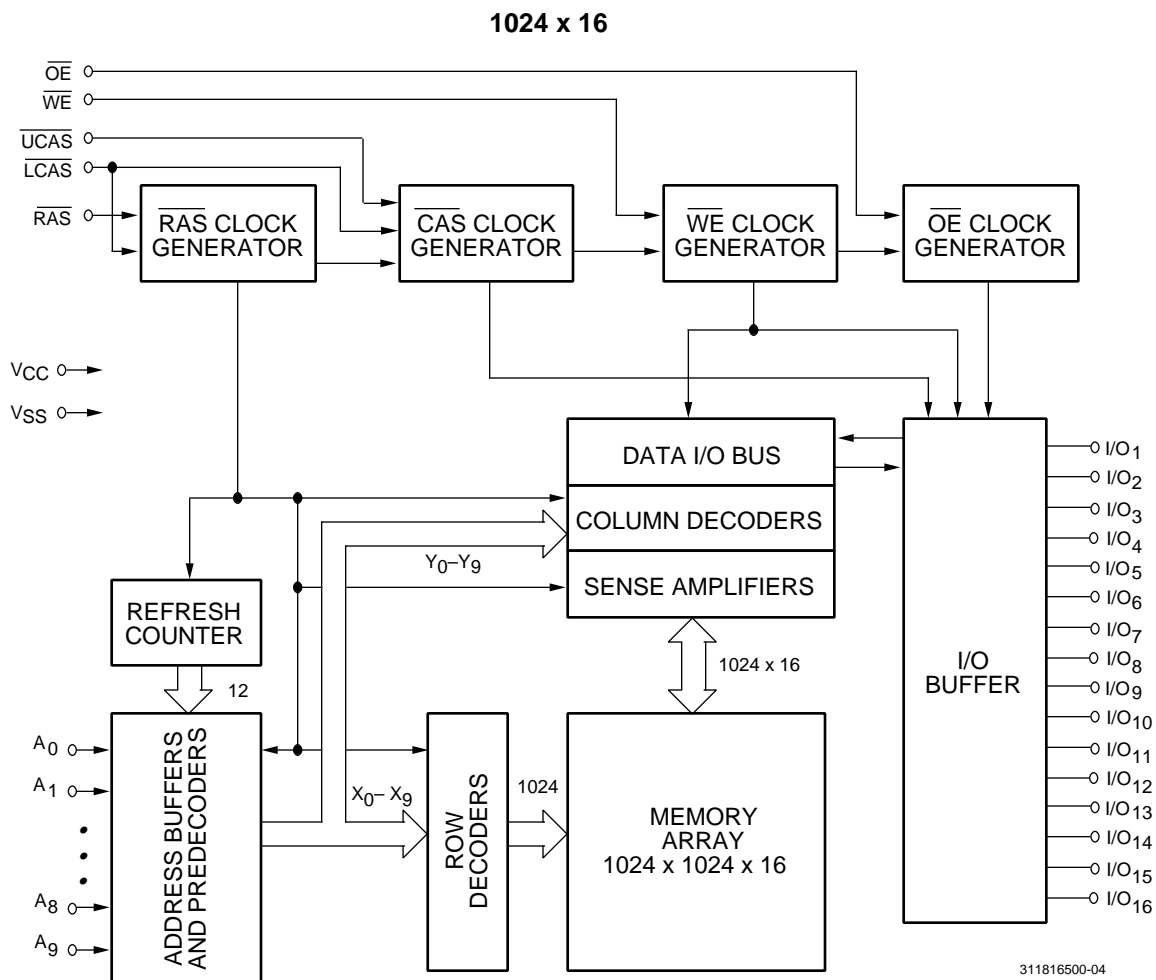
**\*Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

**Capacitance\***

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $f = 1 \text{ MHz}$

Symbol	Parameter	Min.	Max.	Unit
$C_{IN1}$	Address Input	—	5	pF
$C_{IN2}$	RAS, UCAS, LCAS, WE, OE	—	7	pF
$C_{OUT}$	Data Input/Output	—	7	pF

**\*Note:** Capacitance is sampled and not 100% tested.

**Block Diagram**

**DC and Operating Characteristics (1-2)**

$T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $t_T = 2\text{ ns}$ , unless otherwise specified.

Symbol	Parameter	Access Time	V53C318165A			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
$I_{LI}$	Input Leakage Current (any input pin)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{IN} \leq V_{CC} + 0.3\text{V}$	1
$I_{LO}$	Output Leakage Current (for High-Z State)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{OUT} \leq V_{CC} + 0.3\text{V}$ RAS, CAS at $V_{IH}$	1
$I_{CC1}$	$V_{CC}$ Supply Current, Operating	50			200	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 3, 4
		60			180			
		70			160			
$I_{CC2}$	$V_{CC}$ Supply Current, TTL Standby				2	mA	RAS, CAS at $V_{IH}$ other inputs $\geq V_{SS}$	
$I_{CC3}$	$V_{CC}$ Supply Current, RAS-Only Refresh	50			200	mA	$t_{RC} = t_{RC}(\text{min.})$	2, 4
		60			180			
		70			160			
$I_{CC4}$	$V_{CC}$ Supply Current, EDO Page Mode Operation	50			90	mA	Minimum Cycle	2, 3, 4
		60			75			
		70			60			
$I_{CC5}$	$V_{CC}$ Supply Current, CMOS Standby				1.0	mA	RAS $\geq V_{CC} - 0.2\text{ V}$ , CAS $\geq V_{CC} - 0.2\text{ V}$	1
$I_{CC6}$	Average Self Refresh Current CBR cycle with $t_{RAS} > t_{RASS} \text{ min.}$ , (L-version only) CAS held low, $\overline{WE} = V_{CC} - 0.2\text{V}$ , Address and $D_{IN} = V_{CC} - 0.2\text{V}$ or $0.2\text{V}$				1.0	mA		
$I_{CC7}$	$V_{CC}$ Supply Current, during CAS-before-RAS Refresh	50			200	mA	$t_{RC} = t_{RC}(\text{min})$	2, 4
		60			180			
		70			160			
$V_{IL}$	Input Low Voltage		-0.5		0.8	V		1
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.5$	V		1
$V_{OL}$	Output Low Voltage				0.4	V	$I_{OL} = 2\text{ mA}$	1
$V_{OH}$	Output High Voltage		2.4			V	$I_{OH} = -2\text{ mA}$	1

**AC Characteristics**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{V}$ ,  $t_r = 2\text{ns}$  unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	50		60		70		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	$t_{RL1RH1}$	$t_{RAS}$	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
2	$t_{RL2RL2}$	$t_{RC}$	Read or Write Cycle Time	84		104		124		ns	
3	$t_{RH2RL2}$	$t_{RP}$	$\overline{RAS}$ Precharge Time	30		40		50		ns	
4	$t_{RL1CH1}$	$t_{CSH}$	$\overline{CAS}$ Hold Time	40		50		60		ns	
5	$t_{CL1CH1}$	$t_{CAS}$	$\overline{CAS}$ Pulse Width	8	10K	10	10K	12	10K	ns	
6	$t_{RL1CL1}$	$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay	12	37	14	45	14	53	ns	
7	$t_{WH2CL2}$	$t_{RCS}$	Read Command Setup Time	0		0		0		ns	
8	$t_{AVRL2}$	$t_{ASR}$	Row Address Setup Time	0		0		0		ns	
9	$t_{RL1AX}$	$t_{RAH}$	Row Address Hold Time	8		10		10		ns	
10	$t_{AVCL2}$	$t_{ASC}$	Column Address Setup Time	0		0		0		ns	
11	$t_{CL1AX}$	$t_{CAH}$	Column Address Hold Time	8		10		12		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH}$	$\overline{RAS}$ Hold Time	13		15		17		ns	
13	$t_{CH2RL2}$	$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
14	$t_{CH2WX}$	$t_{RCH}$	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	9
15	$t_{RH2WX}$	$t_{RRH}$	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	9
16	$t_{CL1}$	$t_{COH}$	Output Hold after $\overline{CAS}$ LOW	5		5		5		ns	
17	$t_{GL1QV}$	$t_{OAC}$	Access Time from $\overline{OE}$		13		15		17	ns	
18	$t_{CL1QV}$	$t_{CAC}$	Access Time from $\overline{CAS}$		13		15		17	ns	7, 12
19	$t_{RL1QV}$	$t_{RAC}$	Access Time from $\overline{RAS}$		50		60		70	ns	7, 12
20	$t_{AVQV}$	$t_{CAA}$	Access Time from Column Address		25		30		35	ns	7, 13
21	$t_{CL1QX}$	$t_{CLZ}$	$\overline{CAS}$ to Low-Z Output	0		0		0		ns	7
22	$t_{CH2QX}$	$t_{OFF}$	Output Buffer Turnoff Delay	0	13	0	15	0	17	ns	
23	$t_{CL1QZ}$	$t_{DZC}$	Data to $\overline{CAS}$ Low Delay	0		0		0		ns	15
24	$t_{RL1AV}$	$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	10	25	12	30	12	35	ns	
25	$t_{GL2QZ}$	$t_{OEZ}$	Output Buffer Turnoff Delay from $\overline{OE}$	0	13	0	15	0	17	ns	8
26	$t_{WL1CH1}$	$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	13		15		17		ns	
27	$t_{WL1CL2}$	$t_{WCS}$	Write Command Setup Time	0		0		0		ns	11
28	$t_{CL1WH1}$	$t_{WCH}$	Write Command Hold Time	8		10		10		ns	
29	$t_{WL1WH1}$	$t_{WP}$	Write Pulse Width	8		10		10		ns	
30	$t_{GL1QZ}$	$t_{DEO}$	Data to $\overline{OE}$ Delay	0		0		0		ns	15
31	$t_{WL1RH1}$	$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	13		15		17		ns	
32	$t_{DVWL2}$	$t_{DS}$	Data in Setup Time	0		0		0		ns	10

**AC Characteristics** (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	50		60		70		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
33	t <sub>WL1DX</sub>	t <sub>DH</sub>	Data in Hold Time	8		10		12		ns	10
34	t <sub>WL1GL2</sub>	t <sub>WOH</sub>	Write to $\overline{OE}$ Hold Time	10		13		15		ns	10
35	t <sub>CH2RH2</sub>	t <sub>PRWC</sub>	EDO Page Mode Read-Write Cycle Time	58		68		77		ns	
36	t <sub>RL2RL2 (RMW)</sub>	t <sub>RWC</sub>	Read-Modify-Write Cycle Time	113		138		162		ns	
38	t <sub>CL1WL2</sub>	t <sub>CWD</sub>	$\overline{CAS}$ to $\overline{WE}$ Delay	27		32		36		ns	10
39	t <sub>RL1WL2</sub>	t <sub>RWD</sub>	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	64		77		89		ns	10
40	t <sub>AVWL2</sub>	t <sub>AWD</sub>	Column Address to $\overline{WE}$ Delay	39		47		54		ns	10
41	t <sub>CL2CL2</sub>	t <sub>PC</sub>	EDO Page Mode Read or Write Cycle Time	20		25		30		ns	
42	t <sub>CH2CL2</sub>	t <sub>CP</sub>	$\overline{CAS}$ Precharge Time	8		10		10		ns	
43	t <sub>AVRH1</sub>	t <sub>CAR</sub>	Column Address to $\overline{RAS}$ Setup Time	25		30		35		ns	
44	t <sub>CH2QV</sub>	t <sub>CAP</sub>	Access Time from Column Precharge		27		32		37	ns	6
46	t <sub>CL1RL2</sub>	t <sub>CSR</sub>	$\overline{CAS}$ Setup Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	10		10		10		ns	
47	t <sub>RH2CL2</sub>	t <sub>RPC</sub>	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5		5		5		ns	
48	t <sub>RL1CH1</sub>	t <sub>CHR</sub>	$\overline{CAS}$ Hold Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	10		10		10		ns	
50	t <sub>RH2CL2</sub>	t <sub>RASP</sub>	$\overline{RAS}$ Pulse Width (EDO Mode)	50	200K	60	200K	70	200K	ns	
51	t <sub>RH2CL2</sub>	t <sub>RHCP</sub>	$\overline{CAS}$ Precharge Time to $\overline{RAS}$ Delay	27		32		37		ns	
52	t <sub>RH2CL2</sub>	t <sub>CPWD</sub>	$\overline{CAS}$ Precharge Time to $\overline{WE}$	41		49		56		ns	
53	t <sub>RH2CL2</sub>	t <sub>CPT</sub>	$\overline{CAS}$ Precharge Time (CBR Counter Test)	35		40		40		ns	
54	t <sub>RH2CL2</sub>	t <sub>WRP</sub>	Write to $\overline{RAS}$ Precharge time (CRB Cycle)	10		10		10		ns	
55	t <sub>RH2CL2</sub>	t <sub>WRH</sub>	Write Hold time reference to $\overline{RAS}$ (CRB Cycle)	10		10		10		ns	
56	t <sub>RH2CL2</sub>	t <sub>CDD</sub>	$\overline{CAS}$ High to Data delay	10		13		15		ns	16
57	t <sub>RH2CL2</sub>	t <sub>ODD</sub>	$\overline{OE}$ High to Data delay	10		13		15		ns	16
58	t <sub>T</sub>	t <sub>T</sub>	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	
59		t <sub>REF</sub>	Refresh Interval (1024 Cycles)		16		16		16	ms	

**Self Refresh AC Characteristics**

60		t <sub>RASS</sub>	$\overline{RAS}$ Pulse Width During Self Refresh	100K		100K		100K		ns	17
61		t <sub>RPS</sub>	$\overline{RAS}$ Precharge Time During Self Refresh	95		110		130		ns	17
62		t <sub>CHS</sub>	$\overline{CAS}$ Hold Time Width During Self Refresh	50		50		50		ns	17

**Notes:**

1. All voltage are referenced to  $V_{SS}$ .
2.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC7}$  depend on cycle rate.
3.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are measured with the output open.
4. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ . In the case of  $I_{CC4}$  it can be changed once or less during an EDO cycle ( $t_{HPC}$ ).
5. An initial pause of 200  $\mu s$  is required after power-up followed by 8  $\overline{RAS}$  cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Transition times are also measured between  $V_{IH}$  and  $V_{IL}$ .
7. Measured with a load equivalent to 2 TTL gates and 50 pF ( $V_{OL} = 0.8V$  and  $V_{OH} = 2.0V$ ).
8.  $t_{OFF}$  (max.) and  $t_{OEZ}$  (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10. These parameters are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{WE}$  leading edge in read-write cycles.
11.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} > t_{WCS}(\text{min.})$ , the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if  $t_{RWD} > t_{RWD}(\text{min.})$ ,  $t_{CWD} > t_{CWD}(\text{min.})$ ,  $t_{AWD} > t_{AWD}(\text{min.})$ , and  $t_{CPWD} > t_{CPWD}(\text{min.})$ , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
12. Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
13. Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{CAA}$ .
14. AC measurements assume  $t_T = 2 \text{ ns}$ .
15. Either  $t_{DZC}$  or  $t_{DEO}$  must be satisfied.
16. Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
17. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:  
  
If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.  
  
If row addresses are being refreshed in any other manner (ROR – Distributed/Burst; or CBR – Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.
18.  $t_{OFF}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.

The timing diagram illustrates the relationship between several control and data signals over time:

- RAS**: Row Address Strobe. Transitions from V<sub>IH</sub> to V<sub>L</sub> are labeled with  $t_{AR}$ ,  $t_{RAD}$ , and  $t_{RAH}$ . Transitions from V<sub>L</sub> to V<sub>IH</sub> are labeled with  $t_{RSH}$  and  $t_{CRP}$ .
- UCAS, LCAS**: Column Address Strobe / Local Column Address Strobe. Transitions from V<sub>IH</sub> to V<sub>L</sub> are labeled with  $t_{CD}$ ,  $t_{CAH}$ , and  $t_{CRP}$ . Transitions from V<sub>L</sub> to V<sub>IH</sub> are labeled with  $t_{CSH}$  and  $t_{CRP}$ .
- ADDRESS**: Consists of ROW ADDRESS and COLUMN ADDRESS periods. The transition from V<sub>IH</sub> to V<sub>L</sub> at the start of the row address is labeled  $t_{ASR}$ . The transition from V<sub>L</sub> to V<sub>IH</sub> at the end of the column address is labeled  $t_{ACH}$ .
- WE**: Write Enable. A pulse from V<sub>IH</sub> to V<sub>L</sub> with duration  $t_{WCH}$ .
- OE**: Output Enable. A pulse from V<sub>IH</sub> to V<sub>L</sub> with duration  $t_{OAC}$ .
- I/O**: Data bus. Shows VALID DATA-OUT and VALID DATA-IN periods.

Key timing parameters defined include:

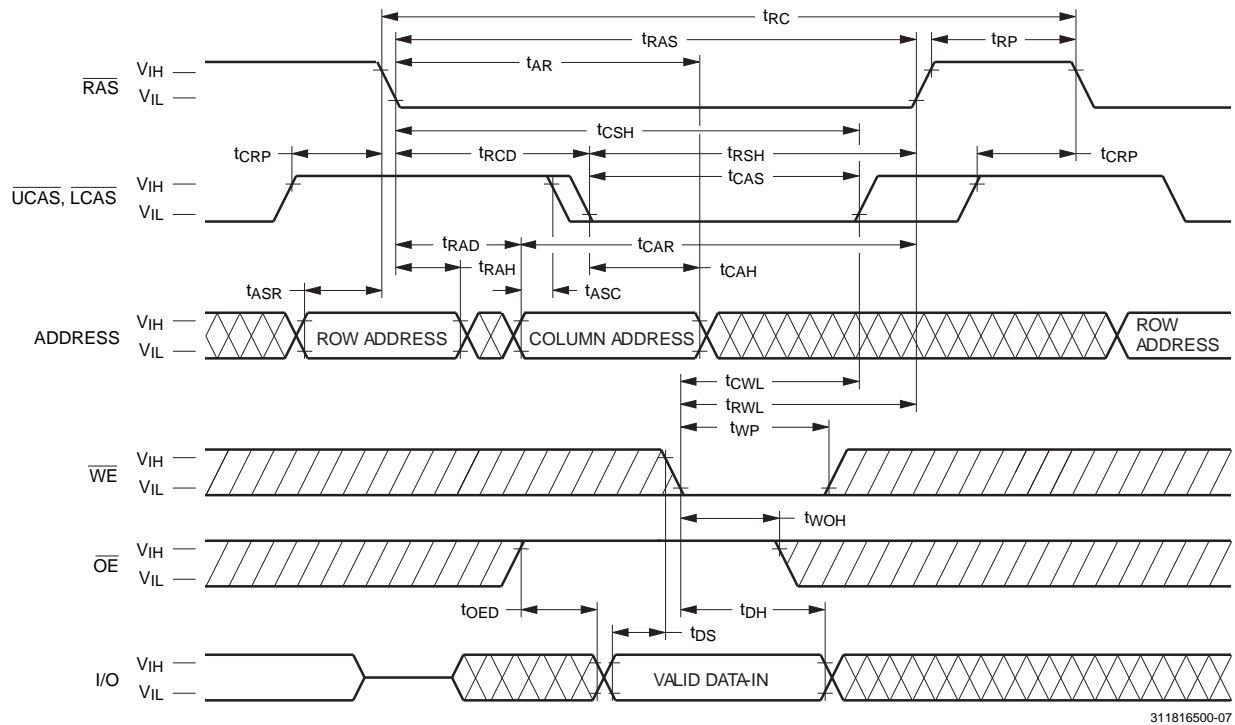
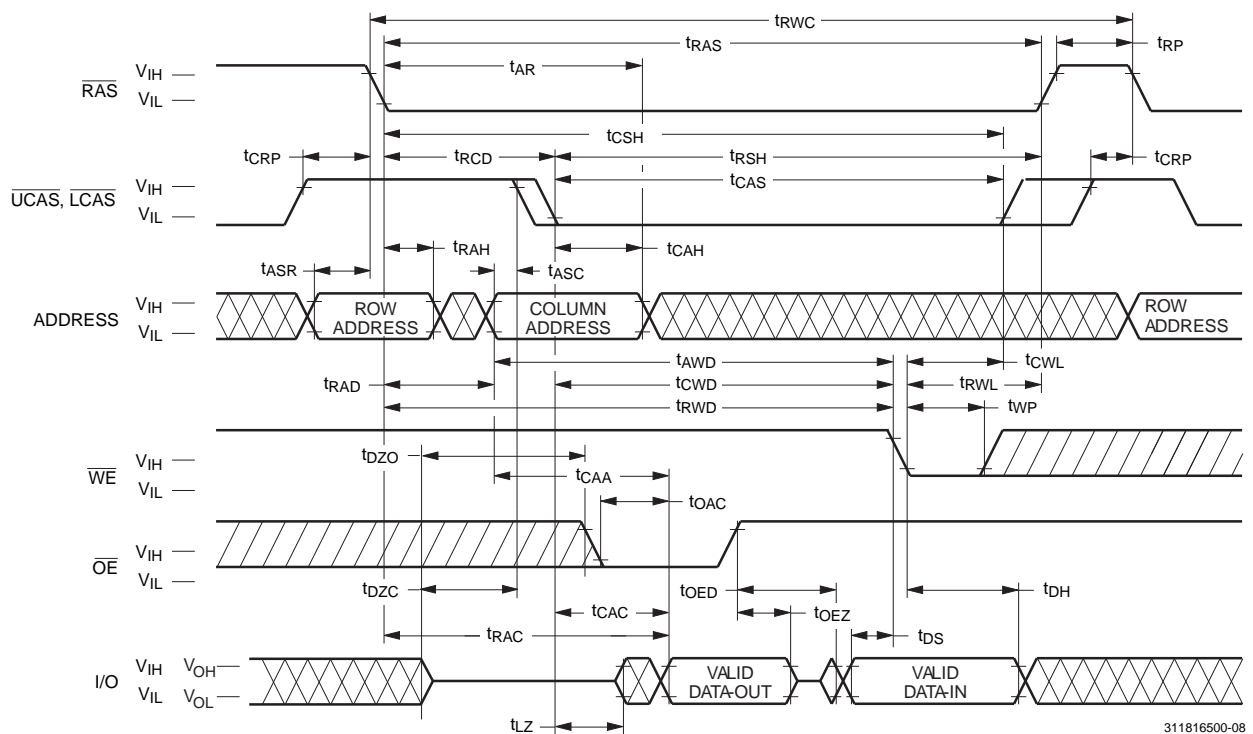
- $t_{AR}$ : RAS access time
- $t_{RC}$ : RAS cycle time
- $t_{RP}$ : RAS precharge time
- $t_{RD}$ : Read delay
- $t_{RSH}$ : RAS-to-column address setup time
- $t_{CRP}$ : RAS-to-column address recovery time
- $t_{AD}$ : Address delay
- $t_{RAH}$ : RAS hold time
- $t_{CAH}$ : Column address hold time
- $t_{ASR}$ : Address setup time
- $t_{ACH}$ : Address hold time
- $t_{WCH}$ : Write enable cycle time
- $t_{OAC}$ : Output enable access time
- $t_{DZC}$ : Data zone change time
- $t_{CAC}$ : Column address to valid data time
- $t_{DZO}$ : Data zone output time
- $t_{LZ}$ : Latency time
- $t_{FZ}$ : Valid data to output time
- $t_{OFF}$ : Output off time
- $t_{CDD}$ : Column address to data delay

The timing diagram illustrates the relationship between several control and data signals for the 311816500-00 device. The signals and their timing parameters are as follows:

- RAS:** Active low signal. Timing parameters include  $t_{AR}$  (RAS to output delay),  $t_{RAS}$  (RAS pulse width),  $t_{RC}$  (RAS to output delay), and  $t_{RP}$  (RAS pulse width).
- UCAS, LCAS:** Active low signals. Timing parameters include  $t_{CRP}$  (RAS to UCAS/LCAS delay),  $t_{RCD}$  (RAS to UCAS/LCAS delay),  $t_{CSH}$  (UCAS/LCAS to output delay),  $t_{RSH}$  (UCAS/LCAS to output delay),  $t_{CAS}$  (UCAS/LCAS to output delay), and  $t_{CRP}$  (UCAS/LCAS to output delay).
- ADDRESS:** Signal for row and column addresses. Timing parameters include  $t_{ASR}$  (RAS to address delay),  $t_{ASC}$  (RAS to address delay),  $t_{RAD}$  (RAS to address delay),  $t_{CWL}$  (RAS to address delay),  $t_{WCH}$  (RAS to address delay),  $t_{WCR}$  (RAS to address delay), and  $t_{RWL}$  (RAS to address delay).
- WE:** Active low signal. Timing parameters include  $t_{DHR}$  (RAS to WE delay),  $t_{DS}$  (RAS to WE delay), and  $t_{DH}$  (RAS to WE delay).
- OE:** Active low signal. Timing parameters include  $t_{DHR}$  (RAS to OE delay),  $t_{DS}$  (RAS to OE delay), and  $t_{DH}$  (RAS to OE delay).
- I/O:** Data bus signal. Timing parameters include  $t_{DHR}$  (RAS to I/O delay),  $t_{DS}$  (RAS to I/O delay), and  $t_{DH}$  (RAS to I/O delay).

The diagram shows the sequence of events during a memory access cycle, including the activation of RAS, the arrival of UCAS/LCAS, the output of data, and the deactivation of RAS and UCAS/LCAS.



**Waveforms of Write Cycle ( $\overline{OE}$  Controlled Write)****Waveforms of Read-Modify-Write Cycle**

Don't Care

Undefined

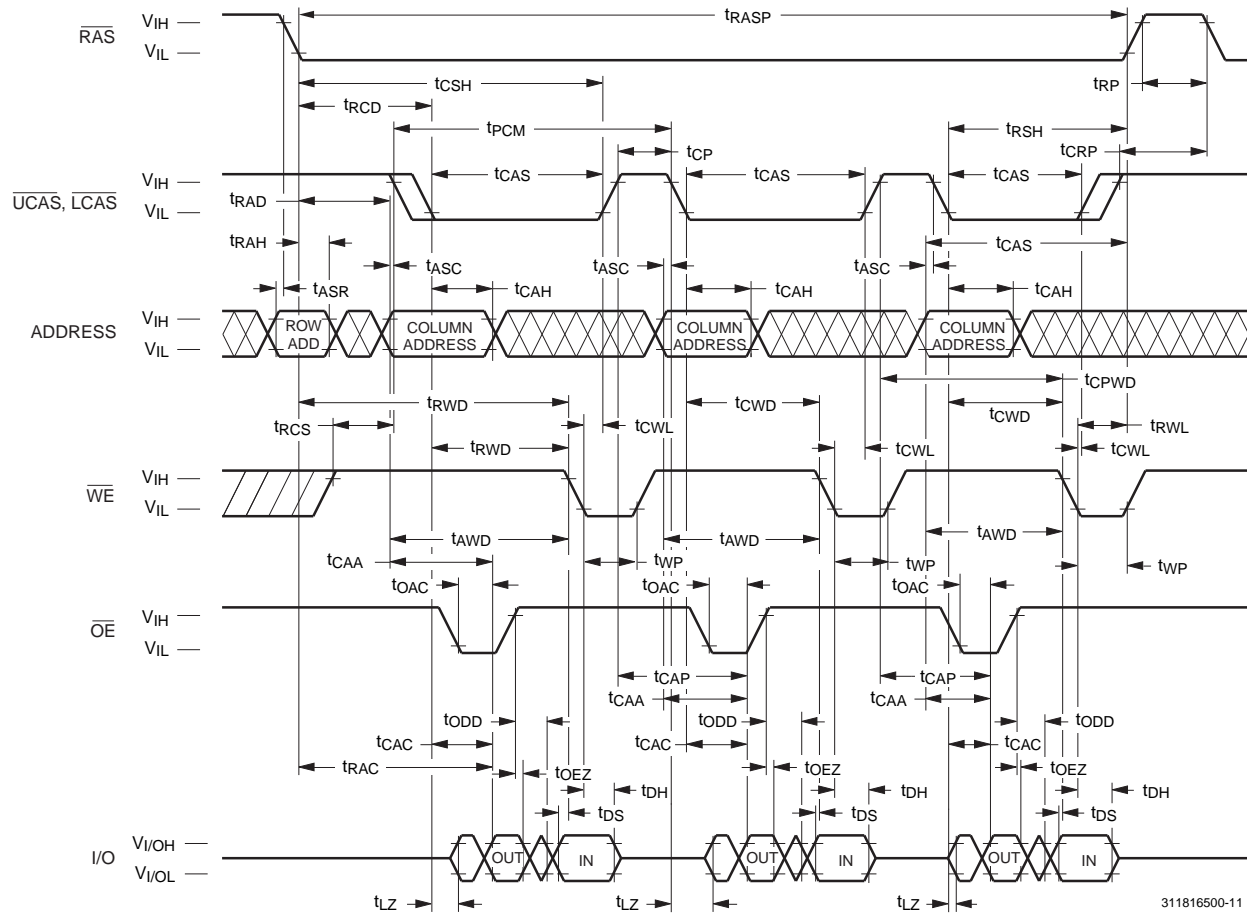
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The timing diagram illustrates the relationship between several control and data signals for the 311816500-1 device. The signals shown are:

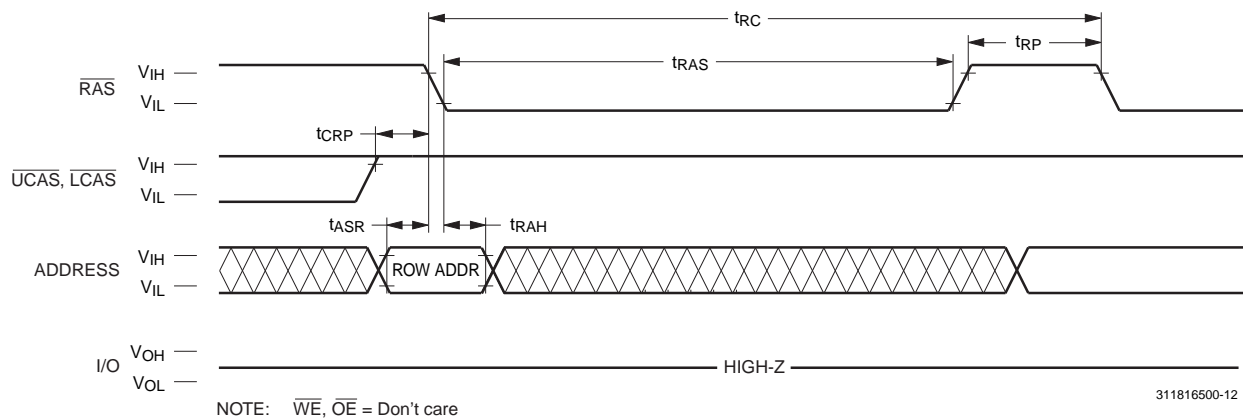
- RAS**: Row Address Strobe, active low. Timing parameters include  $t_{AR}$  (access time),  $t_{RSP}$  (refresh period), and  $t_{RP}$  (refresh period).
- UCAS, LCAS**: Column Address Strobe / Local Column Address Strobe, active low. Timing parameters include  $t_{CRP}$  (column refresh period),  $t_{PC}$  (period),  $t_{CAS}$  (column access time),  $t_{CP}$  (column period),  $t_{RSH}$  (refresh time),  $t_{CASH}$  (column access time),  $t_{RAH}$  (row access time),  $t_{CAH}$  (column access time),  $t_{ASC}$  (access time),  $t_{CAR}$  (column access time),  $t_{CAH}$  (column access time),  $t_{RAD}$  (row access time),  $t_{CWL}$  (column write latency),  $t_{WCS}$  (write cycle time),  $t_{WCH}$  (write cycle time),  $t_{WP}$  (write period),  $t_{DS}$  (data setup time), and  $t_{DH}$  (data hold time).
- ADDRESS**: Data bus address. Timing parameters include  $t_{RAD}$  (row access time),  $t_{CWL}$  (column write latency),  $t_{WCS}$  (write cycle time),  $t_{WCH}$  (write cycle time),  $t_{WP}$  (write period),  $t_{DS}$  (data setup time), and  $t_{DH}$  (data hold time).
- WE**: Write Enable, active low. Timing parameters include  $t_{WP}$  (write period).
- OE**: Output Enable, active low. Timing parameters include  $t_{DS}$  (data setup time) and  $t_{DH}$  (data hold time).
- I/O**: Data bus input/output. Timing parameters include  $t_{DS}$  (data setup time) and  $t_{DH}$  (data hold time).

The diagram shows the timing of these signals relative to each other, with various timing parameters labeled as  $t_{AR}$ ,  $t_{RSP}$ ,  $t_{RP}$ ,  $t_{CRP}$ ,  $t_{PC}$ ,  $t_{CAS}$ ,  $t_{CP}$ ,  $t_{RSH}$ ,  $t_{CASH}$ ,  $t_{RAH}$ ,  $t_{CAH}$ ,  $t_{ASC}$ ,  $t_{CAR}$ ,  $t_{CAH}$ ,  $t_{RAD}$ ,  $t_{CWL}$ ,  $t_{WCS}$ ,  $t_{WCH}$ ,  $t_{WP}$ ,  $t_{DS}$ , and  $t_{DH}$ .

## Waveforms of EDO Page Mode Read-Modify-Write Cycle

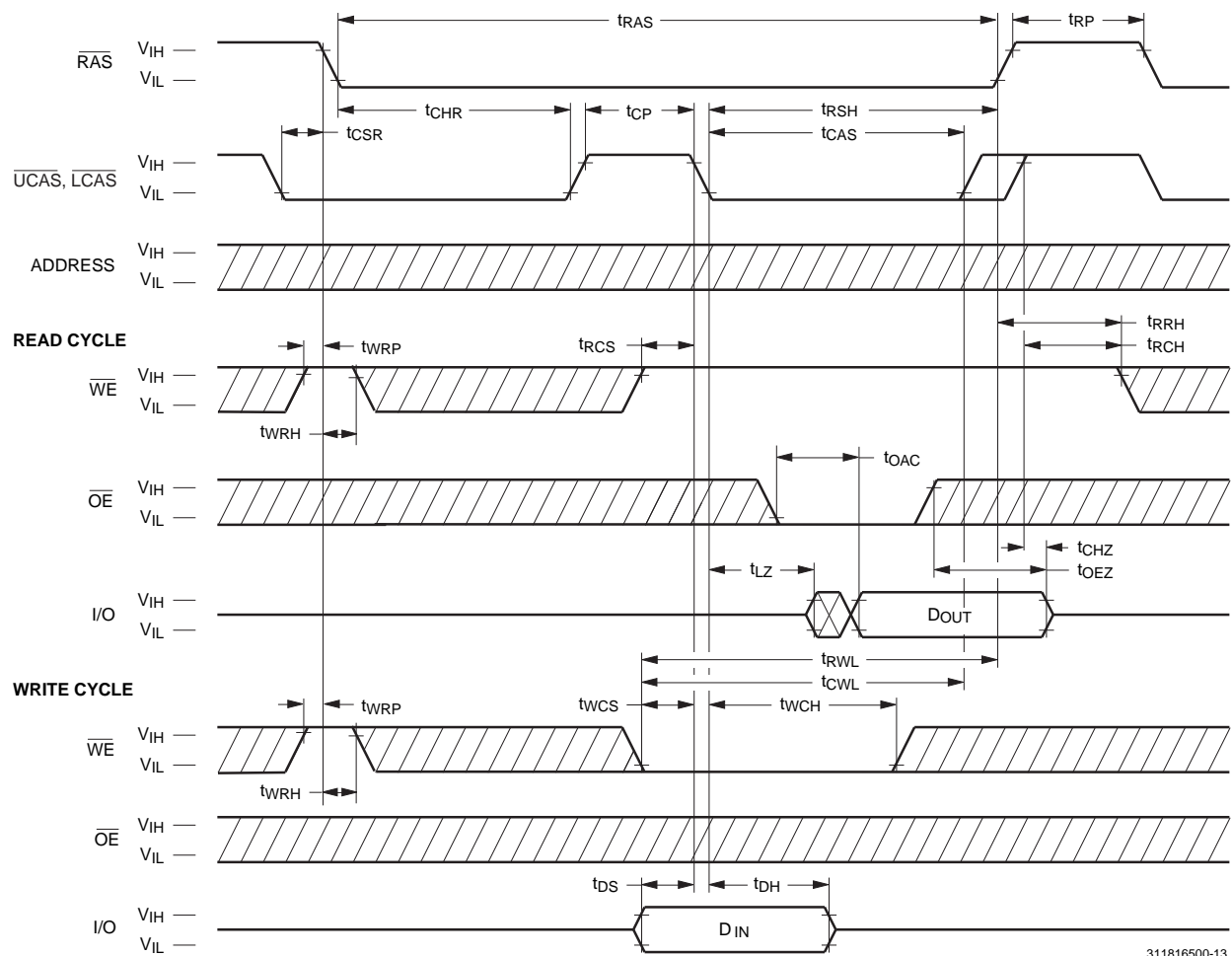


## Waveforms of RAS Only Refresh Cycle

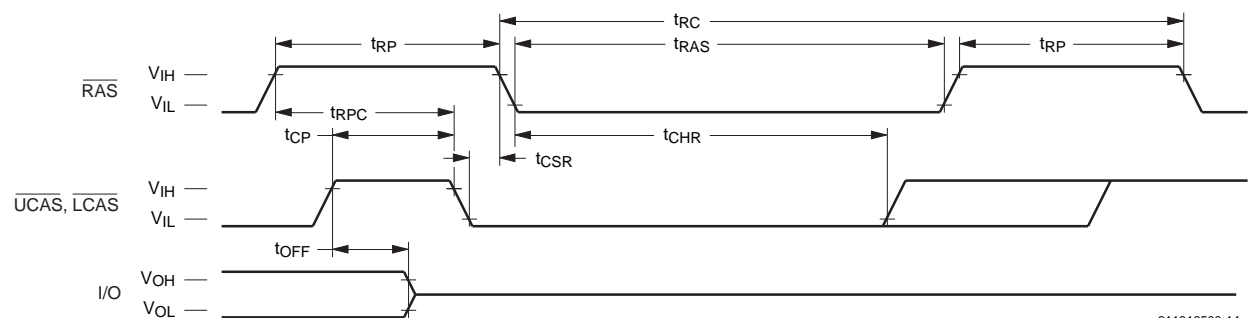


Don't Care

Undefined

**Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Counter Test Cycle**

311816500-13

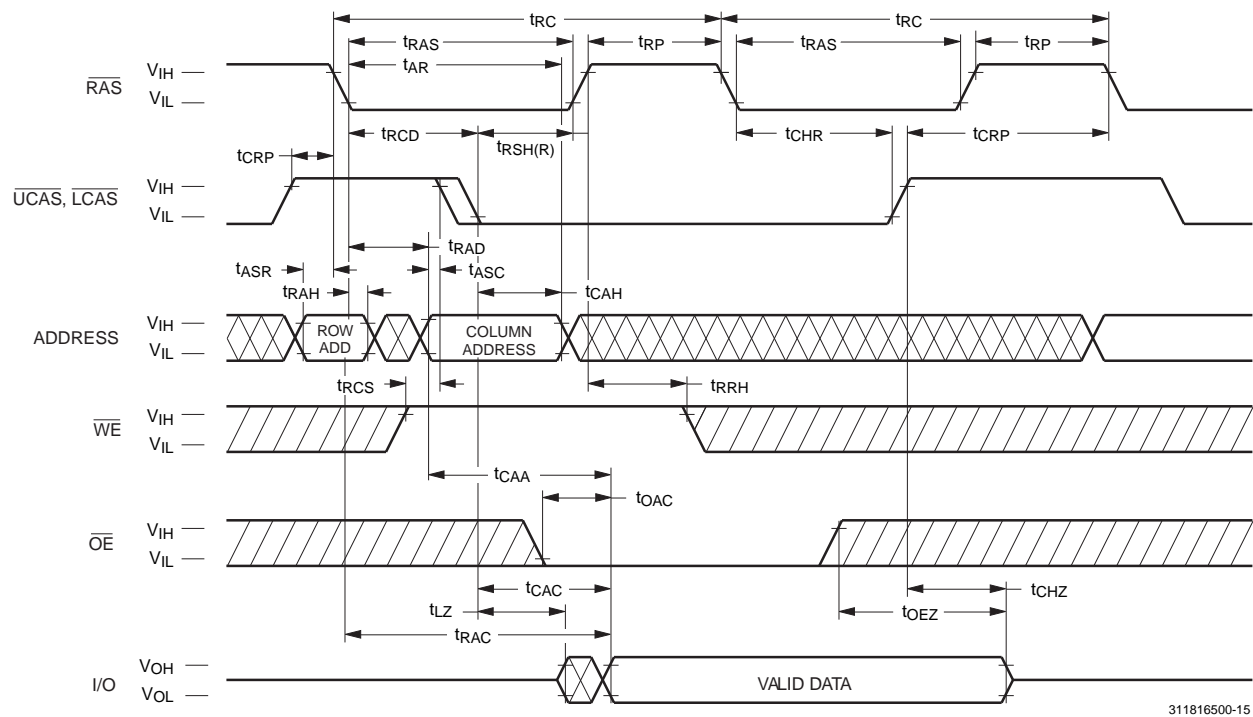
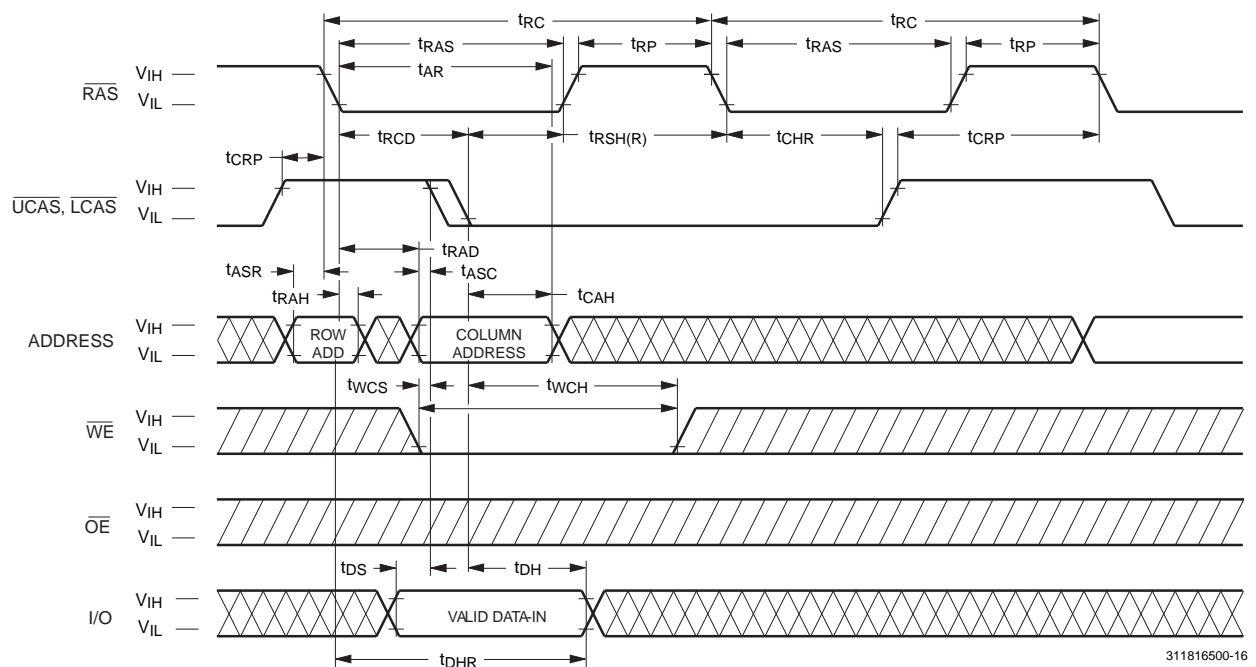
**Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle**

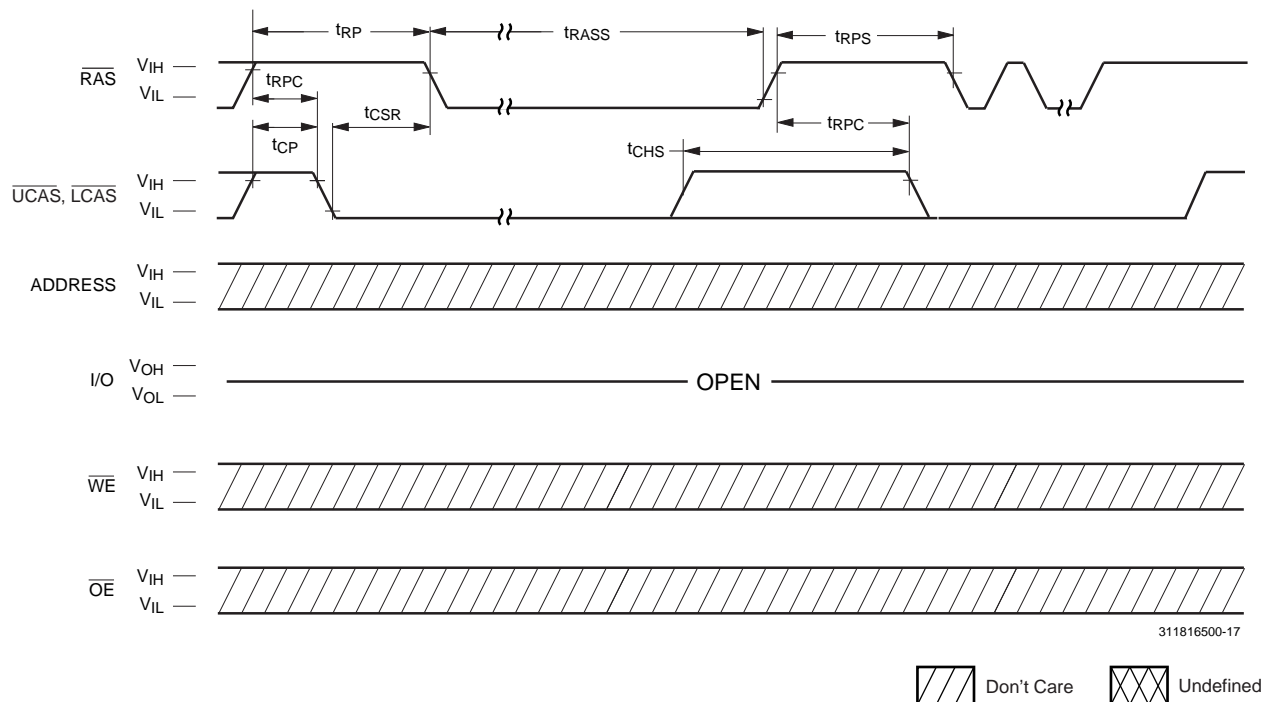
311816500-14

NOTE:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $A_0$ - $A_9$  = Don't care

Don't Care

Undefined

**Waveforms of Hidden Refresh Cycle (Read)****Waveforms of Hidden Refresh Cycle (Write)**

**Waveforms of Self Refresh Cycle (optional)****Functional Description**

The V53C318165A is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C318165A reads and writes data by multiplexing an 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ( $\overline{\text{RAS}}$ ). The column address “flows through” an internal address buffer and is latched by the Column Address Strobe ( $\overline{\text{CAS}}$ ). Because access time is primarily dependent on a valid column address rather than the precise time that the  $\overline{\text{CAS}}$  edge occurs, the delay time from  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  has little effect on the access time.

**Memory Cycle**

A memory cycle is initiated by bringing  $\overline{\text{RAS}}$  low. Any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{\text{RAS}}$  time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time  $t_{\text{RP}}/t_{\text{CP}}$  has elapsed.

**Read Cycle**

A Read cycle is performed by holding the Write Enable ( $\overline{\text{WE}}$ ) signal High during a  $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$  operation. The column address must be held for a minimum specified by  $t_{\text{AR}}$ . Data Out becomes valid only when  $t_{\text{OAC}}$ ,  $t_{\text{RAC}}$ ,  $t_{\text{CAA}}$  and  $t_{\text{CAC}}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by  $t_{\text{CAA}}$  when  $t_{\text{RAC}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{OAC}}$  are all satisfied.

**Write Cycle**

A Write Cycle is performed by taking  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  low during a  $\overline{\text{RAS}}$  operation. The column address is latched by  $\overline{\text{CAS}}$ . The Write Cycle can be  $\overline{\text{WE}}$  controlled or  $\overline{\text{CAS}}$  controlled depending on whether  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$  falls later. Consequently, the input data must be valid at or before the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. In the  $\overline{\text{CAS}}$ -controlled Write Cycle, when the leading edge of  $\overline{\text{WE}}$  occurs prior to the  $\overline{\text{CAS}}$  low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  will maintain the output in the High-Z state.

In the  $\overline{\text{WE}}$  controlled Write Cycle,  $\overline{\text{OE}}$  must be in the high state and  $t_{\text{OED}}$  must be satisfied.

**Extended Data Output Page Mode**

EDO Page operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining  $\overline{\text{RAS}}$  low while performing successive  $\overline{\text{CAS}}$  cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while  $\overline{\text{CAS}}$  is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of  $\overline{\text{CAS}}$ , eliminating  $t_{\text{ASC}}$  and  $t_{\text{T}}$  from the critical timing path.  $\overline{\text{CAS}}$  latches the address into the column address buffer. During EDO operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into EDO Mode, access is  $t_{\text{CAA}}$  or  $t_{\text{CAP}}$  controlled. If the column address is valid prior to the rising edge of  $\overline{\text{CAS}}$ , the access time is referenced to the  $\overline{\text{CAS}}$  rising edge and is specified by  $t_{\text{CAP}}$ . If the column address is valid after the rising  $\overline{\text{CAS}}$  edge, access is timed from the occurrence of a valid address and is specified by  $t_{\text{CAA}}$ . In both cases, the falling edge of  $\overline{\text{CAS}}$  latches the address and enables the output.

EDO provides a sustained data rate of 50 MHz for applications that require high bandwidth such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{\text{RC}} + 1023 \times t_{\text{PC}}}$$

**Self Refresh**

Self Refresh mode provides internal refresh control signals to the DRAM during extended periods of inactivity. Device operation in this mode provides additional power savings and design ease by elimination of external refresh control signals. Self Refresh mode is initiated with a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  (CBR) Refresh cycle, holding both  $\overline{\text{RAS}}$  low ( $t_{\text{RASS}}$ ) and  $\overline{\text{CAS}}$  low ( $t_{\text{CHD}}$ ) for a specified period. Both of these parameters are specified with minimum values to guarantee entry into Self Refresh operation. Once the device has been placed in to Self Refresh mode the  $\overline{\text{CAS}}$  clock is no longer required to maintain Self Refresh operation.

The Self Refresh mode is terminated by returning the  $\overline{\text{RAS}}$  clock to a high level for a specified ( $t_{\text{RPS}}$ ) minimum time. After termination of the Self Refresh cycle normal accesses to the device may be initiated immediately, providing that subsequent refresh cycles utilize the  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  (CBR) mode of operation.

**Data Output Operation**

The V53C318165A Input/Output is controlled by  $\overline{\text{OE}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{RAS}}$ . A  $\overline{\text{RAS}}$  low transition enables the transfer of data to and from the selected row address in the Memory Array. A  $\overline{\text{RAS}}$  high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a  $\overline{\text{RAS}}$  low transition, a  $\overline{\text{CAS}}$  low transition or  $\overline{\text{CAS}}$  low level enables the internal I/O path. A  $\overline{\text{CAS}}$  high transition or a  $\overline{\text{CAS}}$  high level disables the I/O path and the output driver if it is enabled. A  $\overline{\text{CAS}}$  low transition while  $\overline{\text{RAS}}$  is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding  $\overline{\text{OE}}$  high. The  $\overline{\text{OE}}$  signal has no effect on any data stored in the output latches. A  $\overline{\text{WE}}$  low level can also disable the output drivers when  $\overline{\text{CAS}}$  is low. During a Write cycle, if  $\overline{\text{WE}}$  goes low at a time in relationship to  $\overline{\text{CAS}}$  that would normally cause the outputs to be active, it is necessary to use  $\overline{\text{OE}}$  to disable the output drivers prior to the  $\overline{\text{WE}}$  low transition to allow Data In Setup Time ( $t_{\text{DS}}$ ) to be satisfied.

**Power-On**

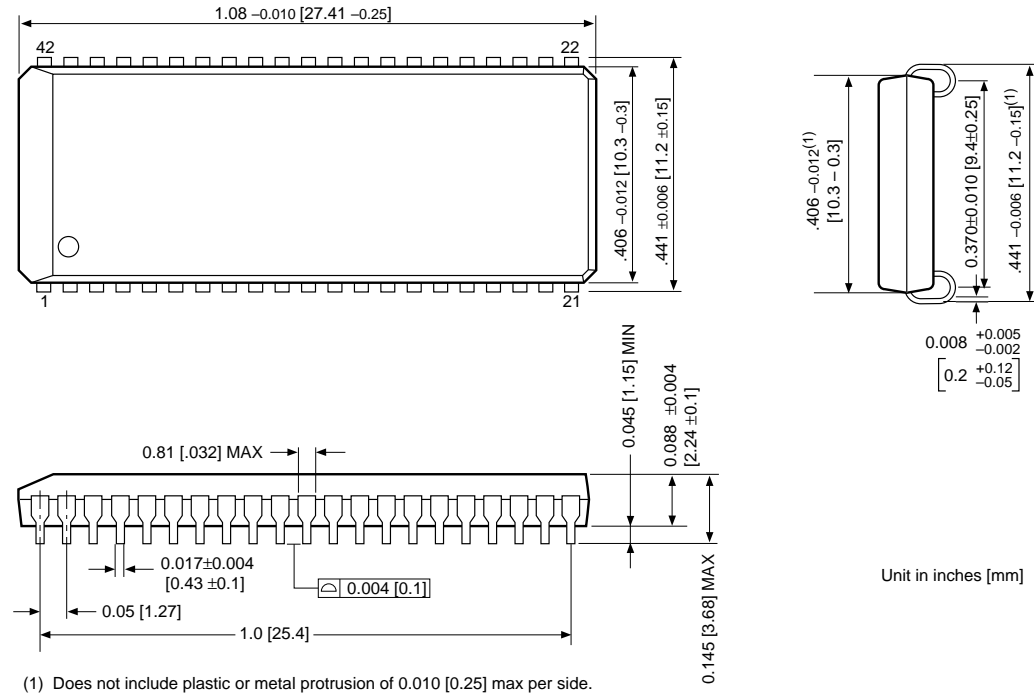
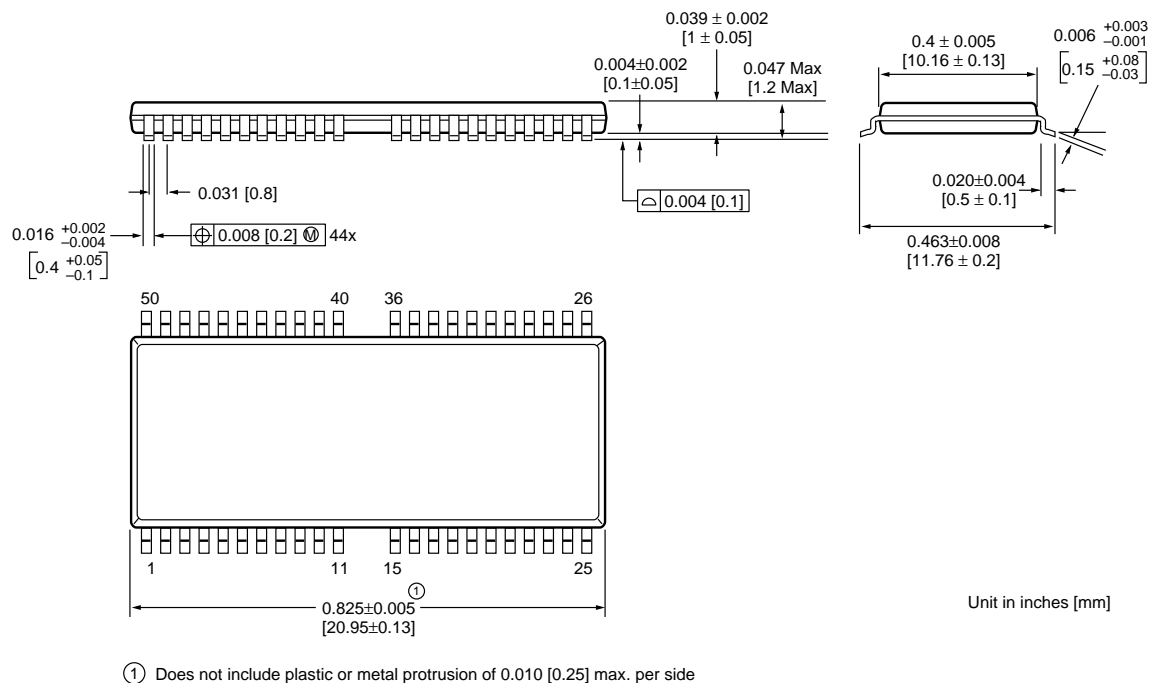
After application of the  $V_{\text{CC}}$  supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the  $V_{\text{CC}}$  current requirement of the V53C318165A is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . If  $\overline{\text{RAS}}$  is low during Power-On, the device will go into an active cycle and  $I_{\text{CC}}$  will exhibit current transients. It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $V_{\text{CC}}$  or be held at a valid  $V_{\text{IH}}$  during Power-On to avoid current surges.

**Table 1. V53C318165A Data Output**  
*Operation for Various Cycle Types*

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
CAS-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$ -Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
EDO Read Cycle	Data from Addressed Memory Cell
EDO Write Cycle (Early Write)	High-Z
EDO Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$ -only Refresh	High-Z
$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle	High-Z
$\overline{CAS}$ -only Cycles	High-Z



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**50/44-Pin 400 mil TSOP-II**


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