

**ULTRA-HIGH PERFORMANCE,  
128K X 8 BIT EDO PAGE MODE  
CMOS DYNAMIC RAM**

HIGH PERFORMANCE	35	40	45	50
Max. $\overline{\text{RAS}}$ Access Time, ( $t_{\text{RAC}}$ )	35 ns	40 ns	45 ns	50 ns
Max. Column Address Access Time, ( $t_{\text{CAA}}$ )	18 ns	20 ns	22 ns	24 ns
Min. Fast Page Mode With EDO Cycle Time, ( $t_{\text{PC}}$ )	14 ns	15 ns	17 ns	19 ns
Min. Read/Write Cycle Time, ( $t_{\text{RC}}$ )	70 ns	75 ns	80 ns	90 ns

### Features

- 128K x 8-bit organization
- $\overline{\text{RAS}}$  access time: 35, 40, 45, 50 ns
- EDO Page Mode supports sustained I/O data rates up to 71.5 MHz
- Low power dissipation
  - V53C8128H-50
    - Operating Current – 135 mA max
    - TTL Standby Current – 2.0 mA max
- Low CMOS Standby Current
  - V53C8128H – 1.0 mA max
- Read-Modify-Write,  $\overline{\text{RAS}}$ -Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh capability
- Refresh Interval
  - V53C8128H – 512 cycles/8 ms
- Available in 26/24 pin 300 mil SOJ package

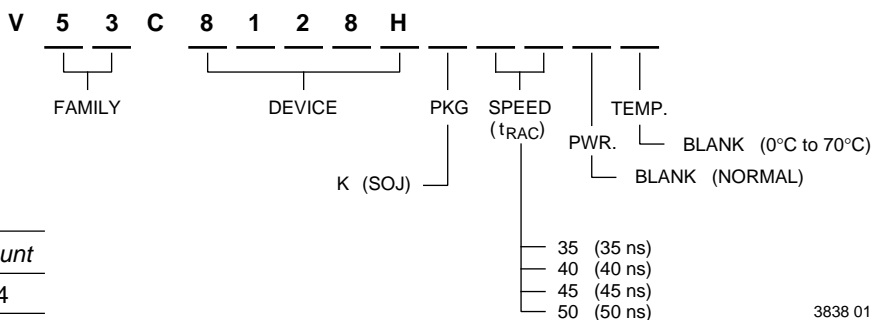
### Description

The V53C8128H is a high speed 131,072 x 8 bit CMOS dynamic random access memory. The V53C8128H offers a combination of features: EDO Page Mode for high data bandwidth, fast usable speed, CMOS standby current.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Page Mode with extended data out operation allows random access of up to 256 columns (x8) bits within a row with cycle times as short as 14 ns. Because of static circuitry, the  $\overline{\text{CAS}}$  clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C8128H ideally suited for graphics, digital signal processing and high performance Peripherals.

### Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)				Power	Temperature Mark
	K	35	40	45	50	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank



<i>Description</i>	<i>Pkg.</i>	<i>Pin Count</i>
SOJ	K	26/24

V <sub>SS</sub>	1	26	V <sub>SS</sub>
I/O <sub>1</sub>	2	25	I/O <sub>8</sub>
I/O <sub>2</sub>	3	24	I/O <sub>7</sub>
I/O <sub>3</sub>	4	23	I/O <sub>6</sub>
I/O <sub>4</sub>	5	22	I/O <sub>5</sub>
WE	6	21	CAS
RAS	8	19	OE
A <sub>0</sub>	9	18	A <sub>8</sub>
A <sub>1</sub>	10	17	A <sub>7</sub>
A <sub>2</sub>	11	16	A <sub>6</sub>
A <sub>3</sub>	12	15	A <sub>5</sub>
V <sub>CC</sub>	13	14	A <sub>4</sub>

3838 02

$A_0-A_8$	Address Inputs ( $A_8$ : Row Address only)
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$I/O_1-I/O_8$	Data Input, Output
$V_{CC}$	+5V Supply
$V_{SS}$	0V Supply

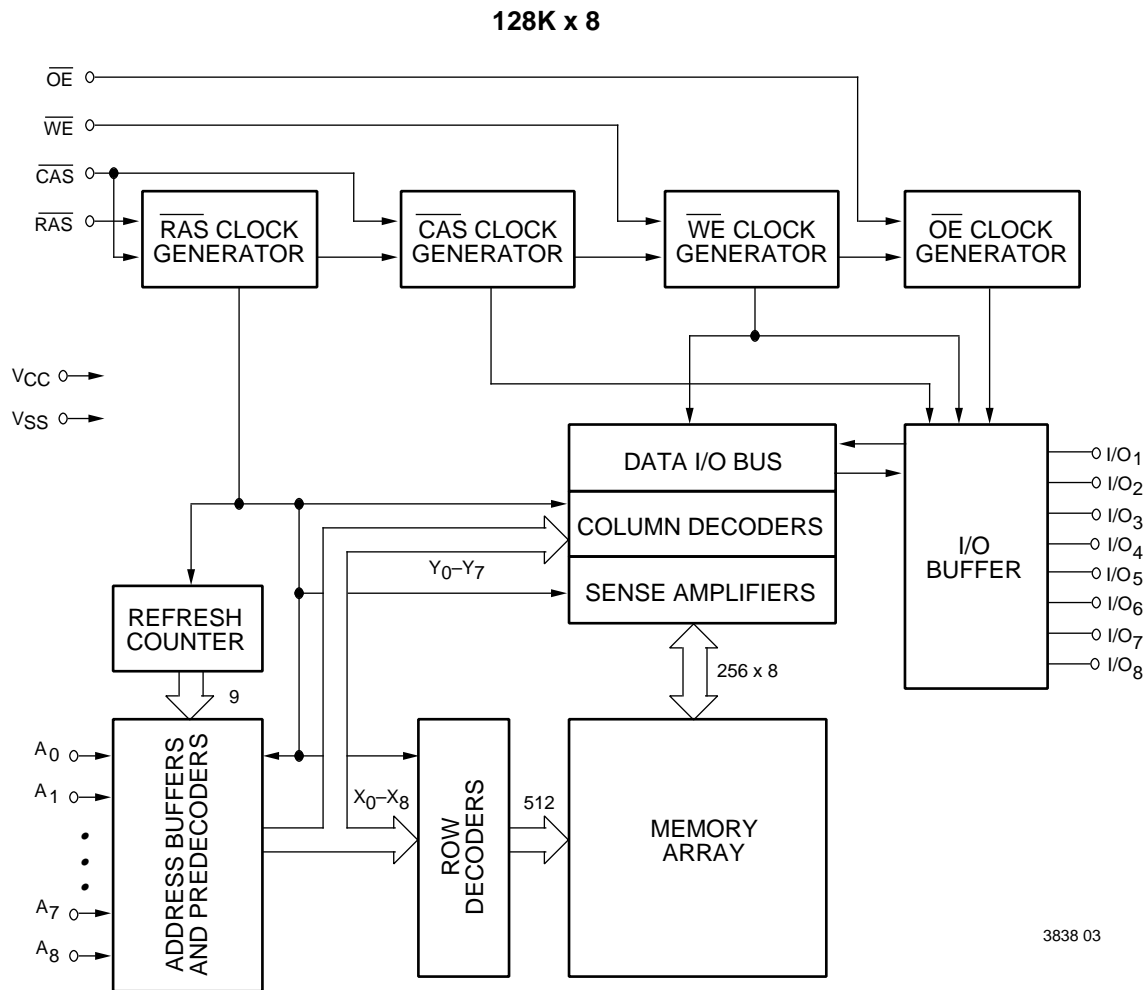
Ambient Temperature  
Under Bias .....  $-10^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$   
Storage Temperature (plastic) ....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Voltage Relative to  $V_{SS}$  .....  $-1.0\text{ V}$  to  $+7.0\text{ V}$   
Data Output Current .....  $50\text{ mA}$   
Power Dissipation .....  $1.0\text{ W}$

**Capacitance\***
$$T_A = 25^\circ\text{C}, V_{CC} = 5\text{ V} \pm 10\%, V_{SS} = 0\text{ V}$$

Symbol	Parameter	Typ.	Max.	Unit
C <sub>IN1</sub>	Address Input	3	4	pF
C <sub>IN2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	4	5	pF
C <sub>OUT</sub>	Data Input/Output	5	7	pF

\* Note: Capacitance is sampled and not 100% tested

Block Diagram



**DC and Operating Characteristics (1-2)**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Access Time	V53C8128H			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
$I_{LI}$	Input Leakage Current (any input pin)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{IN} \leq V_{CC}$	
$I_{LO}$	Output Leakage Current (for High-Z State)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$	
$I_{CC1}$	$V_{CC}$ Supply Current, Operating	35			160	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
		40			150			
		45			145			
		50			135			
$I_{CC2}$	$V_{CC}$ Supply Current, TTL Standby				4	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$ other inputs $\geq V_{SS}$	
$I_{CC3}$	$V_{CC}$ Supply Current, $\overline{\text{RAS}}$ -Only Refresh	35			160	mA	$t_{RC} = t_{RC}(\text{min.})$	2
		40			150			
		45			145			
		50			135			
$I_{CC4}$	$V_{CC}$ Supply Current, EDO Page Mode Operation	35			95	mA	Minimum cycle	1, 2
		40			90			
		45			85			
		50			80			
$I_{CC5}$	$V_{CC}$ Supply Current, Standby, Output Enabled				2	mA	$\overline{\text{RAS}}=V_{IH}, \overline{\text{CAS}}=V_{IL}$ other inputs $\geq V_{SS}$	1
$I_{CC6}$	$V_{CC}$ Supply Current, CMOS Standby				1	mA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V},$ $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V},$ All other inputs $\geq V_{SS}$	
$V_{IL}$	Input Low Voltage		-1		0.8	V		3
$V_{IH}$	Input High Voltage		2.4		$V_{CC}+1$	V		3
$V_{OL}$	Output Low Voltage				0.4	V	$I_{OL} = 4.2\text{ mA}$	
$V_{OH}$	Output High Voltage		2.4			V	$I_{OH} = -5\text{ mA}$	

**AC Characteristics**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	$t_{RL1RH1}$	$t_{RAS}$	$\overline{RAS}$ Pulse Width	35	75K	40	75K	45	75K	50	75K	ns	
2	$t_{RL2RL2}$	$t_{RC}$	Read or Write Cycle Time	70		75		80		90		ns	
3	$t_{RH2RL2}$	$t_{RP}$	$\overline{RAS}$ Precharge Time	25		25		25		30		ns	
4	$t_{RL1CH1}$	$t_{CSH}$	$\overline{CAS}$ Hold Time	35		40		45		50		ns	
5	$t_{CL1CH1}$	$t_{CAS}$	$\overline{CAS}$ Pulse Width	7		8		9		9		ns	
6	$t_{RL1CL1}$	$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay	16	23	17	28	18	32	19	36	ns	
7	$t_{WH2CL2}$	$t_{RCS}$	Read Command Setup Time	0		0		0		0		ns	4
8	$t_{AVRL2}$	$t_{ASR}$	Row Address Setup Time	0		0		0		0		ns	
9	$t_{RL1AX}$	$t_{RAH}$	Row Address Hold Time	6		7		8		9		ns	
10	$t_{AVCL2}$	$t_{ASC}$	Column Address Setup Time	0		0		0		0		ns	
11	$t_{CL1AX}$	$t_{CAH}$	Column Address Hold Time	4		5		6		7		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	14		14		15		15		ns	
13	$t_{CH2RL2}$	$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
14	$t_{CH2WX}$	$t_{RCH}$	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	$t_{RH2WX}$	$t_{RRH}$	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	$t_{OEL1RH2}$	$t_{ROH}$	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	8		8		9		10		ns	
17	$t_{GL1QV}$	$t_{OAC}$	Access Time from $\overline{OE}$		12		12		13		14	ns	
18	$t_{CL1QV}$	$t_{CAC}$	Access Time from $\overline{CAS}$ (EDO)		12		12		13		14	ns	6, 7
19	$t_{RL1QV}$	$t_{RAC}$	Access Time from $\overline{RAS}$		35		40		45		50	ns	6, 8, 9
20	$t_{AVQV}$	$t_{CAA}$	Access Time from Column Address		18		20		22		24	ns	6, 7, 10
21	$t_{CL1QX}$	$t_{LZ}$	$\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	$t_{CH2QZ}$	$t_{HZ}$	Output buffer turn-off delay time	0	6	0	6	0	7	0	8	ns	16
23	$t_{RL1AX}$	$t_{AR}$	Column Address Hold Time from $\overline{RAS}$	28		30		35		40		ns	
24	$t_{RL1AV}$	$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	11	17	12	20	13	23	14	26	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	12		12		13		14		ns	
26	$t_{WL1CH1}$	$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	12		12		13		14		ns	

## AC Characteristics (continued)

#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
27	$t_{WL1CL2}$	$t_{WCS}$	Write Command Setup Time	0		0		0		0		ns	12, 13
28	$t_{CL1WH1}$	$t_{WCH}$	Write Command Hold Time	5		5		6		7		ns	
29	$t_{WL1WH1}$	$t_{WP}$	Write Pulse Width	5		5		6		7		ns	
30	$t_{RL1WH1}$	$t_{WCR}$	Write Command Hold Time from $\overline{RAS}$	28		30		35		40		ns	
31	$t_{WL1RH1}$	$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	12		12		13		14		ns	
32	$t_{DVL2}$	$t_{DS}$	Data in Setup Time	0		0		0		0		ns	14
33	$t_{WL1DX}$	$t_{DH}$	Data in Hold Time	4		5		6		7		ns	14
34	$t_{WL1GL2}$	$t_{WOH}$	Write to $\overline{OE}$ Hold Time	5		6		7		8		ns	14
35	$t_{GH2DX}$	$t_{OED}$	$\overline{OE}$ to Data Delay Time	5		6		7		8		ns	14
36	$t_{RL2RL2}$ (RMW)	$t_{RWC}$	Read-Modify-Write Cycle Time	105		110		115		130		ns	
37	$t_{RL1RH1}$ (RMW)	$t_{RRW}$	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	70		75		80		87		ns	
38	$t_{CL1WL2}$	$t_{CWD}$	$\overline{CAS}$ to $\overline{WE}$ Delay	28		30		32		34		ns	12
39	$t_{RL1WL2}$	$t_{RWD}$	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	54		58		62		68		ns	12
40	$t_{CL1CH1}$	$t_{CRW}$	$\overline{CAS}$ Pulse Width (RMW)	46		48		50		52		ns	
41	$t_{AVWL2}$	$t_{AWD}$	Col. Address to $\overline{WE}$ Delay	35		38		41		42		ns	12
42	$t_{CL2CL2}$	$t_{PC}$	EDO Page Mode Read or Write Cycle Time	14		15		17		19		ns	
43	$t_{CH2CL2}$	$t_{CP}$	$\overline{CAS}$ Precharge Time	4		5		6		7		ns	
44	$t_{AVRH1}$	$t_{CAR}$	Column Address to $\overline{RAS}$ Setup Time	18		20		22		24		ns	
45	$t_{CH2QV}$	$t_{CAP}$	Access Time from Column Precharge		21		23		25		27	ns	7
46	$t_{RL1DX}$	$t_{DHR}$	Data in Hold Time Referenced to $\overline{RAS}$	28		30		35		40		ns	
47	$t_{CL1RL2}$	$t_{CSR}$	$\overline{CAS}$ Setup Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	10		10		10		10		ns	
48	$t_{RH2CL2}$	$t_{RPC}$	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	$t_{RL1CH1}$	$t_{CHR}$	$\overline{CAS}$ Hold Time $\overline{CAS}$ -before- $\overline{RAS}$ Refresh	8		8		10		12		ns	
50	$t_{CL2CL2}$ (RMW)	$t_{PCM}$	EDO Page Mode Read-Modify-Write Cycle Time	58		60		65		70		ns	

**AC Characteristics** (continued)

#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
51	$t_T$	$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
52		$t_{REF}$	Refresh Interval (512 Cycles)		8		8		8		8	ms	
53		$t_{COH}$	Output Hold After $\overline{CAS}$ Low		5		5		5		5	ns	

**Notes:**

1.  $I_{CC}$  is dependent on output loading when the device output is selected. Specified  $I_{CC}$  (max.) is measured with the output open.
2.  $I_{CC}$  is dependent upon the number of address transitions. Specified  $I_{DD}$  (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified  $V_{IL}$  (min.) is steady state operating. During transitions,  $V_{IL}$  (min.) may undershoot to  $-1.0$  V for a period not to exceed 20 ns. All AC parameters are measured with  $V_{IL}$  (min.)  $\geq V_{SS}$  and  $V_{IH}$  (max.)  $\leq V_{DD}$ .
4.  $t_{RCD}$  (max.) is specified for reference only. Operation within  $t_{RCD}$  (max.) limits insures that  $t_{RAC}$  (max.) and  $t_{CAA}$  (max.) can be met. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.), the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
5. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 50 pF.
7. Access time is determined by the longest of  $t_{CAA}$ ,  $t_{CAC}$  and  $t_{CAP}$ .
8. Assumes that  $t_{RAD} \leq t_{RAD}$  (max.). If  $t_{RAD}$  is greater than  $t_{RAD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RAD}$  exceeds  $t_{RAD}$  (max.).
9. Assumes that  $t_{RCD} \leq t_{RCD}$  (max.). If  $t_{RCD}$  is greater than  $t_{RCD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds  $t_{RCD}$  (max.).
10. Assumes that  $t_{RAD} \geq t_{RAD}$  (max.).
11. Operation within the  $t_{RAD}$  (max.) limit ensures that  $t_{RAC}$  (max.) can be met.  $t_{RAD}$  (max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.
13.  $t_{WCS}$  (min.) must be satisfied in an Early Write Cycle.
14.  $t_{DS}$  and  $t_{DH}$  are referenced to the latter occurrence of  $\overline{CAS}$  or  $\overline{WE}$ .
15.  $t_T$  is measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.). AC-measurements assume  $t_T = 3$  ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200  $\mu$ s pause and 8  $\overline{RAS}$ -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

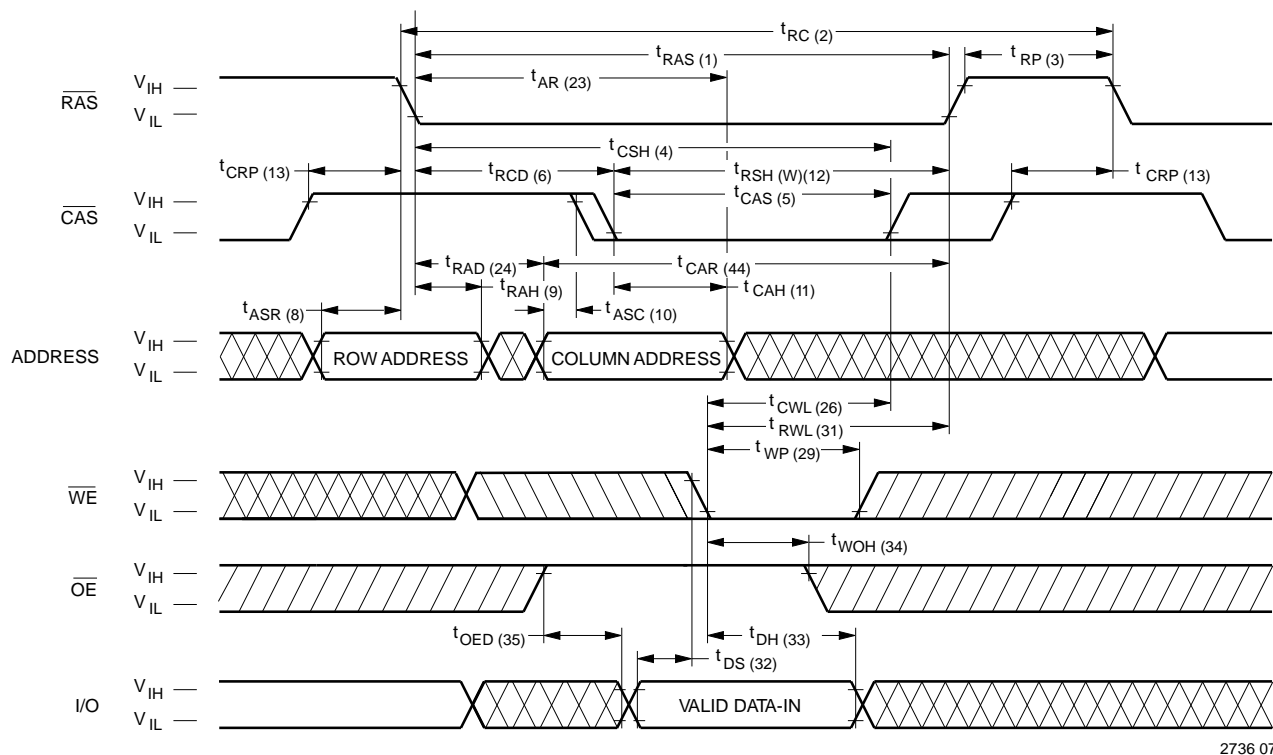


The diagram illustrates the timing relationships for the 2736 0 device. It shows the signals RAS, CAS, ADDRESS, WE, OE, and I/O. The timing parameters are defined as follows:

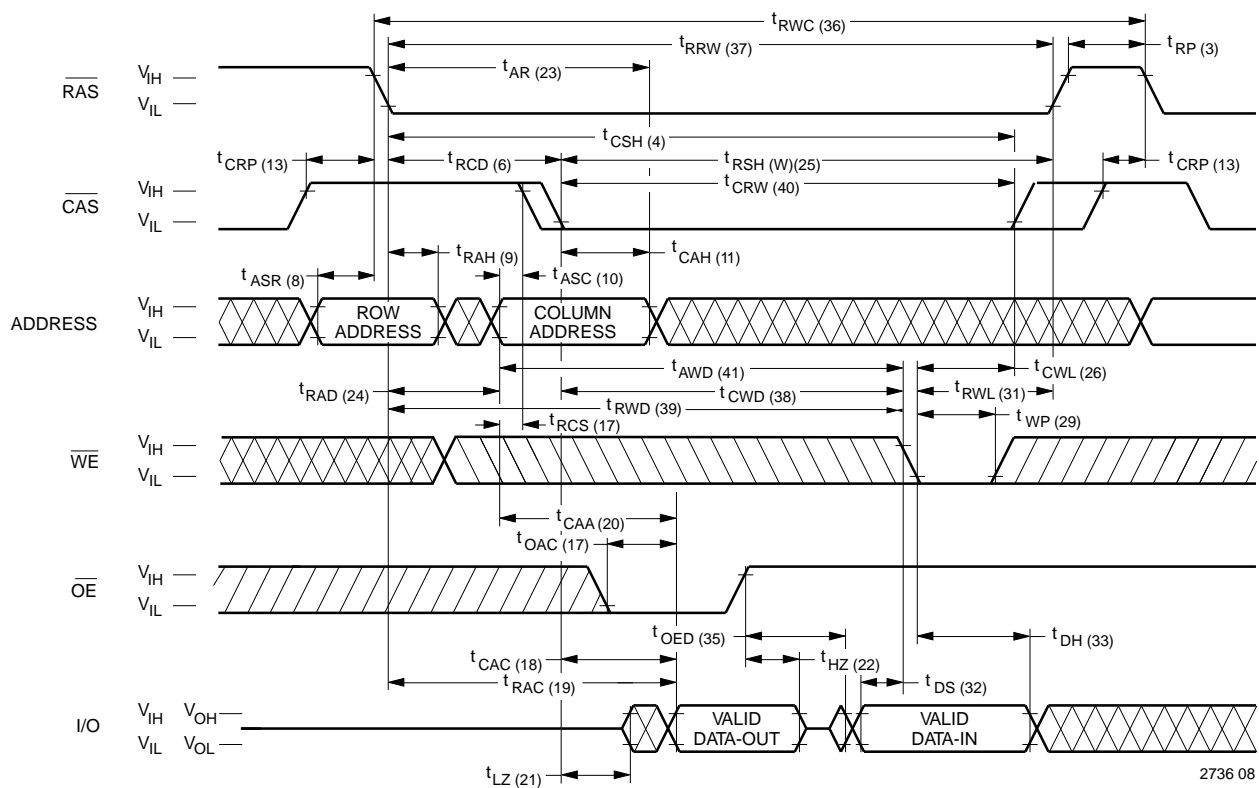
- $t_{AR}$  (23): RAS access time
- $t_{RAS}$  (1): RAS pulse width
- $t_{RC}$  (2): RAS to CAS delay
- $t_{RP}$  (3): RAS precharge time
- $t_{CRP}$  (13): CAS to RAS precharge time
- $t_{RCD}$  (6): RAS to CAS delay
- $t_{CSH}$  (4): CAS setup time
- $t_{RSH}$  (12): RAS setup time
- $t_{CAS}$  (5): CAS pulse width
- $t_{RAD}$  (24): RAS access time
- $t_{RAH}$  (9): RAS hold time
- $t_{ASC}$  (10): Address setup time
- $t_{CAH}$  (11): CAS hold time
- $t_{CAR}$  (44): CAS access time
- $t_{RCH}$  (14): RAS hold time
- $t_{RCS}$  (7): RAS setup time
- $t_{RRH}$  (15): RAS hold time
- $t_{CAA}$  (20): CAS access time
- $t_{OAC}$  (17): Output access time
- $t_{CAC}$  (18): CAS access time
- $t_{RAC}$  (19): RAS access time
- $t_{LZ}$  (21): Load time
- $t_{HZ}$  (22): High impedance time
- $t_{ASR}$  (8): Address setup time
- $t_{RAH}$  (9): RAS hold time
- $t_{ASC}$  (10): Address setup time
- $t_{CAH}$  (11): CAS hold time
- $t_{CAR}$  (44): CAS access time
- $t_{RCH}$  (14): RAS hold time
- $t_{RCS}$  (7): RAS setup time
- $t_{RRH}$  (15): RAS hold time
- $t_{CAA}$  (20): CAS access time
- $t_{OAC}$  (17): Output access time
- $t_{CAC}$  (18): CAS access time
- $t_{RAC}$  (19): RAS access time
- $t_{LZ}$  (21): Load time
- $t_{HZ}$  (22): High impedance time

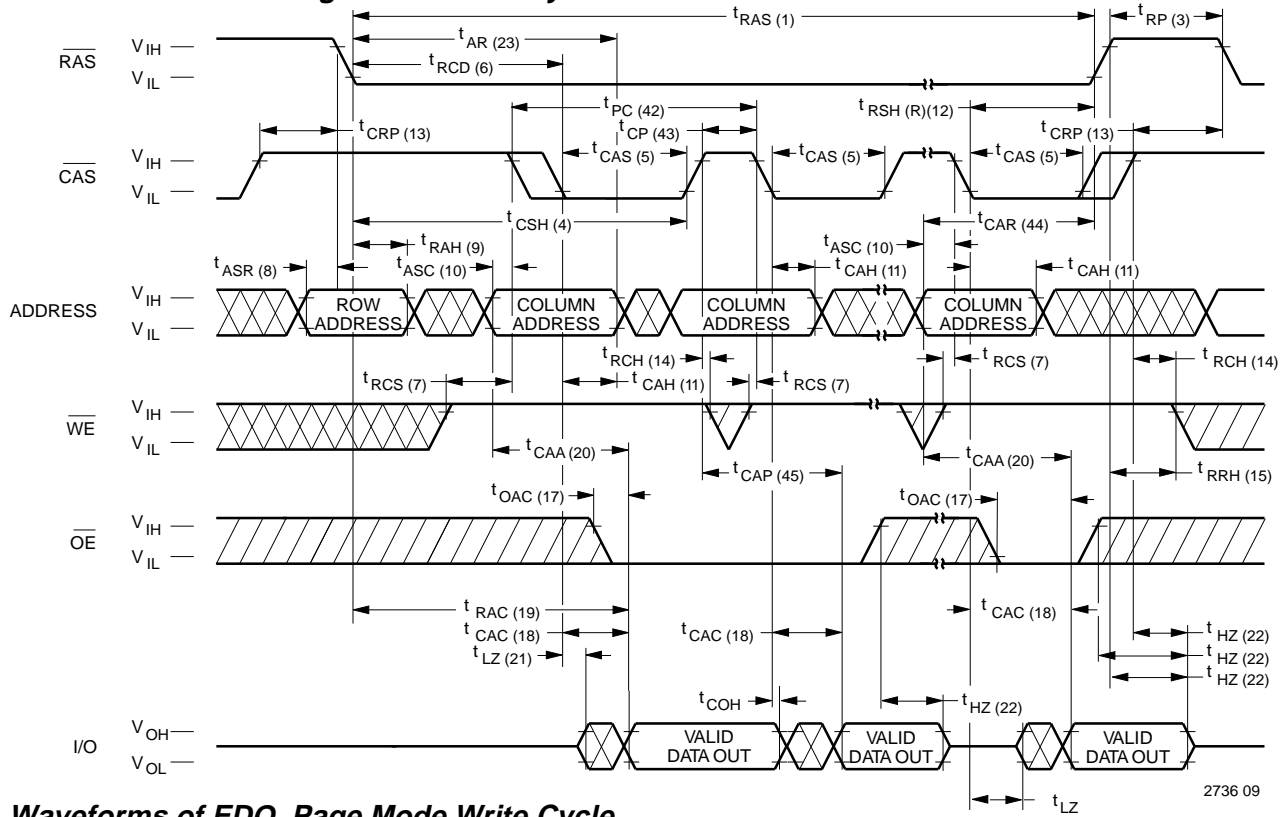
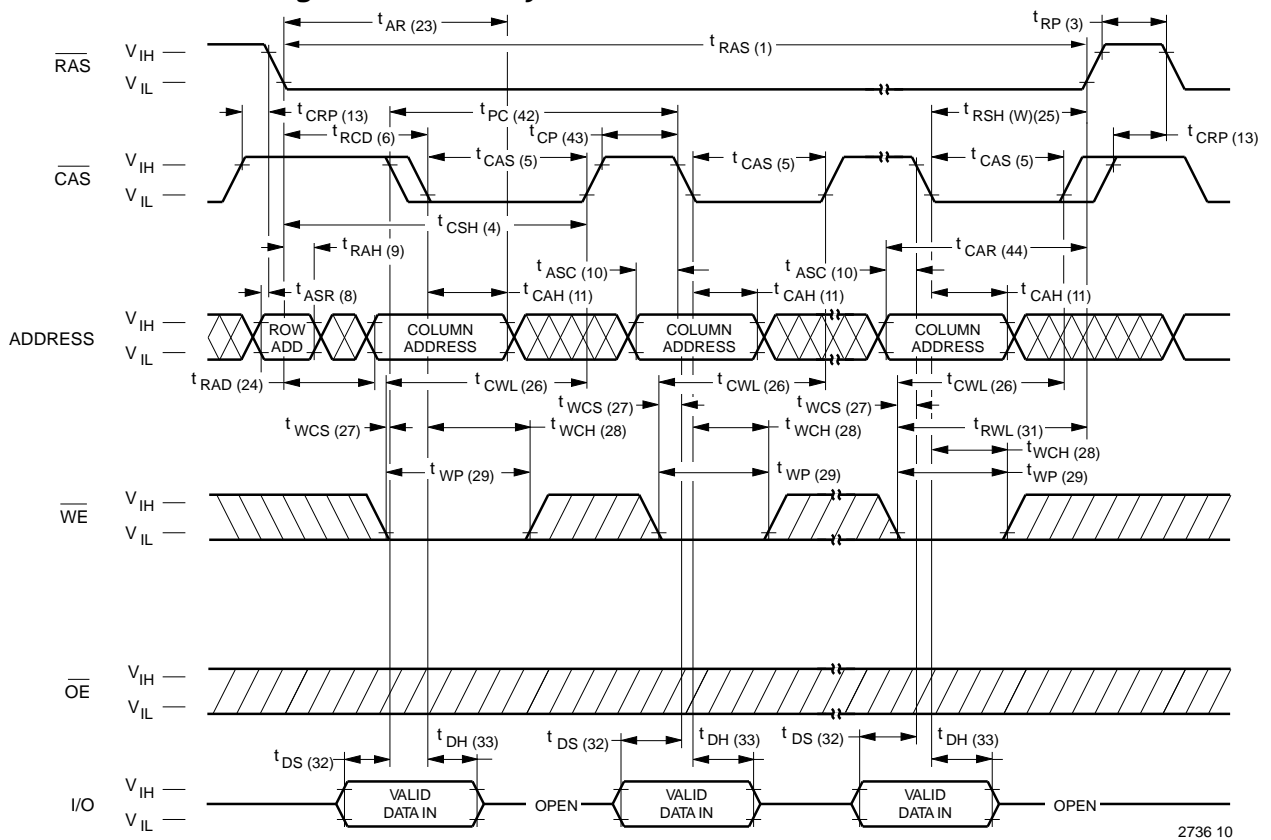
The diagram illustrates the timing relationships for a 2D DRAM array. The signals shown are RAS, CAS, ADDRESS, WE, OE, and I/O. The timing parameters are defined as follows:

- $t_{AR}$  (23): RAS access time.
- $t_{RAS}$  (1): RAS pulse width.
- $t_{RC}$  (2): RAS to CAS delay.
- $t_{RP}$  (3): RAS precharge time.
- $t_{CRP}$  (13): RAS precharge to CAS delay.
- $t_{RCD}$  (6): RAS to CAS delay.
- $t_{CSH}$  (4): CAS setup time.
- $t_{RSH}$  (25): RAS setup time.
- $t_{CAS}$  (5): CAS pulse width.
- $t_{CAR}$  (44): CAS access time.
- $t_{CAH}$  (11): CAS hold time.
- $t_{ASC}$  (10): Address setup time.
- $t_{RAH}$  (9): RAS hold time.
- $t_{ASR}$  (8): Address setup time.
- $t_{RAD}$  (24): RAS access delay.
- $t_{WCH}$  (28): Write command hold time.
- $t_{CWL}$  (26): Write command pulse width.
- $t_{WCR}$  (30): Write command to RAS delay.
- $t_{RWL}$  (31): Write command to RAS delay.
- $t_{DHR}$  (46): Data hold time.
- $t_{DH}$  (33): Data hold time.
- $t_{DS}$  (32): Data setup time.
- $t_{WSR}$ : Write setup time.
- $t_{RWH}$ : RAS hold time.
- $t_{WP}$  (29): Write pulse width.
- $t_{WCS}$  (27): Write command setup time.

Waveforms of  $\overline{\text{OE}}$ -Controlled Write Cycle

## Waveforms of Read-Modify-Write Cycle



**Waveforms of EDO Page Mode Read Cycle****Waveforms of EDO Page Mode Write Cycle**

The timing diagram illustrates the relationship between the RAS, CAS, ADDRESS, WE, OE, and I/O signals for the 2736 1T1 (1T16) device. The signals are shown as digital waveforms with their respective high (V<sub>IH</sub>) and low (V<sub>IL</sub>) levels. The timing parameters are defined as follows:

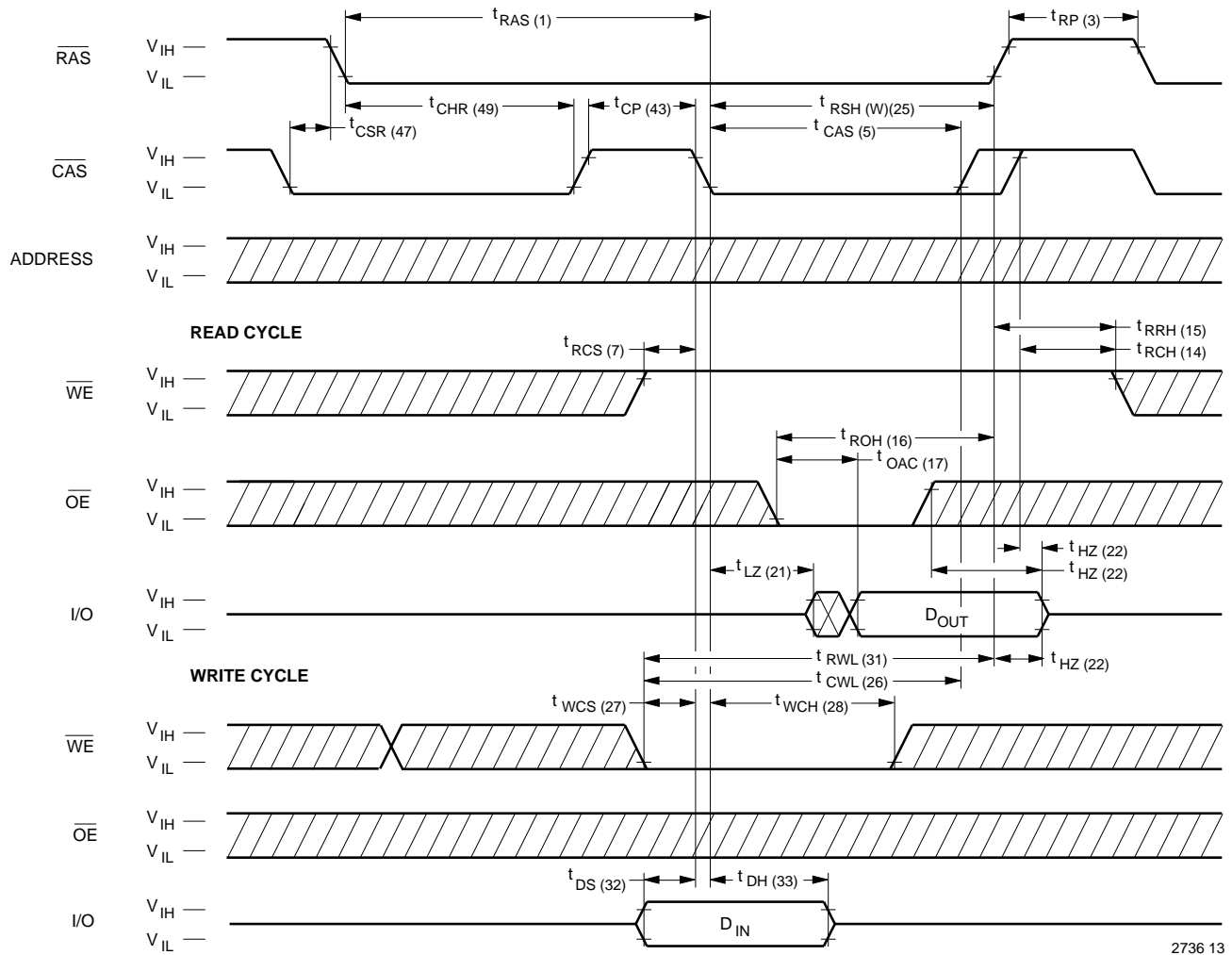
- RAS:**  $t_{RAS}$  (1),  $t_{RCD}$  (6),  $t_{CSH}$  (4),  $t_{RP}$  (3).
- CAS:**  $t_{CAS}$  (5),  $t_{CP}$  (43),  $t_{RSH}$  (W)(25),  $t_{CRP}$  (13),  $t_{CAR}$  (44),  $t_{CAH}$  (11).
- ADDRESS:**  $t_{ASC}$  (10),  $t_{CAH}$  (11),  $t_{RWD}$  (39),  $t_{CWL}$  (26),  $t_{AWD}$  (41),  $t_{WP}$  (29),  $t_{OAC}$  (17),  $t_{EMH}$ ,  $t_{EMS}$ ,  $t_{OED}$  (35),  $t_{CAC}$  (18),  $t_{HZ}$  (22),  $t_{DH}$  (33),  $t_{DS}$  (32),  $t_{LZ}$  (21).
- WE:**  $t_{RCS}$  (7),  $t_{CWL}$  (26),  $t_{AWD}$  (41),  $t_{WP}$  (29),  $t_{OAC}$  (17),  $t_{EMH}$ ,  $t_{EMS}$ ,  $t_{OED}$  (35),  $t_{CAC}$  (18),  $t_{HZ}$  (22),  $t_{DH}$  (33),  $t_{DS}$  (32),  $t_{LZ}$  (21).
- OE:**  $t_{OAC}$  (17),  $t_{EMH}$ ,  $t_{EMS}$ ,  $t_{OED}$  (35),  $t_{CAC}$  (18),  $t_{HZ}$  (22),  $t_{DH}$  (33),  $t_{DS}$  (32),  $t_{LZ}$  (21).
- I/O:**  $t_{LZ}$  (21).

The diagram shows the sequence of operations: RAS and CAS are active low signals. ADDRESS is a bus signal that carries ROW ADDRESS, COLUMN ADDRESS, and DATA. WE is an active low signal used for writing. OE is an active low signal used for reading. I/O is a bidirectional bus signal that carries DATA. The timing parameters are defined for various operations, including RAS and CAS setup and hold times, address setup and hold times, write and read times, and output enable times.

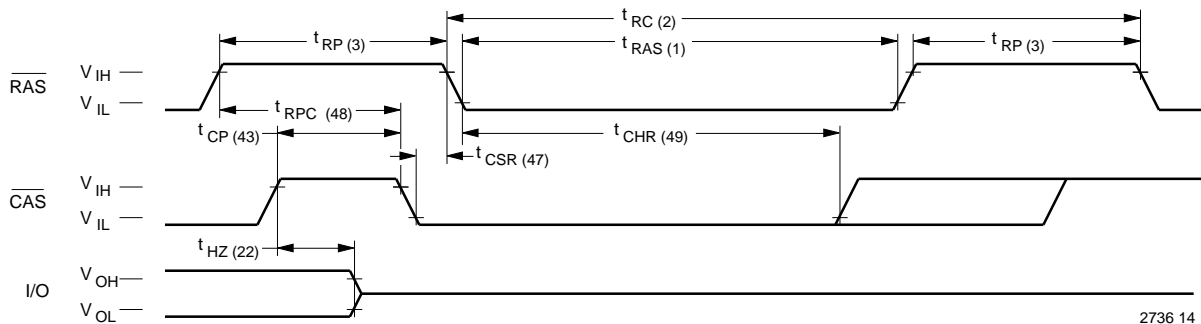
The diagram illustrates the timing relationships for a memory access. It shows three main signals:  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , and ADDRESS. Each signal has two voltage levels,  $V_{IH}$  and  $V_{IL}$ .

- $\overline{\text{RAS}}$  transitions from  $V_{IH}$  to  $V_{IL}$  at the start of the access. Its pulse width is  $t_{\text{RAS}}(1)$ . The time from its falling edge to the start of the ADDRESS pulse is  $t_{\text{RC}}(2)$ . After the ADDRESS pulse,  $\overline{\text{RAS}}$  returns to  $V_{IH}$  for a duration  $t_{\text{RP}}(3)$ .
- $\overline{\text{CAS}}$  transitions from  $V_{IH}$  to  $V_{IL}$  at the start of the access. The time from its falling edge to the start of the ADDRESS pulse is  $t_{\text{CRP}}(13)$ .
- The ADDRESS signal is shown as a bus with  $V_{IH}$  and  $V_{IL}$  levels. The first part of the pulse is labeled "ROW ADD". The time from the start of the ADDRESS pulse to the start of the "ROW ADD" section is  $t_{\text{ASR}}(8)$ . The time from the end of the "ROW ADD" section to the end of the ADDRESS pulse is  $t_{\text{RAH}}(9)$ .

V53C8128H Rev. 1.1 November 1997

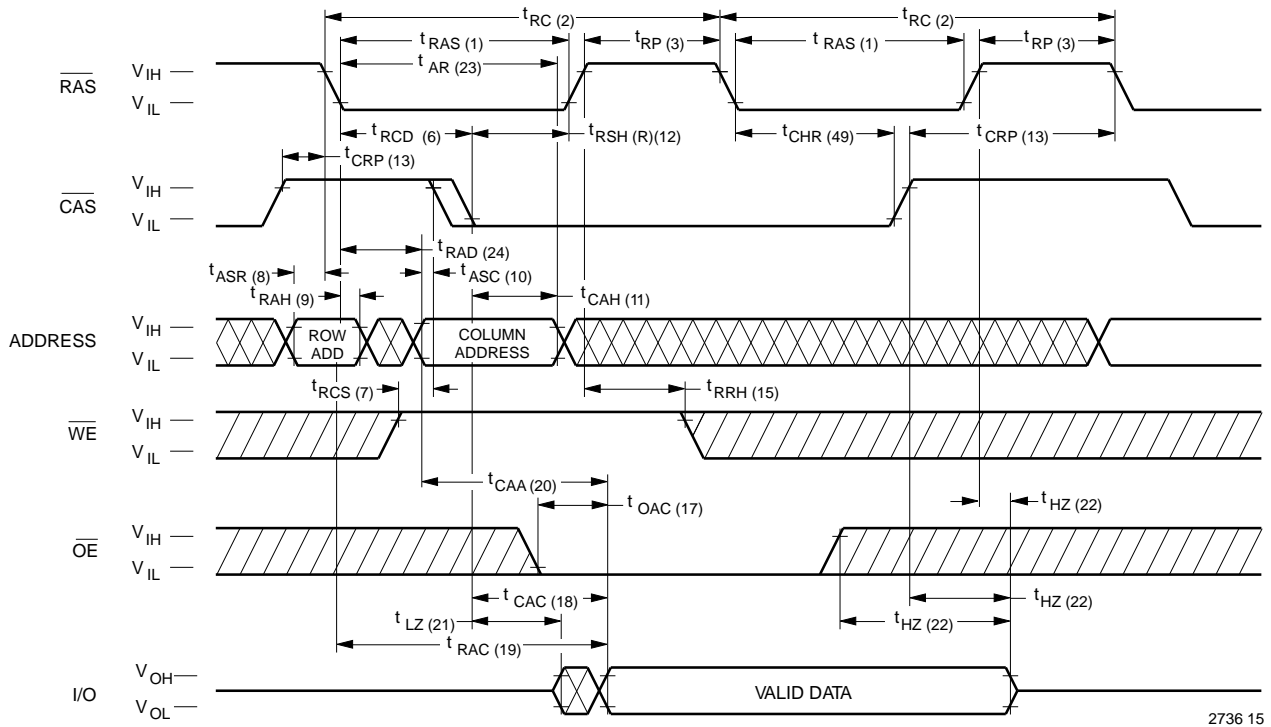
Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Counter Test Cycle

2736 13

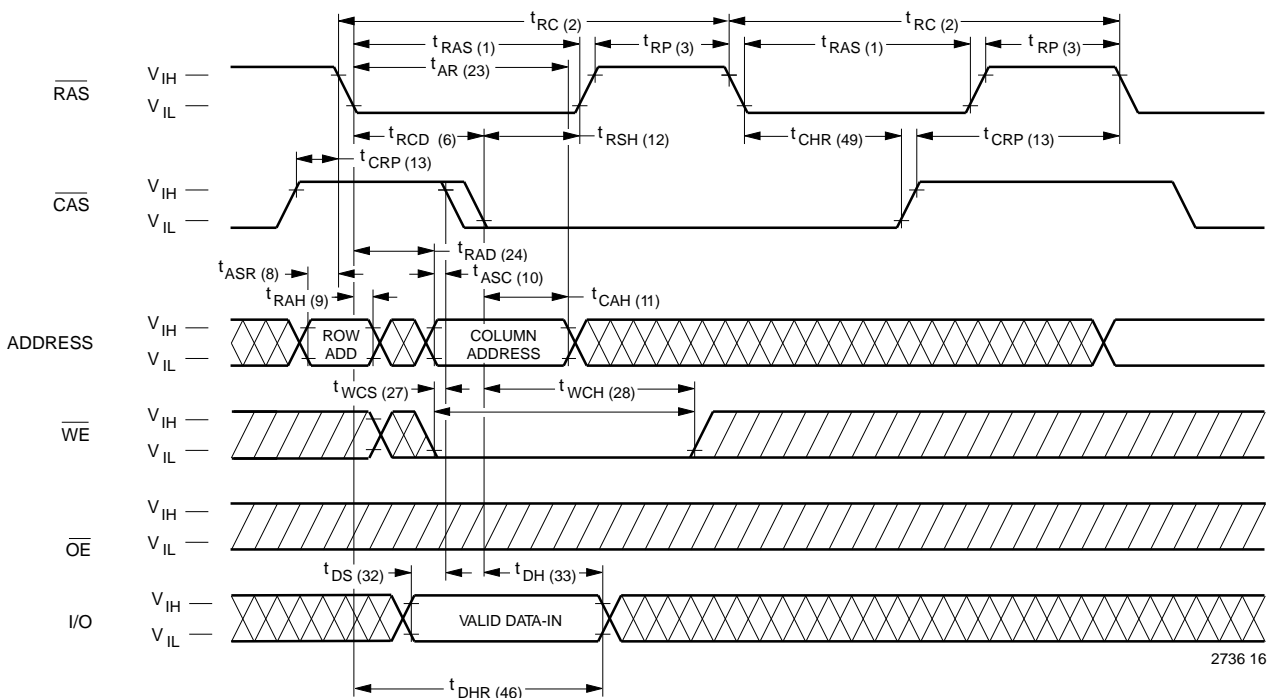
Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle

2736 14

NOTE:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $A_0-A_8$  = Don't care

**Waveforms of Hidden Refresh Cycle (Read)**

2736 15

**Waveforms of Hidden Refresh Cycle (Write)**

2736 16

### Functional Description

The V53C8128H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C8128H reads and writes data by multiplexing an 17-bit address into a 9-bit row and an 8-bit column address. The row address is latched by the Row Address Strobe ( $\overline{\text{RAS}}$ ). The column address “flows through” an internal address buffer and is latched by the Column Address Strobe ( $\overline{\text{CAS}}$ ). Because access time is primarily dependent on a valid column address rather than the precise time that the  $\overline{\text{CAS}}$  edge occurs, the delay time from  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  has little effect on the access time.

### Memory Cycle

A memory cycle is initiated by bringing  $\overline{\text{RAS}}$  low. Any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{\text{RAS}}$  time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time  $t_{\text{RP}}/t_{\text{CP}}$  has elapsed.

### Read Cycle

A Read cycle is performed by holding the Write Enable ( $\overline{\text{WE}}$ ) signal High during a  $\overline{\text{RAS}}/\overline{\text{CAS}}$  operation. The column address must be held for a minimum specified by  $t_{\text{AR}}$ . Data Out becomes valid only when  $t_{\text{OAC}}$ ,  $t_{\text{RAC}}$ ,  $t_{\text{CAA}}$  and  $t_{\text{CAC}}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by  $t_{\text{CAA}}$  when  $t_{\text{RAC}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{OAC}}$  are all satisfied.

### Write Cycle

A Write Cycle is performed by taking  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  low during a  $\overline{\text{RAS}}$  operation. The column address is latched by  $\overline{\text{CAS}}$ . The Write Cycle can be  $\overline{\text{WE}}$  controlled or  $\overline{\text{CAS}}$  controlled depending on whether  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$  falls later. Consequently, the input data must be valid at or before the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. In the  $\overline{\text{CAS}}$ -controlled Write Cycle, when the leading edge of  $\overline{\text{WE}}$  occurs prior to the  $\overline{\text{CAS}}$  low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  will maintain the output in the High-Z state.

In the  $\overline{\text{WE}}$  controlled Write Cycle,  $\overline{\text{OE}}$  must be in the high state and  $t_{\text{OED}}$  must be satisfied.

### Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses ( $A_0$  through  $A_8$ ) with  $\overline{\text{RAS}}$  at least once every 8 ms. Any Read, Write, Read-Modify-Write or  $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle. If  $\overline{\text{CAS}}$  makes a transition from low to high to low after the previous cycle and before  $\overline{\text{RAS}}$  falls,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is activated. The V53C8128H uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  is a “refresh-only” mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  counter test mode is provided to ensure reliable operation of the internal refresh counter.

### Extended Data Out Page Mode

The V53C8128H offers fast access within a row. Unlike ordinary fast page mode DRAM, the V53C8128H output remains active and valid even after  $\overline{\text{CAS}}$  goes high and it will stay valid for 5ns after  $\overline{\text{CAS}}$  changes low. The feature allows the V53C8128H to  $\overline{\text{CAS}}$  cycle faster than ordinary page mode DRAM since the cycle time be short as data access time.

The outputs are disabled at the tHZ time after  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are high. The tHZ time is referenced from rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  whichever occurs last. In addition, high on  $\overline{\text{OE}}$  input and activation of the write-cycle will also disable the outputs.

The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{256}{t_{\text{RC}} + 255 \times t_{\text{PC}}}$$

### Data Output Operation

The V53C8128H Input/Output is controlled by  $\overline{\text{OE}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{RAS}}$ . A  $\overline{\text{RAS}}$  low transition enables the transfer of data to and from the selected row address in the Memory Array. A  $\overline{\text{RAS}}$  high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a  $\overline{\text{RAS}}$  low transition, a  $\overline{\text{CAS}}$  low transition or  $\overline{\text{CAS}}$  low level enables the internal I/O path. A  $\overline{\text{CAS}}$  high transition or a  $\overline{\text{CAS}}$  high level disables the I/O path and the output driver if it is enabled. A  $\overline{\text{CAS}}$  low transition while  $\overline{\text{RAS}}$  is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding  $\overline{\text{OE}}$  high. The  $\overline{\text{OE}}$  signal has no effect on any data stored in the output latches. A  $\overline{\text{WE}}$  low level can also disable the output drivers when  $\overline{\text{CAS}}$  is low. During a Write cycle, if  $\overline{\text{WE}}$  goes low at a time in relationship to  $\overline{\text{CAS}}$  that would normally cause the outputs to be active, it is necessary to use  $\overline{\text{OE}}$  to disable the output drivers prior to the  $\overline{\text{WE}}$  low transition to allow Data In Setup Time ( $t_{\text{DS}}$ ) to be satisfied.

### Power-On

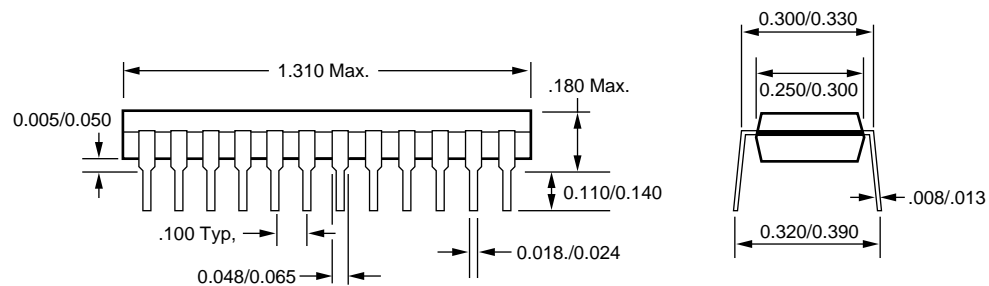
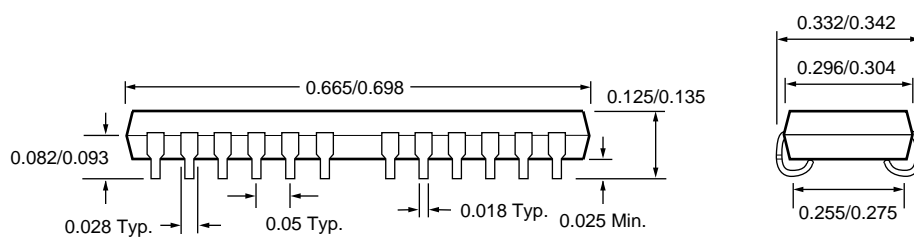
After application of the  $V_{\text{CC}}$  supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the  $V_{\text{CC}}$  current requirement of the V53C8128H is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . If  $\overline{\text{RAS}}$  is low during Power-On, the device will go into an active cycle and  $I_{\text{CC}}$  will exhibit current transients. It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $V_{\text{CC}}$  or be held at a valid  $V_{\text{IH}}$  during Power-On to avoid current surges.

**Table 1. V53C8128H Data Output**  
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{\text{CAS}}$ -Controlled Write Cycle (Early Write)	High-Z
$\overline{\text{WE}}$ -Controlled Write Cycle (Late Write)	$\overline{\text{OE}}$ Controlled. High $\overline{\text{OE}}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{\text{RAS}}$ -only Refresh	High-Z
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle	Data remains as in previous cycle
$\overline{\text{CAS}}$ -only Cycles	High-Z



**Package Outlines**
**24-pin 300 mil PDIP**

**26/24-pin 300 mil SOJ**






**U.S.A.**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0185

**TAIWAN**

7F, NO. 102  
MIN-CHUAN E. ROAD, SEC. 3  
TAIPEI  
PHONE: 011-886-2-545-1213  
FAX: 011-886-2-545-1209

**JAPAN**

RM.302 ANNEX-G  
HIGASHI-NAKANO  
NAKANO-KU, TOKYO 164  
PHONE: 011-81-03-3365-2851  
FAX: 011-81-03-3365-2836

**HONG KONG**

19 DAI FU STREET  
TAIPO INDUSTRIAL ESTATE  
TAIPO, NT, HONG KONG  
PHONE: 011-852-665-4883  
FAX: 011-852-664-7535

1 CREATION ROAD I  
SCIENCE BASED IND. PARK  
HSIN CHU, TAIWAN, R.O.C.  
PHONE: 011-886-35-783344  
FAX: 011-886-35-792838

**U.S. SALES OFFICES****NORTHWESTERN**

3910 NORTH FIRST STREET  
SAN JOSE, CA 95134  
PHONE: 408-433-6000  
FAX: 408-433-0185

**SOUTHWESTERN**

SUITE 200  
5150 E. PACIFIC COAST HWY.  
LONG BEACH, CA 90804  
PHONE: 310-498-3314  
FAX: 310-597-2174

**CENTRAL & SOUTHEASTERN**

604 FIELDWOOD CIRCLE  
RICHARDSON, TX 75081  
PHONE: 214-690-1402  
FAX: 214-690-0341

**NORTHEASTERN**

SUITE 436  
20 TRAFALGAR SQUARE  
NASHUA, NH 03063  
PHONE: 603-889-4393  
FAX: 603-889-9347

The information in this document is subject to change without notice.

MOSEL-VITELIC makes no commitment to update or keep current the information contained in this document. No part of this document may be copied or reproduced in any form or by any means without the prior written consent of MOSEL-VITELIC.

MOSEL-VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. MOSEL-VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.