V53C832L HIGH PERFORMANCE 3.3 VOLT 256K X 32 EDO PAGE MODE CMOS DYNAMIC RAM

PRELIMINARY

HIGH PERFORMANCE	30	35	40
Max. $\overline{RAS}$ Access Time, (t_{RAC})	30 ns	35 ns	40 ns
Max. Column Address Access Time, (t_{CAA})	16 ns	18 ns	20 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	12 ns	14 ns	15 ns
Min. Read/Write Cycle Time, (t_{RC})	65 ns	70 ns	75 ns

Features

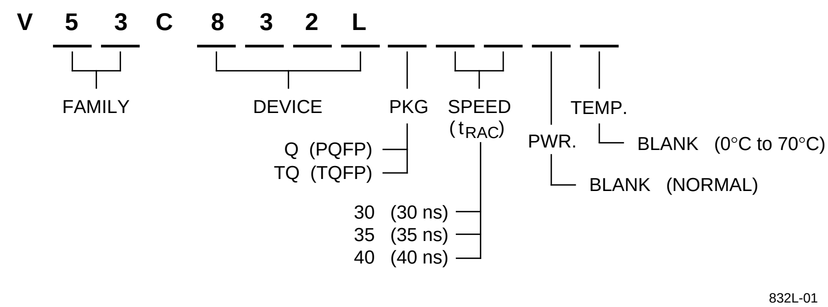
- 256K x 32-bit organization
- EDO Page Mode for a sustained data rate of 83 MHz
- $\overline{RAS}$ access time: 30, 35, 40 ns
- Four $\overline{CAS}$ Inputs for Byte Read and Byte Write Control
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Refresh Interval: 512 cycles/8 ms
- Available in 100-pin PQFP and 100-pin LQFP packages
- Single +3.3V ± 0.3V Power Supply
- TTL Interface

Description

The V53C832L is a high speed 262,144 x 32 bit high performance CMOS dynamic random access memory. The V53C832L offers a combination of unique features including: EDO Page Mode operation for higher sustained bandwidth with Page Mode cycle times as short as 12ns. All inputs are TTL compatible. Input and output capacitance is significantly lowered to increase performance and minimize loading. These features make the V53C832L ideally suited for a wide variety of high performance computer systems and peripheral applications.

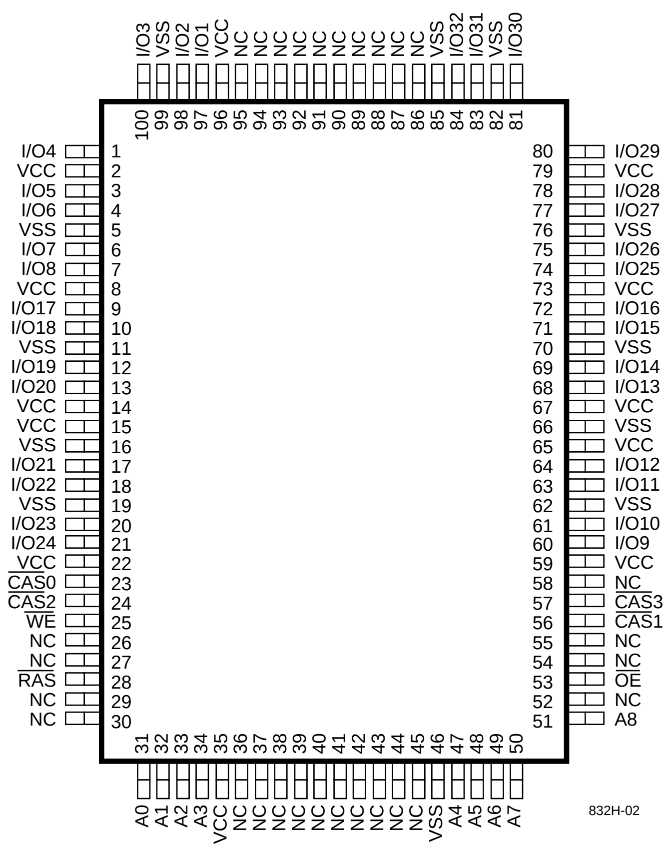
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	Q	TQ	30	35	40	Std.	
0°C to 70°C	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
PQFP	Q	100
TQFP	TQ	100

100-Pin PQFP/TQFP PIN CONFIGURATION Top View



Pin Table

A_0–A_8	Address Inputs
RAS	Row Address Strobe
$\overline{CAS}0$	Column Address Strobe for First Byte (I/O_1–I/O_8)
$\overline{CAS}1$	Column Address Strobe for Second Byte (I/O_9–I/O_{16})
$\overline{CAS}2$	Column Address Strobe for Third Byte (I/O_{17}–I/O_{24})
$\overline{CAS}3$	Column Address Strobe for Fourth Byte (I/O_{25}–I/O_{32})
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_{32}	Data Input, Output
V_{CC}	+3.3V Supply
V_{SS}	0V Supply
NC	No Connect

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias .... –10°C to +80°C
Storage Temperature (plastic)..... –55°C to +125°C
Voltage Relative to V_{SS} ....–1.0 V to +4.6V
Data Output Current .... 50 mA
Power Dissipation... 1.0 W

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Capacitance**

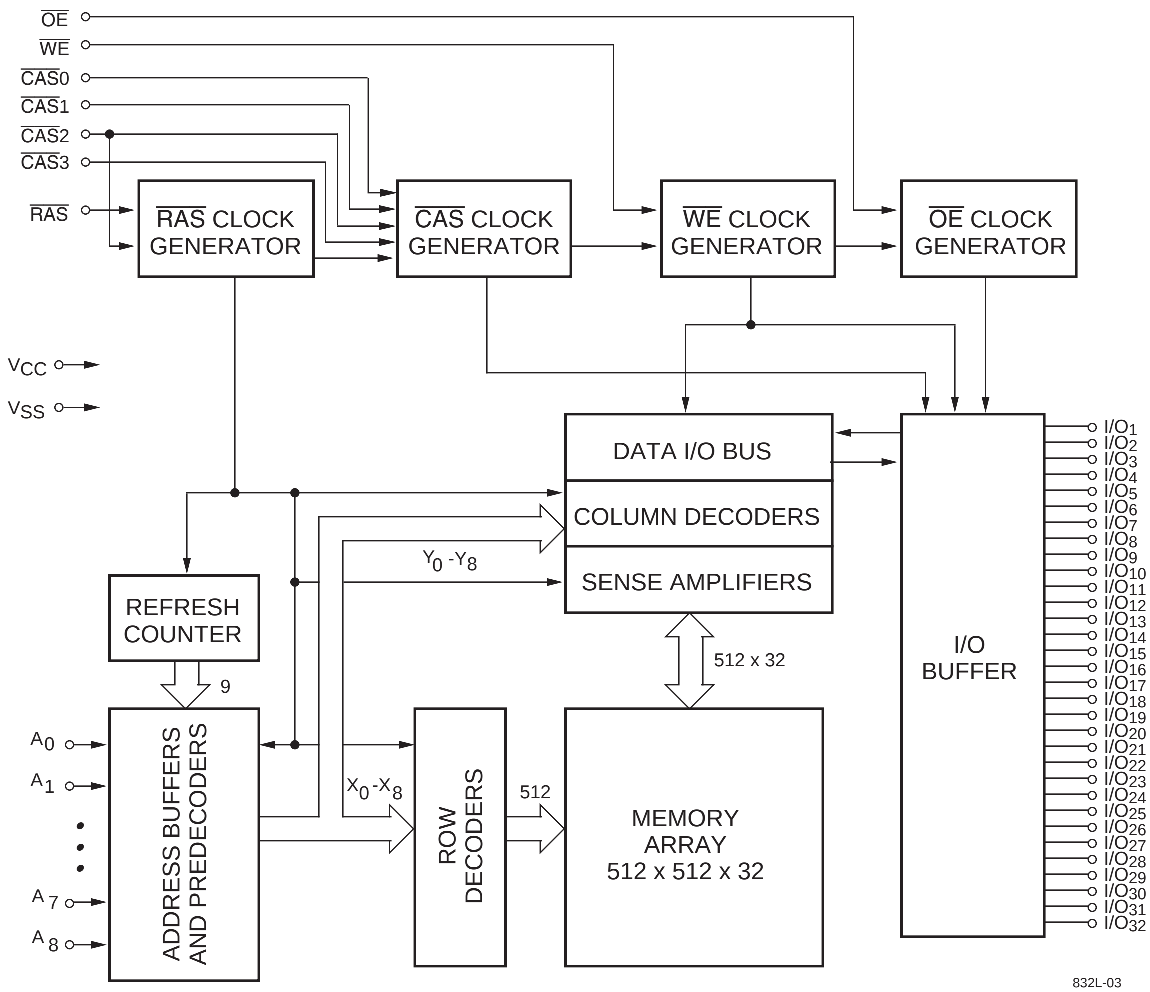
$T_A = 25°C$, $V_{CC} = 3.3V \pm 0.3V$, $V_{SS} = 0$ V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

***Note:** Capacitance is sampled and not 100% tested.

Block Diagram

256K x 32



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Time	V53C832L			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10		10	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	µA	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	30			130	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		35			120			
		40			110			
I_{CC2}	V_{CC} Supply Current, TTL Standby				4	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	30			130	mA	$t_{RC} = t_{RC}$ (min.)	2
		35			120			
		40			110			
I_{CC4}	V_{CC} Supply Current, EDO Page Mode Operation	30			120	mA	Minimum Cycle	1, 2
		35			110			
		40			100			
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled				2.0	mA	$\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				2.0	mA	$\overline{RAS} \geq V_{CC} - 0.2$ V, $\overline{CAS} \geq V_{CC} - 0.2$ V, All other inputs $\geq V_{SS}$	
V_{CC}	Supply Voltage		3.0	3.3	3.6	V		
V_{IL}	Input Low Voltage		–1		0.8	V		3
V_{IH}	Input High Voltage		2.4		$V_{CC}+1$	V		3
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2 mA	
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –2 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	Symbol	Parameter	30		35		40		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	30	75K	35	75K	40	75K	ns	
2	t_{RC}	Read or Write Cycle Time	65		70		75		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	25		25		25		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	30		35		40		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	5		6		7		ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	20	16	24	17	28	ns	
7	t_{RCS}	Read Command Setup Time	0		0		0		ns	4
8	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	5		6		7		ns	
10	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	5		5		5		ns	
12	$t_{RSH (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		10		ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	6		7		8		ns	
17	t_{OAC}	Access Time from $\overline{OE}$		10		11		12	ns	12
18	t_{CAC}	Access Time from $\overline{CAS}$		10		11		12	ns	6,7,14
19	t_{RAC}	Access Time from $\overline{RAS}$		30		35		40	ns	6, 8, 9
20	t_{CAA}	Access Time from Column Address		16		18		20	ns	6,7,10
21	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
22	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	5	0	6	0	6	ns	16
23	t_{AR}	Column Address Hold Time from$\overline{RAS}$	26		28		30		ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	14	11	17	12	20	ns	11
25	$t_{RSH (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	10		10		10		ns	
26	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10		11		12		ns	
27	t_{WCS}	Write Command Setup Time	0		0		0		ns	12, 13
28	t_{WCH}	Write Command Hold Time	5		5		5		ns	
29	t_{WP}	Write Pulse Width	5		5		5		ns	
30	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	26		28		30		ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10		11		12		ns	
32	t_{DS}	Data in Setup Time	0		0		0		ns	14
33	t_{DH}	Data in Hold Time	5		5		5		ns	14

AC Characteristics (Cont'd)

#	Symbol	Parameter	30 Min.	30 Max.	35 Min.	35 Max.	40 Min.	40 Max.	Unit	Notes
34	t_{WOH}	Write to $\overline{OE}$ Hold Time	5		5		6		ns	14
35	t_{OED}	$\overline{OE}$ to Data Delay Time	5		5		6		ns	14
36	t_{RWC}	Read-Modify-Write Cycle Time	100		105		110		ns	
37	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	65		70		75		ns	
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	26		28		30		ns	12
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	50		54		58		ns	12
40	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	44		46		48		ns	
41	t_{AWD}	Col. Address to $\overline{WE}$ Delay	32		35		38		ns	12
42	t_{PC}	EDO Fast Page Mode Read or Write Cycle Time	12		14		15		ns	
43	t_{CP}	$\overline{CAS}$ Precharge Time	3		4		5		ns	
44	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	16		18		20		ns	
45	t_{CAP}	Access Time from Column Precharge		19		21		23	ns	7
46	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	26		28		30		ns	
47	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$- before-$\overline{RAS}$Refresh	10		10		10		ns	
48	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
49	t_{CHR}	$\overline{CAS}$ Hold Time CAS-before-$\overline{RAS}$ Refresh	7		8		8		ns	
50	t_{PCM}	EDO Page Mode Read-Modify-Write Cycle Time	56		58		60		ns	
51	t_{COH}	Output Hold After $\overline{CAS}$ Low	5		5		5		ns	
52	t_{OES}	$\overline{OE}$ Low to $\overline{CAS}$ HIGH setup time	5		5		5		ns	
53	t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$ during Read-Modify Write Cycle	10		10		10		ns	
54	t_{OEP}	$\overline{OE}$ High Pulse Width	10		10		10		ns	
55	t_T	Transition Time (Rise and Fall)	1.5	50	1.5	50	1.5	50	ns	15
56	t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions. Specified I_{CC} (max.) is measured with a maximum of two transitions per address cycle in EDO Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) $\geq V_{SS}$ and V_{IH} (max.) $\leq V_{CC}$.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL inputs and 50 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 3 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

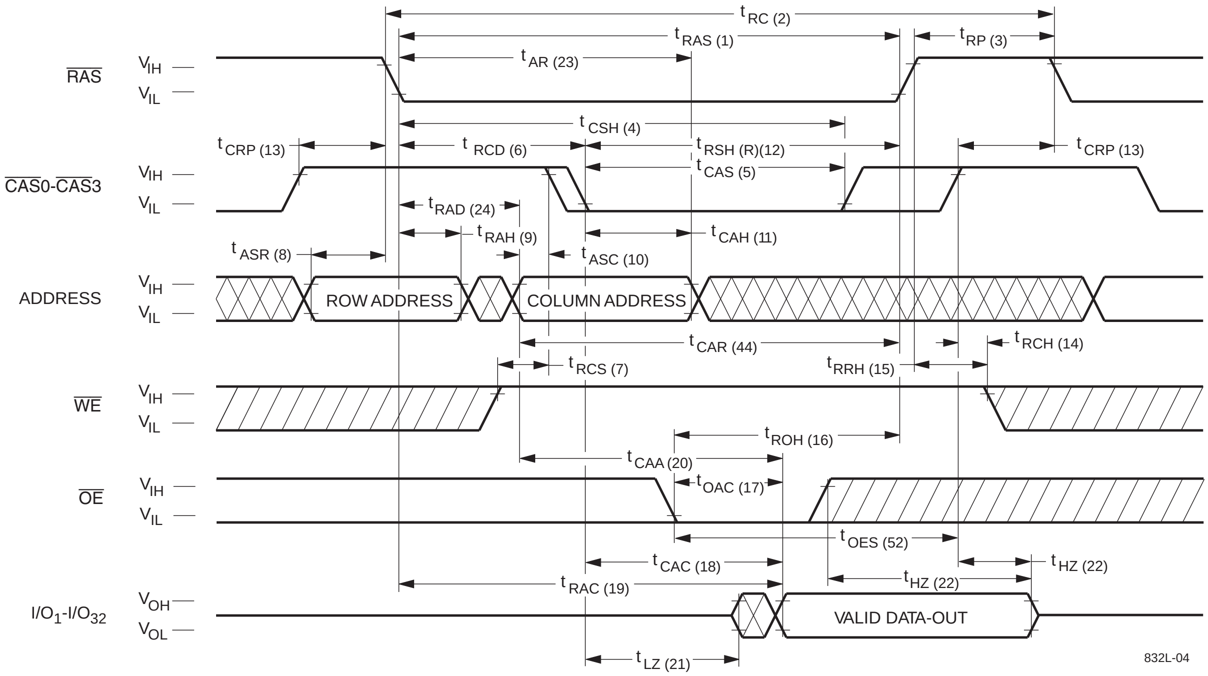
Truth Table

Function	$\overline{RAS}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$	$\overline{WE}$	$\overline{OE}$	ADDRESS	I/O	Notes
Standby	H	H	H	H	H	X	X	X	High-Z	
Read: Double Word	L	L	L	L	L	H	L	ROW/COL	Data Out	
Read: First Byte	L	L	H	H	H	H	L	ROW/COL	I/O_1–I/O_8 = Data Out I/O_9–I/O_{32} = High-Z	
Read: Second Byte	L	H	L	H	H	H	L	ROW/COL	I/O_1–I/O_8 = High-Z I/O_9–I/O_{16} = Data Out I/O_{17}–I/O_{32} = High-Z	
Read: Third Byte	L	H	H	L	H	H	L	ROW/COL	I/O_1–I/O_{16} = High-Z I/O_{17}–I/O_{23} = Data Out I/O_{24}–I/O_{32} = High-Z	
Read: Fourth Byte	L	H	H	H	L	H	L	ROW/COL	I/O_1–I/O_{23} = High-Z I/O_{24}–I/O_{32} = Data Out	
Write: Double Word (Early-Write)	L	L	L	L	L	L	X	ROW/COL	Data In	
Write: First Byte (Early)	L	L	H	H	H	L	X	ROW/COL	I/O_1–I/O_8 = Data In I/O_9–I/O_{32} = X	
Write: Second Byte (Early)	L	H	L	H	H	L	X	ROW/COL	I/O_1–I/O_8 = X I/O_9–I/O_{16} = Data In I/O_{17}–I/O_{32} = X	
Write: Third Byte (Early)	L	H	H	L	H	L	X	ROW/COL	I/O_1–I/O_{16} = X I/O_{17}–I/O_{23} = Data In I/O_{24}–I/O_{32} = X	
Write: Fourth Byte (Early)	L	H	H	H	L	L	X	ROW/COL	I/O_1–I/O_{23} = X I/O_{24}–I/O_{32} = Data In	
Read-Write	L	L	L	L	L	H→L	L→H	ROW/COL	Data Out, Data In	1,2
EDO Page-Mode Read First Cycle	L	H→L	H→L	H→L	H→L	H	L	ROW/COL	Data Out	2
EDO Page-Mode Read Subsequent Cycles	L	H→L	H→L	H→L	H→L	H	L	COL	Data Out	2
EDO Page-Mode Write First Cycle	L	H→L	H→L	H→L	H→L	L	X	ROW/COL	Data In	2
EDO Page-Mode Write Subsequent Cycles	L	H→L	H→L	H→L	H→L	L	X	COL	Data In	2
EDO Page-Mode Read-Write First Cycles	L	H→L	H→L	H→L	H→L	H→L	L→H	ROW/COL	Data Out, Data In	2
EDO Page-Mode Read-Write Subsequent Cycles	L	H→L	H→L	H→L	H→L	H→L	L→H	COL	Data Out, Data In	2
Hidden Refresh Read	L→H→L	L	L	L	L	H	L	ROW/COL	Data-Out	2
$\overline{RAS}$-Only Refresh	L	H	H	H	H	X	X	ROW	High-Z	
CBR Refresh	H→L	L	L	L	L	X	X	X	High-Z	3

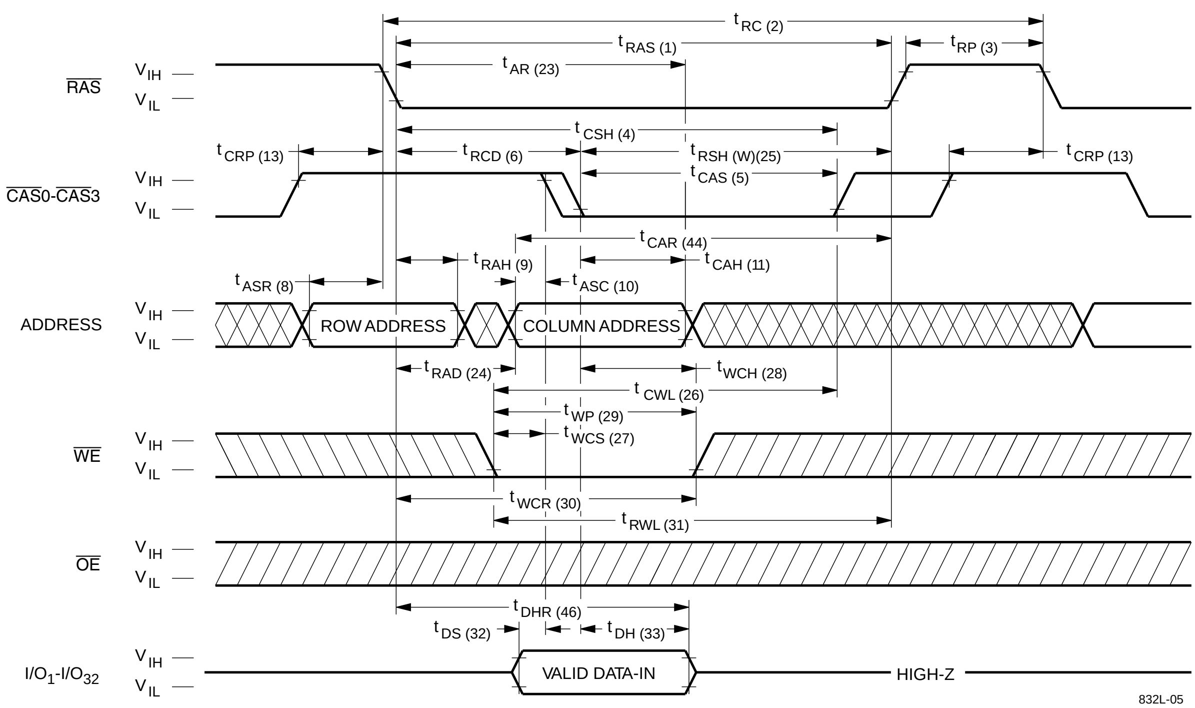
Notes:

1. Byte Write cycles $\overline{CAS}$0, $\overline{CAS}$1, $\overline{CAS}$2, or $\overline{CAS}$3 active.
2. Byte Read cycles $\overline{CAS}$0, $\overline{CAS}$1, $\overline{CAS}$2, or $\overline{CAS}$3 active.
3. Only one of the four $\overline{CAS}$ ($\overline{CAS}$0, $\overline{CAS}$1, $\overline{CAS}$2, or $\overline{CAS}$3) must be active.

Waveforms of Read Cycle

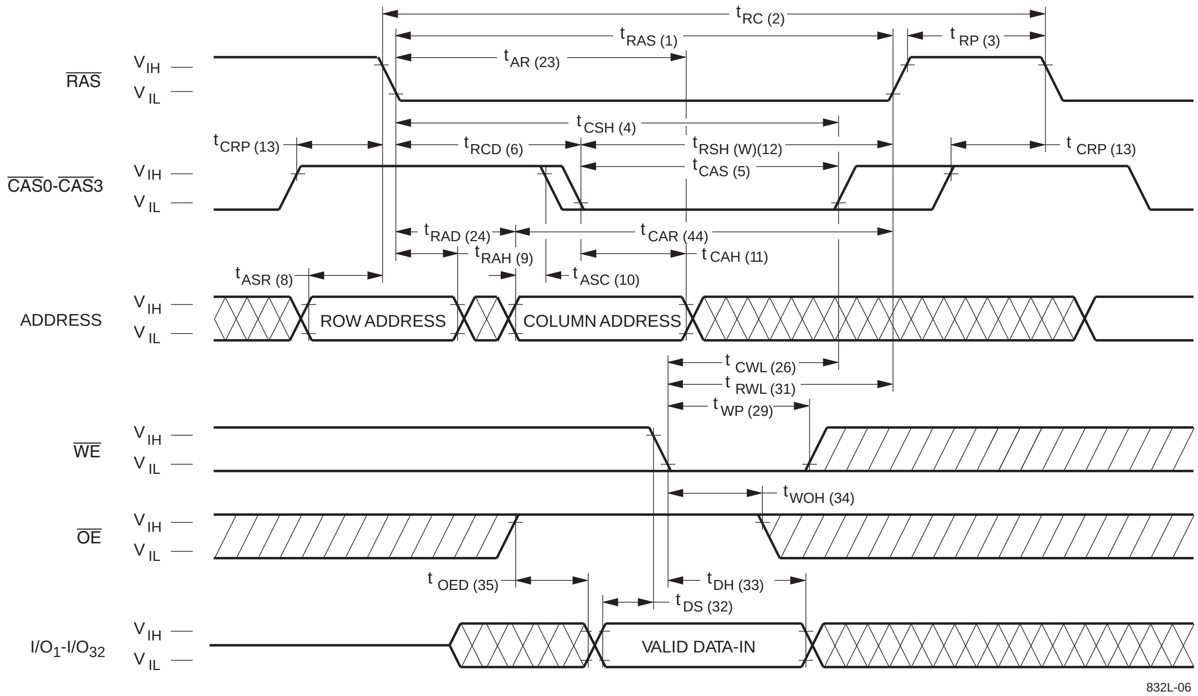


Waveforms of Early Write Cycle

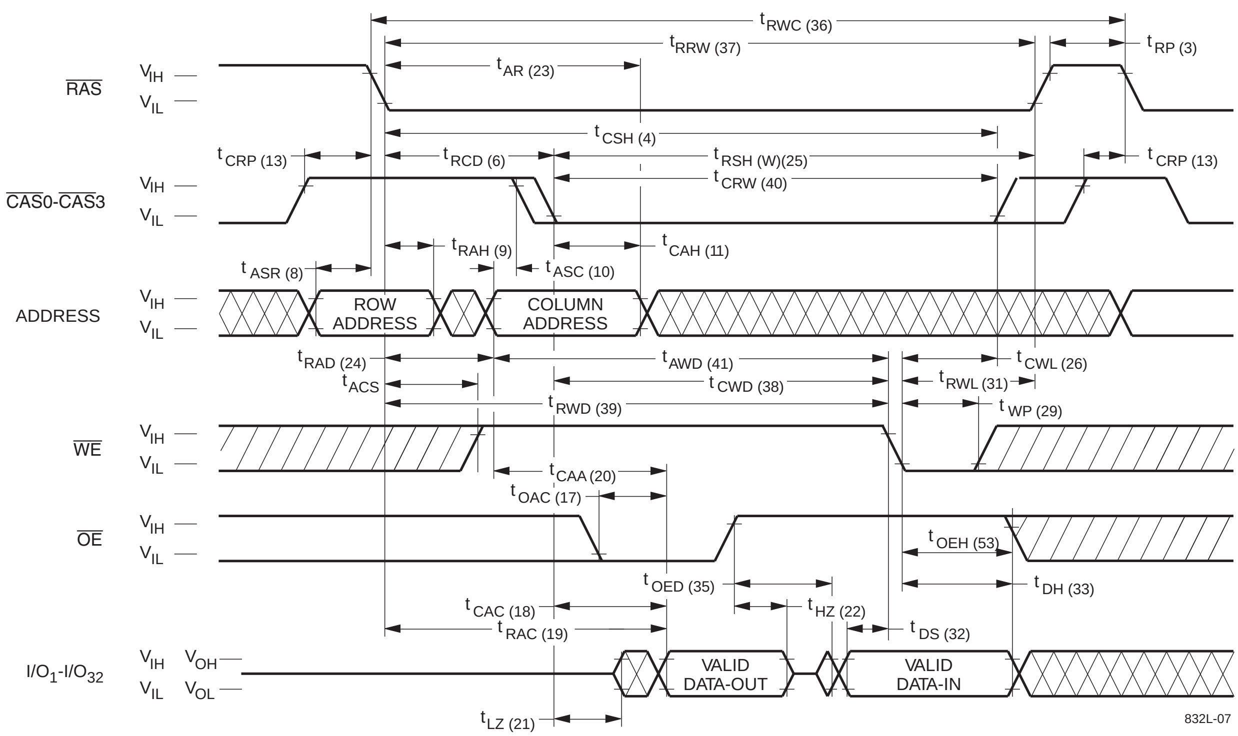


Don't Care Undefined

Waveforms of $\overline{OE}$-Controlled Write Cycle

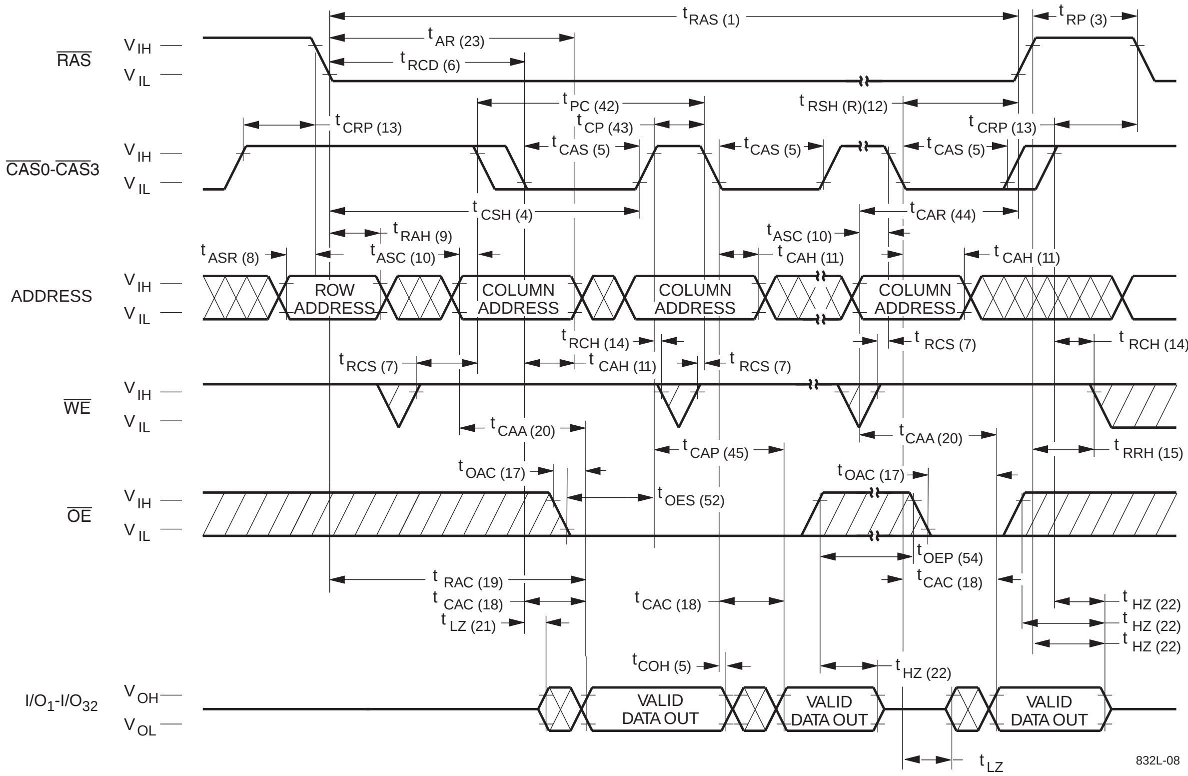


Waveforms of Read-Modify-Write Cycle

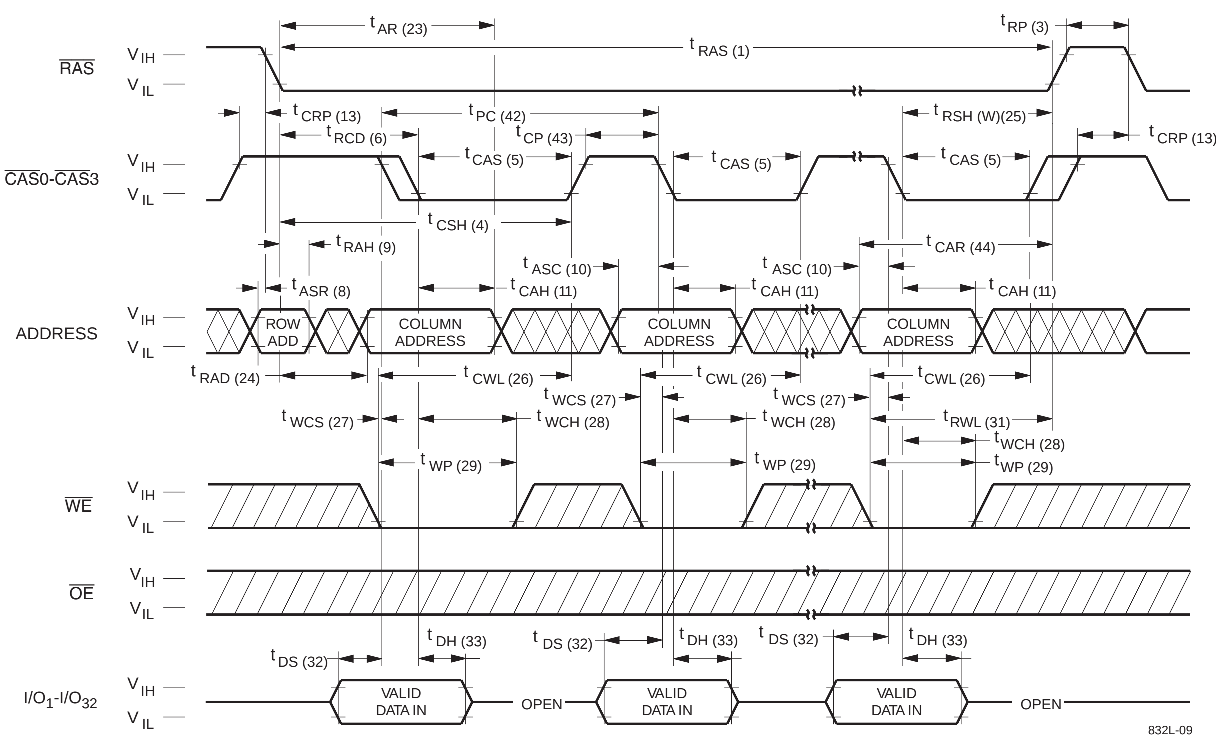


Don't Care   Undefined

Waveforms of EDO Page Mode Read Cycle

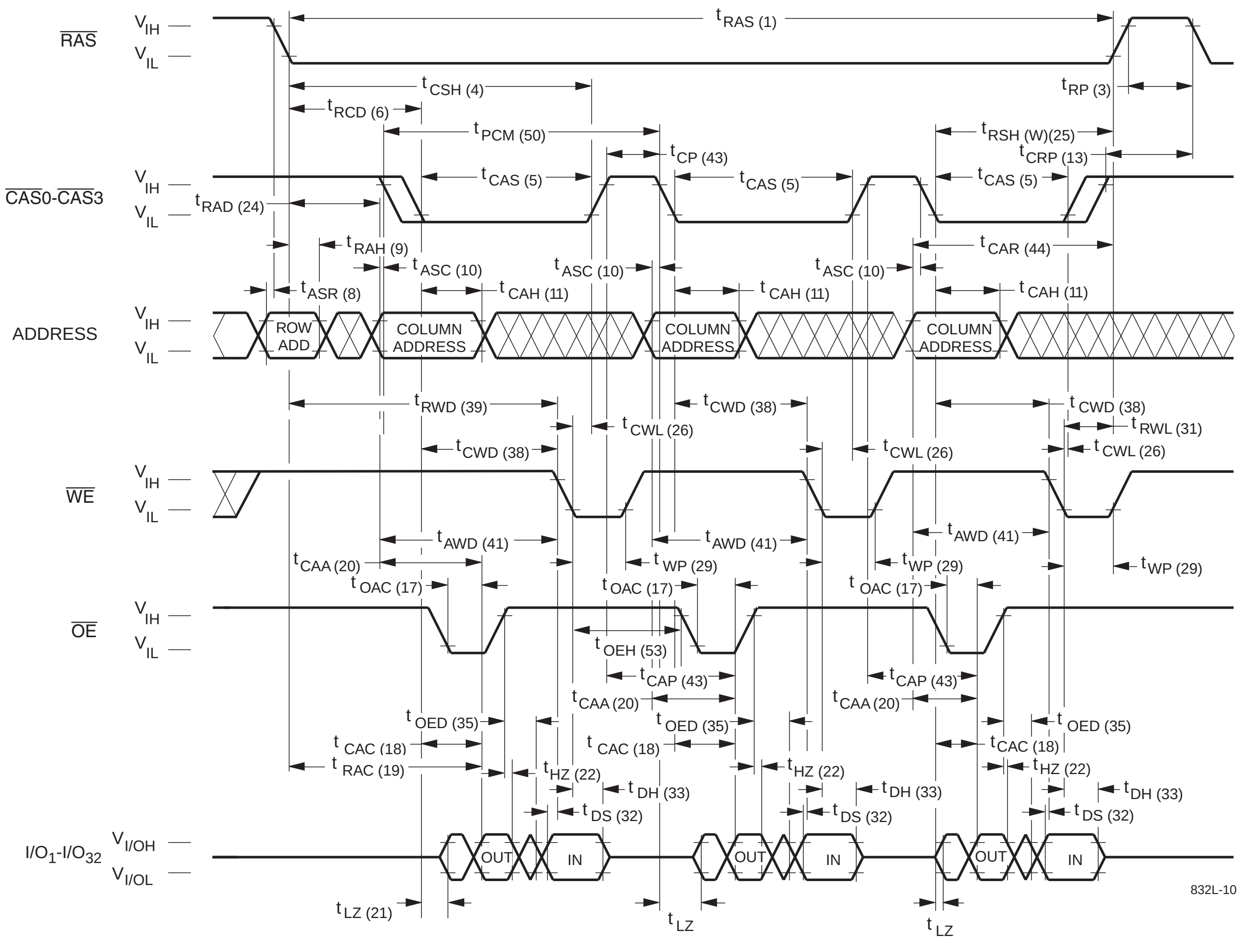


Waveforms of EDO Page Mode Write Cycle

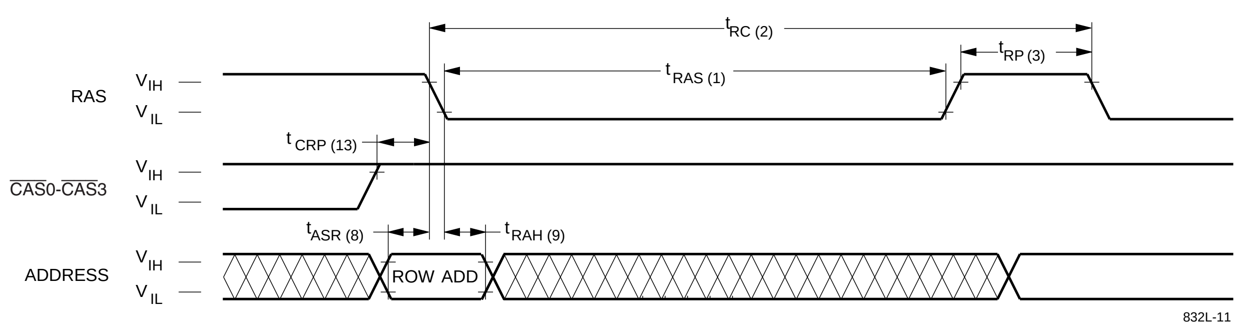


Don't Care Undefined

Waveforms of EDO Page Mode Read-Write Cycle



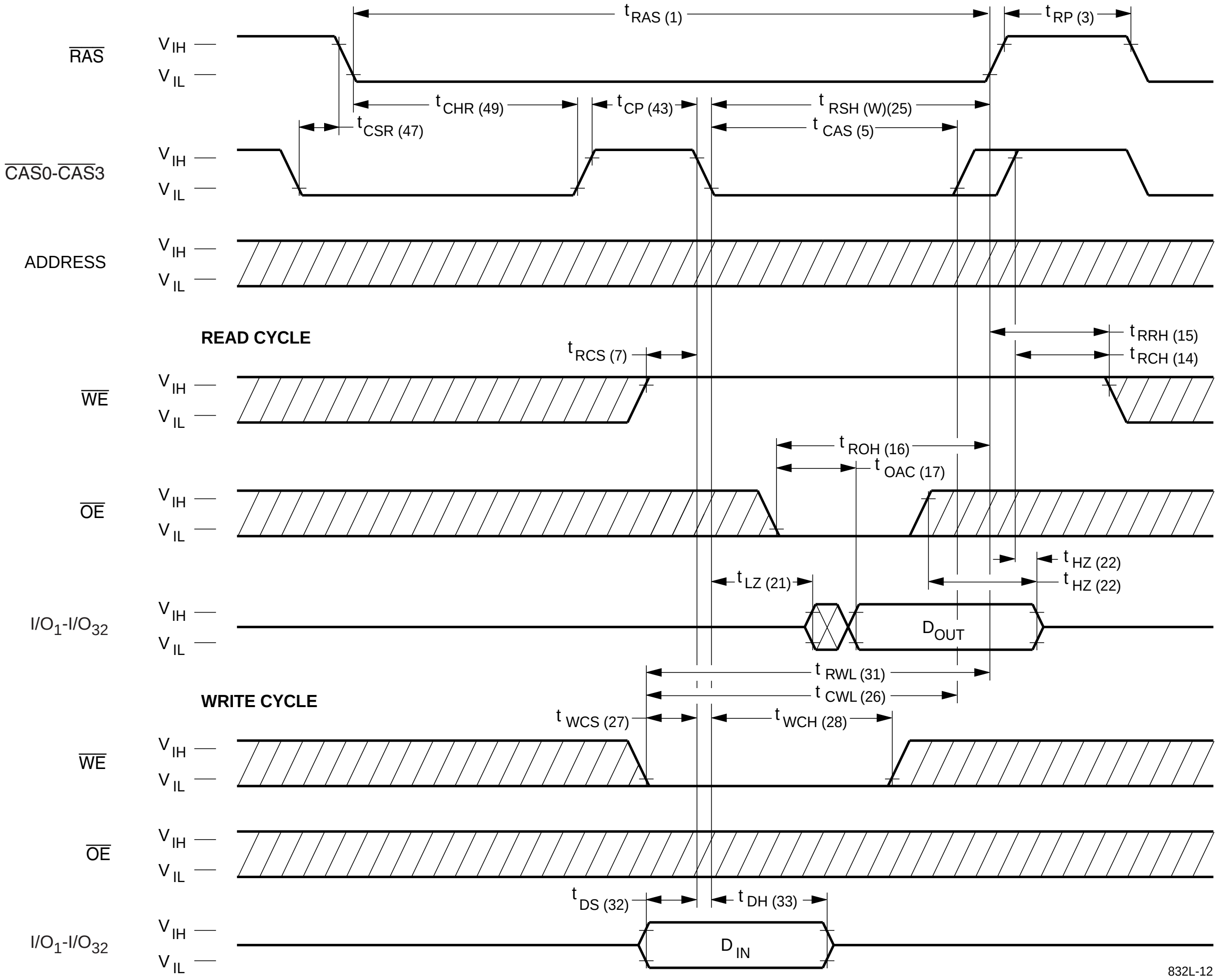
Waveforms of $\overline{RAS}$-Only Refresh Cycle



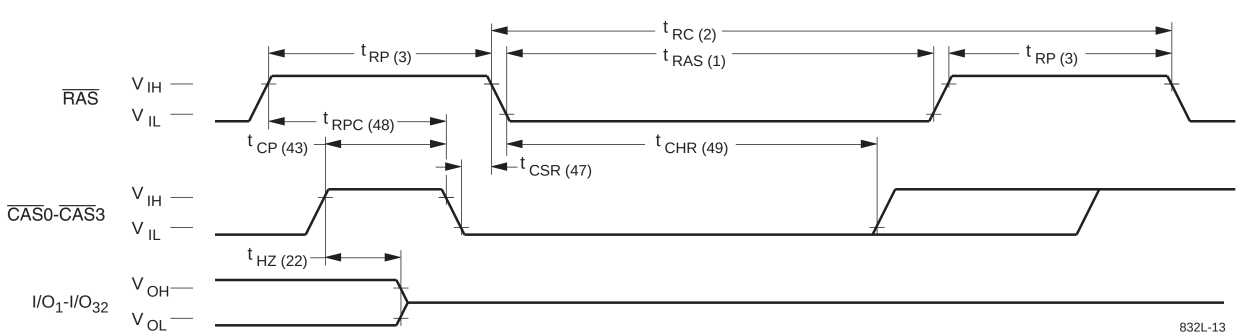
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Don't Care   Undefined

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



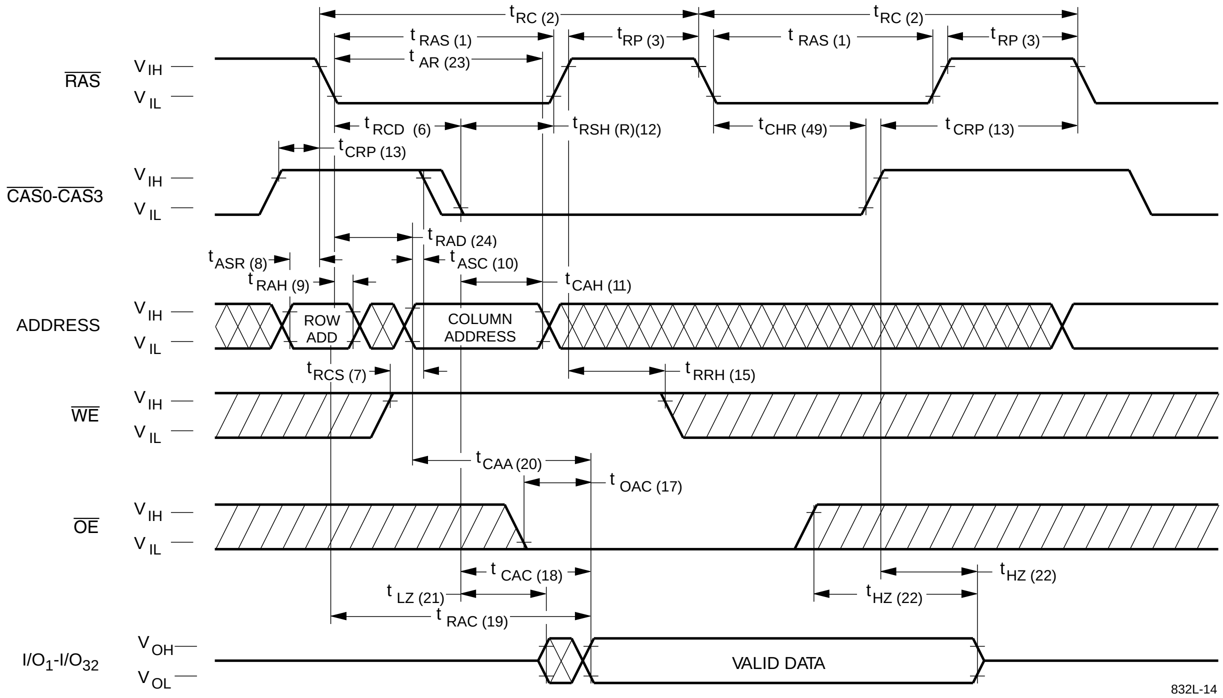
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



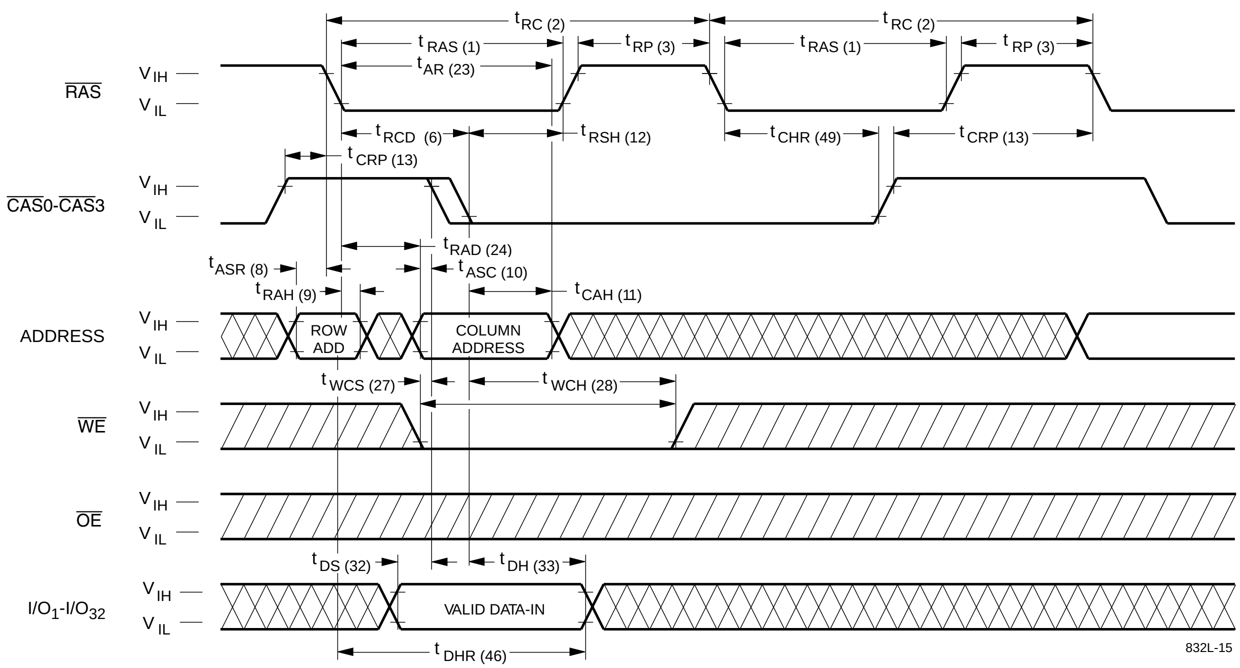
NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_8 = Don't care

Don't Care Undefined

Waveforms of Hidden Refresh Cycle (Read)

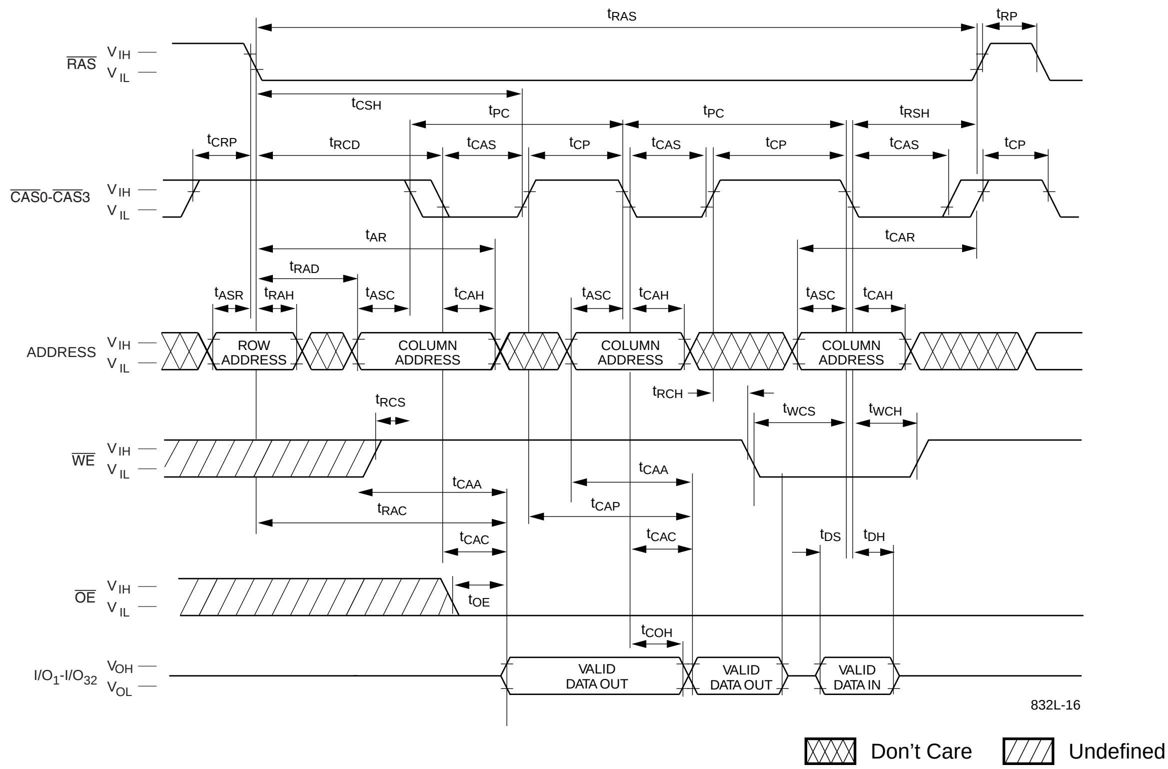


Waveforms of Hidden Refresh Cycle (Write)



Don't Care Undefined

Waveforms of EDO-Page-Mode Read-Early-Write Cycle (Pseudo Read-Modify-Write)



Functional Description

The V53C832L is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C832L reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address.

The V53C832L has four $\overline{CAS}$ inputs. $\overline{CAS}0$ controls I/O_1–I/O_8; $\overline{CAS}1$ controls I/O_9–I/O_{16}; $\overline{CAS}2$ controls I/O_{17}–I/O_{24}; and $\overline{CAS}3$ controls I/O_{23}–I/O_{32}. These four $\overline{CAS}$ inputs control Byte Read and Byte Write.

The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address “flows through” an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Extended Data Output Page Mode

EDO Page operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to re-apply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer. During EDO operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Hyper Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

EDO provides a sustained data rate of 83 MHz for applications that require high bandwidth such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C832L Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{CC} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

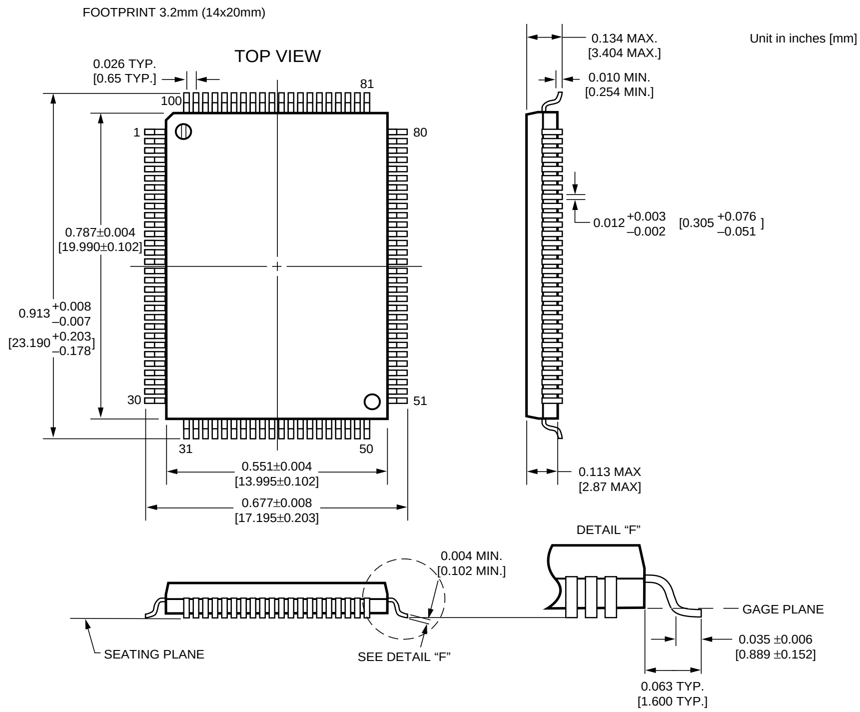
During Power-On, the V_{CC} current requirement of the V53C832L is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{CC} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C832L Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
EDO Read Cycle	Data from Addressed Memory Cell
EDO Write Cycle (Early Write)	High-Z
EDO Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

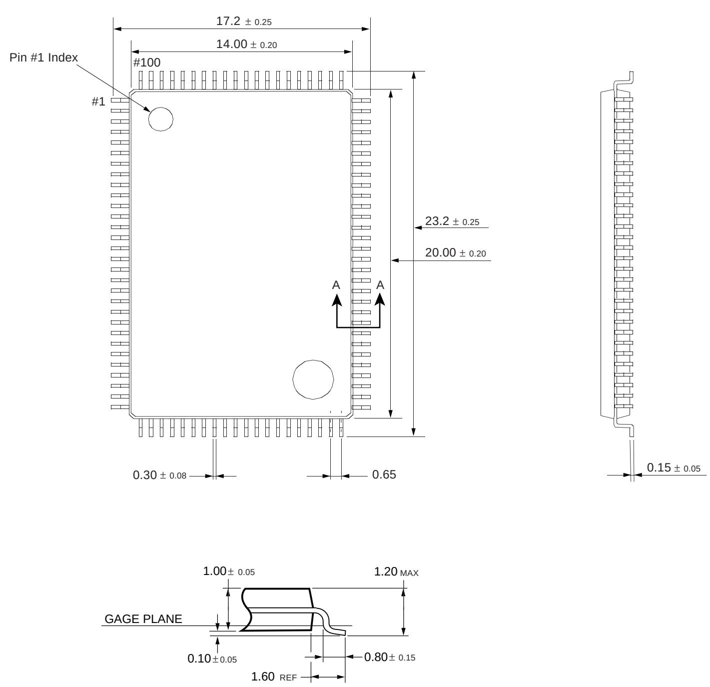
Package Outlines

100-pin PQFP



100-pin TQFP

Dimensions in Millimeters



SECTION: A-A

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FAX: 886-3-566-5888

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IRELAND & UK
BLOCK A UNIT 2
BROOMFIELD BUSINESS PARK
MALAHIDE
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PHONE: +353 1 8038020
FAX: +353 1 8038049

GERMANY (CONTINENTAL EUROPE & ISRAEL)
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GERMANY
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