

Features

- **Low-power consumption**
 - **Active: 65mA I_{CC} at 35ns**
 - **Stand-by: 10 μ A (CMOS input/output)**
2 μ A (CMOS input/output, L version)
- **35/45/55/70/85/100 ns access time**
- **Equal access and cycle time**
- **Single +2.7V to 3.3V Power Supply**
- **Tri-state output**
- **Automatic power-down when deselected**
- **Multiple center power and ground pins for improved noise immunity**
- **Individual byte controls for both Read and Write cycles**
- **Available in 44 pin TSOP II / 48-fpBGA**

Functional Description

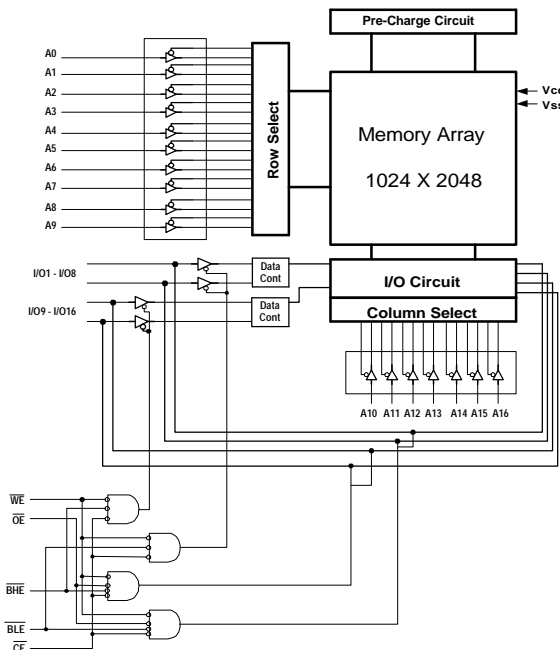
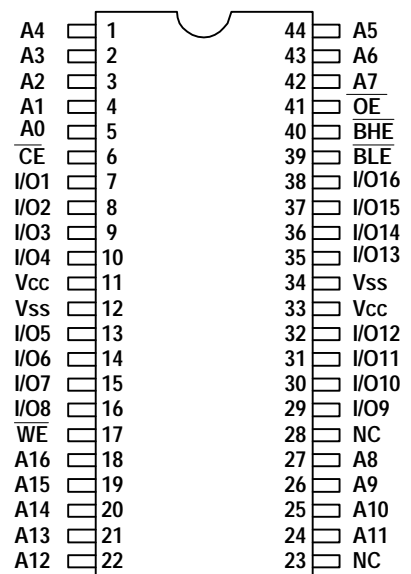
The V62C3162048L is a Low Power CMOS Static RAM organized as 131,072 words by 16 bits. Easy memory expansion is provided by an active LOW ($\overline{\text{CE}}$) and ($\overline{\text{OE}}$) pin.

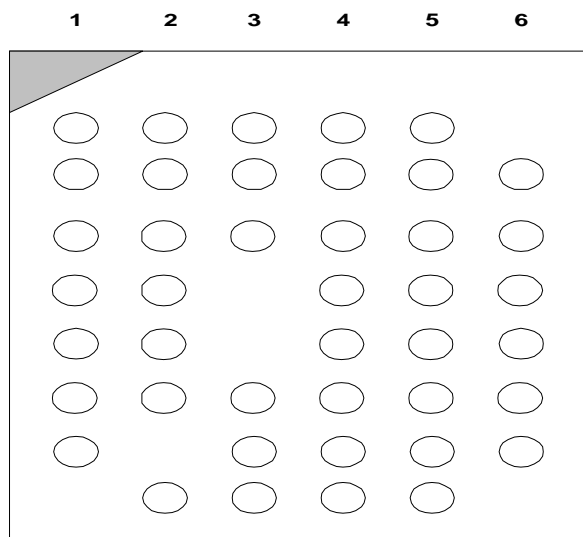
This device has an automatic power-down mode feature when deselected. Separate Byte Enable controls (BLE** and **BHE**) allow individual bytes to be accessed. **BLE** controls the lower bits I/O1 - I/O8. **BHE** controls the upper bits I/O9 - I/O16.**

Writing to these devices is performed by taking Chip Enable (CE) with Write Enable (WE) and Byte Enable (BLE/BHE) LOW.

Reading from the device is performed by taking Chip Enable ($\overline{\text{CE}}$) with Output Enable ($\overline{\text{OE}}$) and Byte Enable ($\overline{\text{BLE/BHE}}$) LOW while Write Enable ($\overline{\text{WE}}$) is held HIGH.

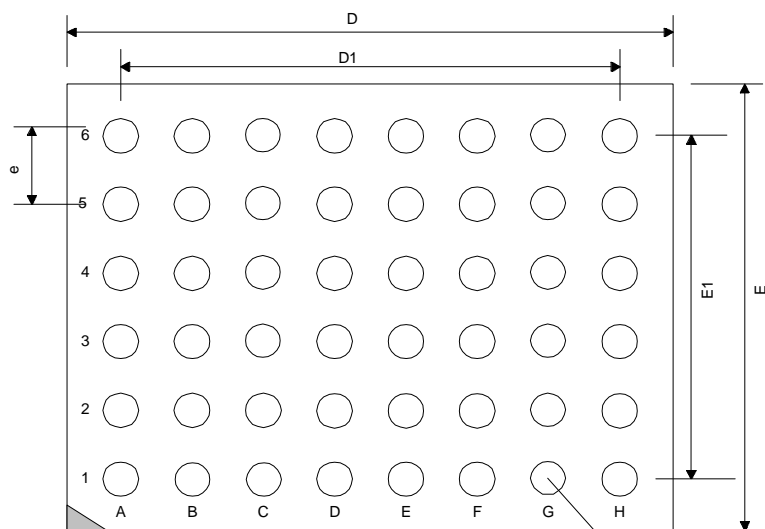
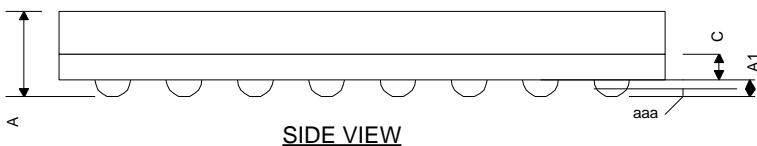
Logic Block Diagram

**TSOPII / 48-fpBGA**

MOSEL VITELIC V62C3162048L(L)B

Top View

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-------|-------|-----|-----|------|------|
| A | BLE | OE | A0 | A1 | A2 | NC |
| B | I/O9 | BHE | A3 | A4 | CE | I/O1 |
| C | I/O10 | I/O11 | A5 | A6 | I/O2 | I/O3 |
| D | VSS | I/O12 | NC | A7 | I/O4 | VCC |
| E | VCC | I/O13 | NC | A16 | I/O5 | VSS |
| F | I/O15 | I/O14 | A14 | A15 | I/O6 | I/O7 |
| G | I/O16 | NC | A12 | A13 | WE | I/O8 |
| H | NC | A8 | A9 | A10 | A11 | NC |

Note: NC means no Ball.

Top View
48 Ball - 9x12 fpBGA (Ultra Low Power)
PACKAGE OUTLINE DWG.

BOTTOM VIEW

b SOLDER BALL

| SYMBOL | UNIT:MM |
|--------|------------|
| A | 1.05±0.15 |
| A1 | 0.25±0.05 |
| b | 0.35±0.05 |
| c | 0.30(TYP) |
| D | 12.00±0.10 |
| D1 | 5.25 |
| E | 9.00±0.10 |
| E1 | 3.75 |
| e | 0.75TYP |
| aaa | 0.10 |

Absolute Maximum Ratings *

| Parameter | Symbol | Minimum | Maximum | Unit |
|------------------------------------|--------|---------|---------|------|
| Voltage on Any Pin Relative to Gnd | Vt | -0.5 | +4.6 | V |
| Power Dissipation | PT | — | 1.0 | W |
| Storage Temperature (Plastic) | Tstg | -55 | +150 | °C |
| Temperature Under Bias | Tbias | -40 | +85 | °C |

* **Note:** Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and function operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

| CE | OE | WE | BLE | BHE | I/O1-I/O8 | I/O9-I/O16 | Power | Mode |
|----|----|----|-----|-----|-----------|------------|---------|-----------------|
| H | X | X | X | X | High-Z | High-Z | Standby | Standby |
| L | L | H | L | H | Data Out | High-Z | Active | Low Byte Read |
| L | L | H | H | L | High-Z | Data Out | Active | High Byte Read |
| L | L | H | L | L | Data Out | Data Out | Active | Word Read |
| L | X | L | L | L | Data In | Data In | Active | Word Write |
| L | X | L | L | H | Data In | High-Z | Active | Low Byte Write |
| L | X | L | H | L | High-Z | Data In | Active | High Byte Write |
| L | H | H | X | X | High-Z | High-Z | Active | Output Disable |
| L | X | X | H | H | High-Z | High-Z | Active | Output Disable |

* **Key:** X = Don't Care, L = Low, H = High

Recommended Operating Conditions ($T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ / -40°C to 85°C^{**})

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-----------------|-------|-----|-----------------------|------|
| Supply Voltage | V _{CC} | 2.7 | 3.0 | 3.3 | V |
| | Gnd | 0.0 | 0.0 | 0.0 | V |
| Input Voltage | V _{IH} | 2.2 | - | V _{CC} + 0.2 | V |
| | V _{IL} | -0.5* | - | 0.8 | V |

* V_{IL} min = -2.0V for pulse width less than t_{RC}/2.

** For Industrial Temperature

DC Operating Characteristics ($V_{CC} = 2.7$ to $3.3V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$)

| Parameter | Sym | Test Conditions | -55 | | -70 | | -85 | | -100 | | Unit |
|---|-----------|--|-----|-----|-----|-----|-----|-----|------|-----|---------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Leakage Current | I_{L_I} | $V_{CC} = \text{Max}$, $V_{in} = \text{Gnd to } V_{CC}$ | - | 1 | - | 1 | - | 1 | - | 1 | μA |
| Output Leakage Current | I_{L_O} | $\overline{CE} = V_{IH}$ or $V_{CC} = \text{Max}$, $V_{OUT} = \text{Gnd to } V_{CC}$ | - | 1 | - | 1 | - | 1 | - | 1 | μA |
| Operating Power Supply Current | I_{CC} | $\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0$ | - | 5 | - | 5 | - | 5 | - | 5 | mA |
| Average Operating Current | I_{CC1} | $I_{OUT} = 0\text{mA}$, Min Cycle, 100% Duty | - | 50 | - | 45 | - | 40 | - | 40 | mA |
| | I_{CC2} | $\overline{CE} \leq 0.2V$ $I_{OUT} = 0\text{mA}$, Cycle Time = $1\mu s$, Duty = 100% | - | 3 | - | 3 | - | 3 | - | 3 | mA |
| Standby Power Supply Current (TTL Level) | I_{SB} | $\overline{CE} = V_{IH}$ | - | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | mA |
| Standby Power Supply Current (CMOS Level) | I_{SB1} | $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ | - | 10 | - | 10 | - | 10 | - | 10 | μA |
| | | L | - | 2 | - | 2 | - | 2 | - | 2 | μA |
| Output Low Voltage | V_{OL} | $I_{OL} = 2\text{ mA}$ | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | V |
| Output High Voltage | V_{OH} | $I_{OH} = -2\text{ mA}$ | 2.4 | - | 2.4 | - | 2.4 | - | 2.4 | - | V |

Capacitance ($f = 1\text{MHz}$, $T_A = 25^{\circ}C$)

| Parameter* | Symbol | Test Condition | Max | Unit |
|-------------------|-----------|-------------------------|-----|------|
| Input Capacitance | C_{in} | $V_{in} = 0V$ | 7 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{in} = V_{out} = 0V$ | 8 | pF |

* This parameter is guaranteed by device characterization and is not production tested.

AC Test Conditions

Input Pulse Level $0.6V$ to $2.2V$

Input Rise and Fall Time 5ns

Input and Output Timing

Reference Level $1.4V$

Output Load Condition

$55\text{ns}/70\text{ns}/85\text{ns}$

Load for 100ns

$C_L = 30\text{pf} + 1\text{TTL Load}$

$C_L = 100\text{pf} + 1\text{TTL Load}$

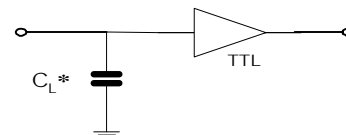


Figure A. * Including Scope and Jig Capacitance



DC Operating Characteristics ($V_{CC} = 2.7$ to $3.3V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$)

| Parameter | Sym | Test Conditions | -35 | | -45 | | Unit |
|---|-----------|--|-----|-----|-----|-----|---------|
| | | | Min | Max | Min | Max | |
| Input Leakage Current | I_{LI} | $V_{CC} = \text{Max}$, $V_{IN} = \text{Gnd to } V_{CC}$ | - | 1 | - | 1 | μA |
| Output Leakage Current | I_{LO} | $\overline{CE} = V_{IH}$ or $V_{CC} = \text{Max}$, $V_{OUT} = \text{Gnd to } V_{CC}$ | - | 1 | - | 1 | μA |
| Operating Power Supply Current | I_{CC} | $\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0$ | - | 5 | - | 5 | mA |
| Average Operating Current | I_{CC1} | $I_{OUT} = 0mA$, Min Cycle, 100% Duty | - | 65 | - | 60 | mA |
| | I_{CC2} | $\overline{CE} \leq 0.2V$ $I_{OUT} = 0mA$, Cycle Time=1 μs , Duty=100% | - | 3 | - | 3 | mA |
| Standby Power Supply Current (TTL Level) | I_{SB} | $\overline{CE} = V_{IH}$ | - | 0.5 | - | 0.5 | mA |
| Standby Power Supply Current (CMOS Level) | I_{SB1} | $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or | - | 10 | - | 10 | μA |
| | | $V_{IN} \geq V_{CC} - 0.2V$ L | - | 2 | - | 2 | μA |
| Output Low Voltage | V_{OL} | $I_{OL} = 2 \text{ mA}$ | - | 0.4 | - | 0.4 | V |
| Output High Voltage | V_{OH} | $I_{OH} = -2 \text{ mA}$ | 2.4 | - | 2.4 | - | V |

Read Cycle ⁽⁹⁾ ($V_{cc} = 2.7$ to $3.3V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $+85^{\circ}C$)

| Parameter | Sym | -55 | | -70 | | -85 | | -100 | | Unit | Note |
|---|-----------|-----|-----|-----|-----|-----|-----|------|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read Cycle Time | t_{RC} | 55 | - | 70 | - | 85 | - | 100 | - | ns | |
| Address Access Time | t_{AA} | - | 55 | - | 70 | - | 85 | - | 100 | ns | |
| Chip Enable Access Time | t_{ACE} | - | 55 | - | 70 | - | 85 | - | 100 | ns | |
| Output Enable Access Time | t_{OE} | - | 35 | - | 40 | - | 40 | - | 50 | ns | |
| Output Hold from Address Change | t_{OH} | 10 | - | 10 | - | 10 | - | 10 | - | ns | |
| Chip Enable to Output in Low-Z | t_{LZ} | 10 | - | 10 | - | 10 | - | 10 | - | ns | 4,5 |
| Chip Disable to Output in High-Z | t_{HZ} | - | 25 | - | 30 | - | 35 | - | 40 | ns | 3,4,5 |
| Output Enable to Output in Low-Z | t_{OLZ} | 5 | - | 5 | - | 5 | - | 5 | - | ns | |
| Output Disable to Output in High-Z | t_{OHZ} | - | 25 | - | 25 | - | 30 | - | 35 | ns | |
| \overline{BLE} , \overline{BHE} Enable to Output in Low-Z | t_{BLZ} | 5 | - | 5 | - | 5 | - | 5 | - | ns | 4,5 |
| \overline{BLE} , \overline{BHE} Disable to Output in High-Z | t_{BHZ} | - | 25 | - | 25 | - | 30 | - | 35 | ns | 3,4,5 |
| \overline{BLE} , \overline{BHE} Access Time | t_{BA} | - | 35 | - | 40 | - | 40 | - | 50 | ns | |

Write Cycle ⁽¹¹⁾ ($V_{cc} = 2.7$ to $3.3V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $+85^{\circ}C$)

| Parameter | Symbol | -55 | | -70 | | -85 | | -100 | | Unit | Note |
|--|-----------|-----|-----|-----|-----|-----|-----|------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | t_{WC} | 55 | - | 70 | - | 85 | - | 100 | - | ns | |
| Chip Enable to Write End | t_{CW} | 50 | - | 60 | - | 70 | - | 80 | - | ns | |
| Address Setup to Write End | t_{AW} | 50 | - | 60 | - | 70 | - | 80 | - | ns | |
| Address Setup Time | t_{AS} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Write Pulse Width | t_{WP} | 45 | - | 50 | - | 60 | - | 70 | - | ns | |
| Write Recovery Time | t_{WR} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Data Valid to Write End | t_{DW} | 25 | - | 30 | - | 35 | - | 40 | - | ns | |
| Data Hold Time | t_{DH} | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| Write Enable to Output in High-Z | t_{WHZ} | - | 25 | - | 30 | - | 35 | - | 40 | ns | |
| Output Active from Write End | t_{OW} | 5 | - | 5 | - | 5 | - | 5 | - | ns | |
| \overline{BLE} , \overline{BHE} Setup to Write End | t_{BW} | 50 | - | 60 | - | 70 | - | 80 | - | ns | |

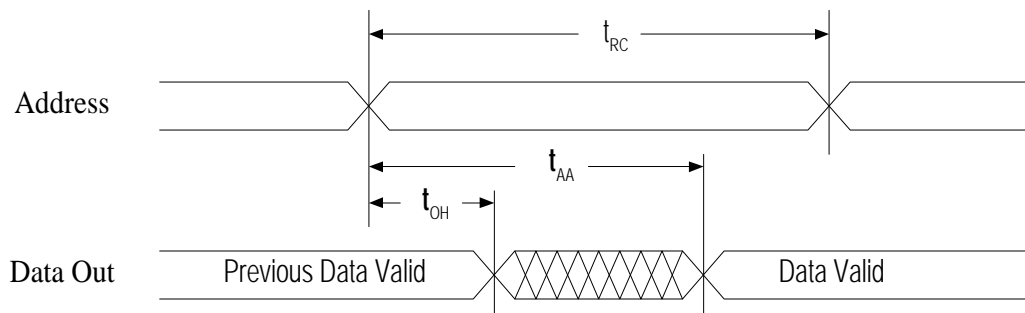
**Read Cycle ⁽⁹⁾** ($V_{cc} = 2.7$ to $3.3V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $+85^{\circ}C$)

| Parameter | Sym | -35 | | -45 | | Unit | Note |
|---|-----------|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Read Cycle Time | t_{RC} | 35 | - | 45 | - | ns | |
| Address Access Time | t_{AA} | - | 35 | - | 45 | ns | |
| Chip Enable Access Time | t_{ACE} | - | 35 | - | 45 | ns | |
| Output Enable Access Time | t_{OE} | - | 20 | - | 25 | ns | |
| Output Hold from Address Change | t_{OH} | 5 | - | 5 | - | ns | |
| Chip Enable to Output in Low-Z | t_{LZ} | 5 | - | 5 | - | ns | 4,5 |
| Chip Disable to Output in High-Z | t_{HZ} | - | 15 | - | 20 | ns | 3,4,5 |
| Output Enable to Output in Low-Z | t_{OLZ} | 5 | - | 5 | - | ns | |
| Output Disable to Output in High-Z | t_{OHZ} | - | 15 | - | 20 | ns | |
| \overline{BLE} , \overline{BHE} Enable to Output in Low-Z | t_{BLZ} | 5 | - | 5 | - | ns | 4,5 |
| \overline{BLE} , \overline{BHE} Disable to Output in High-Z | t_{BHZ} | - | 15 | - | 20 | ns | 3,4,5 |
| \overline{BLE} , \overline{BHE} Access Time | t_{BA} | - | 20 | - | 25 | ns | |

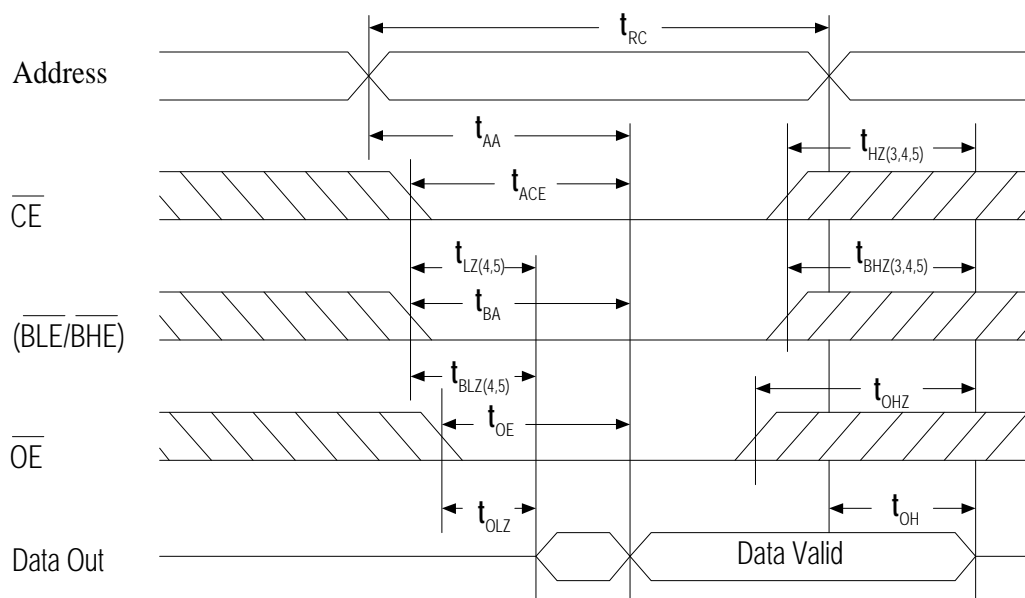
Write Cycle ⁽¹¹⁾ ($V_{cc} = 2.7$ to $3.3V$, $Gnd = 0V$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$ / $-40^{\circ}C$ to $+85^{\circ}C$)

| Parameter | Sym | -35 | | -45 | | Unit | Note |
|--|-----------|-----|-----|-----|-----|------|------|
| | | Min | Max | Min | Max | | |
| Write Cycle Time | t_{WC} | 35 | - | 45 | - | ns | |
| Chip Enable to Write End | t_{CW} | 30 | - | 35 | - | ns | |
| Address Setup to Write End | t_{AW} | 30 | - | 35 | - | ns | |
| Address Setup Time | t_{AS} | 0 | - | 0 | - | ns | |
| Write Pulse Width | t_{WP} | 30 | - | 35 | - | ns | |
| Write Recovery Time | t_{WR} | 0 | - | 0 | - | ns | |
| Data Valid to Write End | t_{DW} | 20 | - | 25 | - | ns | |
| Data Hold Time | t_{DH} | 0 | - | 0 | - | ns | |
| Write Enable to Output in High-Z | t_{WHZ} | - | 25 | - | 25 | ns | |
| Output Active from Write End | t_{OW} | 5 | - | 5 | - | ns | |
| \overline{BLE} , \overline{BHE} Setup to Write End | t_{BW} | 30 | - | 35 | - | ns | |

Timing Waveform of Read Cycle 1 (Address Controlled)

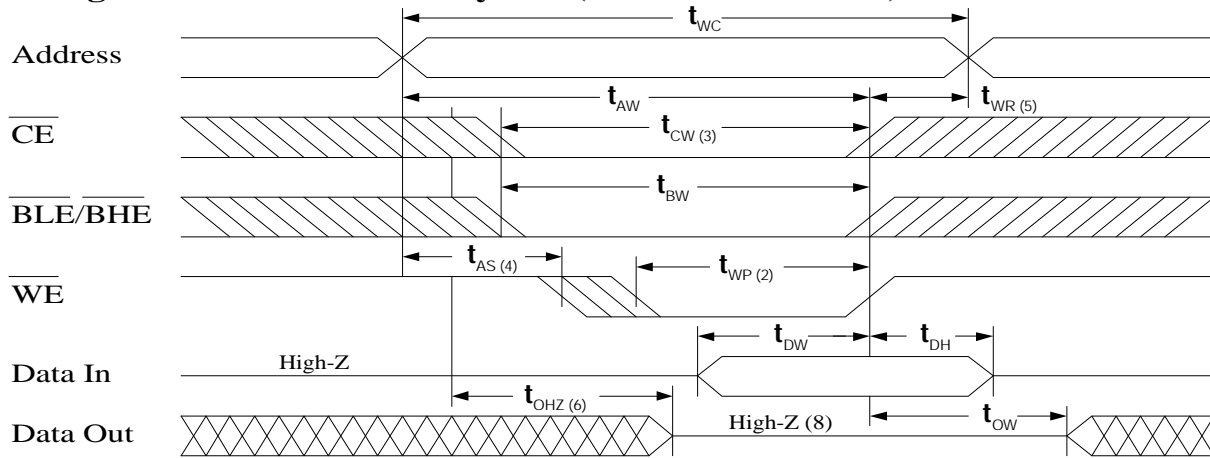
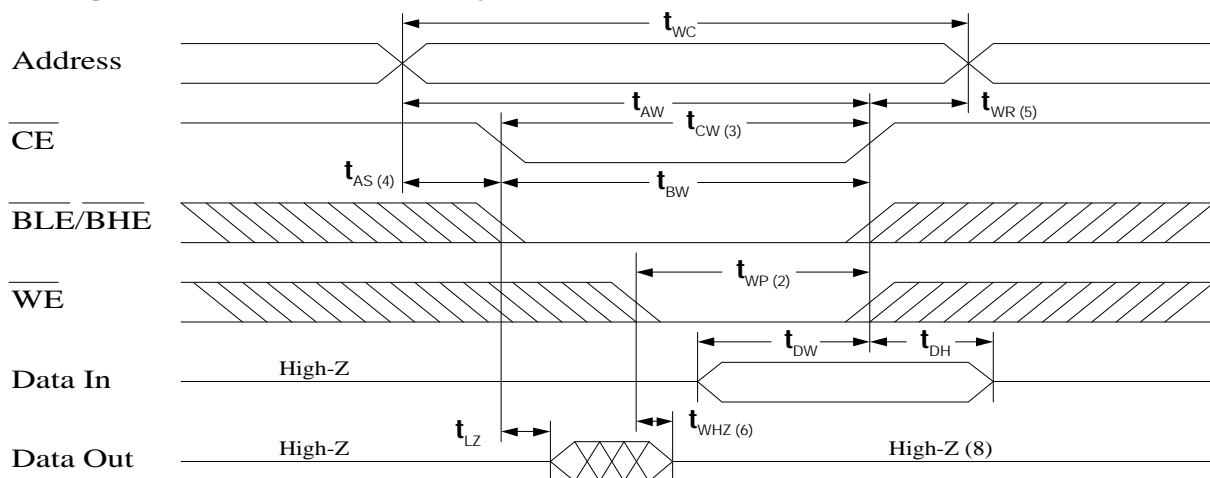
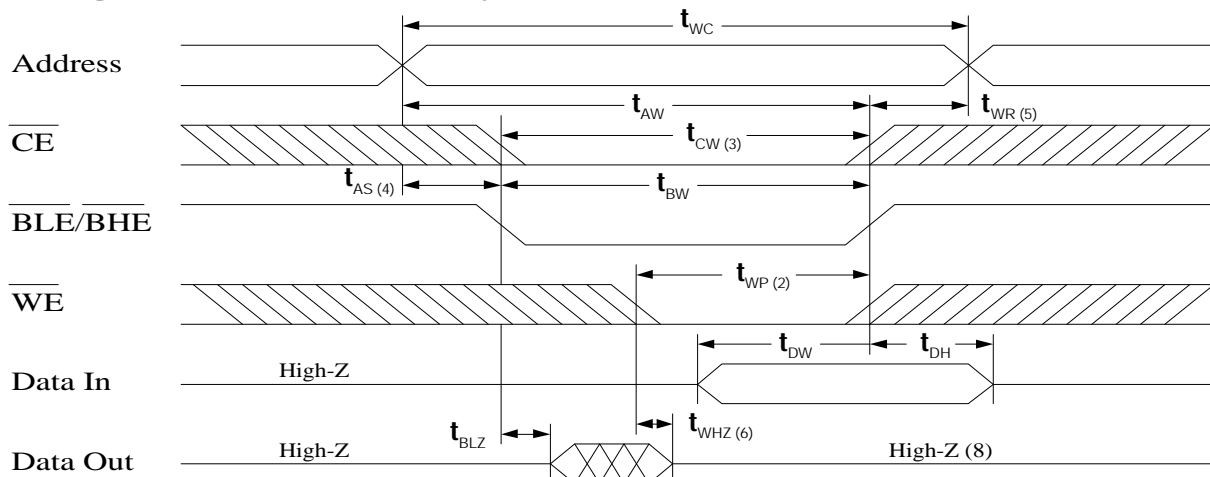


Timing Waveform of Read Cycle 2



Notes (Read Cycle)

1. WE are high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with load. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CE} = V_{IL}$.
7. Address valid prior to coincident with \overline{CE} transition Low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
9. For test conditions, see AC Test Condition, Figure A.

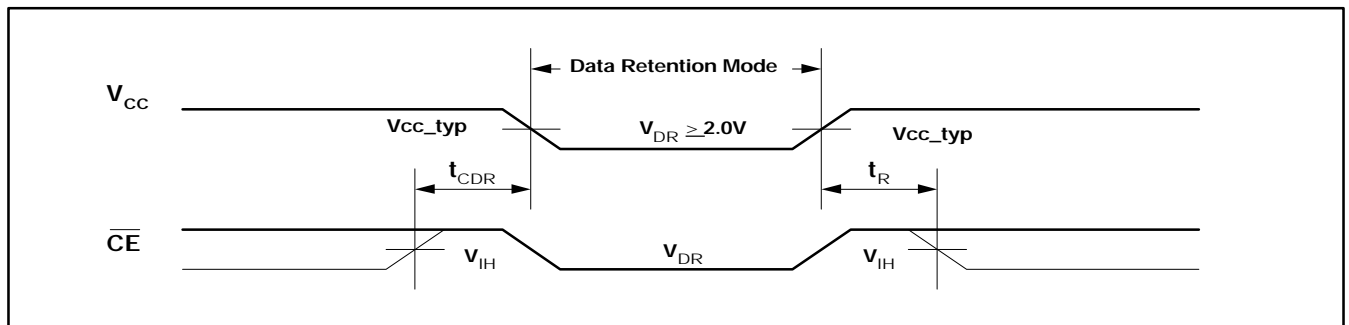
Timing Waveform of Write Cycle 1 (Address Controlled)

Timing Waveform of Write Cycle 2 ($\overline{\text{CE}}$ Controlled)

Timing Waveform of Write Cycle 3 ($\overline{\text{BLE/BHE}}$ Controlled)


Notes (Write Cycle)

1. All write timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CE} and \overline{WE} . A write begins at the latest transition among \overline{CE} and \overline{WE} going low: A write ends at the earliest transition among \overline{CE} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of \overline{CE} going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change.
6. If \overline{OE} , \overline{CE} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If \overline{CE} goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When \overline{CE} is low: I/O pins are in the outputs state. The input signals in the opposite phase leading to the output should not be applied.
11. For test conditions, see *AC Test Condition*, Figure A.

Data Retention Characteristics (L Version Only)⁽¹⁾

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|--|-------------------|---|-----------------|-----|------|
| V _{CC} for Data Retention | V _{DR} | $\overline{CE} \geq V_{CC} - 0.2V$ | 2.0 | - | V |
| Data Retention Current | I _{CCDR} | | - | 1 | μA |
| Chip Deselect to Data Retention Time | t _{CDR} | V _{IN} ≥ V _{CC} - 0.2V or | 0 | - | ns |
| Operation Recovery Time ⁽²⁾ | t _R | V _{IN} ≤ 0.2V | t _{RC} | - | ns |

Data Retention Waveform (L Version Only) (T_A = 0°C to +70°C / -40°C to +85°C)

Notes (Write Cycle)

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see *AC Test Condition*, Figure A.
4. This parameter is tested with CL = 5pF as shown in Figure B. Transition is measured ± 500mV from steady-state voltage.
5. This parameter is guaranteed, but is not tested.
6. \overline{WE} is High for read cycle.
7. \overline{CE} and \overline{OE} are LOW for read cycle.
8. Address valid prior to or coincident with \overline{CE} transition LOW.
9. All read cycle timings are referenced from the last valid address to the first transition address.
10. \overline{CE} or \overline{WE} must be HIGH during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

Ordering Information

| Device Type* | Speed | Package |
|----------------------|--------|--------------------|
| V62C3162048L-35T | 35 ns | 44-pin TSOP Type 2 |
| V62C3162048L-45T | 45 ns | |
| V62C3162048L-55T | 55 ns | |
| V62C3162048L-70T | 70 ns | |
| V62C3162048L-85T | 85 ns | |
| V62C3162048L-100T | 100 ns | |
| V62C3162048LL-35T | 35 ns | |
| V62C3162048LL-45T | 45 ns | |
| V62C3162048LL-55T | 55 ns | |
| V62C3162048LL-70T | 70 ns | |
| V62C3162048LL-85T | 85 ns | |
| V62C3162048LL-100T | 100 ns | |
| V62C3162048L(L)-35B | 35 ns | 48-fpBGA |
| V62C3162048L(L)-45B | 45 ns | |
| V62C3162048L(L)-55B | 55 ns | |
| V62C3162048L(L)-70B | 70 ns | |
| V62C3162048L(L)-85B | 85 ns | |
| V62C3162048L(L)-100B | 100 ns | |

* For Industrial temperature tested devices, an “I” designator will be added to the end of the device number.

U.S.A.

3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0952

TAIWAN

7F, NO. 102
MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
PHONE: 886-2-2545-1213
FAX: 886-2-2545-1209

SINGAPORE

10 ANSON ROAD #23-13
INTERNATIONAL PLAZA
SINGAPORE 079903
PHONE: 65-3231801
FAX: 65-3237013

UK & IRELAND

SUITE 50, GROVEWOOD
BUSINESS CENTRE
STRATHCLYDE BUSINESS
PARK
BELLSHILL, LANARKSHIRE,
SCOTLAND, ML4 3NQ
PHONE: 44-1698-748515
FAX: 44-1698-748516

NO 19 LI HSIN ROAD
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 886-3-579-5888
FAX: 886-3-566-5888

JAPAN

ONZE 1852 BUILDING 6F
2-14-6 SHINTOMI, CHUO-KU
TOKYO 104-0041
PHONE: 03-3537-1400
FAX: 03-3537-1402

**GERMANY
(CONTINENTAL
EUROPE & ISRAEL)**

BENZSTRASSE 32
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GERMANY
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FAX: +49 7032 2796 22

U.S. SALES OFFICES**NORTHWESTERN**

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FAX: 408-433-0952

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FAX: 949-361-7807

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