

Triacs

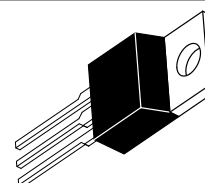
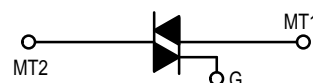
Silicon Bidirectional Triode Thyristors

... designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342, 2N6343, 2N6344, 2N6345) or Four Modes (2N6346, 2N6347, 2N6348, 2N6349)
- For 400 Hz Operation, Consult Factory
- 12 Ampere Devices Available as 2N6342A thru 2N6349A

**2N6342
thru
2N6349**

**TRIACs
8 AMPERES RMS
200 thru 800 VOLTS**



**CASE 221A-04
(TO-220AB)
STYLE 4**

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage ⁽¹⁾ (Gate Open, $T_J = -40$ to $+110^\circ\text{C}$) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}	200 400 600 800	Volts
*RMS On-State Current ($T_C = +80^\circ\text{C}$) Full Cycle Sine Wave 50 to 60 Hz ($T_C = +90^\circ\text{C}$)	$I_{\text{T(RMS)}}$	8 4	Amps
*Peak Non-repetitive Surge Current (One Full Cycle, 60 Hz, $T_C = +80^\circ\text{C}$) Preceded and followed by Rated Current	I_{TSM}	100	Amps
Circuit Fusing ($t = 8.3$ ms)	I^2t	40	A^2s
*Peak Gate Power ($T_C = +80^\circ\text{C}$, Pulse Width = 2 μs)	P_{GM}	20	Watts
*Average Gate Power ($T_C = +80^\circ\text{C}$, $t = 8.3$ ms)	$P_{\text{G(AV)}}$	0.5	Watt
*Peak Gate Current	I_{GM}	2	Amps
*Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to $+125$	$^\circ\text{C}$
*Storage Temperature Range	T_{stg}	-40 to $+150$	$^\circ\text{C}$

1. V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

REV 1

2N6342 thru 2N6349

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, and Either Polarity of MT2 to MT1 Voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current ($V_D = \text{Rated } V_{DRM}$, gate open) $T_J = 25^\circ\text{C}$ $T_J = 100^\circ\text{C}$	I_{DRM}	— —	— —	10 2	μA mA
*Peak On-State Voltage ($I_{TM} = 11 \text{ A Peak}$; Pulse Width = 1 to 2 ms, Duty Cycle $\leq 2\%$)	V_{TM}	—	1.3	1.55	Volts
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 100 \text{ Ohms}$) (Minimum Gate Pulse Width = 2 μs) MT2(+), G(+) All Types MT2(+), G(−) 2N6346 thru 49 MT2(−), G(−) All Types MT2(−), G(+) 2N6346 thru 49 *MT2(+), G(+); MT2(−), G(−) $T_C = -40^\circ\text{C}$ All Types *MT2(+), G(−); MT2(−), G(+) $T_C = -40^\circ\text{C}$ 2N6346 thru 49	I_{GT}	— — — — — —	12 12 20 35 — —	50 75 50 75 100 125	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 100 \text{ Ohms}$) (Minimum Gate Pulse Width = 2 μs) MT2(+), G(+) All Types MT2(+), G(−) 2N6346 thru 49 MT2(−), G(−) All Types MT2(−), G(+) 2N6346 thru 49 *MT2(+), G(+); MT2(−), G(−) $T_C = -40^\circ\text{C}$ All Types *MT2(+), G(−); MT2(−), G(+) $T_C = -40^\circ\text{C}$ 2N6346 thru 49 ($V_D = \text{Rated } V_{DRM}$, $R_L = 10 \text{ k Ohms}$, $T_J = 100^\circ\text{C}$) *MT2(+), G(+); MT2(−), G(−) All Types *MT2(+), G(−); MT2(−), G(−) 2N6346 thru 49	V_{GT}	— — — — — 0.2 0.2	0.9 0.9 1.1 1.4 — — —	2 2.5 2 2.5 2.5 — —	Volts
*Holding Current ($V_D = 12 \text{ Vdc}$, Gate Open) $T_C = 25^\circ\text{C}$ ($I_T = 200 \text{ mA}$) * $T_C = -40^\circ\text{C}$	I_H	— —	6 —	40 75	mA
*Turn-On Time ($V_D = \text{Rated } V_{DRM}$, $I_{TM} = 11 \text{ A}$, $I_{GT} = 120 \text{ mA}$, Rise Time = 0.1 μs , Pulse Width = 2 μs)	t_{gt}	—	1.5	2	μs
Critical Rate of Rise of Commutation Voltage ($V_D = \text{Rated } V_{DRM}$, $I_{TM} = 11 \text{ A}$, Commutating $di/dt = 4.0 \text{ A/ms}$, Gate Unenergized, $T_C = 80^\circ\text{C}$)	$dv/dt(c)$	—	5	—	V/ μs

*Indicates JEDEC Registered Data.

FIGURE 1 – RMS CURRENT DERATING

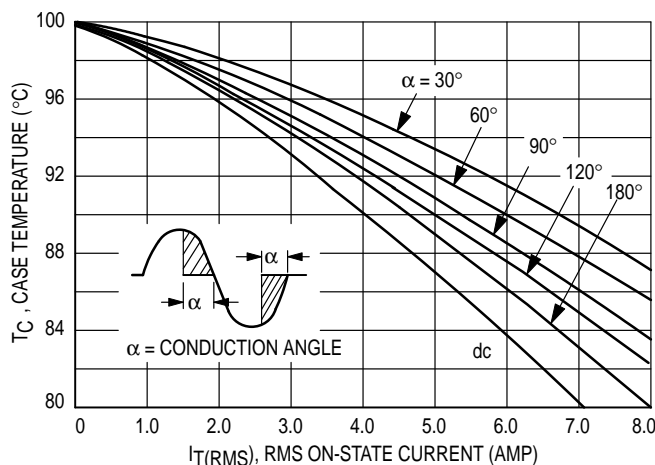


FIGURE 2 – ON-STATE POWER DISSIPATION

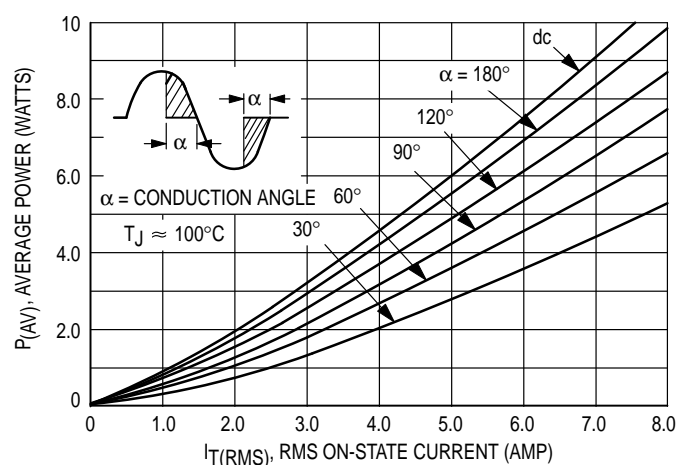


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

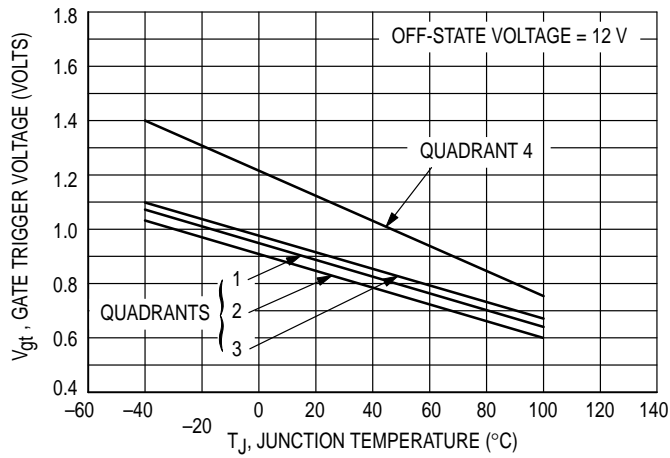


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

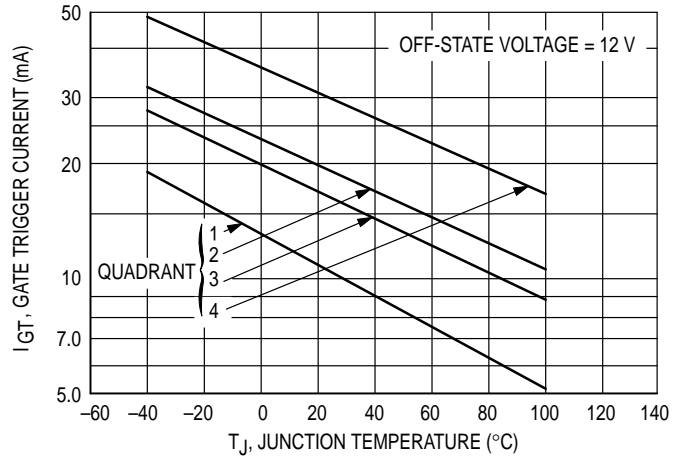


FIGURE 5 – ON-STATE CHARACTERISTICS

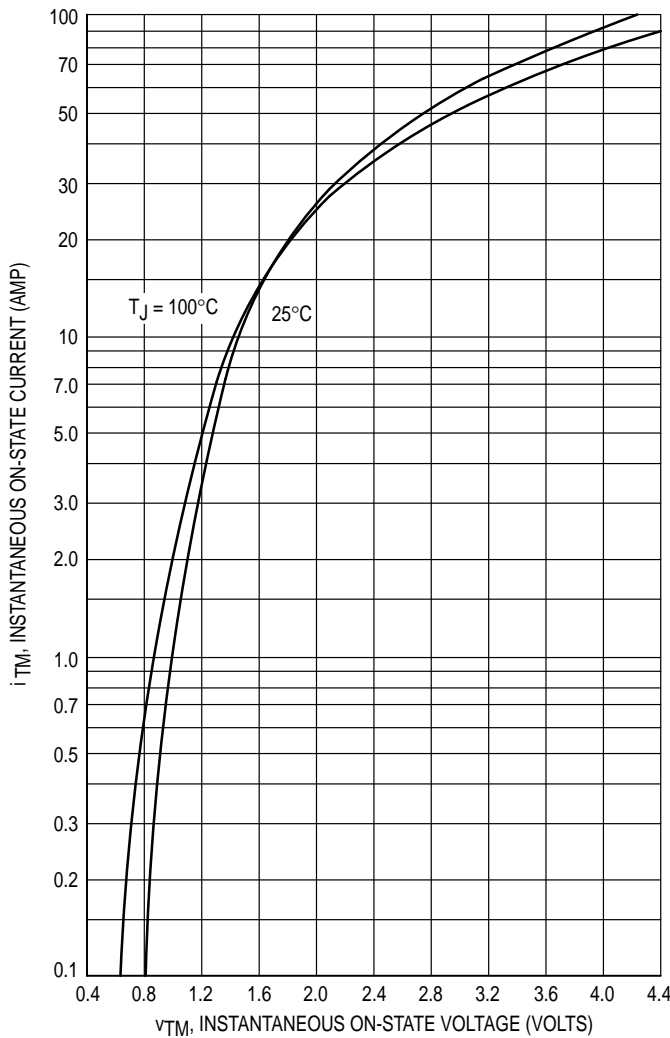


FIGURE 6 – TYPICAL HOLDING CURRENT

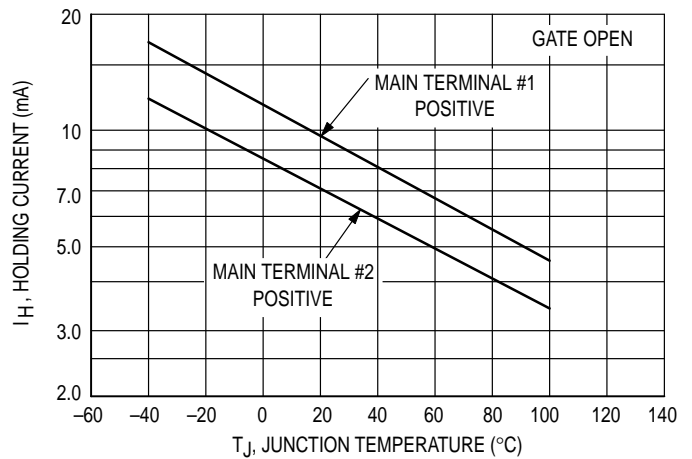


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

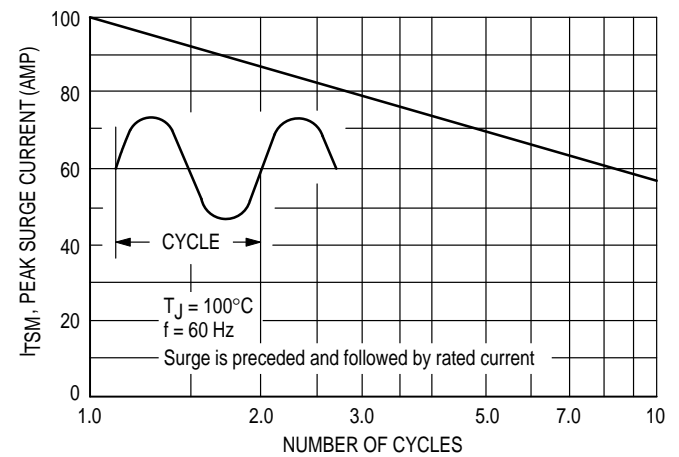
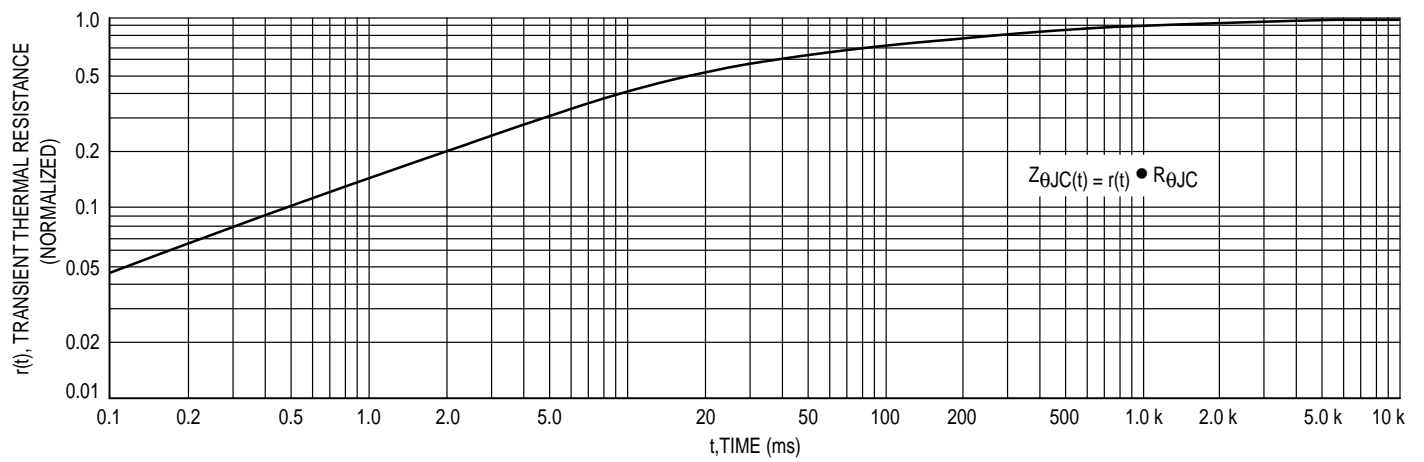
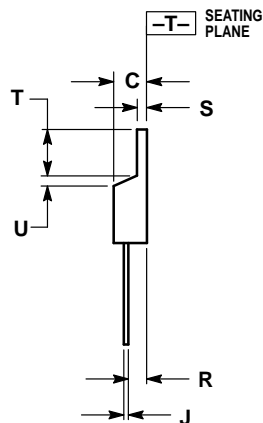
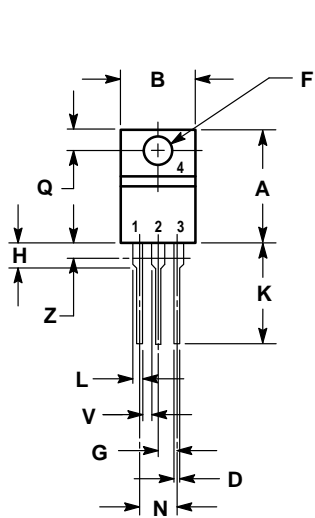


FIGURE 8 – TYPICAL THERMAL RESPONSE



PACKAGE DIMENSIONS




STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.055	1.15	1.39
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-04
(TO-220AB)

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MOTOROLA



2N6342/D

