



8-INPUT PRIORITY ENCODERS WITH 3-STATE OUTPUTS

The SN54/74LS348 and the SN54/74LS848 are eight input priority encoders which provide the 8-line to 3-line function.

The outputs (A0–A2) and inputs (0–7) are active low. The active low input which has the highest priority (input 7 has the highest) is represented on the outputs (output A0 is the lowest bit). An example would be if inputs 1, 2 and 4 were low, then a binary 4 would be represented on the outputs.

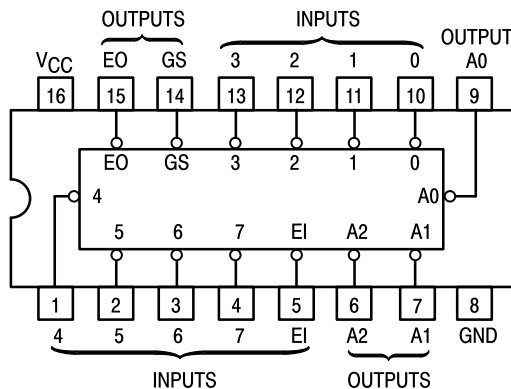
The GS (Group Signal) output is active low when any of the inputs are low. It serves to indicate when any of the inputs are active.

A0, A1 and A2 are three-state outputs. This allows for up to 64 line expansion without the need for special external circuitry.

A logical one on the Enable Input (EI) forces A0, A1 and A2 to the disabled state and outputs GS and EO to the high state. A high on all data inputs (0–7) together with a low on the EI input disables outputs A0, A1, and A2 and forces output GS to the high state and output EO to the low state.

Use of the EI input in conjunction with the EO output provides for the capability of having priority encoding of n input signals.

The LS848 has special internal circuitry providing for a greatly reduced negative going glitch on the GS (Group Signal) output and on a reduced tendency for the A0, A1 and A2 outputs to become momentarily enabled. Both of these occurrences happen when the EI input goes from a logical one to a logical zero and all data inputs (0–7) are held at logical ones. The internal glitch reduction circuitry does add an additional fan-in of one on all data inputs (compared to that of the LS348).



FUNCTION TABLE

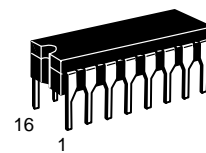
INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = HIGH Logic Level
L = LOW Logic Level
X = Irrelevant
Z = High Impedance State

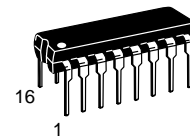
SN54/74LS348
SN54/74LS848

**8-INPUT PRIORITY ENCODERS
WITH 3-STATE OUTPUTS**

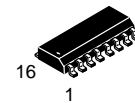
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



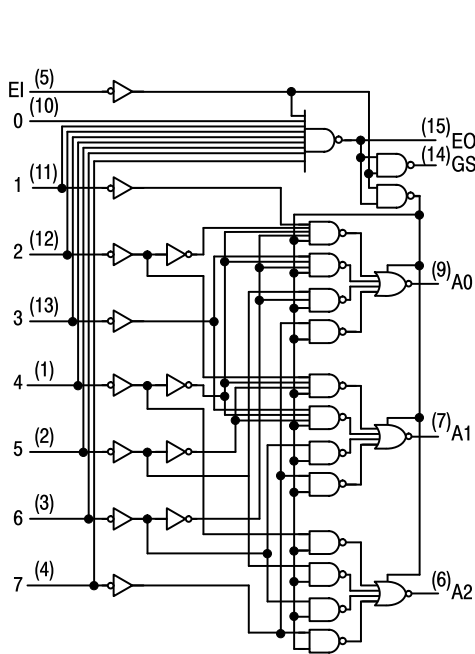
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

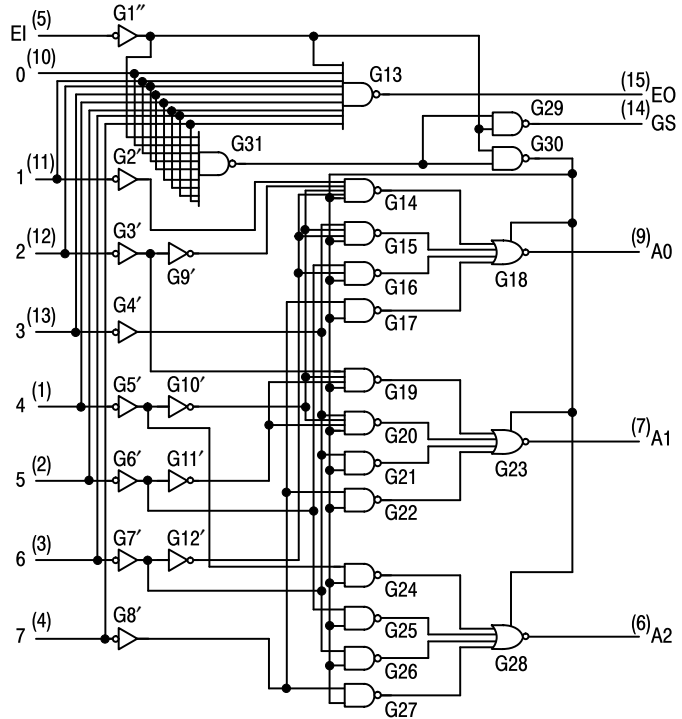
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

SN54/74LS348 • SN54/74LS848

BLOCK DIAGRAMS



SN54/74LS348



SN54/74LS848

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	EO, GS			-0.4	mA
I _{OH}	Output Current — High	A0, A1, A2 A0, A1, A2			-1.0 -2.6	mA
I _{OL}	Output Current — Low	EO, GS			4.0 8.0	mA
I _{OL}	Output Current — Low	A0, A1, A2 A0, A1, A2			12 24	mA

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V _{CC} = MIN, I _{IN} = −18 mA	
V _{OH}	Output HIGH Voltage A0, A1, A2	54, 74	2.4	3.1		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
	EO, GS	54	2.5	3.5		V		
	EO, GS	74	2.7	3.5		V		
V _{OL}	Output LOW Voltage EO, GS	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
V _{OL}	Output LOW Voltage A0, A1, A2	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW				−20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current Input 0, EI — LS348 Input 0 — LS848 Other — LS348 Other — LS848				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					40	μA		
					40 60	μA μA		
	Input HIGH Current Input 0, EI — LS348 Input 0 — LS848 Other — LS348 Other — LS848				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
					0.2	mA		
					0.2 0.3	mA mA		
I _{IL}	Input LOW Current Input 0, EI — LS348 Input 0 — LS848 Other — LS348 Other — LS848				−0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
					−0.8	mA		
					−0.8 −1.2	mA mA		
I _{OS}	Short Circuit Current (Note 1) EO, GS A0, A1, A2		−20		−120	mA	V _{CC} = MAX	
			−30		−130	mA		
I _{CC}	Power Supply Current Total, Output HIGH			12	23	mA	V _{CC} = MAX All Inputs and Outputs Open	
	Total, Output LOW			13	25		V _{CC} = MAX, Inputs 7, EI = GND All Others Open	

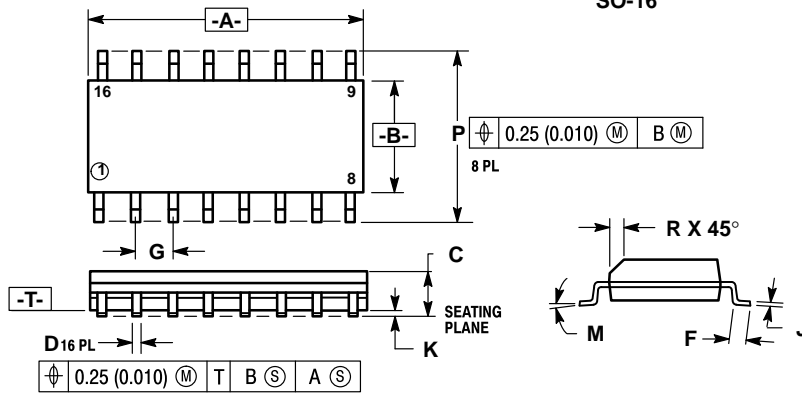
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS348 • SN54/74LS848

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	From (Input)	To (Output)	Waveform	LS348 Limits			LS848 Limits			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max		
tPLH	1 thru 7	A0, A1 or A2	In-Phase output		11	17		12	18	ns	C _L = 45 pF R _L = 667 Ω
tPHL					20	30		20	30		
tPLH	1 thru 7	A0, A1 or A2	Out-of-Phase output		23	35		23	35	ns	
tPHL					23	35		23	35		
tPZH	EI	A0, A1 or A2			25	39		25	39	ns	
tPZL					24	41		24	41		
tPLH	0 thru 7	E0	Out-of-Phase output		11	18		11	18	ns	C _L = 15 pF R _L = 2.0 Ω
tPHL					26	40		26	40		
tPLH	0 thru 7	GS	In-Phase output		38	55		38	55	ns	
tPHL					9.0	21		9.0	21		
tPLH	EI	GS	In-Phase output		11	17		11	17	ns	
tPHL					14	36		14	36		
tPLH	EI	EO	In-Phase output		17	21		17	21	ns	
tPHL					25	40		30	45		
tPHZ	EI	A0, A1 or A2			18	27		18	27	ns	C _L = 5.0 pF R _L = 667 Ω
tPLZ					23	35		23	35		

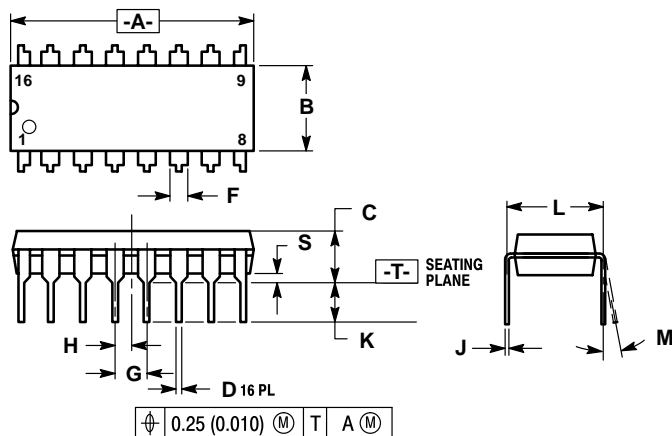
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

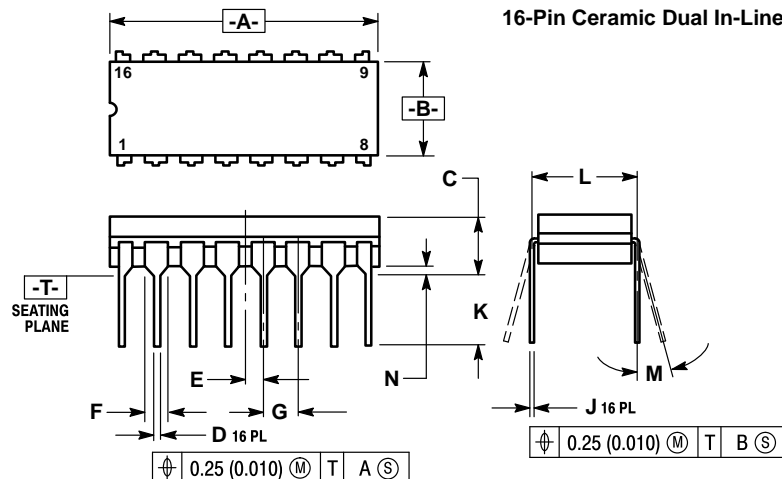
Case 648-08 N Suffix
16-Pin Plastic



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.
 6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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