

In-Circuit Programming of FLASH Memory Using the Monitor Mode for the MC68HC908SR12

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Introduction

This engineering bulletin describes how to perform in-circuit programming (ICP) of the FLASH memory using monitor mode for the MC68HC908SR12.

Two ICP methods are discussed here:

- Using the M68ICS08SR in-circuit simulator (ICS) with P&E[™] Microcomputer Systems software
- Using P&E Microcomputer Systems software with an external communications circuit

ICP is a process where user code is programmed into the device's FLASH memory after the part has been assembled into the application. ICP also allows the original users code to be erased and re-programmed. This method can be used in development, production/manufacturing, and in a field environment.

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Using Monitor Mode for FLASH Programming

Motorola's current solution for ICP is the in-circuit simulators and P&E's software.

The software and ICS allow programming of the parts on the simulator or in the target circuit via a MON08 ribbon cable. The software also allows programming of the part, without the ICS, by using an external communications circuit.

All the programming described here is accomplished by placing the part into monitor mode. In this mode, erasing and programming are done through a single-wire interface with the host computer.

The two ways to enter monitor mode are:

- The ICS provides the entry requirements into standard monitor mode. These entry requirements must be implemented on the target board if the ICS is not used.
- A second way to enter monitor mode, that does not require a high voltage on the $\overline{\text{IRQ1}}$ pin, is forced monitor mode. This mode does not need to meet all the monitor mode entry conditions of the standard monitor mode, but it does require the part to be blank (erased).

This engineering bulletin describes how to connect the part, communicate at different baud rates, place the part into monitor mode, pass security, and erase and program the part. If the security code is not known, the contents of the FLASH can't be read, but the FLASH can be erased and reprogrammed.

Information on the M68ICS08SR can be found at <http://www.motorola.com/semiconductors>, the company's Web site. P&E Microcomputer Systems software can be downloaded free from that company's Web site.

NOTE: *All of the oscillators used in this engineering bulletin are the 4-pin "powered" or "canned" type oscillators. Discussing all the different vendors of crystals, ceramic oscillators, other required external components, and component layout variables would be too extensive.*

ICP Using M68ICS08SR's MON08 Interface

Use this procedure for performing ICP using the ICS's MON08 cable to the target application.

1. Materials required:
 - a. PC with P&E's software installed
 - b. M68ICS08SR ICS
 - c. Adapter/connector to connect the female end of the MON08 cable to the target application
 - d. Pin assignment diagram (see [Figure 1](#) and [Figure 2](#))
 - e. Monitor mode entry requirements (see [Table 1](#))
 - f. Crystal oscillator on the target or from an external clock source with a value from [Table 2](#)
 - g. Target board must have the ability to perform a power-on reset (POR) not just a reset (required to enter monitor mode).
2. Connections (see [Figure 3](#)):
 - a. 9-pin serial cable from PC to the ICS
 - b. 5 volts to the ICS
 - c. MON08 cable (even pins) from J3 of the ICS to the target board with these connections:
 - MON08 GND to the V_{SS} pin on the part
 - MON08 RST to the \overline{RST} pin on the part
 - MON08 IRQ to the $\overline{IRQ1}$ pin on the part
 - MON08 PTA0 to the PTA0 pin on the part
 - MON08 PTA2 to the PTA2 pin on the part
 - MON08 PTA1 to the PTA1 pin on the part
 - MON08 PTC1 to the PTC1 pin on the part
 - d. It is assumed that all V_{DD} and V_{SS} pins on the part are already connected.
3. Operation — Standard monitor mode entry:
 - a. Launch P&E's WINIDE in the ICS08SRZ software.
 - b. Open desired file. (Demo file can be used for testing purposes.)

- c. Assemble/Compile the file (see [Figure 7](#)).
 - d. Plug in power to the ICS.
 - e. Apply power to the target.
 - f. Launch the programmer.
 - g. From “Target Hardware Type,” select “Class II” (see [Figure 8](#)). If this window does not appear and the window in [Figure 9](#) appears instead, you should relaunch the programmer without applying power to the target. You may want to check the “Show this dialog before attempting to contact the target 68HC08 board.”
 - h. From “PC Serial Port Configuration,” select the PC port you are using and the appropriate baud rate (see [Table 2](#)).
 - i. From “Target MCU Security Bytes,” select appropriate security code (blank part = FF).
 - j. Select “Contact Target with these Settings...”
 - k. Follow the instructions in the “Power Down/Up Dialog” windows.
 - l. Select appropriate algorithm for the part. The high-speed algorithm will not work at 14.4 and 28.8 kbaud.
 - m. Double click on “Erase Module” – EM (see [Figure 9](#)).
 - n. Double click on “Program Module” – PM.
 - o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, \$FFF6–\$FFFD.
4. Operation — Forced monitor mode entry:
- Forced monitor mode is not supported by this ICS. However, this mode can be entered by using the procedure found in [ICP Using the External Communications Circuit \(No ICS\)](#).

ICP Using the External Communications Circuit (No ICS)

Use this procedure for performing ICP via an external communications circuit in place of this ICS to the target application.

1. Materials required:
 - a. PC with P&E software installed
 - b. Adapter/connector to connect the male end of the 9-pin serial cable to the target application
 - c. The external communications circuit. Also needed is a 5-volt power source to power this circuit (see [Figure 4](#), [Figure 5](#), and [Figure 6](#)).
 - d. Pin assignment diagram (see [Figure 1](#) and [Figure 2](#))
 - e. Monitor mode entry requirements (see [Table 1](#))
 - f. Crystal oscillator on the target or from an external clock source, with a value from [Table 2](#). If the crystal oscillator in the target application is not a value listed in [Table 2](#), it may be possible to “overdrive” the target crystal with an external clock. An example of this would be overdriving a target’s 32.768-kHz crystal with a 9.8304-MHz external clock.
 - g. Target board must have the ability to perform a POR not just a reset of the part (required to enter monitor mode).
2. Connections (see [Figure 4](#)):
 - a. 9-pin serial cable from PC to the external communications circuit
 - b. V+ pin of the RS-232 part to the $\overline{\text{IRQ1}}$ pin of the part
 - c. Communication pin of HC125 to PTA0 of the part
 - d. Target pin requirements:
 - PTA2 of the part to V_{SS}
 - PTA1 of the part to V_{DD} via a pullup resistor
 - PTC1 of the part to V_{SS} (crystal frequency \div 2) or to V_{DD} via a pullup resistor (crystal frequency \div 4). See [Table 2](#).
 - $\overline{\text{RESET}}$ has an internal pullup resistor.
 - e. It is assumed that all V_{DD} and V_{SS} pins on the part are already connected.

3. Operation — Standard monitor mode entry:
 - a. Launch P&E's WINIDE in the ICS08SRZ software.
 - b. Open desired file. (Demo file can be used for testing purposes.)
 - c. Assemble/Compile the file (see [Figure 7](#)).
 - d. Apply power to the external communications circuit.
 - e. Turn on power to the target.
 - f. Launch the programmer.
 - g. From "Target Hardware Type," select "Class III" (see [Figure 8](#)).
 - h. From "PC Serial Port Configuration," select the PC port in use and the appropriate baud rate ([Table 2](#)).
 - i. From "Target MCU Security Bytes," select appropriate security code (blank part = FF).
 - j. Select "Contact Target with these Settings..."
 - k. Follow the instructions in the "Power Cycle Dialog" window.
 - l. Select appropriate algorithm for the part. The high-speed algorithm will not work at 14.4 and 28.8 kbaud.
 - m. Double click on "Erase Module" – EM (see [Figure 9](#)).
 - n. Double click on "Program Module" – PM.
 - o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, \$FFF6–\$FFFD.

4. Operation — Forced monitor mode entry:
 - a. Blank part with oscillator value from [Table 2](#) (divide-by-4 options). See [Figure 5](#). If the crystal oscillator in the target application is not a value listed in [Table 2](#), it is possible to “overdrive” the target crystal with an external clock for the short duration of the programming sequence. An example of this would be overdriving a target’s 32.768-kHz crystal with a 9.8304-MHz external clock.
 - Remove connection to the $\overline{\text{IRQ1}}$ pin from V+ of the external communications circuit.
 - No connections to PTA1, PTA2, and PTC1 are necessary in this mode.
 - $\overline{\text{IRQ}}$ has an internal pullup resistor.
 - Follow steps in [3. Operation — Standard Monitor Entry](#).
 - b. Blank part with a 32.768-kHz oscillator. See [Figure 6](#).
 - Connect the $\overline{\text{IRQ1}}$ pin to V_{SS}.
 - Follow steps in [3. Operation — Standard Monitor Entry](#).
 - Note that external components are required on the CGMXFC pin, as the PLL will be used. Refer to the *MC68HC908SR12 Technical Data*, Motorola document order number MC68HC908SR12/D, for recommended component values.

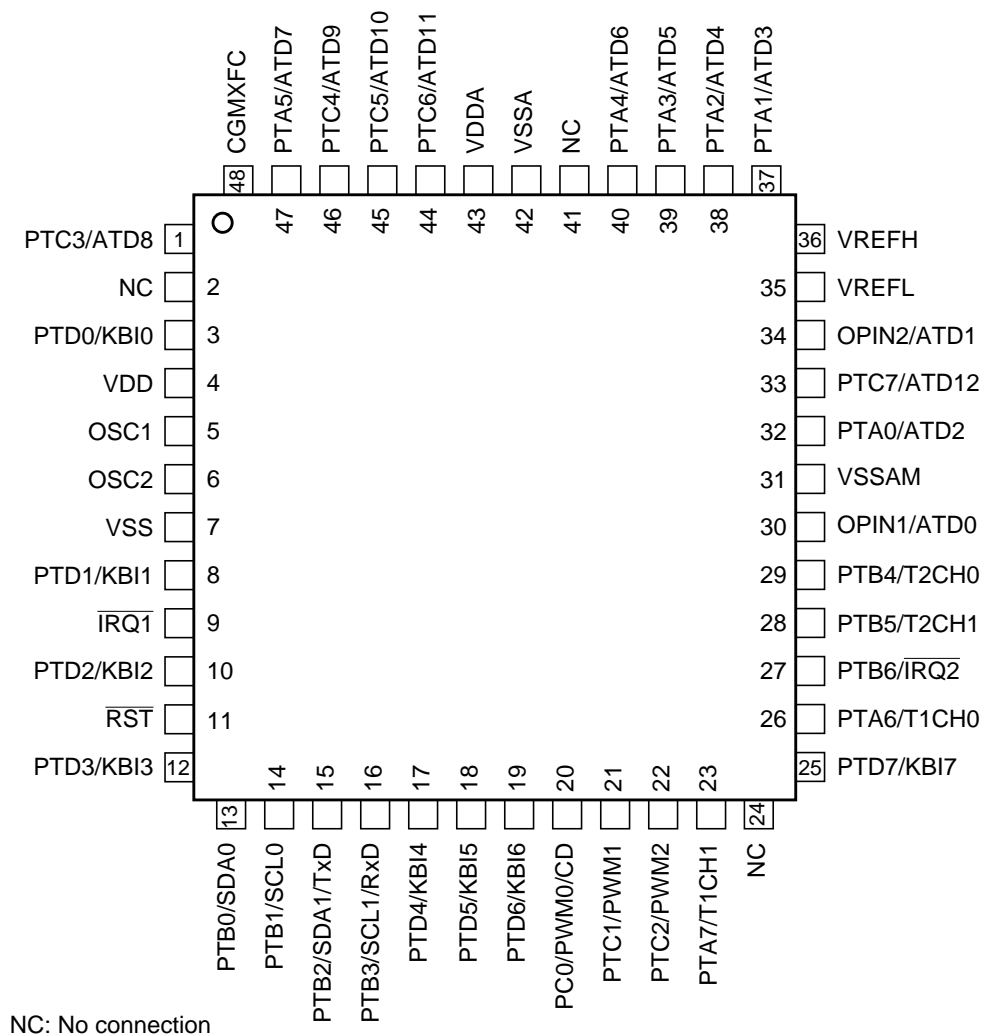
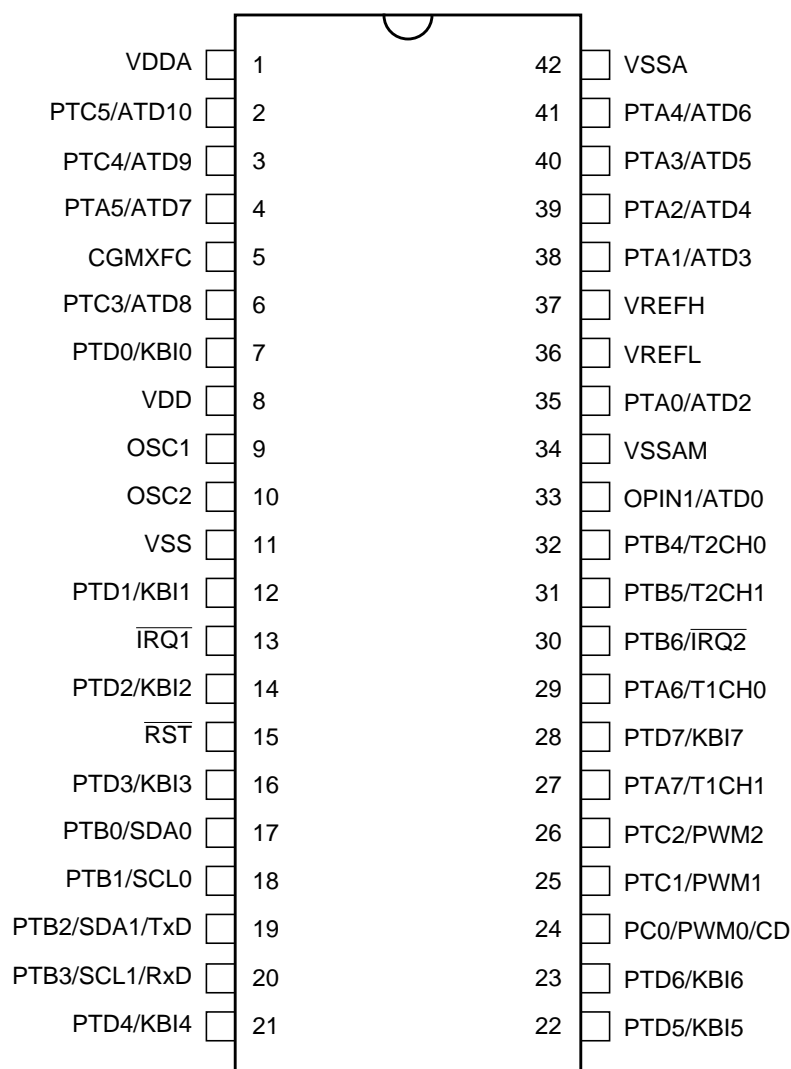


Figure 1. 48-Pin LQFP Pin Assignments



Pins Not Available on 42-Pin Package	Internal Connection
OPIN2/ATD1	Unconnected
PTC6/ATD11	Unconnected
PTC7/ATD12	Unconnected

Figure 2. 42-Pin SDIP Pin Assignments

Table 1. Monitor Mode Signal Requirements and Options

IRQ1	RST	Address \$FFFF/ \$FFFF	PTA2	PTA1	PTA0 (1)	PTC1	External Clock(2)	Bus Frequency	PLL	COP	Baud Rate	Comment
X	GND	X	X	X	X	X	X	0	X	Disabled	0	No operation until reset goes high
V _{TST}	V _{DD} or V _{TST}	X	0	1	1	0	4.9152 MHz	2.4576 MHz	OFF	Disabled	9600	PTA1 and PTA2 voltages only required if IRQ1 = V _{TST} ; PTC1 determines frequency divider
V _{TST}	V _{DD} or V _{TST}	X	0	1	1	1	9.8304 MHz	2.4576 MHz	OFF	Disabled	9600	PTA1 and PTA2 voltages only required if IRQ1 = V _{TST} ; PTC1 determines frequency divider
V _{DD}	V _{DD}	Blank "\$FFFF"	X	X	1	X	9.8304 MHz	2.4576 MHz	OFF	Disabled	9600	External frequency always ÷ by 4
GND	V _{DD}	Blank "\$FFFF"	X	X	1	X	32.768 kHz	2.4576 MHz	ON	Disabled	9600	PLL enabled (BCS set) in monitor mode
V _{DD} or GND	V _{TST}	X	X	X	X	X	X	—	OFF	Enabled	—	Enters user mode; will encounter illegal address reset
V _{DD} or GND	V _{DD} or V _{TST}	X	X	X	X	X	X	—	OFF	Enabled	—	Enters user mode

NOTES:

1. PTA)=1 if serial communication; PTA) = 0 if parallel communication
2. External clock is derived by a 32.768-kHz crystal or a 4.9152/9.8304-MHz off-chip oscillator.

Table 2. Crystal Frequency vs. Baud Rate

Divide-by-2 Option (PTC1 to Development Tool or V _{SS})		
Crystal Frequency (MHz)	Internal Bus Frequency (MHz)	Baud Rate
2.4576	1.2288	4800
4.9152	2.4576	9600
7.3728	3.6864	14,400
9.8304	4.9152	19,200
14.7456	7.3728	28,800
Divide-by-4 Option (PTC1 to V _{DD})		
4.9152	1.2288	4800
9.8304	2.4576	9600
14.7456	3.6864	14,400
19.6608	4.9152	19,200
29.4912	7.3728	28,800

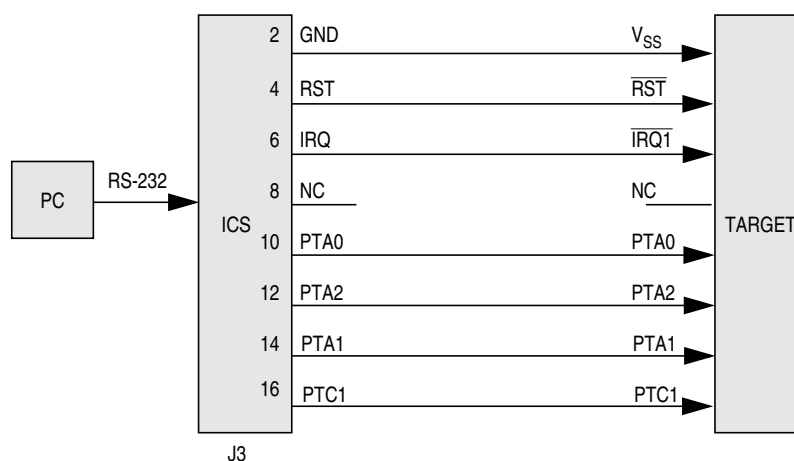


Figure 3. MC68HC908SR12 MON08 Connections

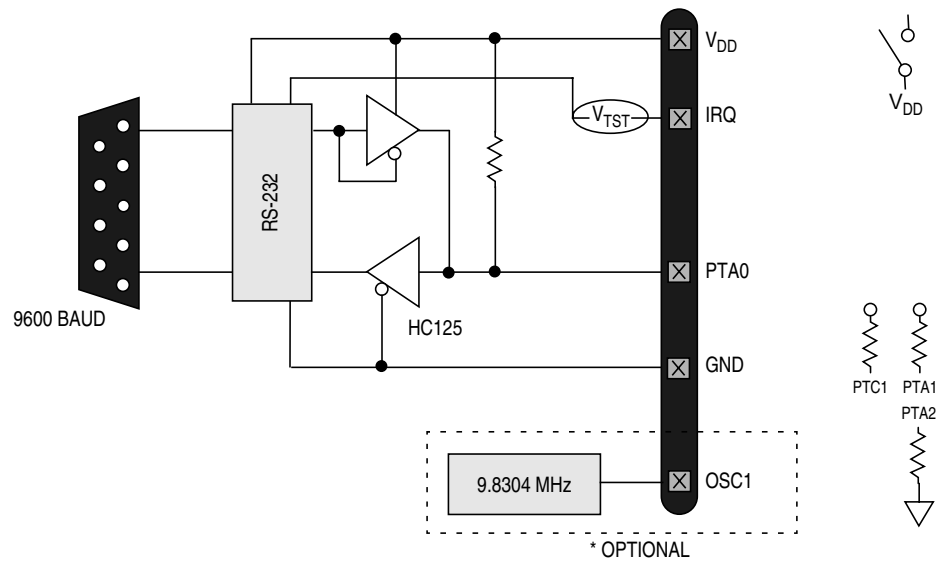


Figure 4. MC68HC908SR12 Standard Monitor Mode (9.8304 MHz)

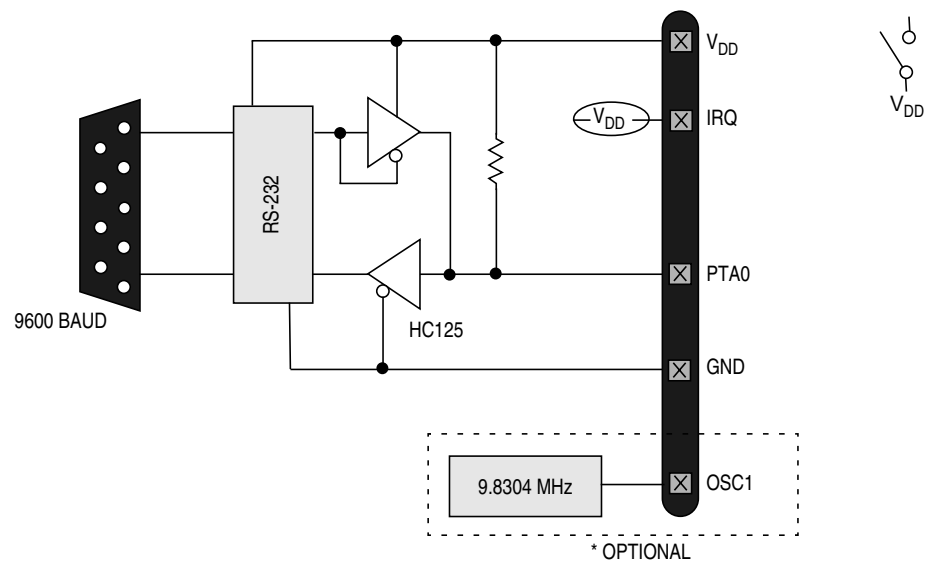


Figure 5. MC68HC908SR12 Forced Monitor Mode (9.8304 MHz)

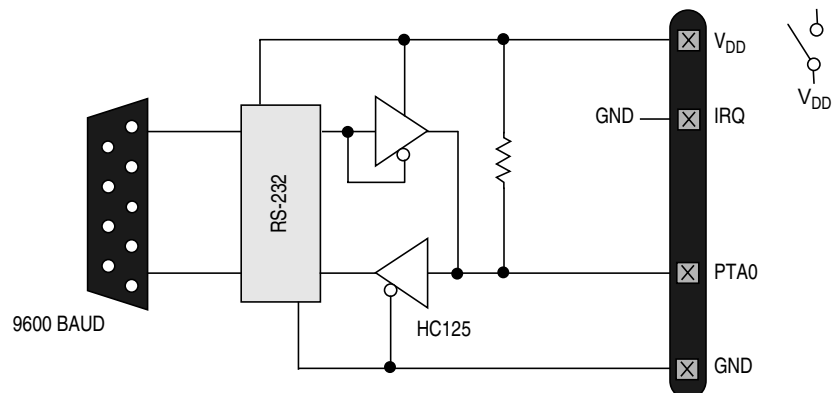


Figure 6. MC68HC908SR12 Forced Monitor Mode (32.768 kHz)

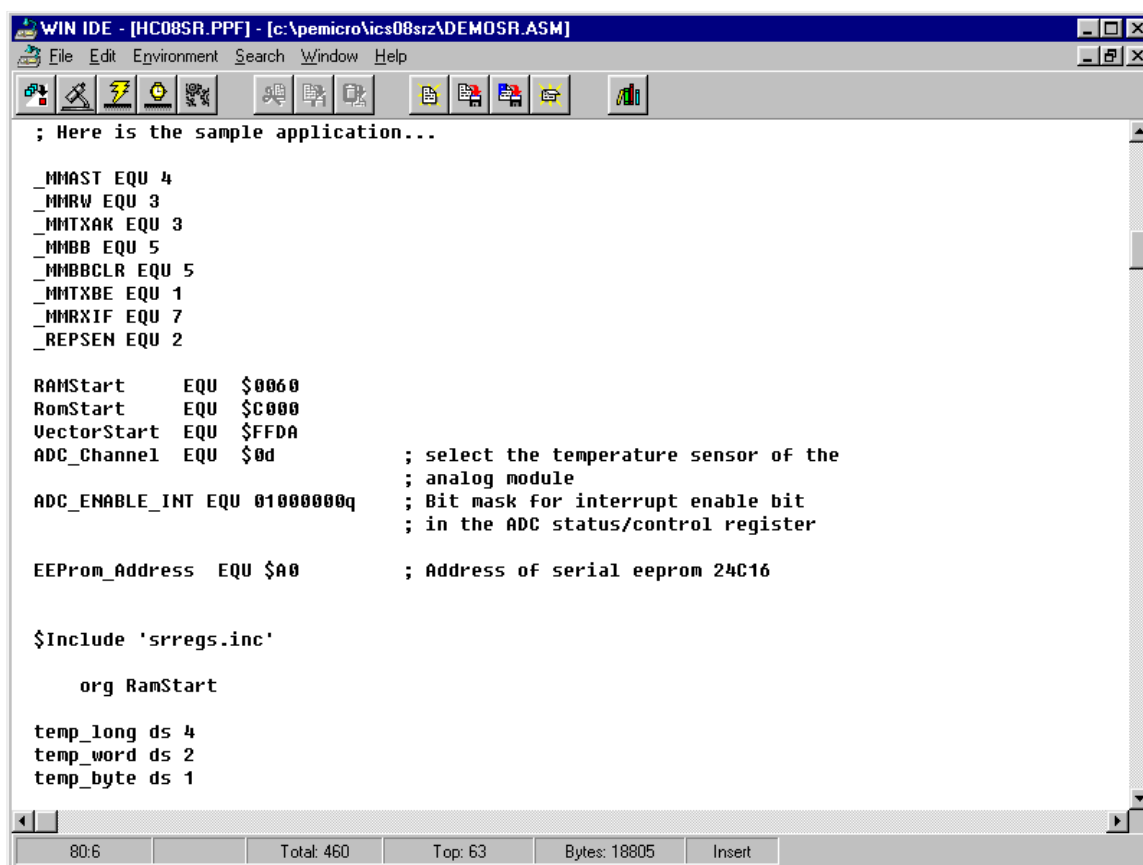


Figure 7. P&E's WINIDE Window

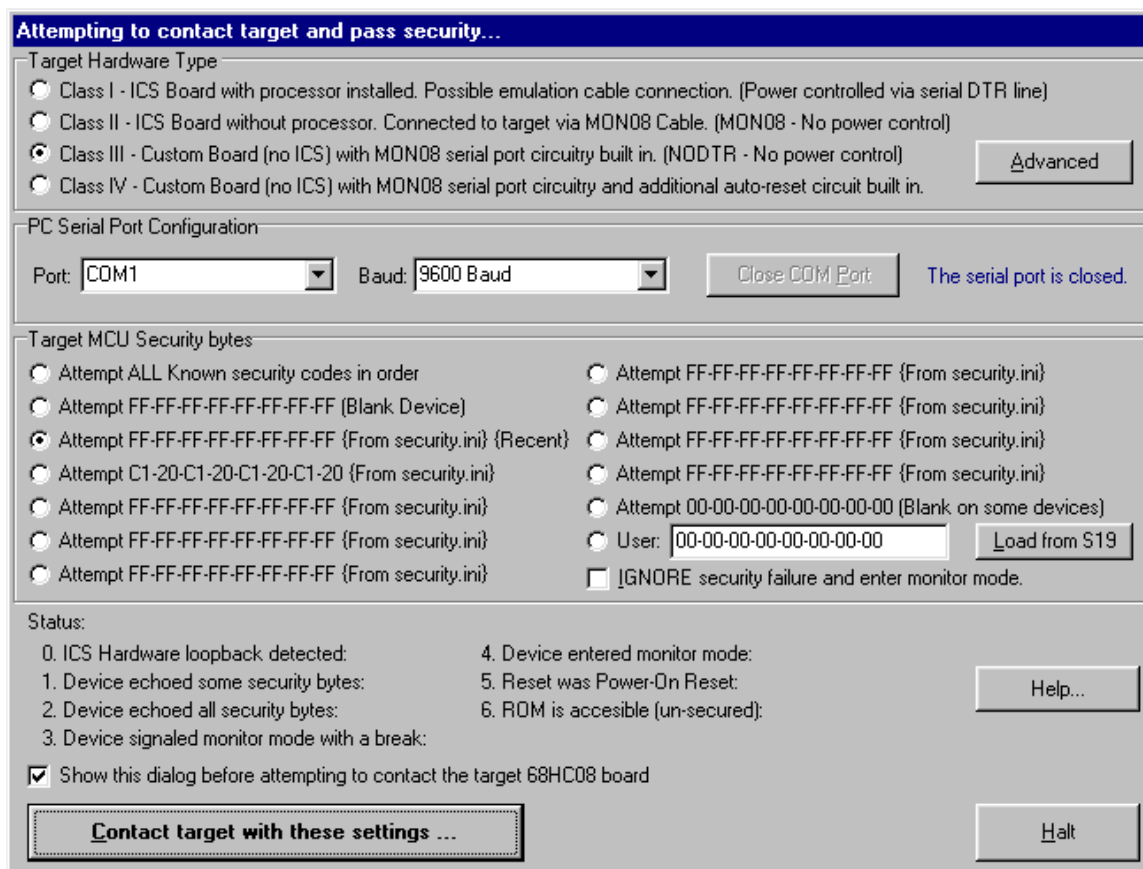


Figure 8. P&E's Target and Security Window

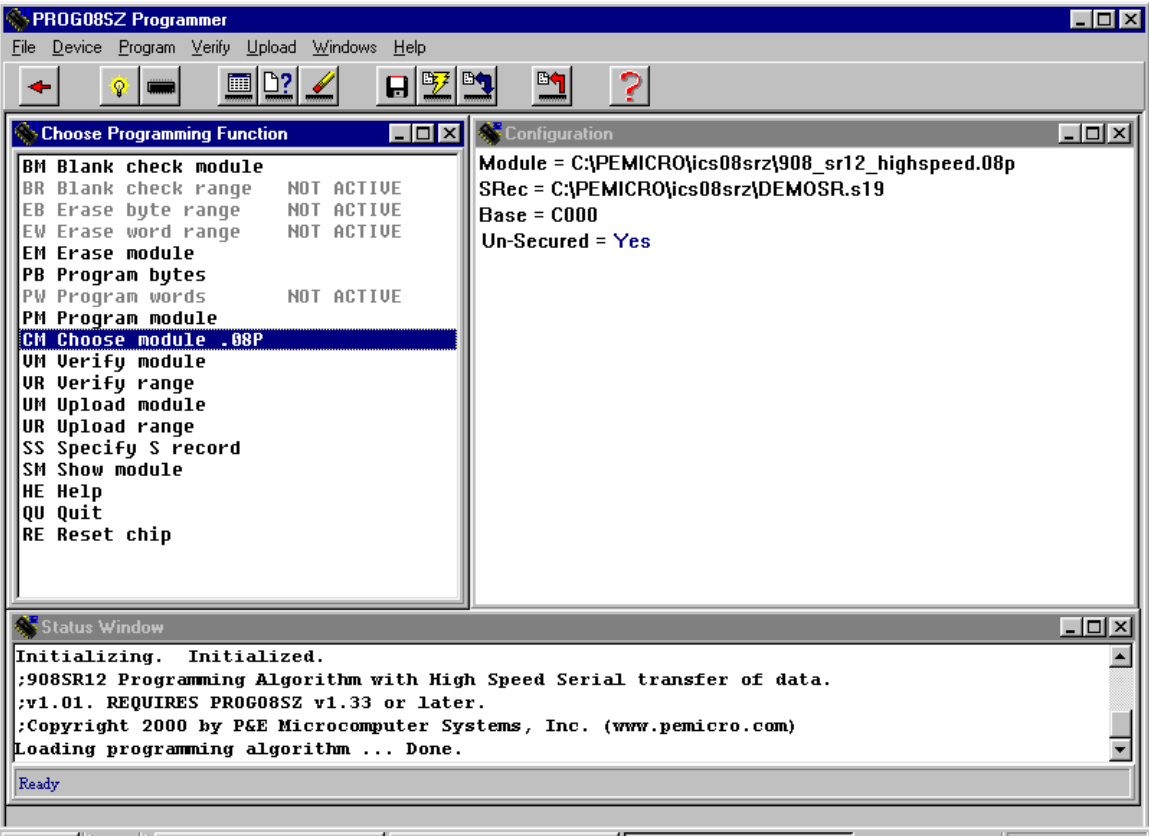



Figure 9. P&E's Programmer Window

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