

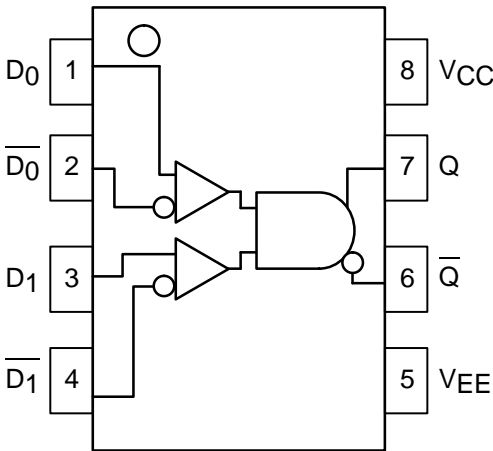
2-Input Differential AND/NAND

The MC100LVEL05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the MC100EL05 device and operates from a 3.3V supply voltage. With propagation delays and output transition times equivalent to the EL05, the LVEL05 is ideally suited for those applications which require the ultimate in AC performance at low voltage power supplies.

Because a negative 2-input NAND is equivalent to a 2-input OR function, the differential inputs and outputs of the device allows the LVEL05 to also be used as a 2-input differential OR/NOR gate.

- 340ps Propagation Delay
- High Bandwidth Output Transitions
- 75k Ω Internal Input Pulldown Resistors
- >2000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MC100LVEL05



D SUFFIX
8-LEAD PLASTIC SOIC PACKAGE
CASE 751-05

PIN DESCRIPTION

PIN	FUNCTION
D0, D1 Q	Data Inputs Data Outputs



DC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = \text{GND}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		18	25		18	25		18	25		19	26	mA
V_{EE}	Power Supply Voltage	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA

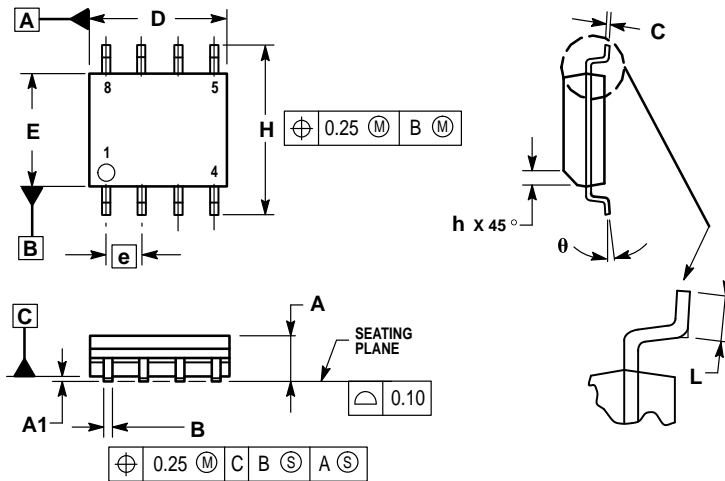
AC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = \text{GND}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay to Output	240	260	440	240		440	240	340	440	250		450	ps
V_{PP}	Minimum Input Swing (Note 1.)	150			150			150			150			mV
V_{CMR}	Common Mode Range (Note 2.) $V_{PP} < 500\text{mV}$ $V_{PP} \geq 500\text{mV}$	-2.1 -1.9		-0.2 -0.2	-2.2 -2.0		-0.2 -0.2	-2.2 -2.0		-0.2 -0.2	-2.2 -2.0		-0.2 -0.2	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100		320	100		320	100	210	320	100		320	ps

1. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The number in the spec table assumes a nominal $V_{EE} = -3.3\text{V}$. Note for PECL operation, the $V_{CMR}(\text{min})$ will be fixed at $3.3\text{V} - |V_{CMR}(\text{min})|$.

OUTLINE DIMENSIONS


D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE R



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

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