

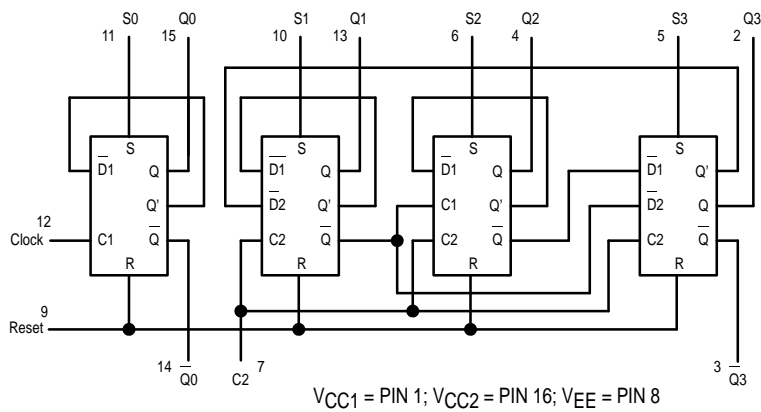
Bi-Quinary Counter

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set–reset master–slave flip–flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous “set” or “clear.” Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits.

$P_D = 370 \text{ mW typ/pkg (No Load)}$
 $f_{\text{tog}} = 150 \text{ MHz typ}$
 $t_r, t_f = 2.5 \text{ ns typ (20\%–80\%)}$

LOGIC DIAGRAM



$V_{CC1} = \text{PIN } 1; V_{CC2} = \text{PIN } 16; V_{EE} = \text{PIN } 8$

COUNTER TRUTH TABLES

BI-QUINARY

(Clock connected to C2
and Q3 connected to C1)

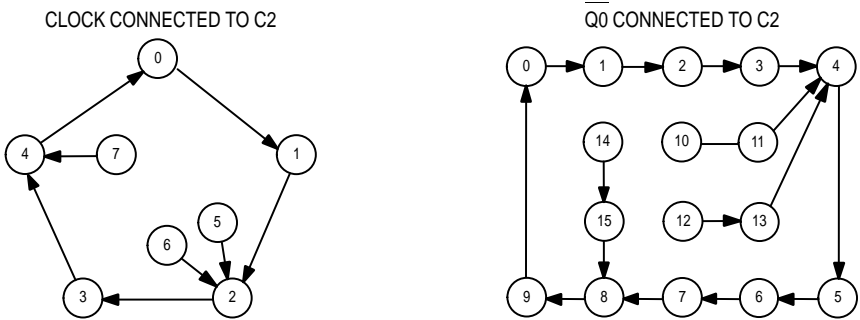
| COUNT | Q1 | Q2 | Q3 | Q0 |
|-------|----|----|----|----|
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | L | L | L | H |
| 6 | H | L | L | H |
| 7 | L | H | L | H |
| 8 | H | H | L | H |
| 9 | L | L | H | H |

BCD

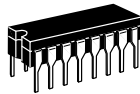
(Clock connected to C1
and Q0 connected to C2)

| COUNT | Q0 | Q1 | Q2 | Q3 |
|-------|----|----|----|----|
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |

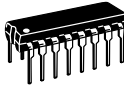
COUNTER STATE DIAGRAM — POSITIVE LOGIC



MC10138



L SUFFIX
CERAMIC PACKAGE
CASE 620–10

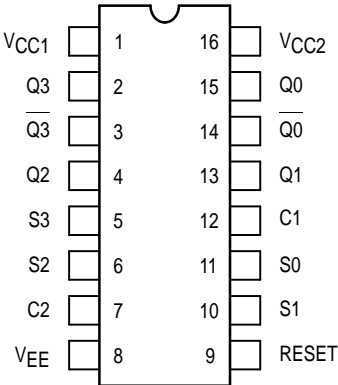


P SUFFIX
PLASTIC PACKAGE
CASE 648–08



FN SUFFIX
PLCC
CASE 775–02

DIP
PIN ASSIGNMENT




Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion
Tables on page 6–11 of the Motorola MECL Data
Book (DL122/D).

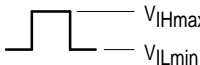


ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Pin Under Test | Test Limits | | | | | | | Unit |
|--|---------------------|---|----------------------------|----------------------------|----------------------------|-----|----------------------------|----------------------------|----------------------------|------|
| | | | −30°C | | +25°C | | | +85°C | | |
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Power Supply Drain Current | I _E | 8 | | 97 | | 70 | 88 | | 97 | mAdc |
| Input Current | I _{inH} | 12 5,6,10,11 7 9 | | 350 390 460 650 | | | 220 245 290 410 | | 220 245 290 | μAdc |
| | I _{inL} | All | 0.5 | | 0.5 | | | 0.3 | | μAdc |
| Output Voltage Logic 1 | V _{OH} | 3,14 (3.) 2,4,13,15 (2.) | −1.060 −1.060 | −0.890 −0.890 | −0.960 −0.960 | | −0.810 −0.810 | −0.890 −0.890 | −0.700 −0.700 | Vdc |
| Output Voltage Logic 0 | V _{OL} | 3,14 (2.) 2,4,13,15 (3.) | −1.890 −1.890 | −1.675 −1.675 | −1.850 −1.850 | | −1.650 −1.650 | −1.825 −1.825 | −1.615 −1.615 | Vdc |
| Threshold Voltage Logic 1 | V _{OHA} | 2,4,13,15 (2.) 3,14 (3.) 13,15 (2.) | −1.080 −1.080 −1.080 | | −0.980 −0.980 −0.980 | | | −0.910 −0.910 −0.910 | | Vdc |
| Threshold Voltage Logic 0 | V _{OLA} | 2,4,13,15 (3.) 3,14 (2.) 13,15 (3.) | | −1.655 −1.655 −1.655 | | | −1.630 −1.630 −1.630 | | −1.595 −1.595 −1.595 | Vdc |
| Switching Times (50Ω Load) | | | | | | | | | | ns |
| Propagation Clock Delays Delay | t ₁₂₊₁₅₊ | 15 | 1.4 | 5.0 | 1.5 | 3.5 | 4.8 | 1.5 | 5.3 | |
| | t ₁₂₊₁₄₊ | 14 | 1.4 | 5.0 | 1.5 | 3.5 | 4.8 | 1.5 | 5.3 | |
| | t ₇₊₁₃₊ | 13 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | |
| | t ₇₊₄₊ | 4 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | |
| | t ₇₊₂₊ | 2 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | |
| | t ₇₊₃₊ | 3 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | |
| | t _{12+15−} | 15 | 1.4 | 5.0 | 1.5 | 3.5 | 4.8 | 1.5 | 5.3 | |
| | t _{12+14−} | 14 | 1.4 | 5.0 | 1.5 | 3.5 | 4.8 | 1.5 | 5.3 | |
| | t _{7+13−} | 13 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | |
| | t _{7+4−} | 4 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | |
| t _{7+2−} | 2 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | | |
| t _{7+3−} | 3 | 1.4 | 5.2 | 1.5 | 3.5 | 5.0 | 1.5 | 5.5 | | |
| Set Delay | t ₁₁₊₁₅₊ | 15 | 1.4 | 5.2 | 1.5 | | 5.0 | 1.5 | 5.5 | |
| | t _{11+14−} | 14 | 1.4 | 5.2 | 1.5 | | 5.0 | 1.5 | 5.5 | |
| Reset Delay | t ₉₊₁₄₊ | 14 | 1.4 | 5.2 | 1.5 | | 5.0 | 1.5 | 5.5 | |
| | t _{9+15−} | 15 | 1.4 | 5.2 | 1.5 | | 5.0 | 1.5 | 5.5 | |
| Rise Time (20 to 80%) | t ₁₄₊ | 14 | 1.1 | 4.7 | 1.1 | 2.5 | 4.5 | 1.1 | 5.0 | |
| | t ₁₅₊ | 15 | 1.1 | 4.7 | 1.1 | 2.5 | 4.5 | 1.1 | 5.0 | |
| Fall Time (20 to 80%) | t _{14−} | 14 | 1.1 | 4.7 | 1.1 | 2.5 | 4.5 | 1.1 | 5.0 | |
| | t _{15−} | 15 | 1.1 | 4.7 | 1.1 | 2.5 | 4.5 | 1.1 | 5.0 | |
| Counting Frequency | f _{count} | 2 | 125 | | 125 | 150 | | 125 | | MHz |
| | | 15 | 125 | | 125 | 150 | | 125 | | |



1. Individually test each input; apply V_{ILmin} to pin under test.

2. Set all four flip-flops by applying pulse  V_{IHmax} to pins 5, 6, 10, and 11 prior to applying test voltage indicated.

3. Reset all four flip-flops by applying pulse  V_{IHmax} to pin 9 prior to applying test voltage indicated.

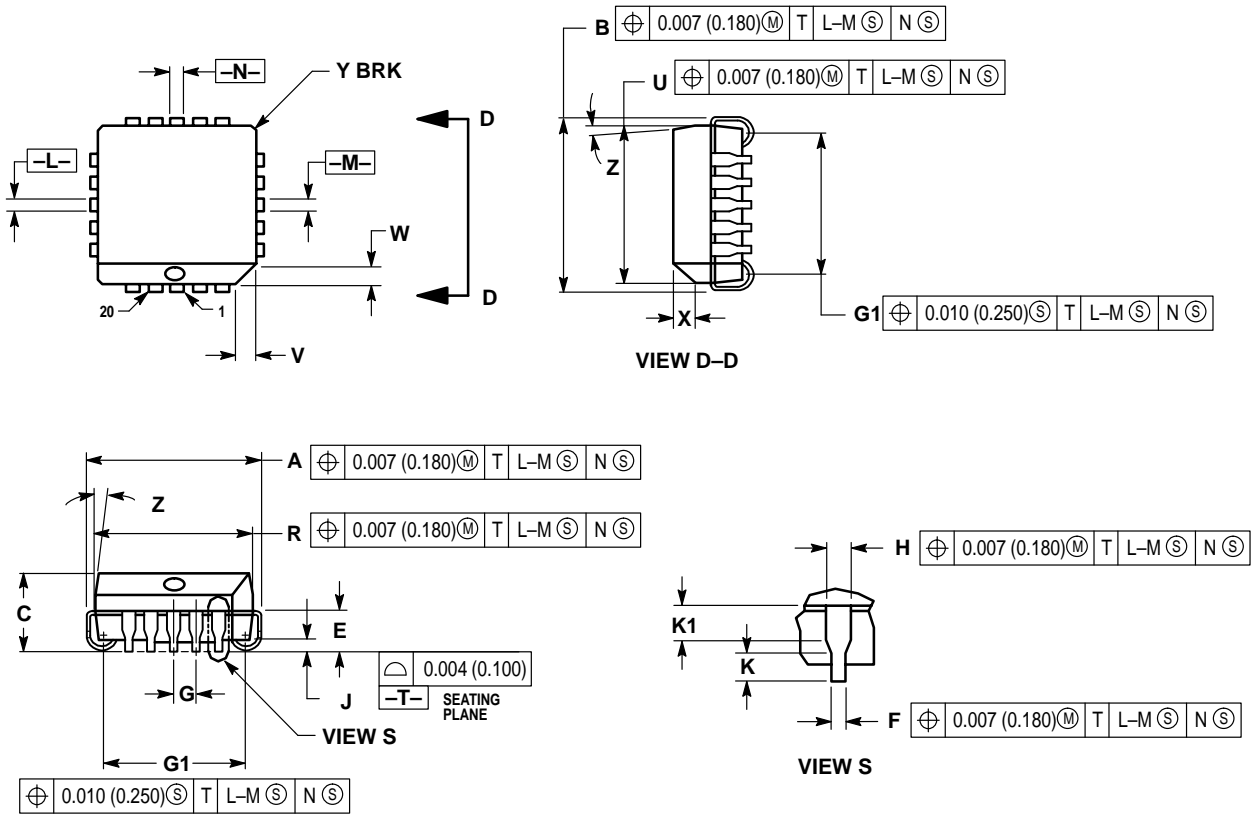
ELECTRICAL CHARACTERISTICS (continued)

| | | | | | | | | | | |
|---|------------------|---------------------|---|---------------------|-----------------------------|------------------------|------------------------|---------------------------|-------------------------|---------------------------|
| NOTE: Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner. | | | @ Test Temperature | | TEST VOLTAGE VALUES (Volts) | | | | | (V _{CC}) Gnd |
| | | | | | | | | | | |
| | | | | | V _{IH} max | V _{IL} min | V _{IH} Amin | V _{IL} Amax | V _{EE} | |
| | | | | | -30°C | | | | | |
| | | | | | +25°C | | | | | |
| | | | | | -0.890 | -1.890 | -1.205 | -1.500 | -5.2 | |
| | | | | | -0.810 | -1.850 | -1.105 | -1.475 | -5.2 | |
| | | | | | -0.700 | -1.825 | -1.035 | -1.440 | -5.2 | |
| Characteristic | Symbol | Pin Under Test | TEST VOLTAGE APPLIED TO PINS LISTED BELOW | | | | | (V _{CC}) Gnd | | |
| | | | V _{IH} max | V _{IL} min | V _{IH} Amin | V _{IL} Amax | V _{EE} | | | |
| Power Supply Drain Current | I _E | 8 | 9 | | | | 8 | 1, 16 | | |
| Input Current | I _{inH} | 12 | 12 | | | | 8 | 1, 16 | | |
| | | 5,6,10,11 | 5,6,10,11 | | | | 8 | 1, 16 | | |
| | | 7 | 7 | | | | 8 | 1, 16 | | |
| | | 9 | 9 | | | | 8 | 1, 16 | | |
| | I _{inL} | All | | Note 1. | | | 8 | 1, 16 | | |
| Output Voltage | Logic 1 | V _{OH} | 3,14 (3.) 2,4,13,15 (2.) | 9 5,6,10,11 | | | 8 8 | 1, 16 1, 16 | | |
| Output Voltage | Logic 0 | V _{OL} | 3,14 (2.) 2,4,13,15 (3.) | 5,6,10,11 9 | | | 8 8 | 1, 16 1, 16 | | |
| Threshold Voltage | Logic 1 | V _{OHA} | 2,4,13,15 (2.) 3,14 (3.) 13,15 (2.) | | | 5,6,10,11 9 7,12 | 8 8 8 | 1, 16 1, 16 1, 16 | | |
| Threshold Voltage | Logic 0 | V _{OLA} | 2,4,13,15 (3.) 3,14 (2.) 13,15 (3.) | | | | 5,6,10,11 9 7,12 | 8 8 8 | 1, 16 1, 16 1, 16 | |
| Switching Times | (50Ω Load) | | | | | Pulse In | Pulse Out | -3.2 V | +2.0 V | |
| Propagation Delay | Clock Delays | t ₁₂₊₁₅₊ | 15 | | | 12 | 15 | 8 | 1, 16 | |
| | | t ₁₂₊₁₄₊ | 14 | | | 12 | 14 | 8 | 1, 16 | |
| | | t ₇₊₁₃₊ | 13 | | | 7 | 13 | 8 | 1, 16 | |
| | | t ₇₊₄₊ | 4 | | | 7 | 4 | 8 | 1, 16 | |
| | | t ₇₊₂₊ | 2 | | | 7 | 2 | 8 | 1, 16 | |
| | | t ₇₊₃₊ | 3 | | | 7 | 3 | 8 | 1, 16 | |
| | | t ₁₂₊₁₅₋ | 15 | | | 12 | 15 | 8 | 1, 16 | |
| | | t ₁₂₊₁₄₋ | 14 | | | 12 | 14 | 8 | 1, 16 | |
| | | t ₇₊₁₃₋ | 13 | | | 7 | 13 | 8 | 1, 16 | |
| | | t ₇₊₄₋ | 4 | | | 7 | 4 | 8 | 1, 16 | |
| | | t ₇₊₂₋ | 2 | | | 7 | 2 | 8 | 1, 16 | |
| | | t ₇₊₃₋ | 3 | | | 7 | 3 | 8 | 1, 16 | |
| Set Delay | | t ₁₁₊₁₅₊ | 15 | | | 11 | 15 | 8 | 1, 16 | |
| | | t ₁₁₊₁₄₋ | 14 | | | 11 | 14 | 8 | 1, 16 | |
| Reset Delay | | t ₉₊₁₄₊ | 14 | | | 9 | 14 | 8 | 1, 16 | |
| | | t ₉₊₁₅₋ | 15 | | | 9 | 15 | 8 | 1, 16 | |
| Rise Time | (20 to 80%) | t ₁₄₊ | 14 | | | 11 | 14 | 8 | 1, 16 | |
| | | t ₁₅₊ | 15 | | | 11 | 15 | 8 | 1, 16 | |
| Fall Time | (20 to 80%) | t ₁₄₋ | 14 | | | 9 | 14 | 8 | 1, 16 | |
| | | t ₁₅₋ | 15 | | | 9 | 15 | 8 | 1, 16 | |
| Counting Frequency | | f _{count} | 2 | | | 7 | 2 | 8 | 1, 16 | |
| | | | 15 | | | 12 | 15 | 8 | 1, 16 | |

1. Individually test each input; apply V_{ILmin} to pin under test.2. Set all four flip-flops by applying pulse  to pins 5, 6, 10, and 11 prior to applying test voltage indicated.3. Reset all four flip-flops by applying pulse  to pin 9 prior to applying test voltage indicated.

OUTLINE DIMENSIONS

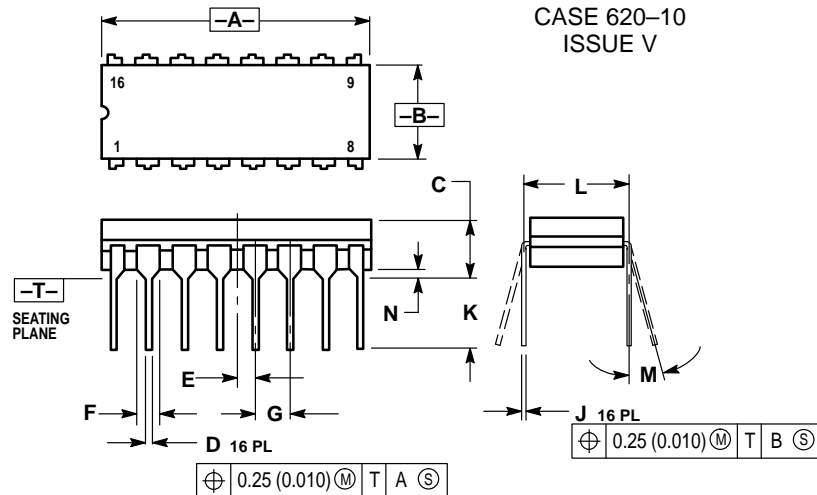
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



- NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 5. CONTROLLING DIMENSION: INCH.
 6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.385 | 0.395 | 9.78 | 10.03 |
| B | 0.385 | 0.395 | 9.78 | 10.03 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.350 | 0.356 | 8.89 | 9.04 |
| U | 0.350 | 0.356 | 8.89 | 9.04 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2 ° | 10 ° | 2 ° | 10 ° |
| G1 | 0.310 | 0.330 | 7.88 | 8.38 |
| K1 | 0.040 | — | 1.02 | — |

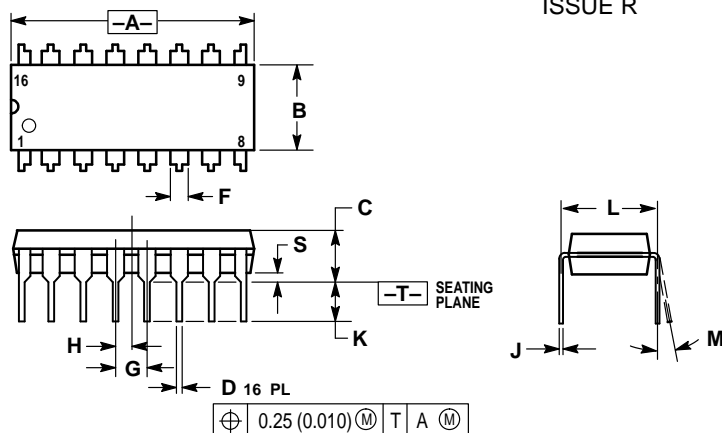
OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 620-10
ISSUE V


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.


| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | — | 0.200 | — | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE R


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

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