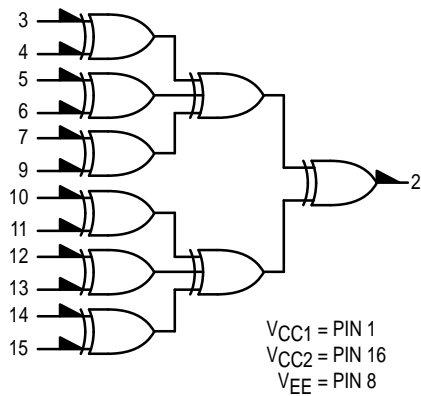


# 12-Bit Parity Generator-Checker

The MC10160 consists of nine Exclusive-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

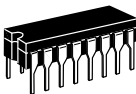
$P_D = 320 \text{ mW typ/pkg (No Load)}$   
 $t_{pd} = 5.0 \text{ ns typ}$   
 $t_r, t_f = 2.0 \text{ ns typ (20\%–80\%)}$

LOGIC DIAGRAM

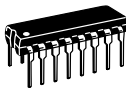


INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

## MC10160

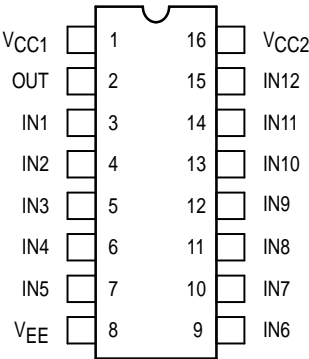


**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08

PIN ASSIGNMENT



## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I <sub>E</sub>	8		86		62	78		86	mAdc
Input Current	I <sub>inH</sub> (Note 1.)	3		425			265		265	μAdc
		4		350			220		220	
	I <sub>inL</sub>	3	0.5		0.5			0.3		μAdc
Output Voltage      Logic 1	V <sub>OH</sub>	2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc
Output Voltage      Logic 0	V <sub>OL</sub>	2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc
Threshold Voltage    Logic 1	V <sub>OHA</sub>	2	−1.080		−0.980			−0.910		Vdc
Threshold Voltage    Logic 0	V <sub>OLA</sub>	2		−1.655			−1.630		−1.595	Vdc
Switching Times    (50Ω Load)										ns
Propagation Delay	t <sub>3+2+</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t <sub>3+2−</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t <sub>3−2−</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t <sub>3−2+</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t <sub>4+2+</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t <sub>4+2−</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t <sub>4−2−</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t <sub>4−2+</sub>	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
Rise Time            (20 to 80%)	t <sub>2+</sub>	2	1.1	3.5	1.1	2.0	3.3	1.0	3.5	
Fall Time            (20 to 80%)	t <sub>2−</sub>	2	1.1	3.5	1.1	2.0	3.3	1.0	3.5	

1. Pins 3, 6, 7, 11, 12, 15 are similar. Pins 4, 5, 9, 10, 13, 14 are similar.

**ELECTRICAL CHARACTERISTICS** (continued)

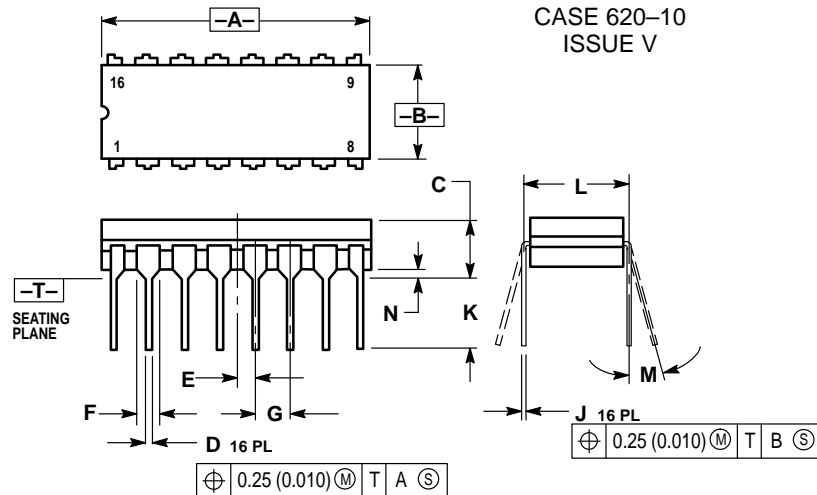
@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V <sub>CC</sub> ) Gnd
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
			−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
			+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
			+85°C	−0.700	−1.825	−1.035	−1.440	−5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V <sub>CC</sub> ) Gnd
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>	
Power Supply Drain Current	I <sub>E</sub>	8	4,5,9, 10,13,14				8	1,16
Input Current	I <sub>inH</sub> (Note 1.)	3 4	3 4				8 8	1,16 1,16
	I <sub>inL</sub>	3		3			8	1,16
Output Voltage Logic 1	V <sub>OH</sub>	2	3	4,5,6,7,9,10, 11,12,13,14,15			8	1,16
Output Voltage Logic 0	V <sub>OL</sub>	2		3,4,5,6,7,9,10, 11,12,13,14,15			8	1,16
Threshold Voltage Logic 1	V <sub>OHA</sub>	2		4,5,6,7,9,10, 11,12,13,14,15	3		8	1,16
Threshold Voltage Logic 0	V <sub>OLA</sub>	2		3,5,6,7,9,10, 11,12,13,14,15		4	8	1,16
Switching Times (50Ω Load)			+1.11V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t <sub>3+2+</sub>	2			3	2	8	1,16
	t <sub>3+2−</sub>	2	4		3	2	8	1,16
	t <sub>3−2−</sub>	2			3	2	8	1,16
	t <sub>3−2+</sub>	2	4		3	2	8	1,16
	t <sub>4+2+</sub>	2			4	2	8	1,16
	t <sub>4+2−</sub>	2	3		4	2	8	1,16
	t <sub>4−2−</sub>	2			4	2	8	1,16
	t <sub>4−2+</sub>	2	3		4	2	8	1,16
Rise Time (20 to 80%)	t <sub>2+</sub>	2			3	2	8	1,16
Fall Time (20 to 80%)	t <sub>2−</sub>	2			3	2	8	1,16

1. Pins 3, 6, 7, 11, 12, 15 are similar. Pins 4, 5, 9, 10, 13, 14 are similar.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

## OUTLINE DIMENSIONS

**L SUFFIX**  
**CERAMIC DIP PACKAGE**  
**CASE 620-10**  
**ISSUE V**

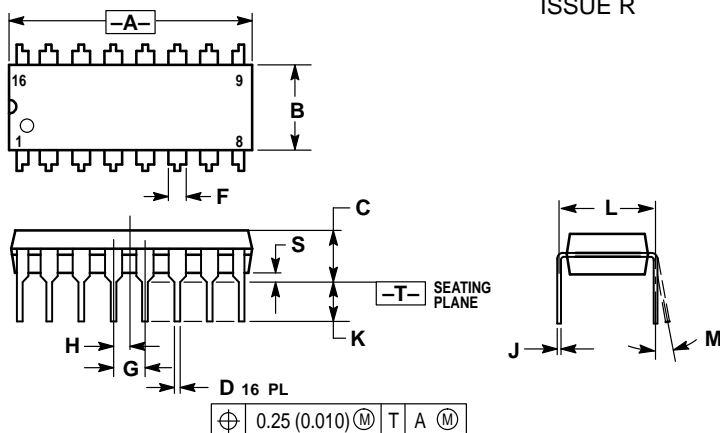


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01


**P SUFFIX**  
**PLASTIC DIP PACKAGE**  
**CASE 648-08**  
**ISSUE R**



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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