

## 16 x 4 Bit Register File (RAM)

The MC10H145 is a 16 x 4 bit register file. The active-low chip select allows easy expansion.

The operating mode of the register file is controlled by the  $\overline{WE}$  input. When  $\overline{WE}$  is "low" the device is in the write mode, the outputs are "low" and the data present at  $D_n$  input is stored at the selected address, when  $\overline{WE}$  is "high," the device is in the read mode — the data state at the selected location is present at the  $Q_n$  outputs.

- Address Access Time, 4.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

### MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply ( $V_{CC} = 0$ )	$V_{EE}$	-8.0 to 0	Vdc
Input Voltage ( $V_{CC} = 0$ )	$V_I$	0 to $V_{EE}$	Vdc
Output Current — Continuous — Surge	$I_{out}$	50 100	mA
Operating Temperature Range	$T_A$	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	$T_{stg}$	-55 to +150 -55 to +165	°C

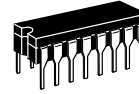
### ELECTRICAL CHARACTERISTICS ( $V_{EE} = -5.2 \text{ V} \pm 5\%$ ) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	$I_E$	—	160	—	163	—	165	mA
Input Current High	$I_{inH}$	—	375	—	220	—	220	$\mu\text{A}$
Input Current Low	$I_{inL}$	0.5	—	0.5	—	0.3	—	$\mu\text{A}$
High Output Voltage	$V_{OH}$	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	$V_{OL}$	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	$V_{IH}$	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	$V_{IL}$	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

#### NOTE:

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

## MC10H145



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



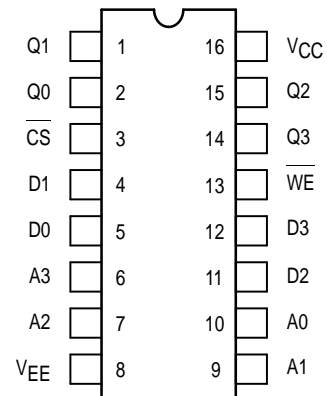
**FN SUFFIX**  
PLCC  
CASE 775-02

### TRUTH TABLE

MODE	INPUT			OUTPUT
	CS	WE	$D_n$	$Q_n$
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	X	Q
Disabled	H	X	X	L

Q-State of Addressed Cell

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6-11 of the Motorola MECL Data Book (DL122/D).

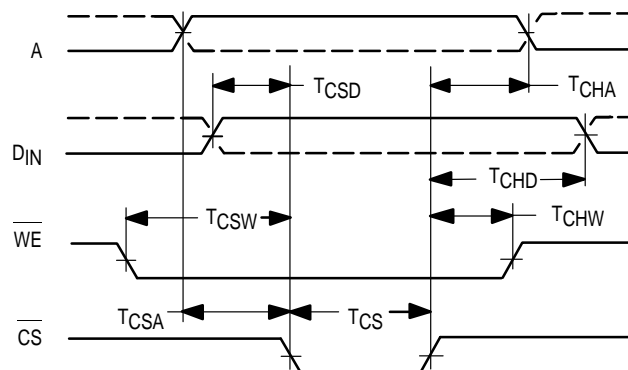


## AC PARAMETERS

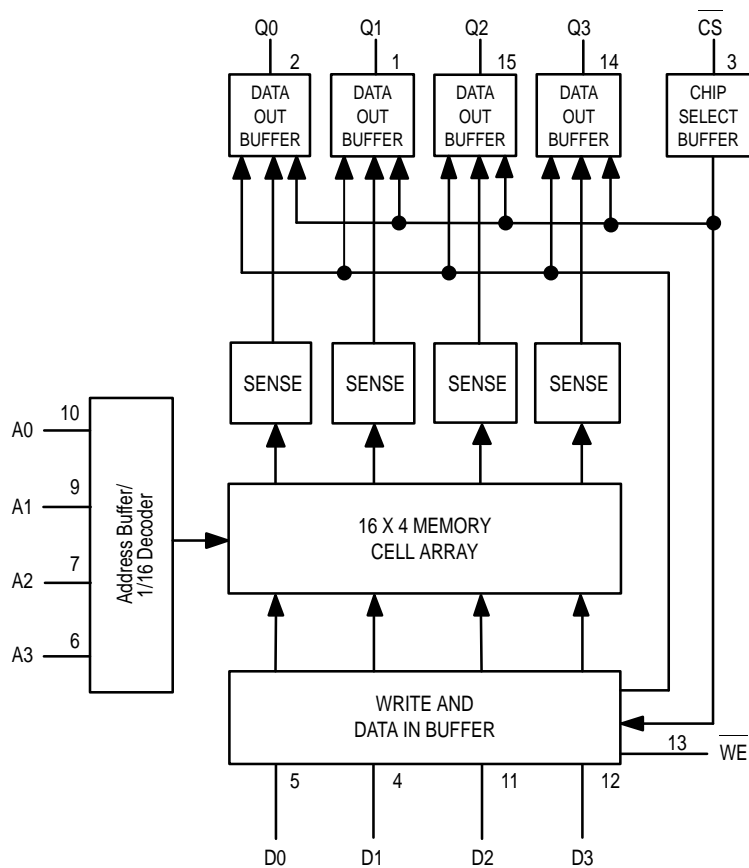
Characteristics	Symbol	MC10H145 $T_A = 0 \text{ to } +75^\circ\text{C}$ , $V_{EE} = -5.2 \text{ Vdc} \pm 5\%$		Unit	Conditions
		Min	Max		
Read Mode					
Chip Select Access Time	$t_{ACS}$	0	4.0	ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Recovery Time	$t_{RCS}$	0	4.0		
Address Access Time	$t_{AA}$	0	6.0		
Write Mode					
Write Pulse Width	$t_W$	6.0	—	ns	$t_{WSA} = 3.5 \text{ ns}$ Measured at 50% of input to 50% of output. $t_{WV} = 6.0 \text{ ns}$ .
Data Setup Time Prior to Write	$t_{WSD}$	0	—		
Data Hold Time After Write	$t_{WHD}$	1.5	—		
Address Setup Time Prior to Write	$t_{WSA}$	3.5	—		
Address Hold Time After Write	$t_{WHA}$	1.5	—		
Chip Select Setup Time Prior to Write	$t_{WSCS}$	0	—		
Chip Select Hold Time After Write	$t_{WHCS}$	1.5	—		
Write Disable Time	$t_{WS}$	1.0	4.0		
Write Recovery Time	$t_{WR}$	1.0	4.0		
Chip Enable Strobe Mode					
Data Setup Prior to Chip Select	$t_{CSD}$	0	—	ns	Guaranteed but not tested on standard product. See Figure 1.
Write Enable Setup Prior to Chip Select	$t_{CSW}$	0	—		
Address Setup Prior to Chip Select	$t_{CSA}$	0	—		
Data Hold Time After Chip Select	$t_{CHD}$	1.0	—		
Write Enable Hold Time After Chip Select	$t_{CHW}$	0	—		
Address Hold Time After Chip Select	$t_{CHA}$	2.0	—		
Chip Select Minimum Pulse Width	$t_{CS}$	4.0	—		
Rise and Fall Time	$t_r, t_f$				
Address to Output		0.6	2.5	ns	Measured between 20% and 80% points.
CS to Output		0.6	2.5		
Capacitance					
Input Capacitance	$C_{in}$	—	6.0	pF	Measured with a pulse technique.
Output Capacitance	$C_{out}$	—	8.0		

- NOTES: 1. Test circuit characteristics:  $R_T = 50 \, \Omega$ , MC10H145.  $C_L \leq 5.0 \text{ pF}$  (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

FIGURE 1 — CHIP ENABLE STROBE MODE

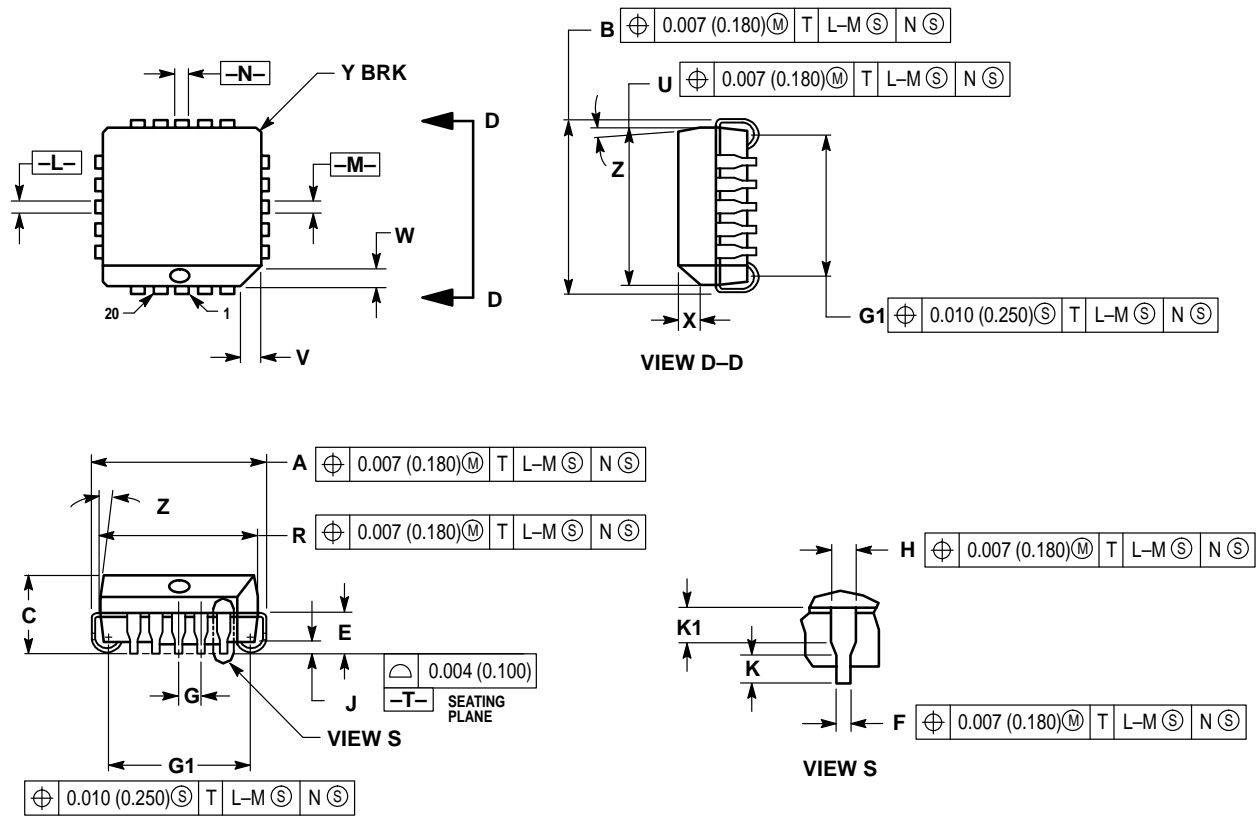


### BLOCK DIAGRAM



OUTLINE DIMENSIONS

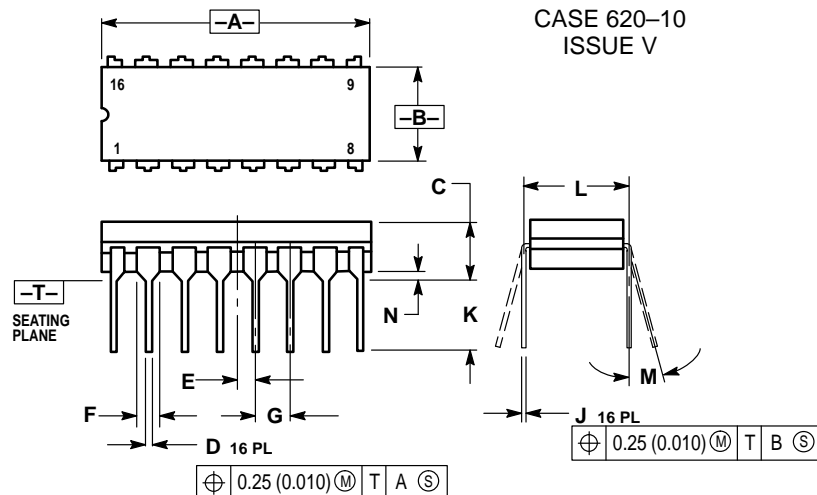
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE C



- NOTES:
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
  - DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  - DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.
  - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
  - DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

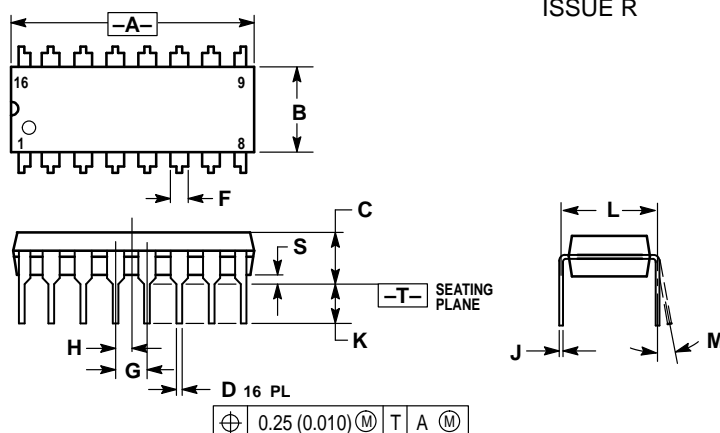
## OUTLINE DIMENSIONS

**L SUFFIX**  
**CERAMIC DIP PACKAGE**  
**CASE 620-10**  
**ISSUE V**


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**P SUFFIX**  
**PLASTIC DIP PACKAGE**  
**CASE 648-08**  
**ISSUE R**


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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