

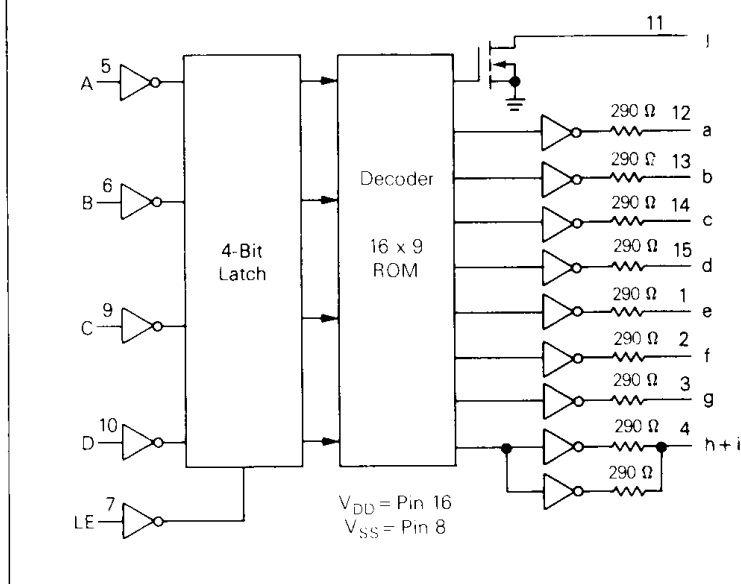
### HEXADECIMAL-TO-SEVEN SEGMENT LATCH/ DECODER LED DRIVER

The MC14495-1 is constructed with CMOS enhancement-mode devices and NPN bipolar output drivers in a monolithic structure. The circuit provides the functions of a 4-bit storage latch. The decoder is implemented utilizing a mask-programmable ROM. With a 5-volt power supply, it can be used without resistor interface to drive seven segment LEDs. The series output resistors of, typically, 290 ohms are internal to the device.

Applications include MPU systems display driver, instrument display driver, computer/calculator display driver, clockpit display driver, and various clock, watch, and timer uses.

- Low Logic-Circuit Power Dissipation
- High Current-Sourcing Outputs with Internal Limiting Resistors
- Latch Storage of Code
- Supply Voltage Range=4.5 to 18 V
- CMOS Input Switching Levels
- Standard ROM Provides Hex-to-Seven Segment Decoding
- Other ROM Options Available Upon Request (Contact your Motorola Sales Office)
- Chip Complexity: 187 FETs plus 9 NPNs or 49 Equivalent Gates

BLOCK DIAGRAM

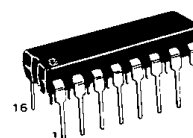


## MC14495-1

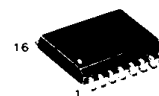
### CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

### HEXADECIMAL-TO-SEVEN SEGMENT LATCH/DECODER LED DRIVER



P SUFFIX  
PLASTIC DIP  
CASE 648

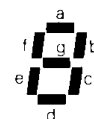
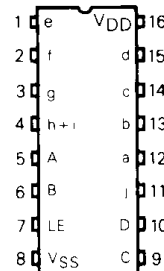


DW SUFFIX  
SOG  
CASE 751G

#### ORDERING INFORMATION

MC14495P1  
MC14495DW1

Plastic DIP  
SOG Package



ALPHANUMERIC DISPLAY

0 1 2 3 4 5 6 7 8 9 A B C D E F  
 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

TRUTH TABLE (LE = Low)

INPUTS				OUTPUTS										DISPLAY
D	C	B	A	a	b	c	d	e	f	g	h+i	:		
0	0	0	0	1	1	1	1	1	1	0	0	Open		0
0	0	0	1	0	1	1	0	0	0	0	0	Open		1
0	0	1	0	1	1	0	1	1	0	1	0	Open		2
0	0	1	1	1	1	1	0	0	1	0	0	Open		3
0	1	0	0	0	1	1	0	0	1	1	0	Open		4
0	1	0	1	1	0	1	1	0	1	1	0	Open		5
0	1	1	0	1	0	1	1	1	1	1	0	Open		6
0	1	1	1	1	1	1	0	0	0	0	0	Open		7
1	0	0	0	1	1	1	1	1	1	1	0	Open		8
1	0	0	1	1	1	1	0	1	0	1	0	Open		9
1	0	1	0	1	1	1	0	1	1	1	1	Open		A
1	0	1	1	0	0	1	1	1	1	1	1	Open		b
1	1	0	0	1	0	0	1	1	1	0	1	Open		C
1	1	0	1	0	1	1	1	0	1	1	1	Open		d
1	1	1	0	1	0	0	1	1	1	1	1	Open		E
1	1	1	1	1	0	0	0	1	1	1	1	0		F

MAXIMUM RATINGS (Voltages referenced to  $V_{SS}$ ).

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	-0.5 to +18	V
Input Voltage, All Inputs	$V_{in}$	-0.5 to $V_{DD} + 0.5$	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	$T_A$	-40 to +85	°C
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Maximum Continuous Output Power (Source) per Output @ 25°C Pins 1, 2, 3, 12, 13, 14, 15 Pin 4	$P_{OHmax}^\dagger$	50 100	mW

$^\dagger P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that  $V_{in}$  and  $V_{out}$  be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

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ELECTRICAL CHARACTERISTICS (Voltages referenced to  $V_{SS}$ )

Characteristic	Symbol	V <sub>DD</sub> V	- 40°C		25°C			85°C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Input Voltage "0" Level (V <sub>O</sub> = 3.8 or 0.5 V) (V <sub>O</sub> = 8.8 or 1.0 V) (V <sub>O</sub> = 13.8 or 1.5 V)	V <sub>IL</sub>	5 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.00	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V		
Input Voltage "1" Level (V <sub>O</sub> = 0.5 or 3.8 V) (V <sub>O</sub> = 1.0 or 8.8 V) (V <sub>O</sub> = 1.5 or 13.8 V)	V <sub>IH</sub>	5 10 15	3.5 7.0 11.0	— — —	3.5 7.0 11.0	2.75 5.50 8.25	— — —	3.5 7.0 11.0	— — —	V		
Output Voltage: a – g, h + i V <sub>in</sub> = V <sub>DD</sub> or 0, I <sub>out</sub> = 0 μA	V <sub>OL</sub>	5 10 15	— — —	0.1 0.1 0.1	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V		
Output Drive Voltage: a – g, h + i (I <sub>OH</sub> = 0 mA) (I <sub>OH</sub> = 5 mA) (I <sub>OH</sub> = 10 mA)	V <sub>OH</sub>	5	4.0 2.45 1.3	— — —	4.0 2.4 0.8	4.8 3.0 1.7	— — —	4.0 2.05 —	— — —	V		
(I <sub>OH</sub> = 0 mA) (I <sub>OH</sub> = 5 mA) (I <sub>OH</sub> = 10 mA)			10	9.0 7.4 6.4	— — —	9.0 7.2 5.8	9.8 8.0 6.7	— — —	9.0 6.9 5.0	— — —	V	
(I <sub>OH</sub> = 15 mA)				15	5.3	—	4.4	5.3	—	3.05	—	
(I <sub>OH</sub> = 0 mA) (I <sub>OH</sub> = 5 mA) (I <sub>OH</sub> = 10 mA)		14.0 12.2 10.9			— — —	14.0 12.0 10.4	14.8 13.0 11.7	— — —	14.0 11.7 9.6	— — —	V	
(I <sub>OH</sub> = 15 mA) (I <sub>OH</sub> = 20 mA) (I <sub>OH</sub> = 25 mA)		9.7 8.5 7.4	— — —		8.8 7.2 5.6	10.3 8.8 7.1	— — —	7.45 5.25 3.0	— — —			
Output Sink Current: j (V <sub>OL</sub> = 0.4 V) (V <sub>OL</sub> = 0.5 V) (V <sub>OL</sub> = 1.5 V)	I <sub>OL</sub>	5 10 15	— — —	— — —	0.3 — 0.5	1.00 — 1.25	— — —	— — —	— — —	mA		
Input Current (L Device)	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μA		
Input Current (P Device)	I <sub>in</sub>	15	—	± 0.3	—	± 0.00001	± 0.3	—	± 1.0	μA		
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF		
Quiescent Current V <sub>in</sub> = 0 or V <sub>DD</sub> , I <sub>out</sub> = 0 μA (Per Package)	I <sub>DD</sub>	5 10 15	— — —	0.3 1.5 3.0	— — —	0.08 0.40 0.85	0.25 1.25 2.50	— — —	0.2 1.0 2.0	mA		
Total Supply Current***† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5 10 15	I <sub>T</sub> = (1.9 μA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (3.8 μA/kHz)f + I <sub>DD</sub> I <sub>T</sub> = (5.7 μA/kHz)f + I <sub>DD</sub>							μA		

†To calculate total supply current at loads other than 50 pF:  $I_T(C_L = I_T(50 \text{ pF}) + 3.5 \times 10^{-3}(C_L - 50) V_{DD}f$   
where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V_{DD}$  in V, and  $f$  in kHz is input frequency.

\*\*The formulas given are for the typical characteristics only at 25°C.

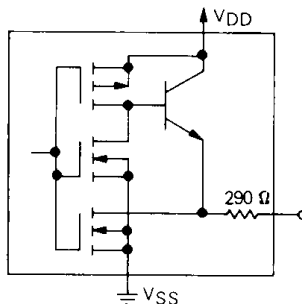
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ V	Min	Typ <sup>#</sup>	Max	Unit
Output Rise Time, a–g, h+i Outputs (Figure 1)	$t_{TLH}$	5 10 15	— — —	210 145 90	450 300 200	ns
Output Fall Time, a–g, h+i Outputs (Figure 1)	$t_{THL}$	5 10 15	— — —	1.5 1.3 1.1	3.5 2.75 2.25	$\mu\text{s}$
Output Fall Time, j Output (Figures 3 and 4)	$t_{THL}$	5 10 15	— — —	105 40 30	250 100 75	ns
Propagation Delay Time, A, B, C, D to a–g, h+i Outputs (Figure 2)	$t_{PLH}$	5 10 15	— — —	935 340 230	2400 900 500	ns
	$t_{PHL}$	5 10 15	— — —	7.0 3.5 2.0	18.0 9.0 5.0	$\mu\text{s}$
Propagation Delay Time, A, B, C, D to j Output (Figures 3 and 4)	$t_{PLZ}$	5 10 15	— — —	11.0 8.0 4.0	25.0 20.0 10.0	$\mu\text{s}$
	$t_{PZL}$	5 10 15	— — —	800 400 200	1500 1000 500	ns
Propagation Delay Time, LE to a–g, h+i Outputs (Figure 5)	$t_{PLH}$	5 10 15	— — —	1300 500 350	3000 1500 1000	ns
	$t_{PHL}$	5 10 15	— — —	16.0 6.0 5.0	30.0 15.0 10.0	$\mu\text{s}$
Propagation Delay Time, LE to j Output (Figures 4 and 6)	$t_{PLZ}$	5 10 15	— — —	14.0 8.0 6.0	30 20 15	$\mu\text{s}$
	$t_{PZL}$	5 10 15	— — —	10.0 5.0 4.0	25 15 10	$\mu\text{s}$
Setup Time, A, B, C, D to LE (Figure 7)	$t_{su}$	5 10 15	100 65 65	35 25 25	— — —	ns
Hold Time, LE to A, B, C, D (Figure 7)	$t_h$	5 10 15	125 75 75	45 30 25	— — —	ns
Latch Enable Pulse Width, LE (Figure 7)	$t_w$	5 10 15	525 200 140	210 80 55	— — —	ns

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OUTPUT CIRCUIT  
(Except Pin 11)



## INPUT/OUTPUT FUNCTIONS

**SEGMENT DRIVER (a, b, c, d, e, f, g, h + i; PINS 12, 13, 14, 15, 1, 2, 3, 4)**

The segment drivers are emitter-follower NPN transistors. To limit the output current, a resistor, typically 290 ohms, is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of  $V_{DD} = 5.0$  volts.

**OUTPUT (j; PIN 11)**

This open-drain output is activated (goes low) whenever inputs A, B, C, and D are all set to a logic one. Otherwise the output is in the high-impedance state. See the truth table.

**INPUT DATA (A, B, C, D; PINS 5, 6, 9, 10)**

The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by the Latch Enable input.

**LATCH ENABLE (LE; PIN 7)**

The data on inputs A, B, C and D will pass through the latch and will be decoded immediately when LE is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when LE = low and will be latched with the rising edge of LE. The data will remain stored as long as LE is high.

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## SWITCHING WAVEFORMS

Figure 1

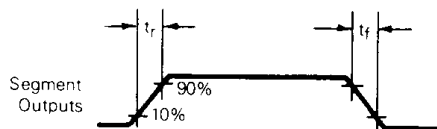


Figure 3

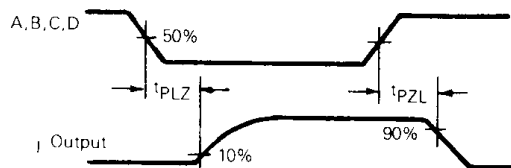


Figure 4

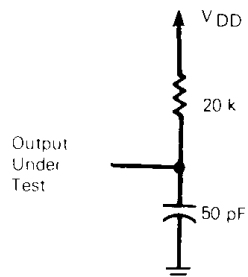


Figure 2

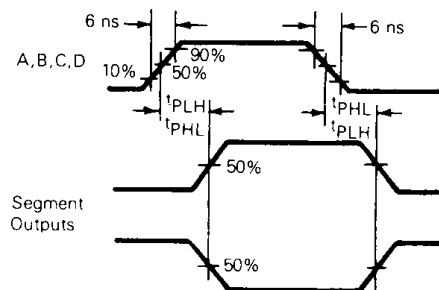
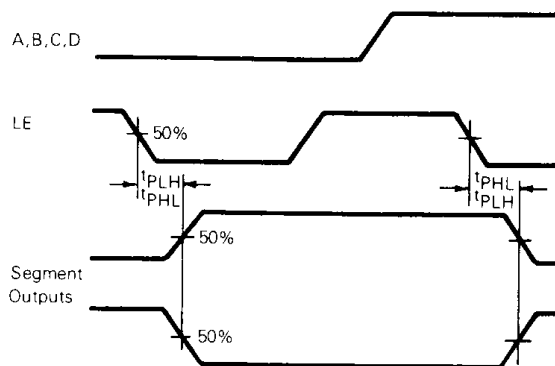


Figure 5



SWITCHING WAVEFORMS

Figure 6

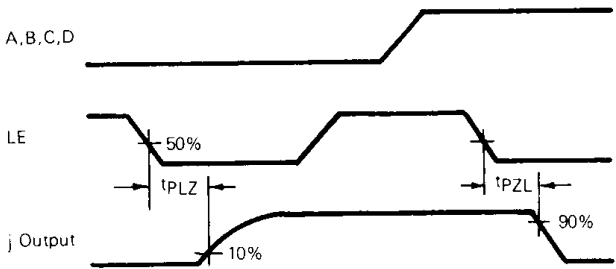
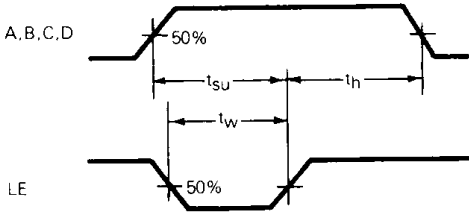


Figure 7



TYPICAL CIRCUIT @  $V_{DD} = 5.0\text{ V}$

