

## Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

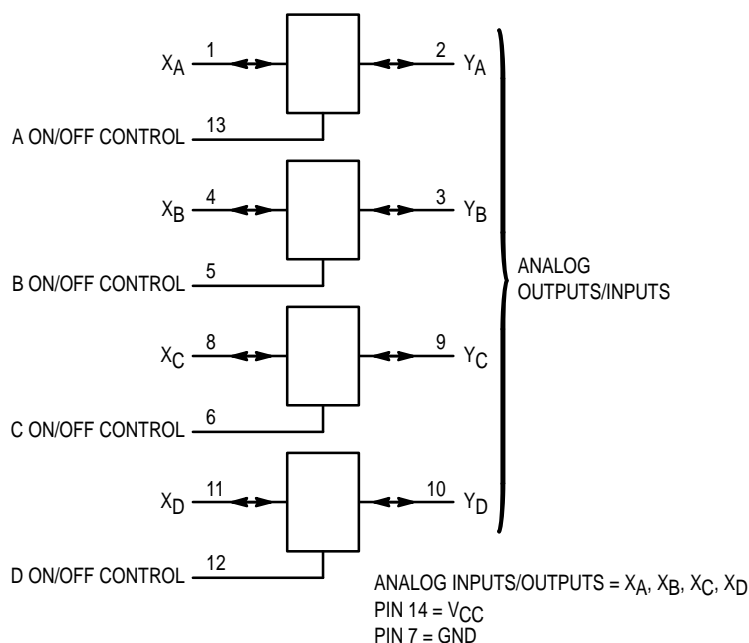
The MC54/74HC4066 utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

The HC4066 is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so that the ON resistances ( $R_{ON}$ ) are much more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

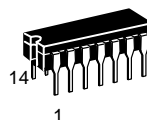
This device is identical in both function and pinout to the HC4016. The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066 or HC4016
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

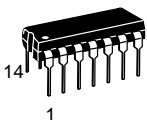
### LOGIC DIAGRAM



## MC54/74HC4066



**J SUFFIX**  
CERAMIC PACKAGE  
CASE 632-08



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



**D SUFFIX**  
SOIC PACKAGE  
CASE 751A-03



**DT SUFFIX**  
TSSOP PACKAGE  
CASE 948G-01

### ORDERING INFORMATION

MC54HCXXXXJ	Ceramic
MC74HCXXXXN	Plastic
MC74HCXXXXD	SOIC
MC74HCXXXXDT	TSSOP

### PIN ASSIGNMENT

$X_A$	1	14	$V_{CC}$
$Y_A$	2	13	A ON/OFF CONTROL
$Y_B$	3	12	D ON/OFF CONTROL
$X_B$	4	11	$X_D$
B ON/OFF CONTROL	5	10	$Y_D$
C ON/OFF CONTROL	6	9	$Y_C$
GND	7	8	$X_C$

### FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND)	– 0.5 to + 14.0	V
$V_{IS}$	Analog Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
$V_{in}$	Digital Input Voltage (Referenced to GND)	– 1.5 to $V_{CC} + 1.5$	V
$I$	DC Current Into or Out of Any Pin	$\pm 25$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
$T_{stg}$	Storage Temperature	– 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) (Ceramic DIP)	260 300	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C  
Ceramic DIP: – 10 mW/°C from 100° to 125°C  
SOIC Package: – 7 mW/°C from 65° to 125°C  
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage (Referenced to GND)	2.0	12.0	V
$V_{IS}$	Analog Input Voltage (Referenced to GND)	GND	$V_{CC}$	V
$V_{in}$	Digital Input Voltage (Referenced to GND)	GND	$V_{CC}$	V
$V_{IO}^*$	Static or Dynamic Voltage Across Switch	—	1.2	V
$T_A$	Operating Temperature, All Package Types	– 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10) $V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 9.0 \text{ V}$ $V_{CC} = 12.0 \text{ V}$	0 0 0 0	1000 500 400 250	ns

\* For voltage drops across the switch greater than 1.2 V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

**DC ELECTRICAL CHARACTERISTIC** Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
$V_{IH}$	Minimum High-Level Voltage ON/OFF Control Inputs	$R_{on} = \text{Per Spec}$	2.0 4.5 9.0 12.0	1.5 3.15 6.3 8.4	1.5 3.15 6.3 8.4	1.5 3.15 6.3 8.4	V
$V_{IL}$	Maximum Low-Level Voltage ON/OFF Control Inputs	$R_{on} = \text{Per Spec}$	2.0 4.5 9.0 12.0	0.3 0.9 1.8 2.4	0.3 0.9 1.8 2.4	0.3 0.9 1.8 2.4	V
$I_{in}$	Maximum Input Leakage Current ON/OFF Control Inputs	$V_{in} = V_{CC} \text{ or } GND$	12.0	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	μA
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $V_{IO} = 0 \text{ V}$	6.0 12.0	2 8	20 80	40 160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**DC ELECTRICAL CHARACTERISTICS** Analog Section (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
R <sub>on</sub>	Maximum “ON” Resistance	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> to GND I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0† 4.5 9.0 12.0	— 170 85 85	— 215 106 106	— 255 130 130	Ω
		V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Endpoints) I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)	2.0 4.5 9.0 12.0	— 85 63 63	— 106 78 78	— 130 95 95	
ΔR <sub>on</sub>	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = 1/2 (V <sub>CC</sub> – GND) I <sub>S</sub> ≤ 2.0 mA	2.0 4.5 9.0 12.0	— 30 20 20	— 35 25 25	— 40 30 30	Ω
I <sub>off</sub>	Maximum Off–Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IL</sub> V <sub>IO</sub> = V <sub>CC</sub> or GND Switch Off (Figure 3)	12.0	0.1	0.5	1.0	μA
I <sub>on</sub>	Maximum On–Channel Leakage Current, Any One Channel	V <sub>in</sub> = V <sub>IH</sub> V <sub>IS</sub> = V <sub>CC</sub> or GND (Figure 4)	12.0	0.1	0.5	1.0	μA

†At supply voltage (V<sub>CC</sub> – GND) approaching 2 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0	50	65	75	ns
		4.5	10	13	15	
		9.0	10	13	15	
		12.0	10	13	15	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11)	2.0	150	190	225	ns
		4.5	30	38	45	
		9.0	30	30	30	
		12.0	30	30	30	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 1 1)	2.0	125	160	185	ns
		4.5	25	32	37	
		9.0	25	32	37	
		12.0	25	32	37	
C	Maximum Capacitance	ON/OFF Control Input	—	10	10	pF
		Control Input = GND	—	35	35	
		Analog I/O Feedthrough	—	1.0	1.0	

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Switch) (Figure 13)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		15	

\* Used to determine the no–load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

**ADDITIONAL APPLICATION CHARACTERISTICS** (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Limit* 25°C 54/74HC	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f <sub>in</sub> = 1 MHz Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub> Increase f <sub>in</sub> Frequency Until dB Meter Reads – 3 dB R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0	150 160 160	MHz
—	Off-Channel Feedthrough Isolation (Figure 6)	f <sub>in</sub> ≡ Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0  4.5 9.0 12.0	– 50 – 50 – 50  – 40 – 40 – 40	dB
—	Feedthrough Noise, Control to Switch (Figure 7)	V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns) Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF	4.5 9.0 12.0  4.5 9.0 12.0	60 130 200  30 65 100	mV <sub>PP</sub>
—	Crosstalk Between Any Two Switches (Figure 12)	f <sub>in</sub> ≡ Sine Wave Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub> f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF	4.5 9.0 12.0  4.5 9.0 12.0	– 70 – 70 – 70  – 80 – 80 – 80	dB
THD	Total Harmonic Distortion (Figure 14)	f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF THD = THD <sub>Measured</sub> – THD <sub>Source</sub> V <sub>IS</sub> = 4.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 8.0 V <sub>PP</sub> sine wave V <sub>IS</sub> = 11.0 V <sub>PP</sub> sine wave	4.5 9.0 12.0	0.10 0.06 0.04	%

\* Guaranteed limits not tested. Determined by design and verified by qualification.

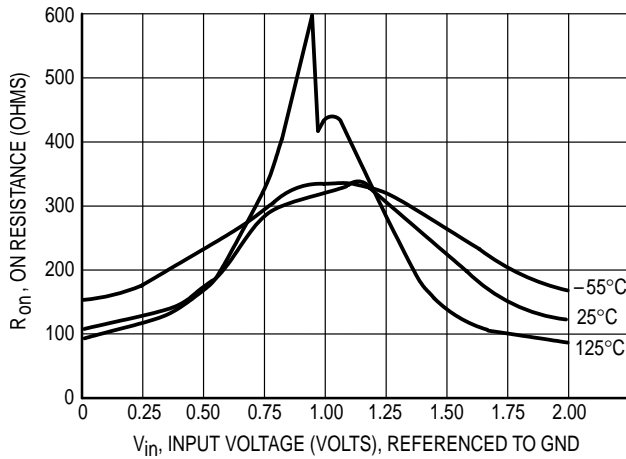
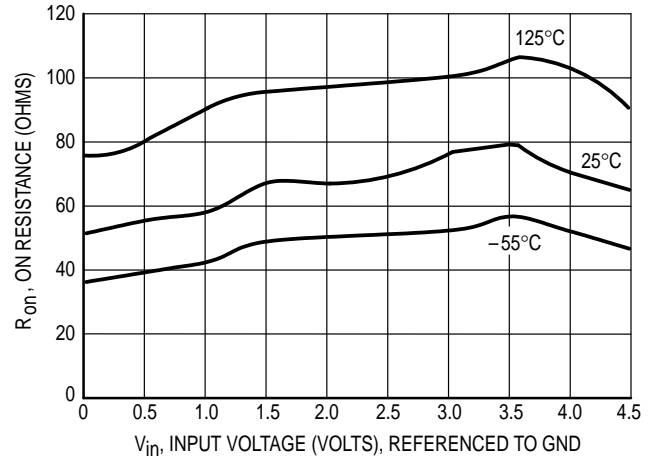
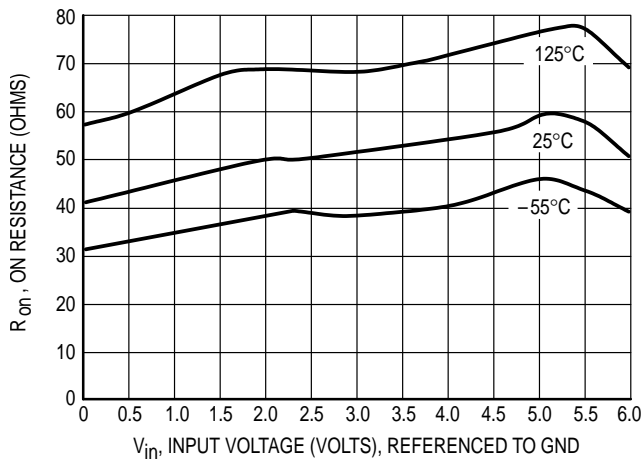
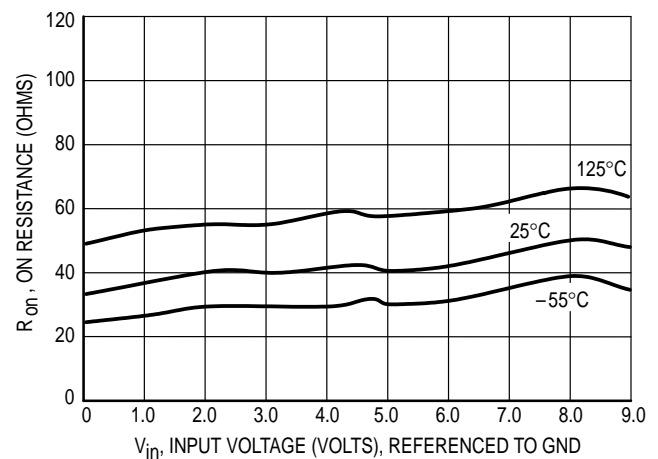
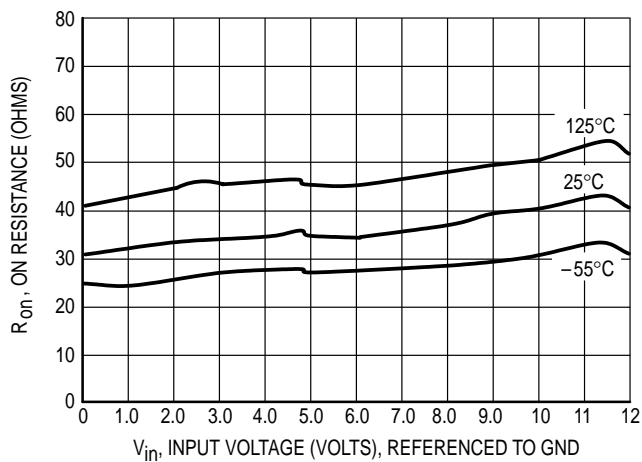
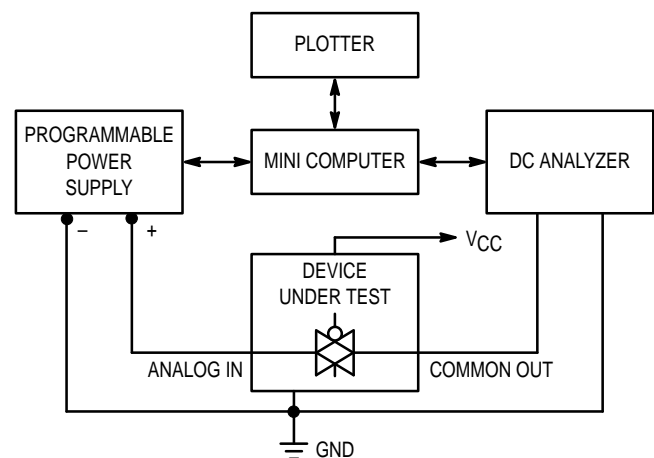
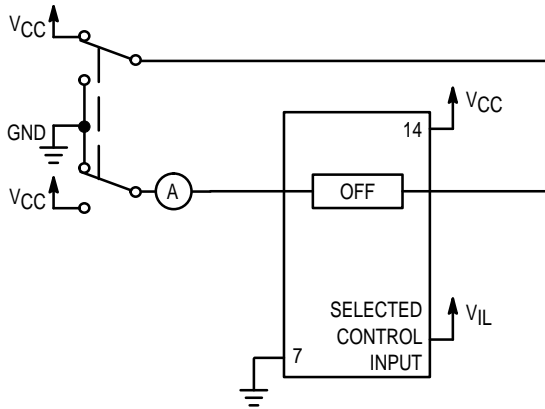
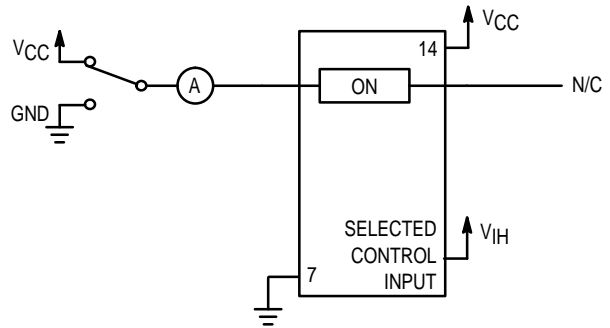
Figure 1a. Typical On Resistance,  $V_{CC} = 2.0 \text{ V}$ Figure 1b. Typical On Resistance,  $V_{CC} = 4.5 \text{ V}$ Figure 1c. Typical On Resistance,  $V_{CC} = 6.0 \text{ V}$ Figure 1d. Typical On Resistance,  $V_{CC} = 9.0 \text{ V}$ Figure 1e. Typical On Resistance,  $V_{CC} = 12 \text{ V}$ 

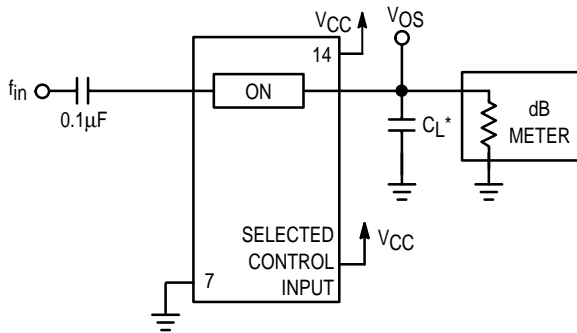
Figure 2. On Resistance Test Set-Up



**Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up**

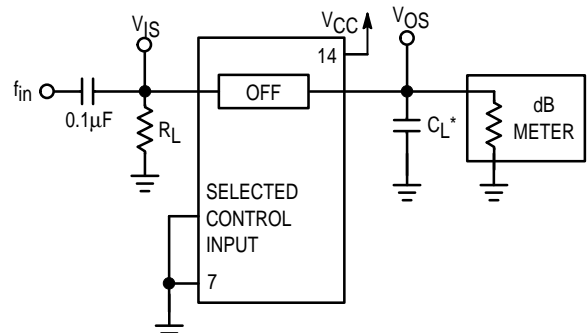


**Figure 4. Maximum On Channel Leakage Current, Test Set-Up**



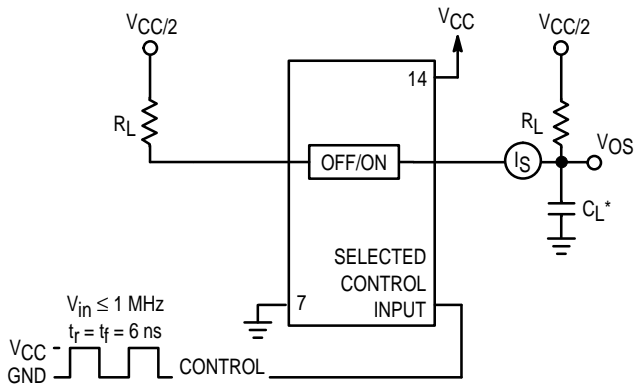
\*Includes all probe and jig capacitance.

**Figure 5. Maximum On-Channel Bandwidth Test Set-Up**



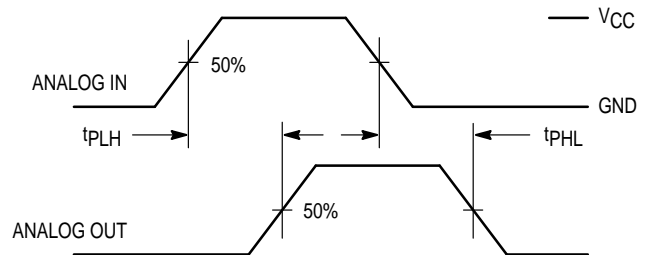
\*Includes all probe and jig capacitance.

**Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up**

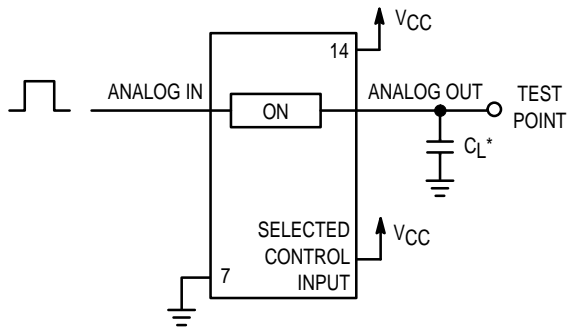


\*Includes all probe and jig capacitance.

**Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up**

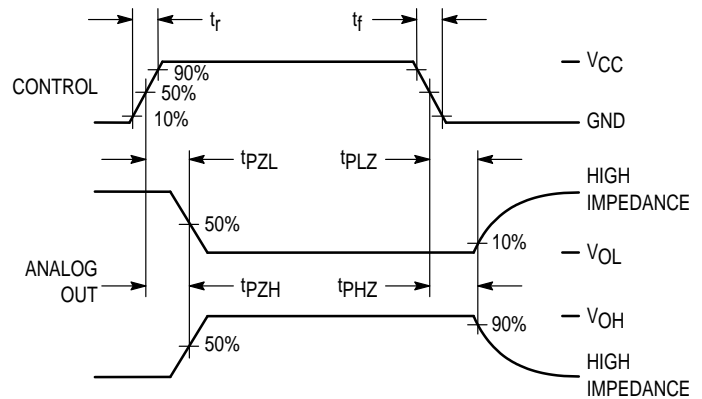


**Figure 8. Propagation Delays, Analog In to Analog Out**

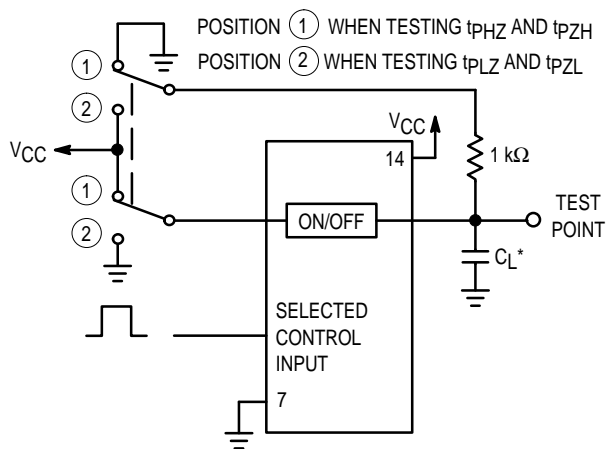


\*Includes all probe and jig capacitance.

**Figure 9. Propagation Delay Test Set-Up**

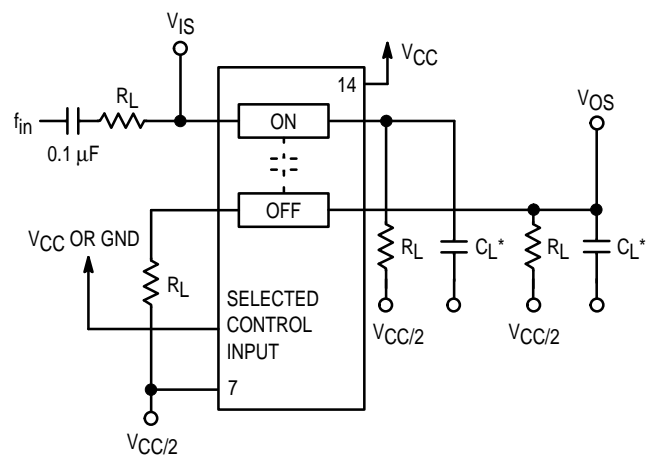


**Figure 10. Propagation Delay, ON/OFF Control to Analog Out**



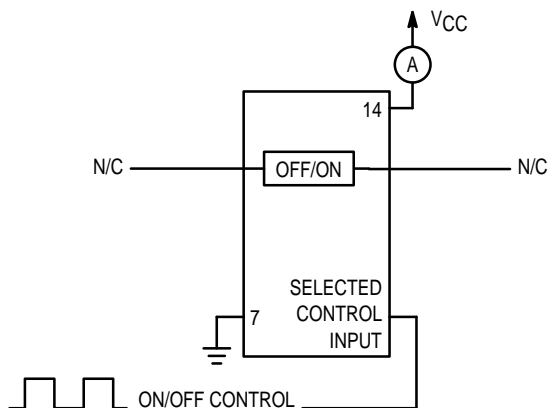
\*Includes all probe and jig capacitance.

**Figure 11. Propagation Delay Test Set-Up**

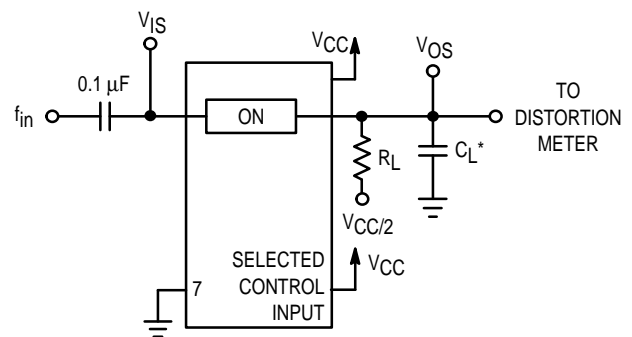


\*Includes all probe and jig capacitance.

**Figure 12. Crosstalk Between Any Two Switches, Test Set-Up**



**Figure 13. Power Dissipation Capacitance Test Set-Up**



\*Includes all probe and jig capacitance.

**Figure 14. Total Harmonic Distortion, Test Set-Up**

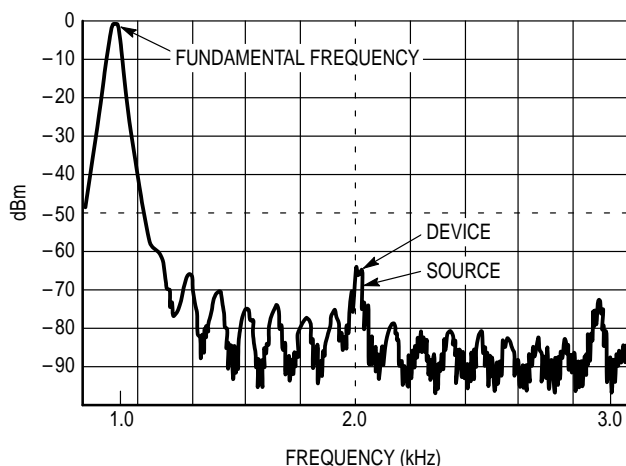


Figure 15. Plot, Harmonic Distortion

### APPLICATION INFORMATION

The ON/OFF Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In the example

below, the difference between  $V_{CC}$  and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below GND are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with MO•sorbs (Motorola high current surge protectors). MO•sorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

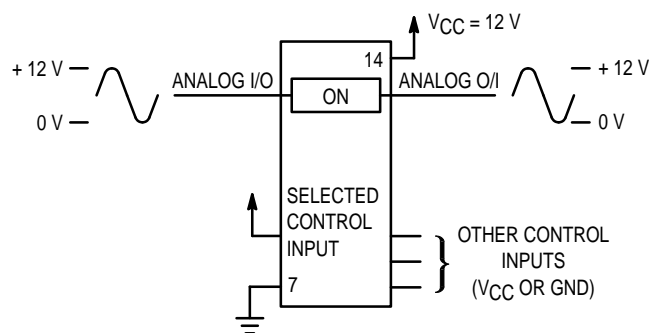


Figure 16. 12 V Application

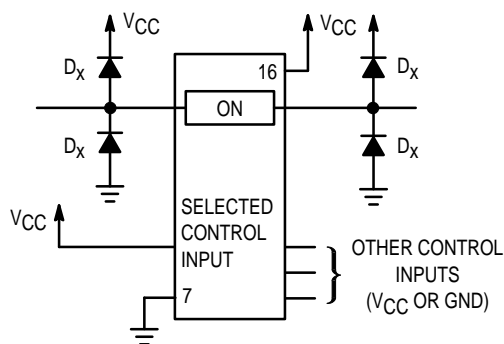


Figure 17. Transient Suppressor Application



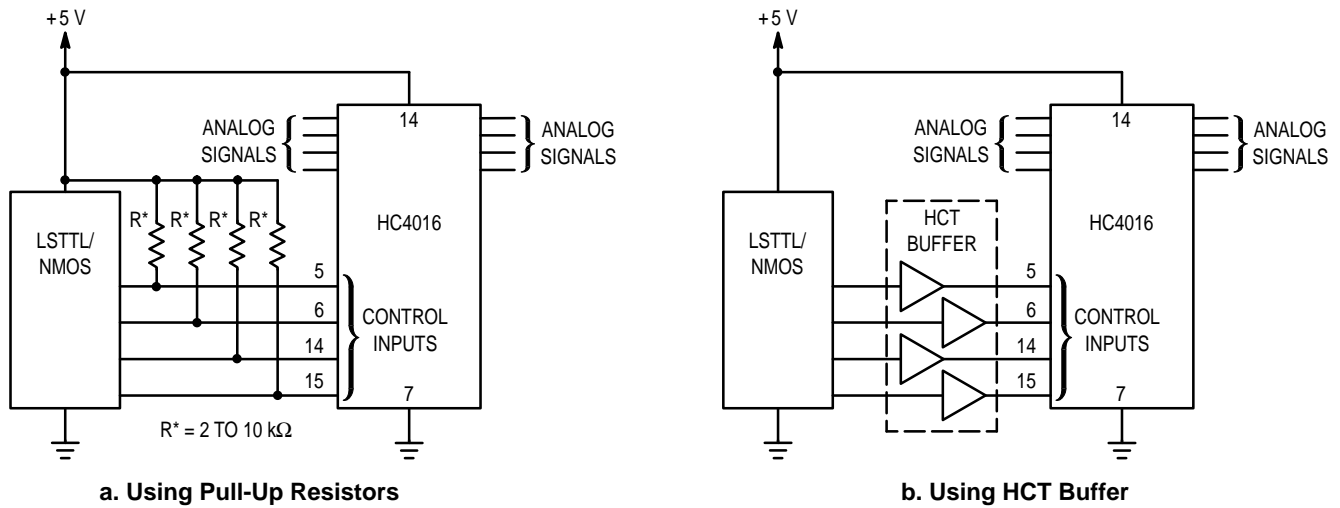


Figure 18. LSTTL/NMOS to HCMOS Interface

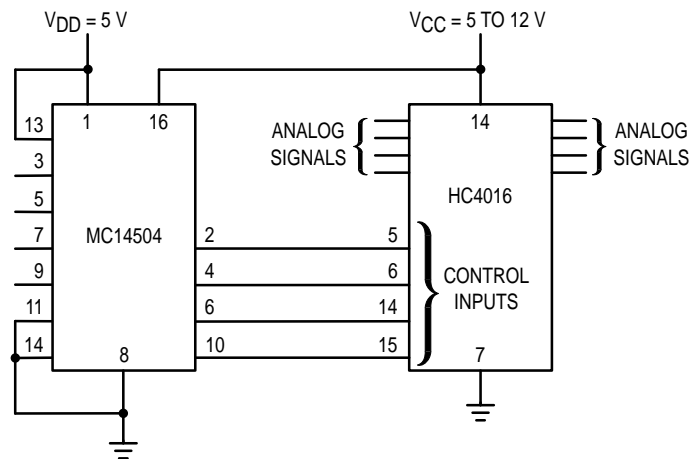
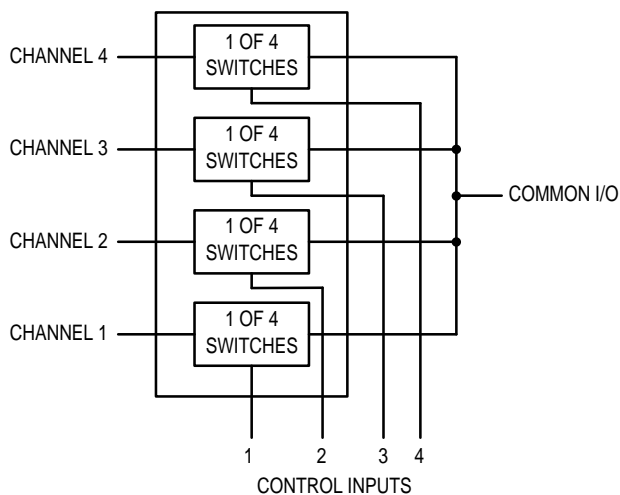
Figure 19. TTL/NMOS-to-CMOS Level Converter  
Analog Signal Peak-to-Peak Greater than 5 V  
(Also see HC4316)

Figure 20. 4-Input Multiplexer

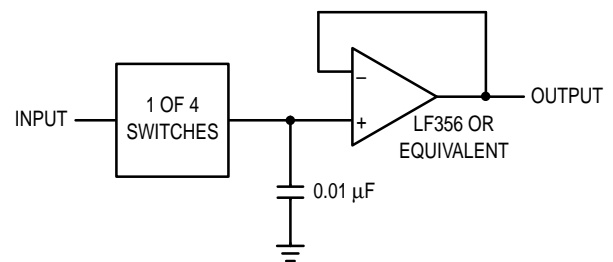
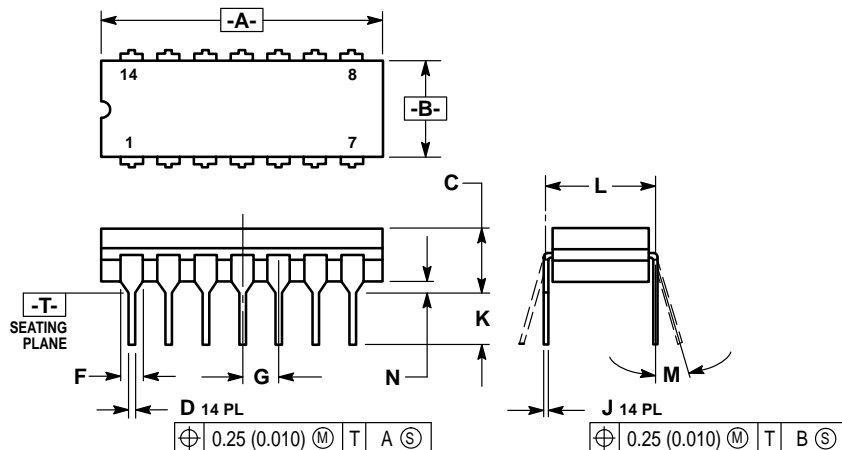


Figure 21. Sample/Hold Amplifier

## OUTLINE DIMENSIONS

**J SUFFIX**  
 CERAMIC DIP PACKAGE  
 CASE 632-08  
 ISSUE Y

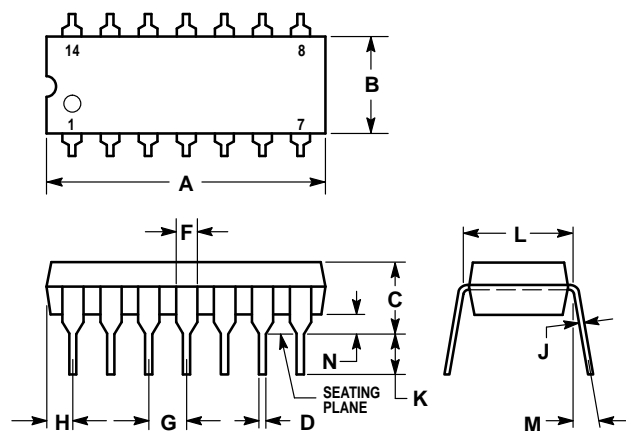


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**N SUFFIX**  
 PLASTIC DIP PACKAGE  
 CASE 646-06  
 ISSUE L



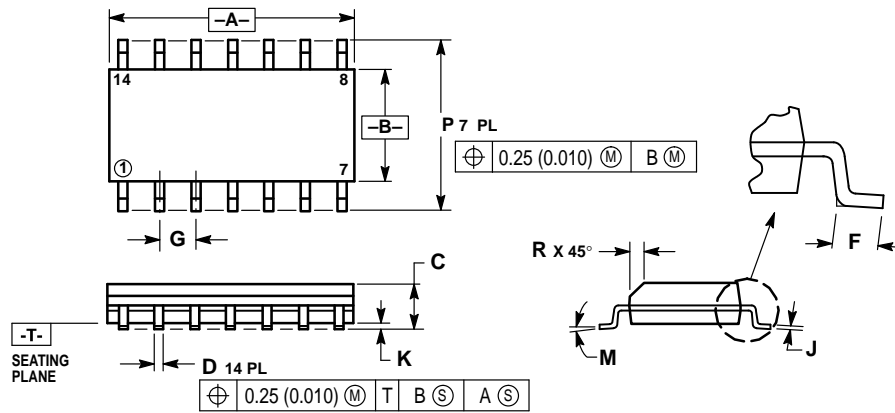
## NOTES:

1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

## OUTLINE DIMENSIONS

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751A-03**  
**ISSUE F**

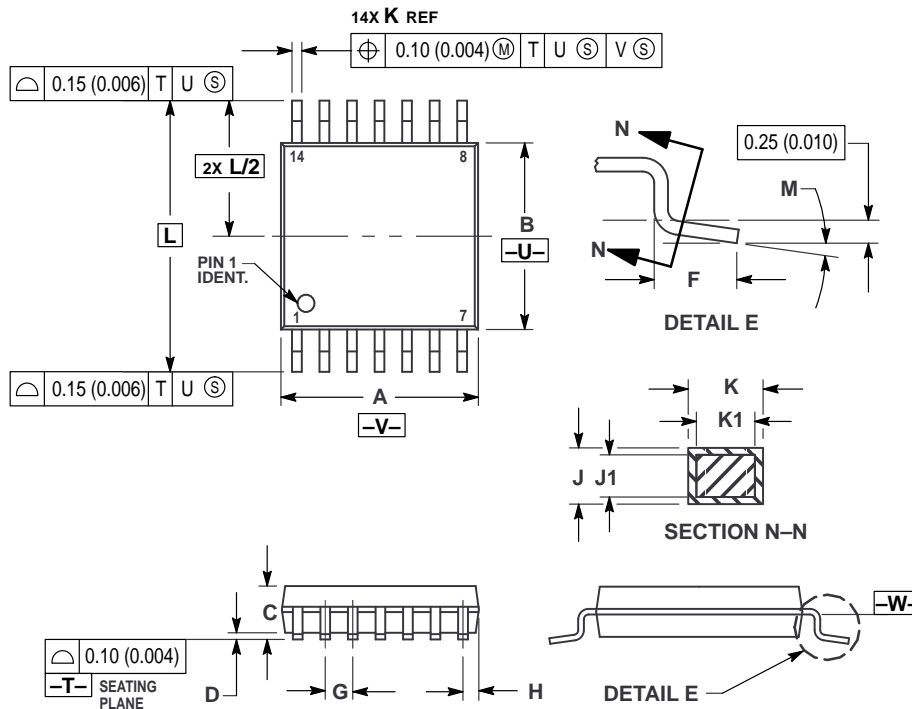


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019


**DT SUFFIX**  
**PLASTIC TSSOP PACKAGE**  
**CASE 948G-01**  
**ISSUE O**



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**How to reach us:**

**USA/EUROPE:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

**MFAX:** RMFAX0@email.sps.mot.com -TOUCHTONE (602) 244-6609  
**INTERNET:** <http://Design-NET.com>

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,  
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**HONG KONG:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

**MOTOROLA**

◇ CODELINE

**MC54/74HC4066/D**