

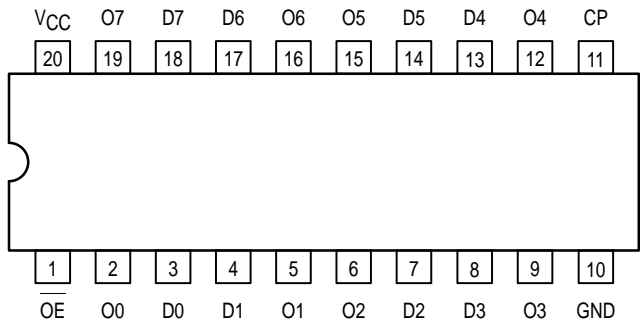
Low-Voltage CMOS  
Octal D-Type Flip-Flop  
With 5V-Tolerant Inputs and Outputs  
(3-State, Non-Inverting)

The MC74LCX374 is a high performance, non-inverting octal D-type flip-flop operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX374 inputs to be safely driven from 5V devices.

The MC74LCX374 consists of 8 edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable (OE) are common to all flip-flops. The eight flip-flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the OE LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. The OE input level does not affect the operation of the flip-flops.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 $\mu$ A)  
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

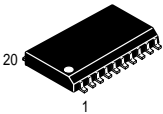
Pinout: 20-Lead (Top View)



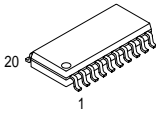
MC74LCX374

LCX

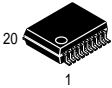
LOW-VOLTAGE CMOS  
OCTAL D-TYPE FLIP-FLOP



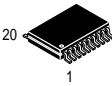
DW SUFFIX  
PLASTIC SOIC  
CASE 751D-04



M SUFFIX  
PLASTIC SOIC EIAJ  
CASE 967-01



SD SUFFIX  
PLASTIC SSOP  
CASE 940C-03

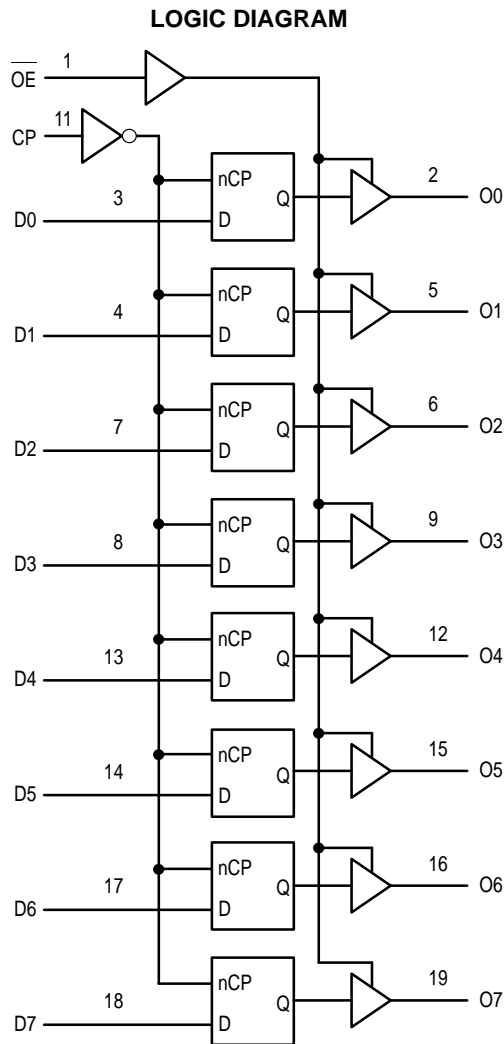


DT SUFFIX  
PLASTIC TSSOP  
CASE 948E-02

PIN NAMES

Pins	Function
OE	Output Enable Input
CP	Clock Pulse Input
D0-D7	Data Inputs
O0-O7	3-State Outputs





INPUTS			OUTPUTS	OPERATING MODE
OE	CP	Dn	On	
L L	↑ ↑	l h	L H	Load and Read Register
L	↑ ↓	X	NC	Hold and Read Register
H	↑ ↓	X	Z	Hold and Disable Outputs
H H	↑ ↑	l h	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; NC = No Change, State Prior to Low-to-High Clock Transition; X = High or Low Voltage Level and Transitions are Acceptable; Z = High Impedance State; ↑ = Low-to-High Transition; ↓ = Not a Low-to-High Transition; For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	$-0.5$ to $+7.0$		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3–State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1.	V
$I_{IK}$	DC Input Diode Current	$-50$	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	$-50$	$V_O < \text{GND}$	mA
		$+50$	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	$-65$ to $+150$		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

1. Output in HIGH or LOW State.  $I_O$  absolute maximum rating must be observed.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	2.0	3.3	3.6	V
	Operating Data Retention Only	1.5	3.3	3.6	V
$V_I$	Input Voltage	0		5.5	V
$V_O$	Output Voltage (HIGH or LOW State) (3–State)	0		$V_{CC}$	V
		0		5.5	V
$I_{OH}$	HIGH Level Output Current, $V_{CC} = 3.0\text{V} - 3.6\text{V}$			$-24$	mA
$I_{OL}$	LOW Level Output Current, $V_{CC} = 3.0\text{V} - 3.6\text{V}$			24	mA
$I_{OH}$	HIGH Level Output Current, $V_{CC} = 2.7\text{V} - 3.0\text{V}$			$-12$	mA
$I_{OL}$	LOW Level Output Current, $V_{CC} = 2.7\text{V} - 3.0\text{V}$			12	mA
$T_A$	Operating Free–Air Temperature	$-40$		$+85$	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8V to 2.0V, $V_{CC} = 3.0\text{V}$	0		10	ns/V

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		Unit
			Min	Max	
$V_{IH}$	HIGH Level Input Voltage (Note 2.)	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}$	2.0		V
$V_{IL}$	LOW Level Input Voltage (Note 2.)	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}$		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}$ ; $I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.7\text{V}$ ; $I_{OH} = -12\text{mA}$	2.2		
		$V_{CC} = 3.0\text{V}$ ; $I_{OH} = -18\text{mA}$	2.4		
		$V_{CC} = 3.0\text{V}$ ; $I_{OH} = -24\text{mA}$	2.2		
$V_{OL}$	LOW Level Output Voltage	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}$ ; $I_{OL} = 100\mu\text{A}$		0.2	V
		$V_{CC} = 2.7\text{V}$ ; $I_{OL} = 12\text{mA}$		0.4	
		$V_{CC} = 3.0\text{V}$ ; $I_{OL} = 16\text{mA}$		0.4	
		$V_{CC} = 3.0\text{V}$ ; $I_{OL} = 24\text{mA}$		0.55	

2. These values of  $V_I$  are used to test DC electrical characteristics only.

**DC ELECTRICAL CHARACTERISTICS** (continued)

Symbol	Characteristic	Condition	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		Unit
			Min	Max	
$I_I$	Input Leakage Current	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_I \leq 5.5\text{V}$		$\pm 5.0$	$\mu\text{A}$
$I_{OZ}$	3-State Output Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_O \leq 5.5\text{V}; V_I = V_{IH} \text{ or } V_{IL}$		$\pm 5.0$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$V_{CC} = 0\text{V}; V_I \text{ or } V_O = 5.5\text{V}$		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_I = \text{GND or } V_{CC}$		10	$\mu\text{A}$
		$2.7 \leq V_{CC} \leq 3.6\text{V}; 3.6 \leq V_I \text{ or } V_O \leq 5.5\text{V}$		$\pm 10$	$\mu\text{A}$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_{IH} = V_{CC} - 0.6\text{V}$		500	$\mu\text{A}$

**AC CHARACTERISTICS** ( $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits				Unit	
			T <sub>A</sub> = −40°C to +85°C					
			V <sub>CC</sub> = 3.0V to 3.6V		V <sub>CC</sub> = 2.7V			
			Min	Max	Min	Max		
f <sub>max</sub>	Clock Pulse Frequency	1	150					MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5		ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to HIGH and LOW Levels	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5		ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time from HIGH and LOW Levels	2	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5		ns
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	1	2.5		2.5			ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	1	1.5		1.5			ns
t <sub>w</sub>	CP Pulse Width, HIGH or LOW	3	3.3		3.3			ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 3.)			1.0 1.0				ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

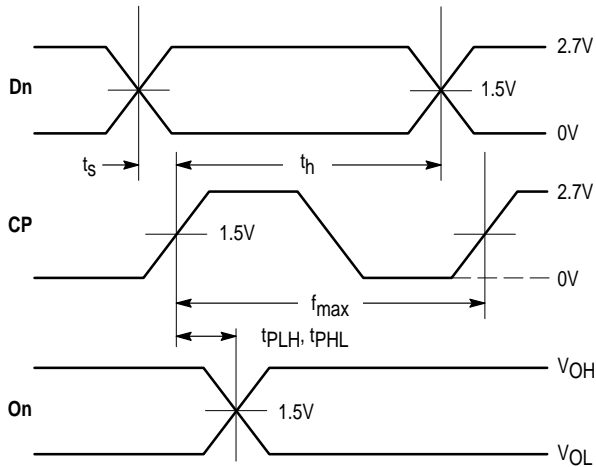
**DYNAMIC SWITCHING CHARACTERISTICS**

Symbol	Characteristic	Condition	$T_A = +25^{\circ}\text{C}$			Unit
			Min	Typ	Max	
$V_{OLP}$	Dynamic LOW Peak Voltage (Note 4.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V
$V_{OLV}$	Dynamic LOW Valley Voltage (Note 4.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V

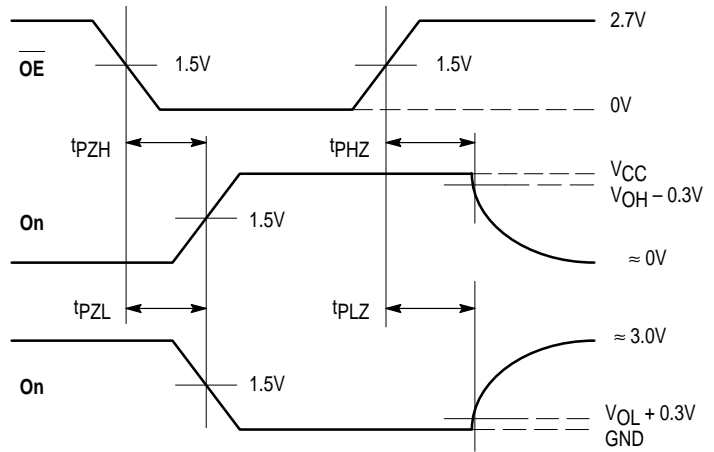
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

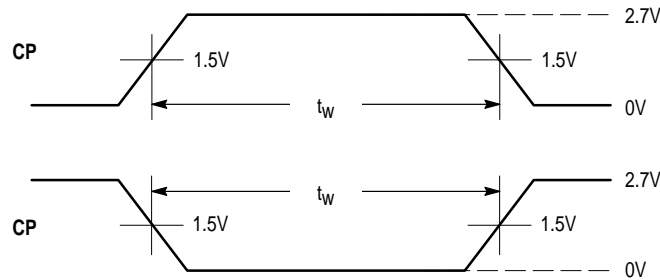
Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	25	pF



**WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

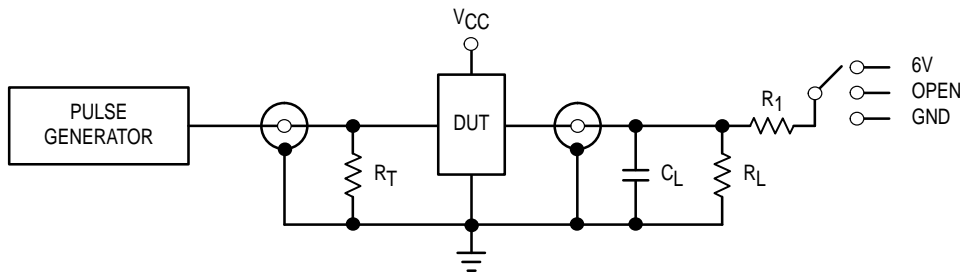


**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 3 – PULSE WIDTH**  
 $t_R = t_F = 2.5\text{ns}$  (or fast as required) from 10% to 90%;  
 Output requirements:  $V_{OL} \leq 0.8\text{V}$ ,  $V_{OH} \geq 2.0\text{V}$

**Figure 1. AC Waveforms**



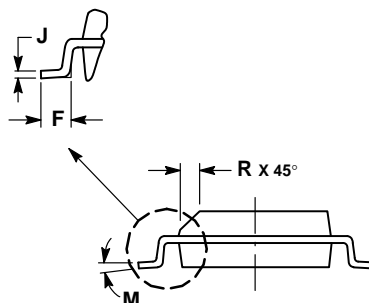
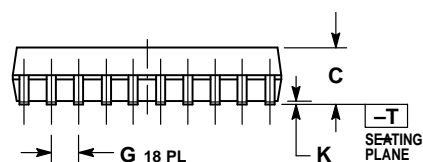
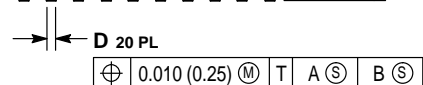
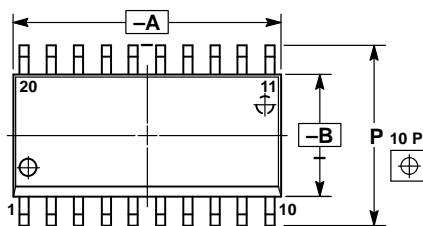
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 2. Test Circuit**

## OUTLINE DIMENSIONS

**DW SUFFIX**  
**PLASTIC SOIC PACKAGE**  
CASE 751D-04  
ISSUE E

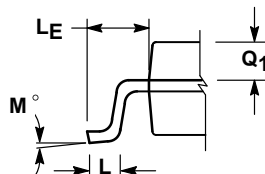
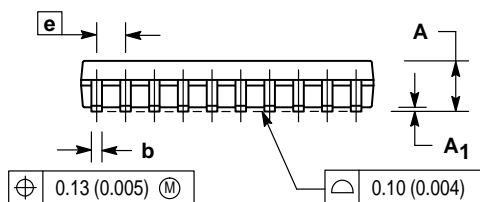
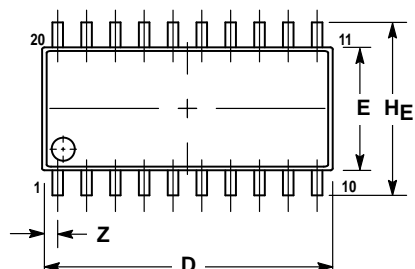


## NOTES:

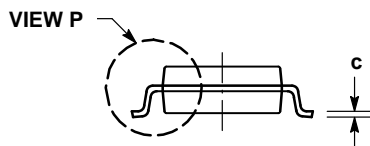
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

**M SUFFIX**  
**PLASTIC SOIC PACKAGE**  
CASE 967-01  
ISSUE O



DETAIL P



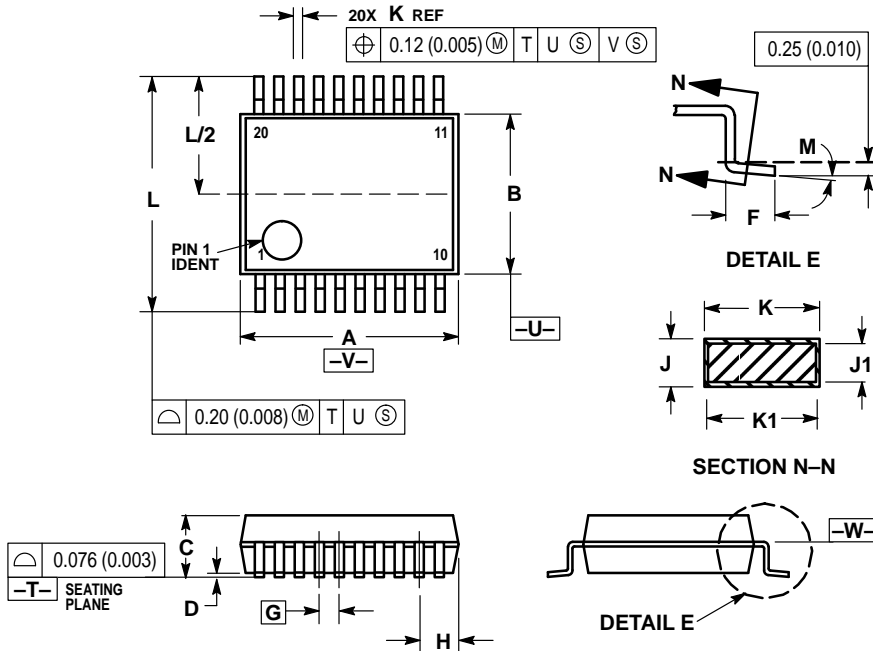
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

## OUTLINE DIMENSIONS

**SD SUFFIX**  
**PLASTIC SSOP PACKAGE**  
 CASE 940C-03  
 ISSUE B

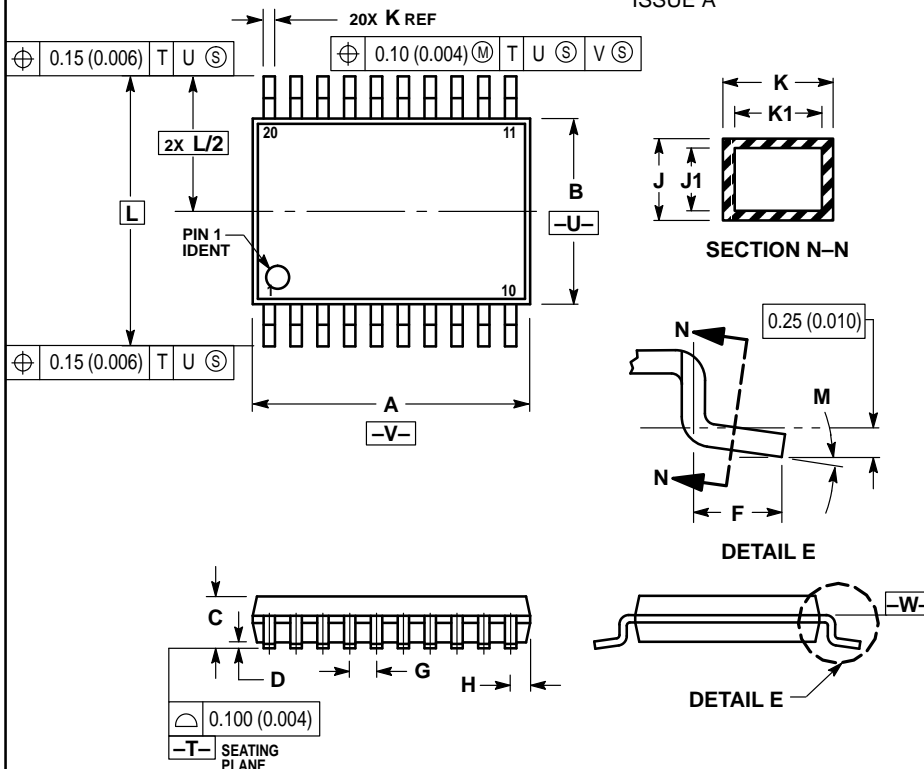


## NOTES:

- 13 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 14 CONTROLLING DIMENSION: MILLIMETER.
- 15 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 16 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 17 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
- 18 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 19 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°


**DT SUFFIX**  
**PLASTIC TSSOP PACKAGE**  
 CASE 948E-02  
 ISSUE A



## NOTES:

- 6 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 7 CONTROLLING DIMENSION: MILLIMETER.
- 8 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 9 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 10 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 11 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 12 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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