

## 256KB and 512KB BurstRAM™ Secondary Cache Module for PowerPC™ – Based Systems

The MPC2002SG and MPC2003SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the PowerPC 60x processors. The modules are configured as 32K x 72 and 64K x 72 bits in a 136 pin dual readout single inline memory module (DIMM). The module uses four of Motorola's MCM67M518 or MCM67M618 BiCMOS BurstRAMs.

Bursts can be initiated with either transfer start processor ( $\overline{TSP}$ ) or transfer start controller ( $\overline{TSC}$ ). Subsequent burst addresses are generated internal to the BurstRAM by the burst address advance ( $\overline{BAA}$ ) pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with the PowerPC 60x bus and requires external tag.

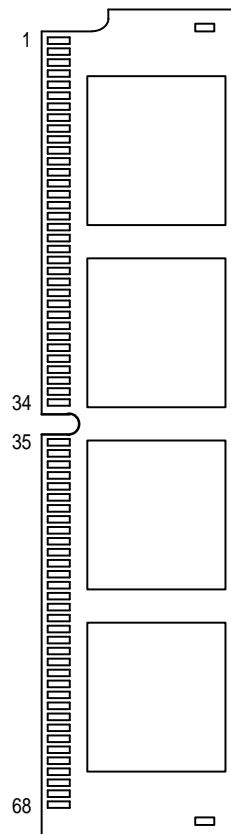
PD0 – PD2 are reserved for density and speed identification.

- PowerPC–style Burst Counter on Board
- Dual Readout SIMM for Circuit Density
- Single 5 V  $\pm$  5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz, 60 MHz, 50MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible

### MPC2002 MPC2003

(Formerly MCM72MS32/64)

136–LEAD DIMM  
CASE 1104–01  
TOP VIEW



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**PIN ASSIGNMENT**  
**136-LEAD DIMM**  
**CASE 1104-01**  
**TOP VIEW**

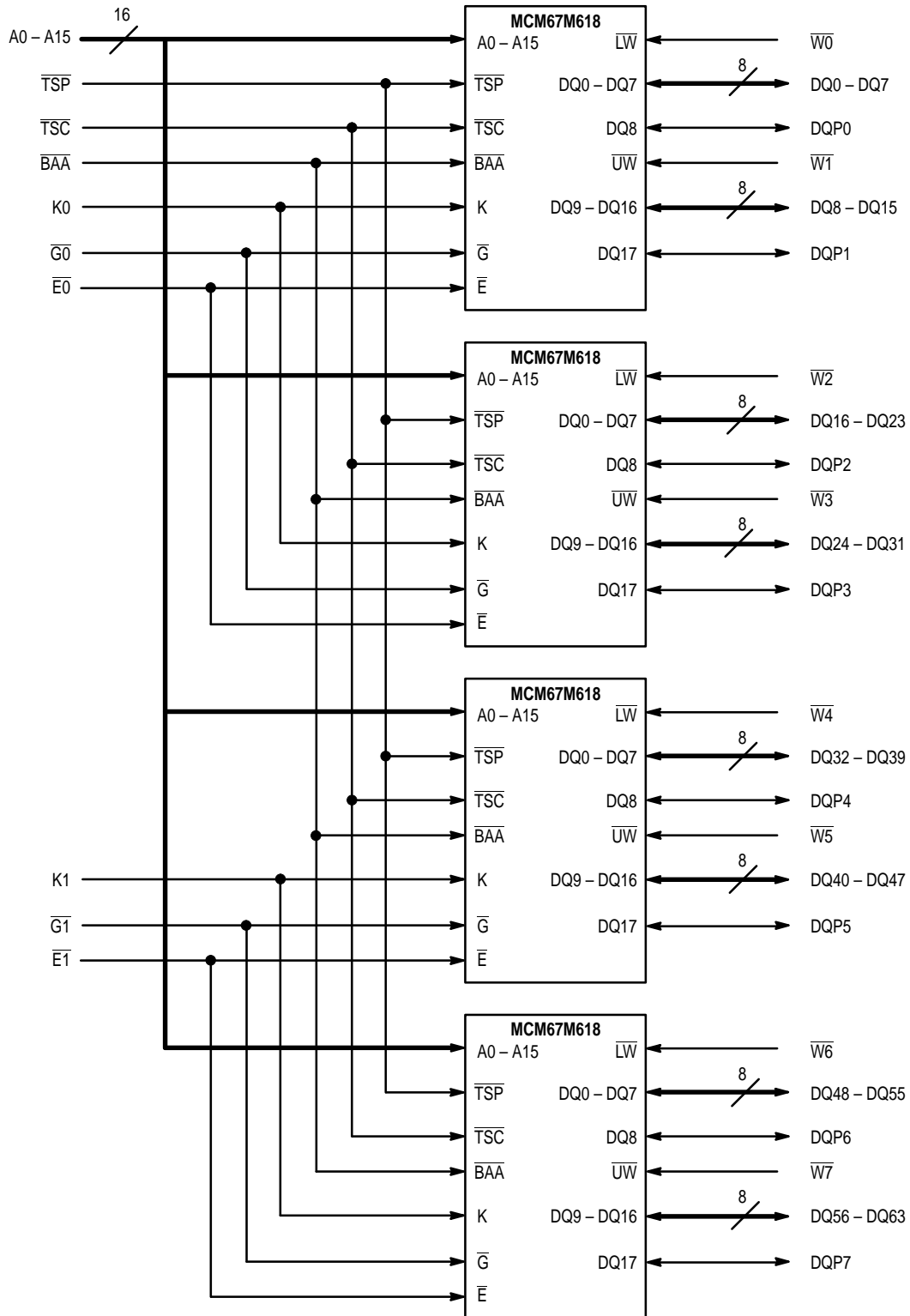
PD2	PD1	PD0	Cache Size	Module
V <sub>SS</sub>	NC	NC	512KB	MPC2003SG66/60
V <sub>SS</sub>	NC	V <sub>SS</sub>	512KB	MPC2003SG50
V <sub>SS</sub>	V <sub>SS</sub>	NC	256KB	MPC2002SG66/60
V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	256KB	MPC2002SG50

PIN NAMES	
A0 – A15	Address Inputs
K0, K1	Clock
$\overline{W0} - \overline{W7}$	Byte Write
$\overline{E0}, \overline{E1}$	Module Enable
$\overline{G0}, \overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{TSC}$	Transfer Start Controller
$\overline{TSP}$	Transfer Start Processor
$\overline{BAA}$	Burst Address Advance
PD0 – PD2	Presence Detect
V <sub>CC</sub>	+ 5 V Power Supply
V <sub>SS</sub>	Ground

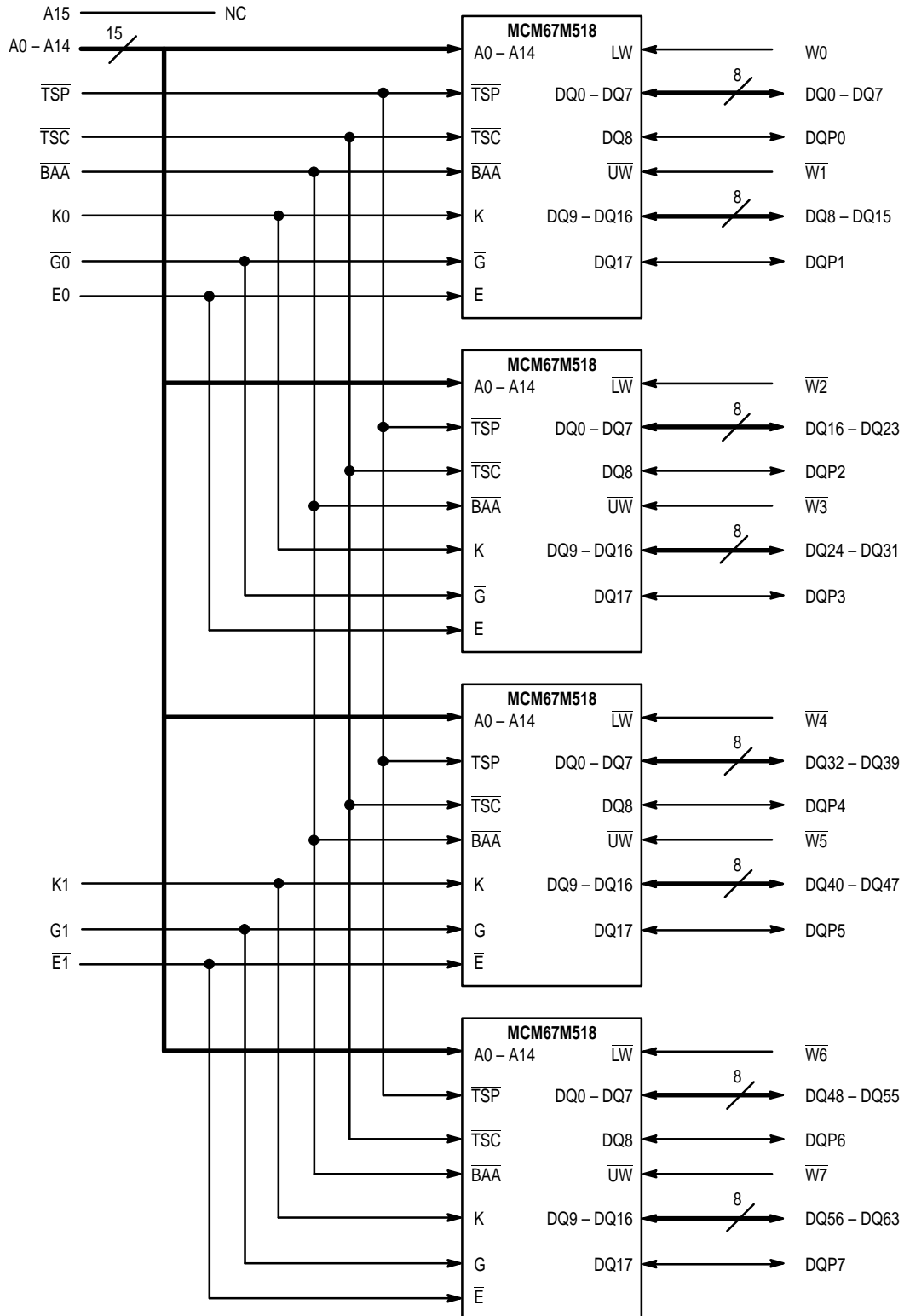
PD0	1	69	V <sub>SS</sub>
PD1	2	70	PD2
DQ0	3	71	V <sub>CC</sub>
DQ1	4	72	DQ2
V <sub>CC</sub>	5	73	DQ3
DQ4	6	74	DQ5
DQ6	7	75	DQ7
DQP0	8	76	V <sub>SS</sub>
DQ8	9	77	DQ9
DQ10	10	78	DQ11
V <sub>SS</sub>	11	79	DQ12
K0	12	80	V <sub>SS</sub>
V <sub>SS</sub>	13	81	DQ13
DQ14	14	82	DQ15
V <sub>CC</sub>	15	83	DQP1
DQ16	16	84	V <sub>SS</sub>
DQ17	17	85	DQ18
DQ19	18	86	DQ20
DQ21	19	87	DQ22
V <sub>CC</sub>	20	88	DQ23
DQP2	21	89	V <sub>SS</sub>
DQ24	22	90	DQ25
DQ26	23	91	DQ27
DQ28	24	92	DQ29
V <sub>SS</sub>	25	93	DQ30
DQ31	26	94	V <sub>SS</sub>
DQP3	27	95	$\overline{E0}$
V <sub>SS</sub>	28	96	$\overline{W1}$
$\overline{W0}$	29	97	$\overline{W3}$
$\overline{W2}$	30	98	$\overline{G0}$
$\overline{TSP}$	31	99	$\overline{TSC}$
$\overline{BAA}$	32	100	V <sub>SS</sub>
V <sub>CC</sub>	33	101	$\overline{G1}$
$\overline{W4}$	34	102	$\overline{W5}$
$\overline{W6}$	35	103	$\overline{W7}$
DQ32	36	104	$\overline{E1}$
DQ33	37	105	DQ34
V <sub>SS</sub>	38	106	DQ35
DQ36	39	107	DQ37
DQ38	40	108	V <sub>CC</sub>
DQ39	41	109	DQP4
DQ40	42	110	DQ41
V <sub>CC</sub>	43	111	DQ42
DQ43	44	112	DQ44
DQ45	45	113	V <sub>SS</sub>
DQ46	46	114	DQ47
DQP5	47	115	DQ48
V <sub>SS</sub>	48	116	DQ49
K1	49	117	V <sub>SS</sub>
V <sub>SS</sub>	50	118	DQ50
DQ52	51	119	DQ51
DQ53	52	120	DQ54
DQ55	53	121	DQ56
DQP6	54	122	V <sub>SS</sub>
V <sub>CC</sub>	55	123	DQ57
DQ58	56	124	DQ59
DQ60	57	125	DQ61
DQ62	58	126	DQ63
DQP7	59	127	V <sub>CC</sub>
A0	60	128	A1
A2	61	129	A3
A4	62	130	A5
A6	63	131	A7
A8	64	132	NC
A10	65	133	A9
A12	66	134	A11
A14	67	135	A13
V <sub>SS</sub>	68	136	A15*

\* This pin on the MPC2002 is a No Connect (NC)

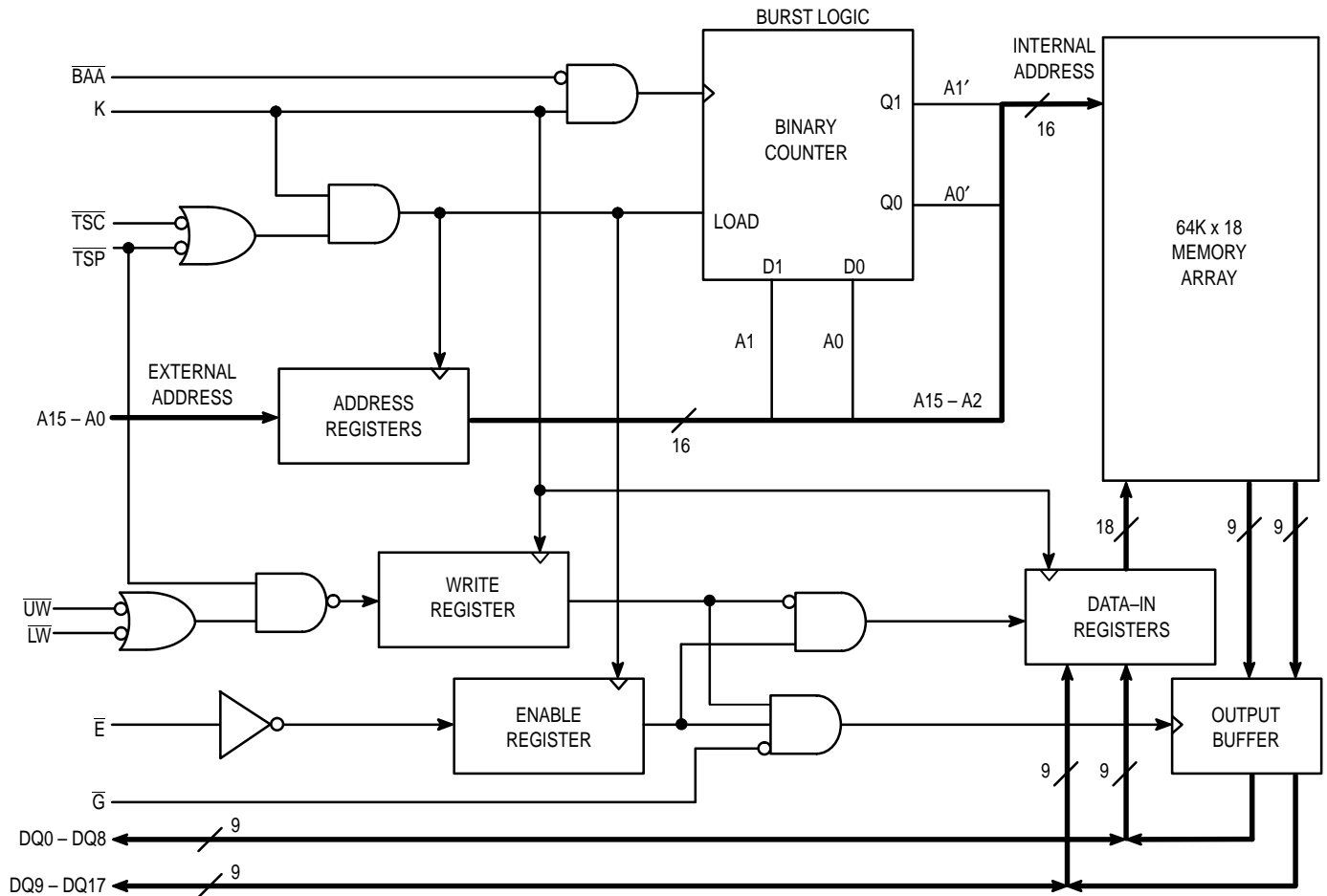
# MPC2003 (64K x 72) MODULE BLOCK DIAGRAM



# MPC2002 (32K x 72) MODULE BLOCK DIAGRAM

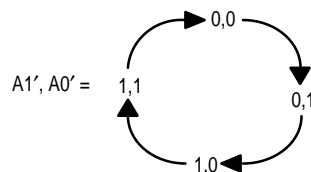


## BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The  $\overline{TSC}$  or  $\overline{TSP}$  signals control the duration of the burst and the start of the next burst. When  $\overline{TSP}$  is sampled low, any ongoing burst is interrupted and a read (independent of  $\overline{W}$  and  $\overline{TSC}$ ) is performed using the new external address. Alternatively, a  $\overline{TSP}$ -initiated two cycle WRITE can be performed by asserting  $\overline{TSP}$  and a valid address on the first cycle, then negating both  $\overline{TSP}$  and  $\overline{TSC}$  and asserting  $\overline{LW}$  and/or  $\overline{UW}$  with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram). When  $\overline{TSC}$  is sampled low (and  $\overline{TSP}$  is sampled high), any ongoing burst is interrupted and a read or write (dependent on  $\overline{W}$ ) is performed using the new external address. Chip enable ( $\overline{E}$ ) is sampled only when a new base address is loaded. After the first cycle of the burst,  $\overline{BAA}$  controls subsequent burst cycles. When  $\overline{BAA}$  is sampled low, the internal address is advanced prior to the operation. When  $\overline{BAA}$  is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**. Write refers to either or both byte write enables ( $\overline{LW}$ ,  $\overline{UW}$ ).

## BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

# **SYNCHRONOUS TRUTH TABLE** (See Notes 1, 2, and 3)

$\bar{E}$	TSP	TSC	BAA	LW or UW	K	Address	Operation
H	L	X	X	X	L-H	N/A	Deselected
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

## **NOTES:**

1. X means Don't Care.
2. All inputs except  $\bar{G}$  must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

# **ASYNCHRONOUS TRUTH TABLE** (See Notes 1 and 2)

Operation	$\bar{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Write	X	High-Z — Data In
Deselected	X	High-Z

## **NOTES:**

1. X means Don't Care.
2. For a write operation following a read operation,  $\bar{G}$  must be high before the input data required setup time and held high through the input data hold time.

# **ABSOLUTE MAXIMUM RATINGS** (Voltages Referenced to $V_{SS} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	- 0.5 to + 7.0	V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$	$V_{in}, V_{out}$	- 0.5 to $V_{CC} + 0.5$	V
Output Current (per I/O)	$I_{out}$	$\pm 30$	mA
Power Dissipation	$P_D$	6.0	W
Temperature Under Bias	$T_{bias}$	- 10 to + 85	°C
Operating Temperature	$T_A$	0 to +70	°C
Storage Temperature	$T_{stg}$	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 5\%$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.75	5.25	V
Input High Voltage	$V_{IH}$	2.2	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	$V_{IL}$	$-0.5^*$	0.8	V

\*  $V_{IL}(\text{min}) = -0.5 \text{ V dc}$ ;  $V_{IL}(\text{min}) = -2.0 \text{ V ac}$  (pulse width  $\leq 20.0 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .

\*\*  $V_{IH}(\text{max}) = V_{CC} + 0.3 \text{ V dc}$ ;  $V_{IH}(\text{max}) = V_{CC} + 2.0 \text{ V ac}$  (pulse width  $\leq 20.0 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .

### DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0 \text{ to } V_{CC}$ )	$I_{lkg(I)}$	—	$\pm 1.0$	$\mu\text{A}$
Output Leakage Current ( $\bar{G} = V_{IH}$ )	$I_{lkg(O)}$	—	$\pm 1.0$	$\mu\text{A}$
AC Supply Current ( $\bar{G} = V_{IH}$ , $\bar{E} = V_{IL}$ , $I_{out} = 0 \text{ mA}$ , All Inputs = $V_{IL}$ or $V_{IH}$ , $V_{IL} = 0.0 \text{ V}$ and $V_{IH} \geq 3.0 \text{ V}$ , Cycle Time $\geq t_{KHKH} \text{ min}$ )	$I_{CCA66}$ $I_{CCA60}$ $I_{CCA50}$	—	1160 1100 1000	mA
AC Standby Current ( $\bar{E} = V_{IH}$ , $I_{out} = 0 \text{ mA}$ , All Inputs = $V_{IL}$ and $V_{IH}$ , $V_{IL} = 0.0 \text{ V}$ and $V_{IH} \geq 3.0 \text{ V}$ , Cycle Time $\geq t_{KHKH} \text{ min}$ )	$I_{SB1}$	—	300	mA
Output Low Voltage ( $I_{OL} = +8.0 \text{ mA}$ )	$V_{OL}$	—	0.4	V
Output High Voltage ( $I_{OH} = -4.0 \text{ mA}$ )	$V_{OH}$	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible PowerPC bus cycles.

### CAPACITANCE ( $f = 1.0 \text{ MHz}$ , $dV = 3.0 \text{ V}$ , $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (A0 – A15, $\bar{TSP}$ , $\bar{TSC}$ , BAA)	$C_{in}$	25	32	pF
Input/Output Capacitance (DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	10	pF
Input Capacitance (Kx, $\bar{Gx}$ , $\bar{Ex}$ , $\bar{Wx}$ )	$C_{in}$	12	15	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 5\%$   $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V  
 Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V  
 Output Load ..... See Figure 1A Unless Otherwise Noted

### READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ( $\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol	MPC2002SG66/ MPC2003SG66		MPC2002SG60/ MPC2003SG60		MPC2002SG50/ MPC2003SG50		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
Cycle Time	t <sub>KHKH</sub>	15	—	16.6	—	20	—	ns		
Clock Access Time	t <sub>KHQV</sub>	—	9	—	11	—	14	ns	4	
Output Enable to Output Valid	t <sub>GLQV</sub>	—	5	—	5	—	6	ns		
Clock High to Output Active	t <sub>KHQX1</sub>	6	—	6	—	6	—	ns		
Clock High to Output Change	t <sub>KHQX2</sub>	3	—	3	—	3	—	ns		
Output Enable to Output Active	t <sub>GLQX</sub>	0	—	0	—	0	—	ns		
Output Disable to Q High–Z	t <sub>GHQZ</sub>	2	6	2	6	2	6	ns	5	
Clock High to Q High–Z	t <sub>KHQZ</sub>	—	6	—	6	—	6	ns	5	
Clock High Pulse Width	t <sub>KHKL</sub>	5	—	5	—	6	—	ns		
Clock Low Pulse Width	t <sub>KLKH</sub>	5	—	5	—	6	—	ns		
Setup Times:	Address Address Status Data In Write Address Advance Chip Select	t <sub>AVKH</sub> t <sub>TSVKH</sub> t <sub>DVKH</sub> t <sub>WVKH</sub> t <sub>BAVKH</sub> t <sub>EVKH</sub>	2.5	—	2.5	—	2.5	—	ns	6
Hold Times:	Address Address Status Data In Write Address Advance Chip Select	t <sub>KHAX</sub> t <sub>KHTSX</sub> t <sub>KHDX</sub> t <sub>KHWX</sub> t <sub>KHBAX</sub> t <sub>KHEX</sub>	0.5	—	0.5	—	0.5	—	ns	6

#### NOTES:

1. A read cycle is defined by  $\overline{UW}$  and  $\overline{LW}$  high or  $\overline{TSP}$  low for the setup and hold times. A write cycle is defined by  $\overline{LW}$  or  $\overline{UW}$  low and  $\overline{TSP}$  high for the setup and hold times.
2. All read and write cycle timings are referenced from K or  $\overline{G}$ .
3.  $\overline{G}$  is a don't care when  $\overline{UW}$  or  $\overline{LW}$  is sampled low.
4. Maximum access times are guaranteed for all possible PowerPC 60x external bus cycles.
5. Transition is measured  $\pm 500 \text{ mV}$  from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature,  $t_{KHQZ}$  max is less than  $t_{KHQX1}$  min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for **ALL** rising edges of clock (K) whenever  $\overline{TSP}$  or  $\overline{TSC}$  are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for **ALL** rising edges of K when the chip is selected. Chip enable must be valid at each rising edge of clock for the device (when  $\overline{TSP}$  or  $\overline{TSC}$  is low) to remain enabled.

### AC TEST LOADS

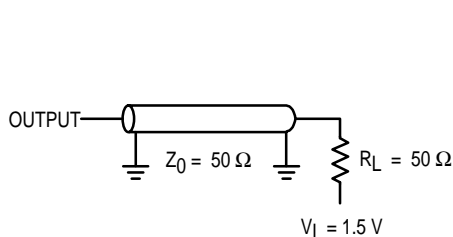


Figure 1A

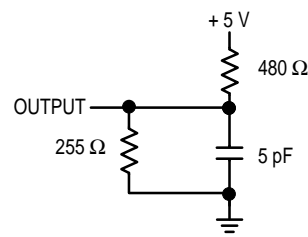
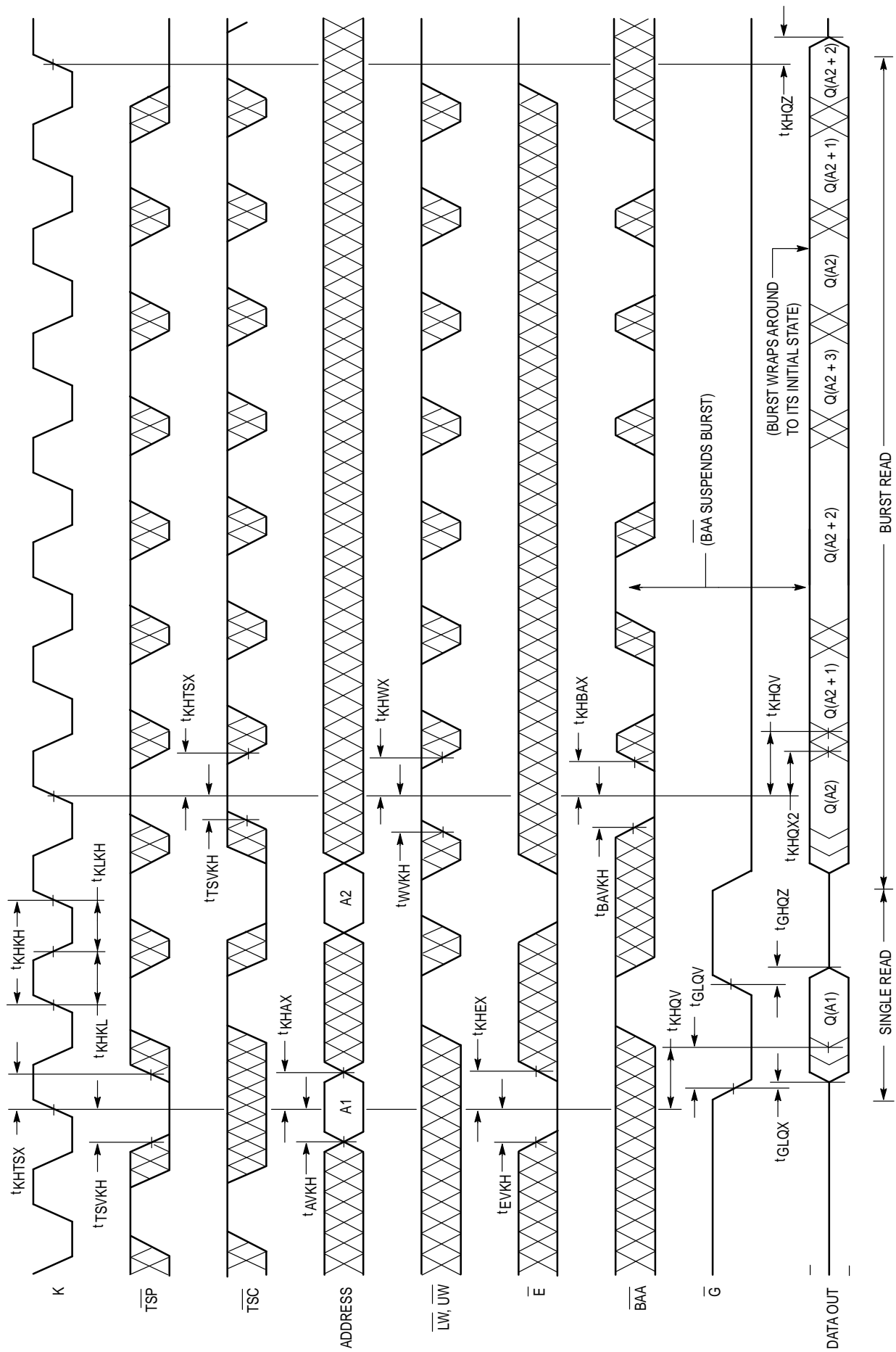


Figure 1B



# READ CYCLES

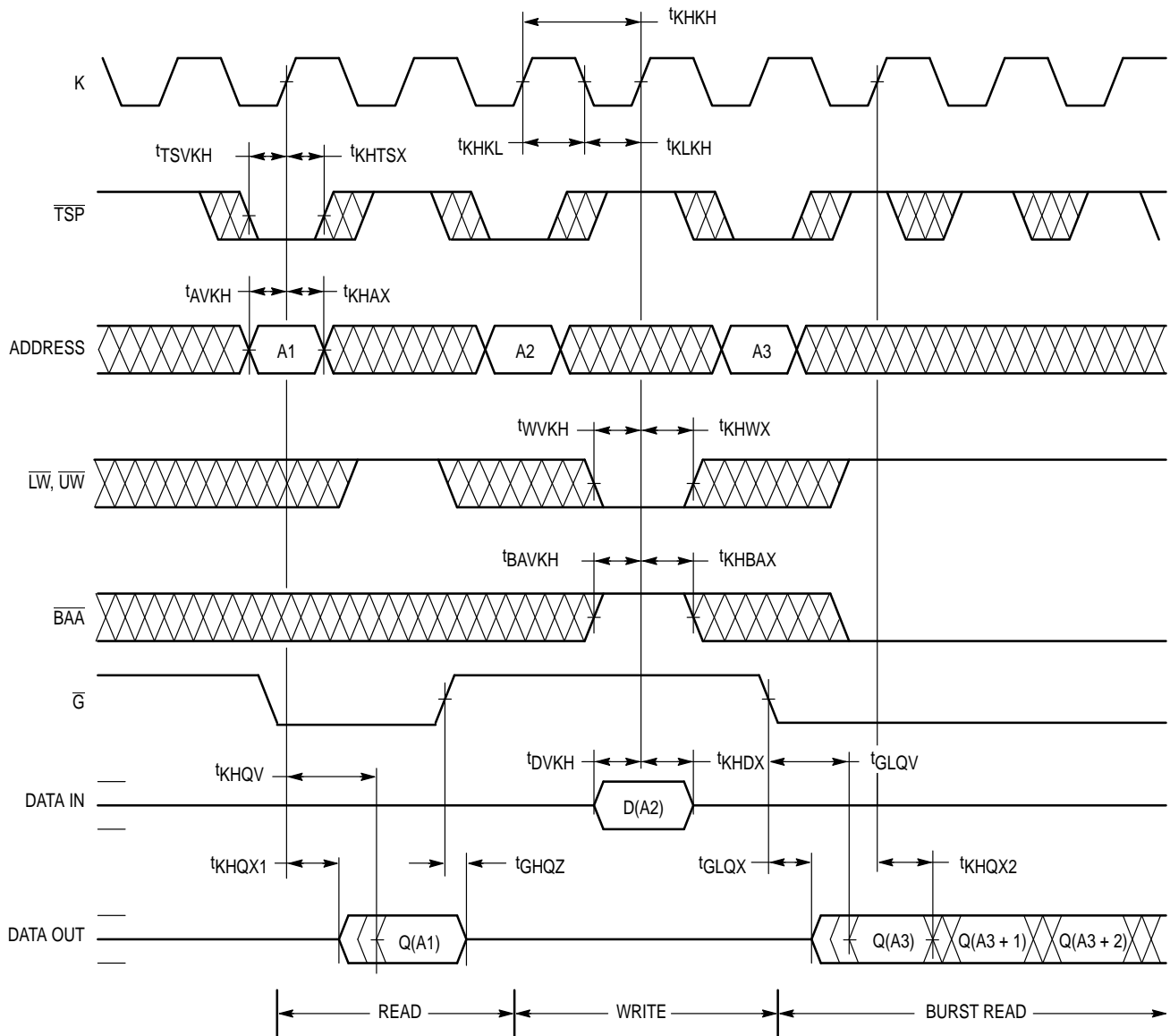


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

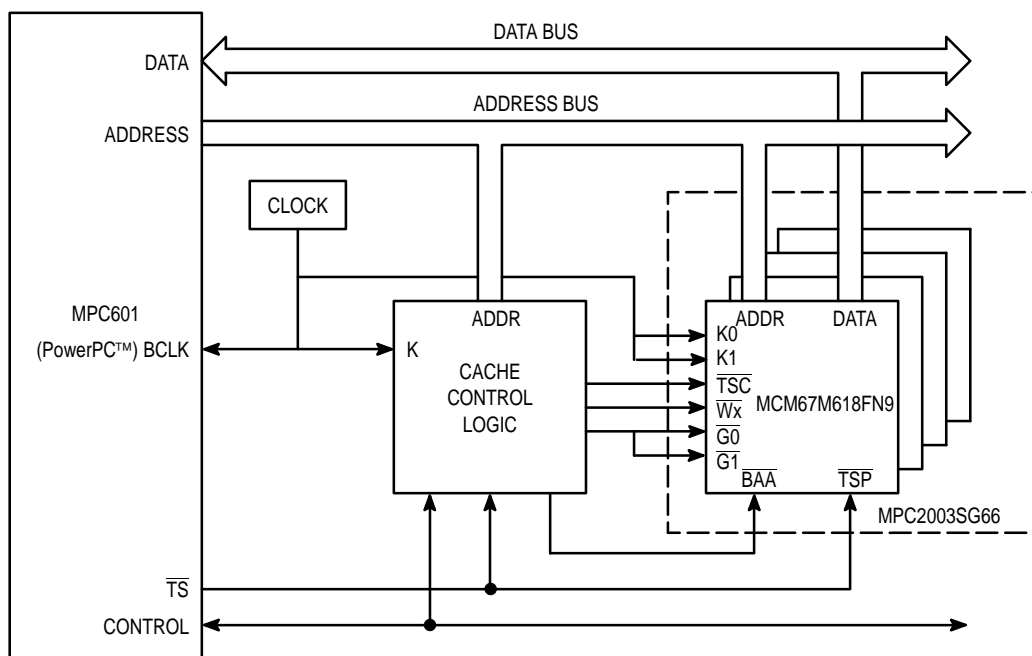
**MPC2002•MPC2003**  
**10**



# COMBINATION READ/WRITE CYCLE ( $\overline{E}$ low, $\overline{TSC}$ high)



## APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache  
Using MPC2003SG66 with a 66 MHz MPC601 PowerPC™

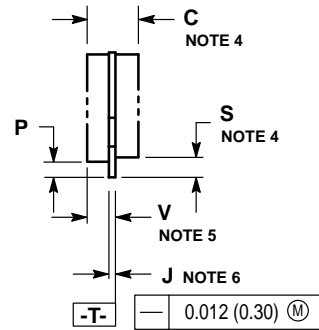
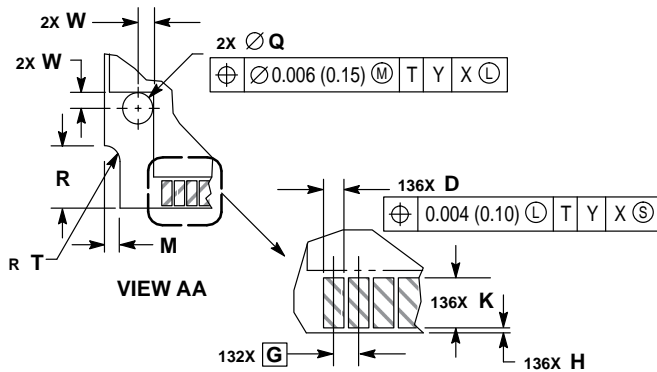
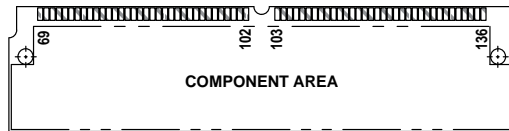
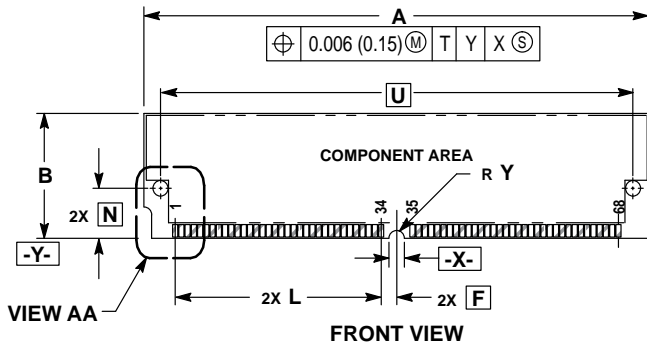
Figure 2

## ORDERING INFORMATION (Order by Full Part Number)

		<u>MPC2002</u>		<u>MPC2003</u>		<u>XX</u>		<u>XX</u>	
Motorola Memory Prefix		MCM							
Part Number									
Speed (66 = 66 MHz, 60 = 60 MHz, 50 = 50 MHz)									
Package (SG = Gold Pad SIMM)									
Full Part Numbers —									
		MPC2002SG66		MPC2002SG60		MPC2002SG50			
		MPC2003SG66		MPC2003SG60		MPC2003SG50			

## PACKAGE DIMENSIONS


### 136-LEAD DIMM CASE 1104-01



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND S DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION V DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	4.045	4.055	102.74	103.00
B	0.995	1.005	25.27	25.53
C	—	0.413	—	10.50
D	0.040	0.042	1.02	1.07
F	0.125 BSC	—	3.18 BSC	—
G	0.050 BSC	—	1.27 BSC	—
H	—	0.010	—	0.25
J	0.046	0.054	1.17	1.37
K	0.100	—	2.54	—
L	1.650 BSC	—	41.91 BSC	—
M	0.075	0.085	1.91	2.16
N	0.400 BSC	—	10.16 BSC	—
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.22
R	0.245	0.255	6.22	6.48
S	0.157	—	4.00	—
T	0.060	0.064	1.52	1.63
U	3.784 BSC	—	96.11 BSC	—
V	—	0.236	—	6.00
W	0.062	—	1.57	—
Y	0.060	0.064	1.52	1.63

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**MOTOROLA**



**MPC2002/D**

