

## Technical Data

MPC8280EC  
Rev. 1.0, 2/2004

MPC8280  
PowerQUICC II™ Family  
Hardware Specifications



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This document contains detailed information about power considerations, DC/AC electrical characteristics, and AC timing specifications for .13μm (HiP7) members of the PowerQUICC II™ family of integrated communications processors—the MPC8280, the MPC8275, and the MPC8270 (collectively called 'the MPC8280' throughout this document ).

The following topics are addressed:

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# 1 Overview

Table 1 shows the functionality supported by each device in the MPC8280 family.

**Table 1. MPC8280 PowerQUICC II Family Functionality**

Functionality	Package <sup>1</sup>	Devices			
		MPC8270		MPC8275	MPC8280
		480 TBGA	516 PBGA	516 PBGA	480 TBGA
Serial communications controllers (SCCs)		4	4	4	4
QUICC multi-channel controller (QMC)		—	—	—	—
Fast communication controllers (FCCs)		3	3	3	3
I-Cache (Kbyte)		16	16	16	16
D-Cache (Kbyte)		16	16	16	16
Ethernet (10/100)		3	3	3	3
UTOPIA II Ports		0	0	2	2
Multi-channel controllers (MCCs)		1	1	1	2
PCI bridge		Yes	Yes	Yes	Yes
Transmission convergence (TC) layer		—	—	—	Yes
Inverse multiplexing for ATM (IMA)		—	—	—	Yes
Universal serial bus (USB) 2.0 full/low rate		1	1	1	1
Security engine (SEC)		—	—	—	—

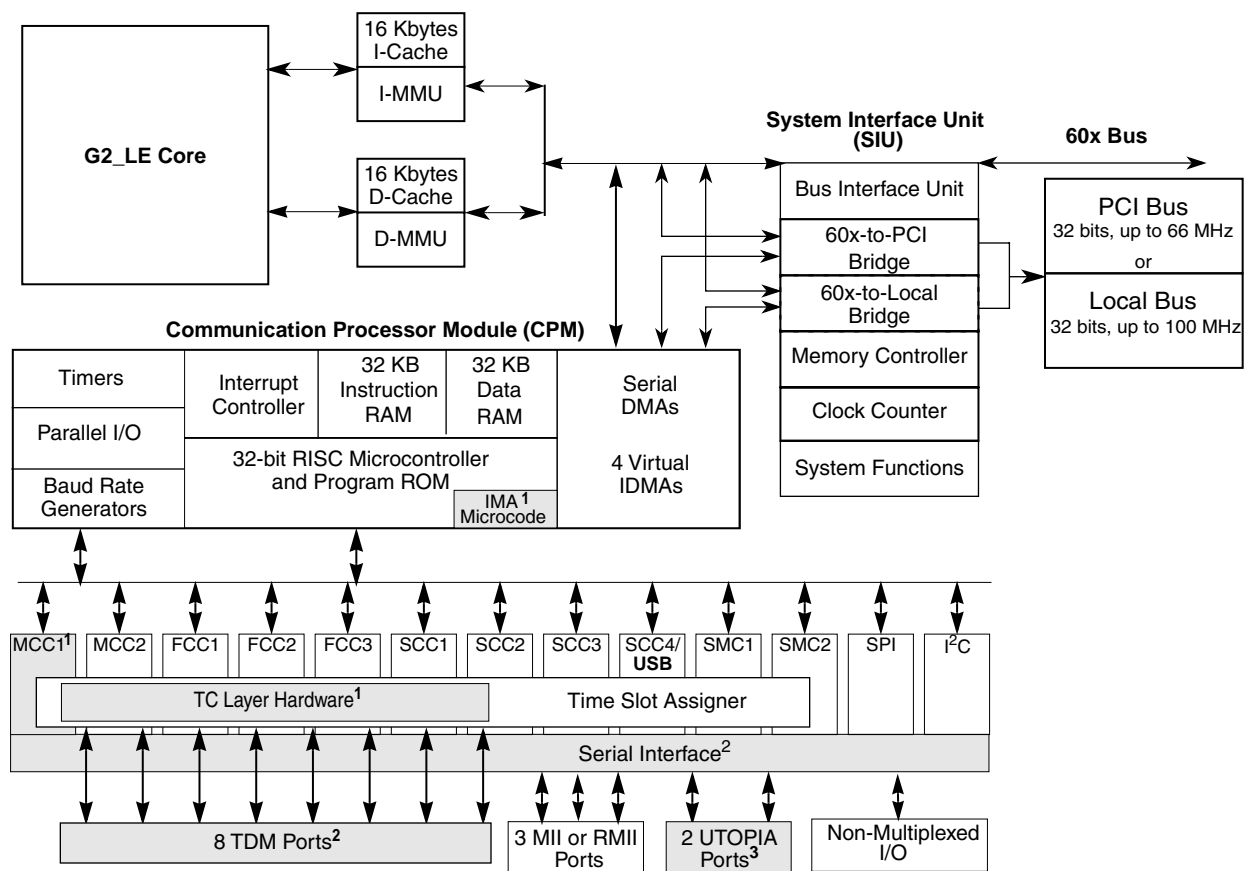
<sup>1</sup> Refer to Table 2.

Devices in the MPC8280 family are available in three packages—the standard ZU package and the alternate VR or ZQ packages—as shown in Table 2. Note that throughout this document references to the MPC8280 and the MPC8270 are inclusive of VR and ZQ package devices unless otherwise specified. For more information on VR and ZQ packages, contact your Motorola sales office. For package ordering information, refer to Section 10, “Ordering Information.”

**Table 2. HiP7 PowerQUICC II Device Packages**

Code (Package)	ZU (480 TBGA—Leaded)	VR (516 PBGA—Lead free)	ZQ (516 PBGA—Lead spheres)
Device	MPC8280	MPC8275VR	MPC8275ZQ
	MPC8270	MPC8270VR	MPC8270ZQ

Figure 1 shows the block diagram. Shaded portions are device-specific; refer to the notes below.



Notes:

<sup>1</sup> MPC8280 only (not on MPC8270, the VR package, nor the ZQ package)

<sup>2</sup> MPC8280 has 2 serial interface (SI) blocks and 8 TDM ports. MPC8270 and the VR and ZQ packages have only 1 SI block and 4 TDM ports (TDM2[A–D]).

<sup>3</sup> MPC8280, MPC8275VR, MPC8275ZQ only (not on MPC8270, MPC8270VR, nor MPC8270ZQ)

Figure 1. MPC8280 Block Diagram

## 1.1 Features

The major features of the MPC8280 are as follows:

- Dual-issue integer (G2\_LE) core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 166–450 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - PowerPC™ architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface

## Overview

- High-performance (SPEC95 benchmark at 450 MHz; 855 Dhrystones MIPS at 450 MHz)
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2\_LE core and for the CPM
  - G2\_LE core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, 5:1, 6:1, 7:1, 8:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1, 8:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66.67/83.3/100 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI-to-60x-memory and 60x-memory-to-PCI streaming
  - PCI host bridge or peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8280) required by the PCI standard as well as message and doorbell registers
  - Supports the I<sub>2</sub>O standard
  - Hot-swap friendly (supports the hot swap specification as defined by PICMG 2.1 R1.0 August 3, 1998)

- Support for 66.67/83.33/100 MHz, 3.3 V specification
- 60x-PCI bus core logic that uses a buffer pool to allocate buffers for each port
- Uses the local bus signals, removing need for additional pins
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- 12-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user-programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64-bus width (60x) and byte selects for 32-bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2\_LE core through an on-chip 32-Kbyte dual-port data RAM, an on-chip 32-Kbyte dual-port instruction RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through media independent interface (MII) or reduced media independent interface (RMII)
    - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 64 K external connections (no ATM support for the MPC8270)
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
    - FCC2 can also be connected to the TC layer (MPC8280 only)
  - Two multichannel controllers (MCCs) (one MCC on the MPC8270)
    - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC

## Overview

- Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
  - Ethernet/IEEE 802.3 CDMA/CS
  - HDLC/SDLC and HDLC bus
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Binary synchronous (BISYNC) communications
  - Transparent
- Universal serial bus (USB) controller
  - Supports USB 2.0 full/low rate compatible
  - USB host mode
    - Supports control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - NRZI encoding/decoding with bit stuffing
    - Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - Flexible data buffers with multiple buffers per frame
    - Supports local loopback mode for diagnostics (12 Mbps only)
  - Supports USB slave mode
    - Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - CRC16 generation and checking
    - CRC5 checking
    - NRZI encoding/decoding with bit stuffing
    - 12- or 1.5-Mbps data rate
    - Flexible data buffers with multiple buffers per frame
    - Automatic retransmission upon transmit error
- Two serial management controllers (SMCs), identical to those of the MPC860
  - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I<sup>2</sup>C) controller (identical to the MPC860 I<sup>2</sup>C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8270)
  - Supports two groups of four TDM channels for a total of eight TDMs (one group of four on the MPC8270 and the MPC8275)
  - 2,048 bytes of SI RAM
  - Bit or byte resolution

- Independent transmit and receive routing, frame synchronization
- Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Motorola interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers
- Inverse multiplexing for ATM capabilities (IMA) (MPC8280 only). Supported by eight transfer transmission convergence (TC) layers between the TDMs and FCC2.
- Transmission convergence (TC) layer (MPC8280 only)

## 2 Operating Conditions

Table 3 shows the maximum electrical ratings.

**Table 3. Absolute Maximum Ratings<sup>1</sup>**

Rating	Symbol	Value	Unit
Core supply voltage <sup>2</sup>	VDD	-0.3 – 2.25	V
PLL supply voltage <sup>2</sup>	VCCSYN	-0.3 – 2.25	V
I/O supply voltage <sup>3</sup>	VDDH	-0.3 – 4.0	V
Input voltage <sup>4</sup>	VIN	GND(-0.3) – 3.6	V
Junction temperature	T <sub>j</sub>	120	°C
Storage temperature range	T <sub>STG</sub>	(-55) – (+150)	°C

<sup>1</sup> Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

<sup>2</sup> **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

<sup>3</sup> **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

<sup>4</sup> **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 4 lists recommended operational voltage conditions.

**Table 4. Recommended Operating Conditions<sup>1</sup>**

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.45 – 1.60	V
PLL supply voltage	VCCSYN	1.45 – 1.60	V
I/O supply voltage	VDDH	3.135 – 3.465	V
Input voltage	VIN	GND (-0.3) – 3.465	V
Junction temperature (maximum)	T <sub>j</sub>	105 <sup>2</sup>	°C
Ambient temperature	T <sub>A</sub>	0–70 <sup>2</sup>	°C

<sup>1</sup> **Caution:** These are the recommended and tested operating conditions. Proper operation outside of these conditions is not guaranteed.

## DC Electrical Characteristics

<sup>2</sup> Note that for extended temperature parts the range is  $(-40)_{T_A} - 105_{T_J}$ .

### NOTE: Core, PLL, and I/O Supply Voltages

After power up sequence is complete, VDDH and VDD/VCCSYN must track each other and both voltages must vary in the same direction. When varying in the positive direction, VDDH may vary up to 5% from nominal or  $3.3 + 0.165 = 3.465$  V, in which case VDD/VCCSYN must also vary upward by 5% from nominal or  $1.525 + 0.075 = 1.6$  V. The same applies to the negative direction: VDDH may vary downward up to -5% from nominal or  $3.3 - 0.165 = 3.135$  V, in which case VDD/VCCSYN must vary downward by -5% from nominal or  $1.525 - 0.075 = 1.45$  V. A/C timing specification violation may occur during the time that voltage tracking is not correct.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or  $V_{CC}$ ).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

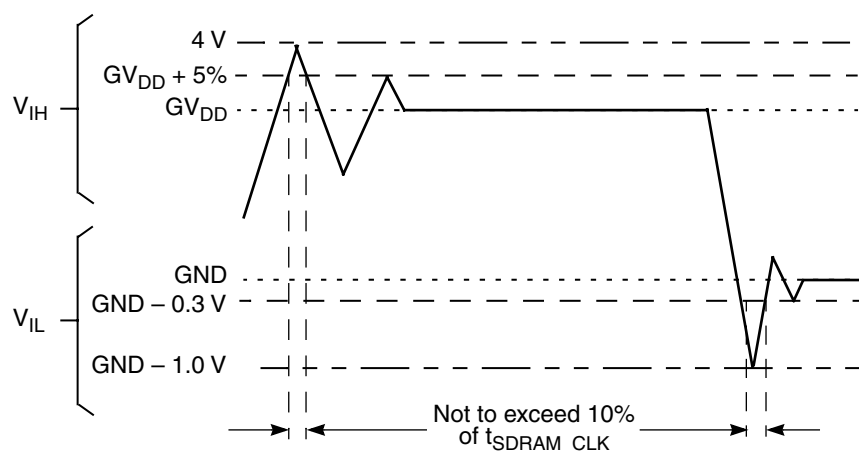


Figure 2. Overshoot/Undershoot Voltage

## 3 DC Electrical Characteristics

Table 5 shows DC electrical characteristics.

Table 5. DC Electrical Characteristics<sup>1</sup>

Characteristic	Symbol	Min	Max	Unit
Input high voltage— all inputs except $\overline{TRST}$ and $\overline{PORESET}^2$	$V_{IH}$	2.0	3.465	V
Input low voltage	$V_{IL}$	GND	0.8	V
CLKIN input high voltage	$V_{IHC}$	2.4	3.465	V
CLKIN input low voltage	$V_{ILC}$	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}^3$	$I_{IN}$	—	10	$\mu A$



Table 5. DC Electrical Characteristics<sup>1</sup> (Continued)

Characteristic	Symbol	Min	Max	Unit
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}^3$	$I_{OZ}$	—	10	$\mu A$
Signal low input current, $V_{IL} = 0.8 V$	$I_L$	—	1	$\mu A$
Signal high input current, $V_{IH} = 2.0 V$	$I_H$	—	1	$\mu A$
Output high voltage, $I_{OH} = -2 mA$ except UTOPIA mode, and open drain pins  In UTOPIA mode <sup>4</sup> (UTOPIA pins only): $I_{OH} = -8.0mA$ PA[0-31] PB[4-31] PC[0-31] PD[4-31]	$V_{OH}$	2.4	—	V
In UTOPIA mode <sup>4</sup> (UTOPIA pins only): $I_{OL} = 8.0mA$ PA[0-31] PB[4-31] PC[0-31] PD[4-31]	$V_{OL}$	—	0.5	V

## DC Electrical Characteristics

Table 5. DC Electrical Characteristics<sup>1</sup> (Continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 6.0\text{mA}$ $\overline{\text{BR}}$ $\overline{\text{BG}}$ $\overline{\text{ABB/IRQ2}}$ $\overline{\text{TS}}$ $\text{A}[0-31]$ $\text{TT}[0-4]$ $\overline{\text{TBST}}$ $\text{TSIZE}[0-3]$ $\overline{\text{AACK}}$ $\overline{\text{ARTRY}}$ $\overline{\text{DBG}}$ $\overline{\text{DBB/IRQ3}}$ $\text{D}[0-63]$ $\text{DP}(0)/\overline{\text{RSRV/EXT\_BR2}}$ $\text{DP}(1)/\overline{\text{IRQ1/EXT\_BG2}}$ $\text{DP}(2)/\overline{\text{TLBISYNC/IRQ2/EXT\_DBG2}}$ $\text{DP}(3)/\overline{\text{IRQ3/EXT\_BR3/CKSTP\_OUT}}$ $\text{DP}(4)/\overline{\text{IRQ4/EXT\_BG3/CORE\_SREST}}$ $\text{DP}(5)/\overline{\text{TBEN/EXT\_DBG3/IRQ5/CINT}}$ $\text{DP}(6)/\overline{\text{CSE}(0)/\text{IRQ6}}$ $\text{DP}(7)/\overline{\text{CSE}(1)/\text{IRQ7}}$ $\overline{\text{PSDVAL}}$ $\overline{\text{TA}}$ $\overline{\text{TEA}}$ $\overline{\text{GBL/IRQ1}}$ $\overline{\text{CI/BADDR29/IRQ2}}$ $\overline{\text{WT/BADDR30/IRQ3}}$ $\overline{\text{L2\_HIT/IRQ4}}$ $\overline{\text{CPU\_BG/BADDR31/IRQ5/CINT}}$ $\overline{\text{CPU\_DBG}}$ $\overline{\text{CPU\_BR}}$ $\overline{\text{IRQ0/NMI\_OUT}}$ $\overline{\text{IRQ7/INT\_OUT/APE}}$ $\overline{\text{PORESET}}$ $\overline{\text{HRESET}}$ $\overline{\text{SRESET}}$ $\overline{\text{RSTCONF}}$	$V_{OL}$	—	0.4	V

Table 5. DC Electrical Characteristics<sup>1</sup> (Continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ $\overline{ALE}$ $\overline{BCTL0}$ $\overline{PWE}[0-7]/\overline{PSDDQM}[0-7]/\overline{PBS}[0-7]$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI\_CFG}[0-3]$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI\_MODCKH0}$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI\_MODCKH1}$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI\_MODCKH2}$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI\_MODCKH3}$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI\_MODCK}$ $\overline{LWR}$ $\overline{MODCK}[1-3]/\overline{AP}[1-3]/\overline{TC}[0-2]/\overline{BNKSEL}[0-2]$	$V_{OL}$	—	0.4	V
$I_{OL} = 3.2\text{mA}$ $\overline{L\_A14}/\overline{PAR}$ $\overline{L\_A15}/\overline{FRAME}/\overline{SMI}$ $\overline{L\_A16}/\overline{TRDY}$ $\overline{L\_A17}/\overline{IRDY}/\overline{CKSTP\_OUT}$ $\overline{L\_A18}/\overline{STOP}$ $\overline{L\_A19}/\overline{DEVSEL}$ $\overline{L\_A20}/\overline{IDSEL}$ $\overline{L\_A21}/\overline{PERR}$ $\overline{L\_A22}/\overline{SERR}$ $\overline{L\_A23}/\overline{REQ0}$ $\overline{L\_A24}/\overline{REQ1}/\overline{HSEJSW}$ $\overline{L\_A25}/\overline{GNT0}$ $\overline{L\_A26}/\overline{GNT1}/\overline{HSLED}$ $\overline{L\_A27}/\overline{GNT2}/\overline{HSENUM}$ $\overline{L\_A28}/\overline{RST}/\overline{CORE\_SRESET}$ $\overline{L\_A29}/\overline{INTA}$ $\overline{L\_A30}/\overline{REQ2}$ $\overline{L\_A31}$ $\overline{LCL\_D}[0-31]/\overline{AD}[0-31]$ $\overline{LCL\_DP}[0-3]/\overline{C}/\overline{BE}[0-3]$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ $\overline{TDO}$ $\overline{QREQ}$				

<sup>1</sup> The default configuration of the CPM pins ( $\overline{PA}[0-31]$ ,  $\overline{PB}[4-31]$ ,  $\overline{PC}[0-31]$ ,  $\overline{PD}[4-31]$ ) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

<sup>2</sup>  $\overline{TRST}$  and  $\overline{PORESET}$  should be tied to VDDH via a 2K  $\Omega$  external pull-up resistor.

<sup>3</sup> The leakage current is measured for nominal VDDH, VCCSYN, and VDD.

<sup>4</sup> MPC8280, MPC8275VR, MPC8275ZQ only

## 4 Thermal Characteristics

Table 6 describes thermal characteristics for both the packages. See Table 2 for information about a given device's package. For the discussions sections 4.1 and 4.2,  $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ , where  $P_{I/O}$  is the power dissipation of the I/O drivers.

**Table 6. Thermal Characteristics**

Characteristic	Symbol	Value		Unit	Air Flow
		480 TBGA	516 PBGA		
Junction to ambient—single-layer board <sup>1</sup>	$R_{\theta JA}$	16	27	°C/W	Natural convection
		11	21		1 m/s
Junction to ambient—four-layer board	$R_{\theta JA}$	12	19	°C/W	Natural convection
		9	16		1 m/s
Junction to board <sup>2</sup>	$R_{\theta JB}$	6	11	°C/W	—
Junction to case <sup>3</sup>	$R_{\theta JC}$	2	8	°C/W	—
Junction-to-package top <sup>4</sup>	$\Psi_{JT}$	2	2	°C/W	—

<sup>1</sup> Assumes no thermal vias

<sup>2</sup> Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>3</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

<sup>4</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 4.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature,  $T_J$ , in °C can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$  = ambient temperature (°C)

$R_{\theta JA}$  = package junction-to-ambient thermal resistance (°C/W)

$P_D$  = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity  $T_J - T_A$ ) are possible.

## 4.2 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$  = thermal characterization parameter

$T_T$  = thermocouple temperature on top of package

$P_D$  = power dissipation in package

The thermal characterization parameter is measured per JEDEC JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 4.3 Layout Practices

Each  $V_{CC}$  pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The  $V_{CC}$  power supply should be bypassed to ground using at least four 0.1  $\mu$ F by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip  $V_{CC}$  and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as  $V_{CC}$  and GND planes.

All output pins on the MPC8280 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the  $V_{CC}$  and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

## 5 Power Dissipation

Table 7 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink. For a complete list of possible clock configurations, refer to Section 7, “Clock Configuration Modes.”

**Table 7. Estimated Power Dissipation for Various Configurations<sup>1</sup>**

Bus (MHz)	CPM Multiplication Factor	CPM (MHz)	CPU Multiplication Factor	CPU (MHz)	$P_{INT}(W)^{2,3}$	
					V <sub>DDI</sub> 1.5 Volts	
					Nominal	Maximum
66.67	2.5	166	3.5	233	0.95	1.0
66.67	2.5	166	4	266	1.0	1.05
66.67	3	200	4	266	1.05	1.1
66.67	3.5	233	4.5	300	1.05	1.15
83.33	3	250	4	333	1.25	1.35
83.33	3	250	4.5	375	1.3	1.4
83.33	3.5	292	5	417	1.45	1.55
100	3	300	4	400	1.5	1.6
100	3	300	4.5	450	1.55	1.65

<sup>1</sup> Test temperature = 105° C

<sup>2</sup>  $P_{INT} = I_{DD} \times V_{DD}$  Watts

<sup>3</sup> Values do not include I/O. Add the following estimates for active I/O based on the following bus speeds:

66.7 MHz = 0.45 W (nominal), 0.5 W (maximum)

83.3 MHz = 0.5W (nominal), 0.6 W (maximum)

100 MHz = 0.6 W (nominal), 0.7 W (maximum)

## 6 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for 66.67/83.33/100 MHz devices. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in Table 8.

**Table 8. Output Buffer Impedances<sup>1</sup>**

Output Buffers	Typical Impedance (Ω)
60x bus	45 or 27 <sup>2</sup>
Local bus	45
Memory controller	45 or 27 <sup>2</sup>
Parallel I/O	45
PCI	27

<sup>1</sup> These are typical values at 65° C. Impedance may vary by ±25% with process and temperature.

<sup>2</sup> On silicon revision 0.0 (mask #: 0K49M), selectable impedance is not available. Impedance is set at 45 Ω.

On all other revisions, impedance value is selected through the SIUMCR[20,21]. Refer to the *MPC8280 Addendum to the MPC8260 PowerQUICC II Family Reference Manual*.

## 6.1 CPM AC Characteristics

Table 9 lists CPM output characteristics.

**Table 9. AC Characteristics for CPM Outputs<sup>1</sup>**

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	5.5	0.5	0.5	0.5
sp36b	sp37b	FCC outputs—external clock (NMSI)	8	8	8	2	2	2
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	10	10	10	0	0	0
sp38b	sp39b	SCC/SMC/SPI/I2C outputs—external clock (NMSI)	8	8	8	2	2	2
sp40	sp41	TDM outputs/SI	11	11	11	2.5	2.5	2.5
sp42	sp43	TIMER/IDMA outputs	14	11	11	1	0.5	0.5
sp42a	sp43a	PIO outputs	14	11	11	0.5	0.5	0.5

<sup>1</sup> Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 10 lists CPM input characteristics.

**Table 10. AC Characteristics for CPM Inputs<sup>1</sup>**

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	6	6	6	0	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	2.5	2	2	2
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	6	6	6	0	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	4	2	2	2
sp20	sp21	TDM inputs/SI	3	3	3	2.5	2.5	2.5
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	8	0.5	0.5	0.5

<sup>1</sup> Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

### NOTE

Although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

AC Electrical Characteristics

Figure 3 shows the FCC internal clock.

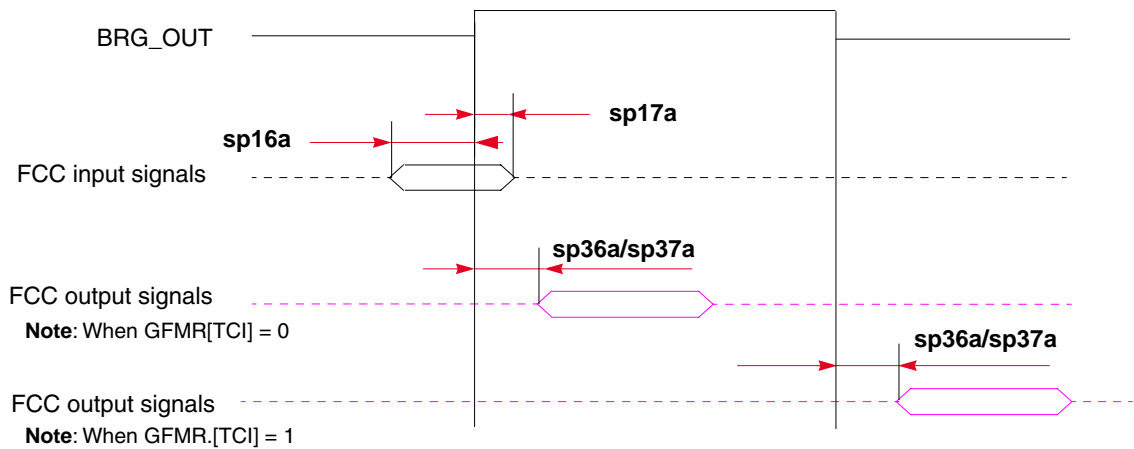


Figure 3. FCC Internal Clock Diagram

Figure 4 shows the FCC external clock.

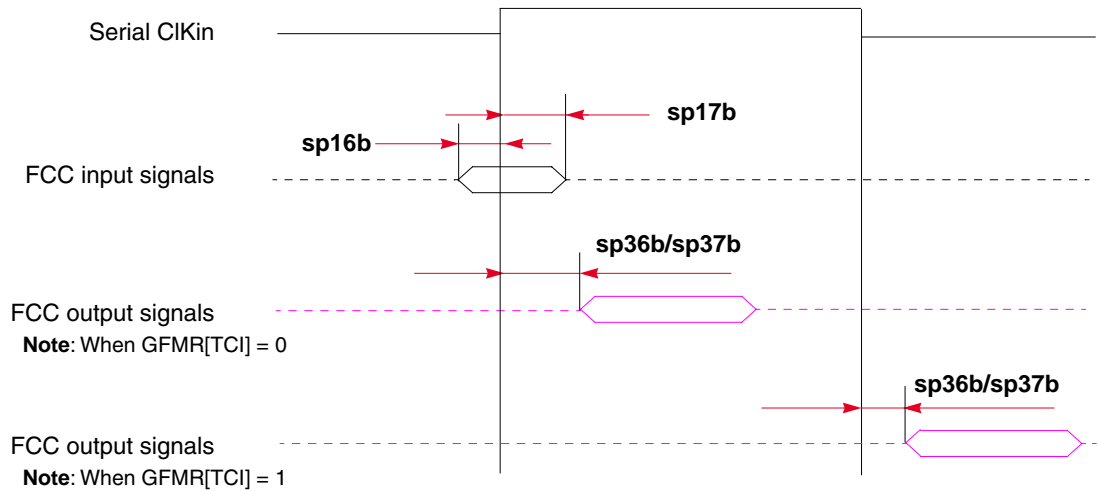
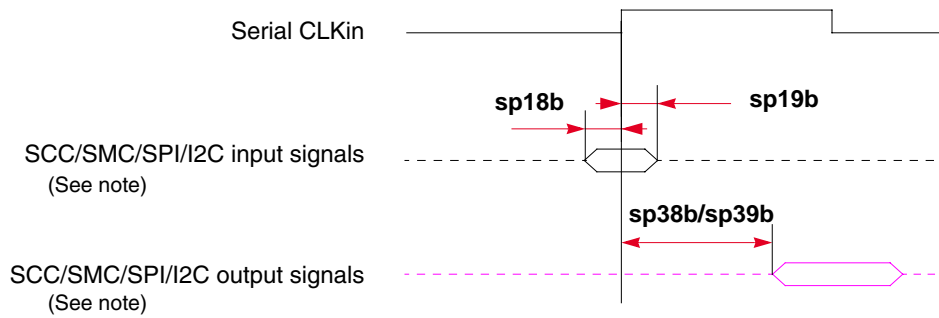


Figure 4. FCC External Clock Diagram



Figure 5 shows the SCC/SMC/SPI/I<sup>2</sup>C external clock.

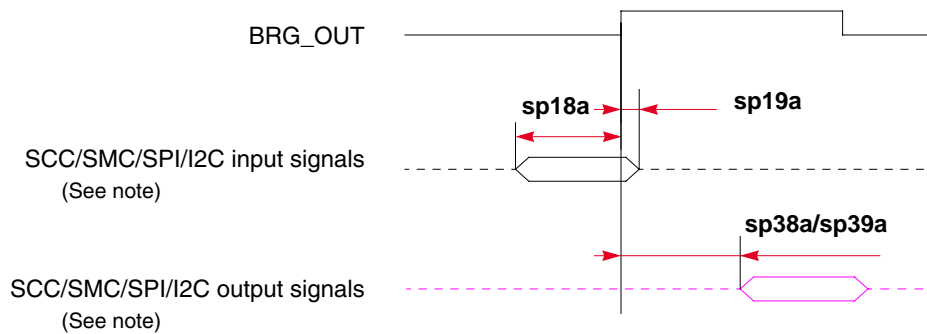


**Note:** There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 5. SCC/SMC/SPI/I<sup>2</sup>C External Clock Diagram**

Figure 6 shows the SCC/SMC/SPI/I<sup>2</sup>C internal clock.



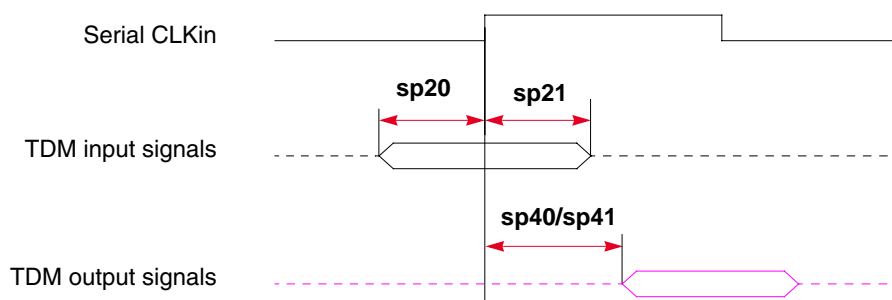
**Note:** There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 6. SCC/SMC/SPI/I<sup>2</sup>C Internal Clock Diagram**

## AC Electrical Characteristics

Figure 7 shows TDM input and output signals.

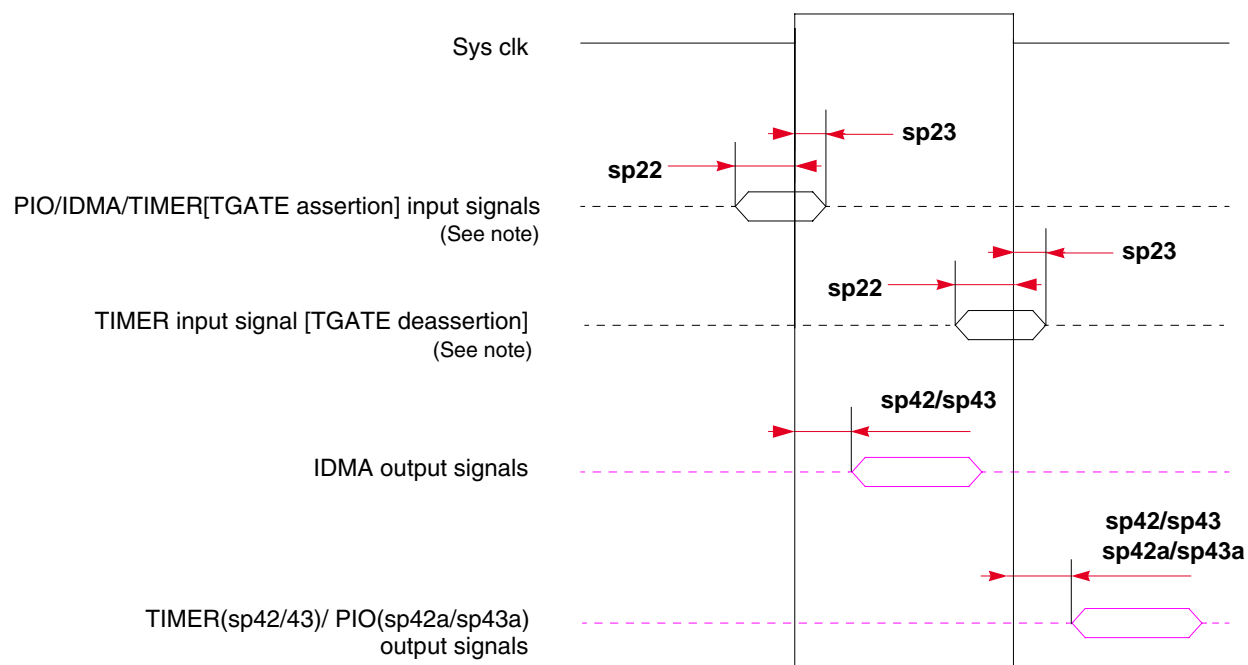


**Note:** There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

**Figure 7. TDM Signal Diagram**

Figure 8 shows PIO and timer signals.



**Note:** TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

**Figure 8. PIO and Timer Signal Diagram**

## 6.2 SIU AC Characteristics

### NOTE: CLKIN Jitter and Duty Cycle

The CLKIN input to the MPC8280 should not exceed  $\pm 150$  psec. This represents total input jitter—the combination of short term (peak-to-peak) and long term (cumulative). The duty cycle of CLKIN should not exceed the ratio of 40:60.

### NOTE: PCI AC Timing

The MPC8280 meets the timing requirements of *PCI Specification Revision 2.2*. Refer to Sections 7.2 and 7.3 and “Note: Tval (Output Hold)” to determine if a specific clock configuration is compliant.

Table 11 lists SIU input characteristics.

**Table 11. AC Characteristics for SIU Inputs<sup>1</sup>**

Spec Number		Characteristic	Value (ns)					
Setup	Hold		Setup			Hold		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp11	sp10	AACK/TA/TS/DBG/BG/BR	6	5	3.5	0.5	0.5	0.5
sp11a	sp10	ARTRY/ TEA	6	5	4	0.5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	3.5	0.5	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	7	5	3.5	0.5	0.5	0.5
sp13a	sp10	Pipeline mode— Data bus in ECC and PARITY modes	5	4	2.5	0.5	0.5	0.5
sp14	sp10	DP pins	7	5	3.5	0.5	0.5	0.5
sp14a	sp10	Pipeline mode—DP pins	—	4	2.5	—	0.5	0.5
sp15	sp10	All other pins	5	4	3.5	0.5	0.5	0.5

<sup>1</sup> Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

## AC Electrical Characteristics

Table 12 lists SIU output characteristics.

**Table 12. AC Characteristics for SIU Outputs<sup>1</sup>**

Spec Number		Characteristic	Value (ns)					
Max	Min		Maximum Delay			Minimum Delay		
			66 MHz	83 MHz	100 MHz	66 MHz	83 MHz	100 MHz
sp31	sp30	PSDVAL/TEA/TA	7	6	5.5	1	1	1
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	5.5	1	1	1
sp33a	sp30	Data bus	6.5	6.5	5.5	0.7	0.7	0.7
sp33b	sp30	DP	6	5.5	5.5	1	1	1
sp34	sp30	Memory controller signals/ALE	6	5.5	5.5	1	1	1
sp35	sp30	All other signals	6	5.5	5.5	1	1	1
sp35a	sp30	AP	7	7	7	1	1	1

<sup>1</sup> Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

### NOTE

Activating data pipelining (setting BR<sub>x</sub>[DR] in the memory controller) improves the AC timing.

Figure 9 shows the interaction of several bus signals.

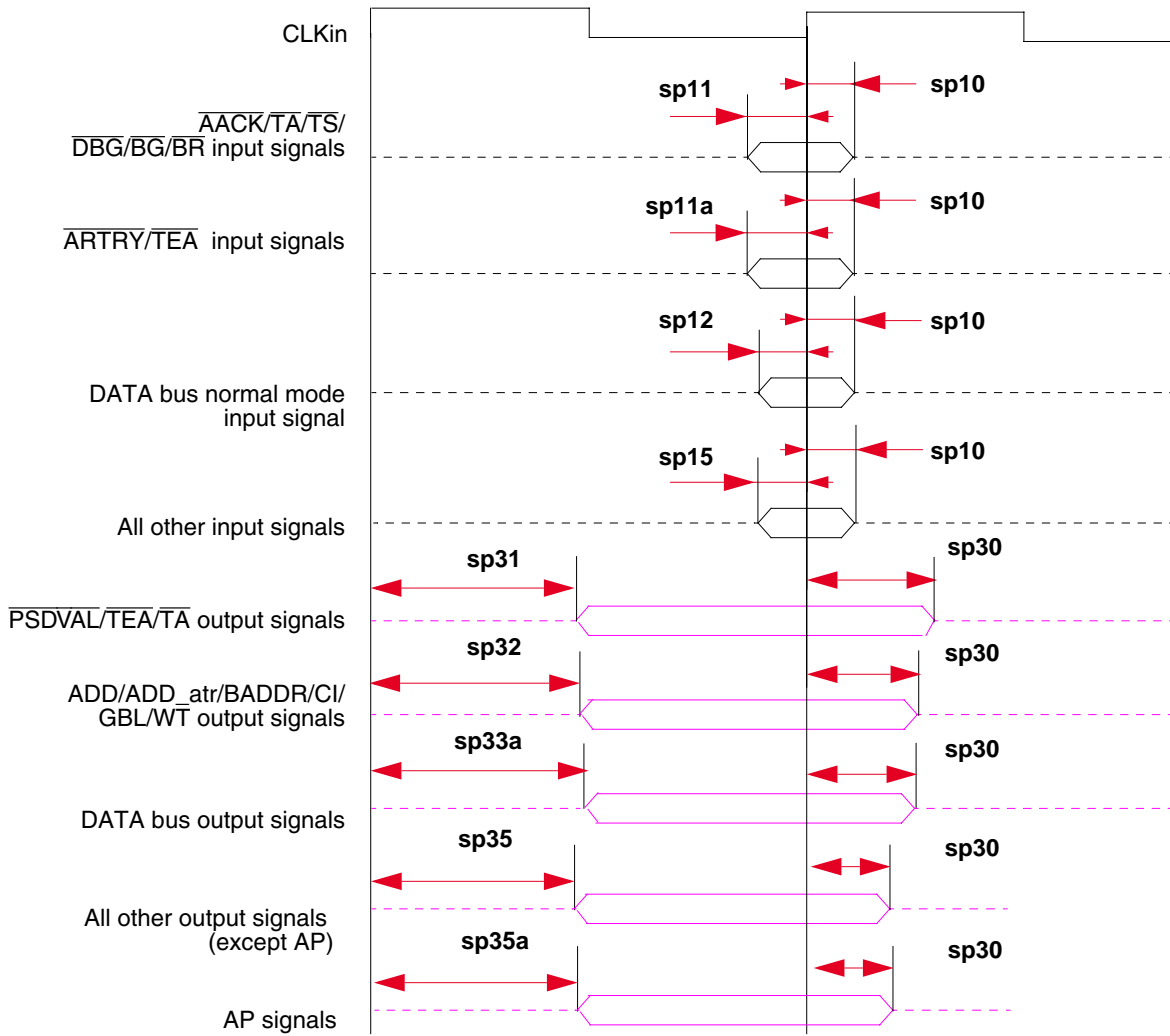
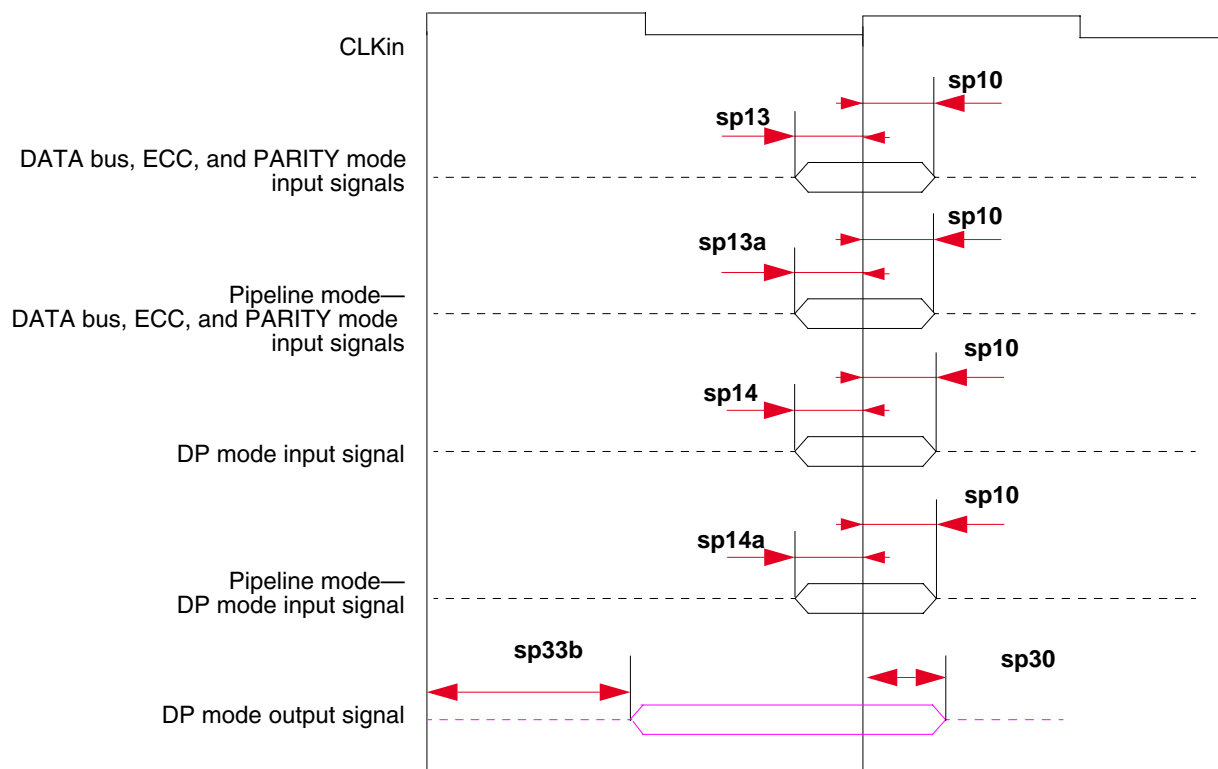


Figure 9. Bus Signals

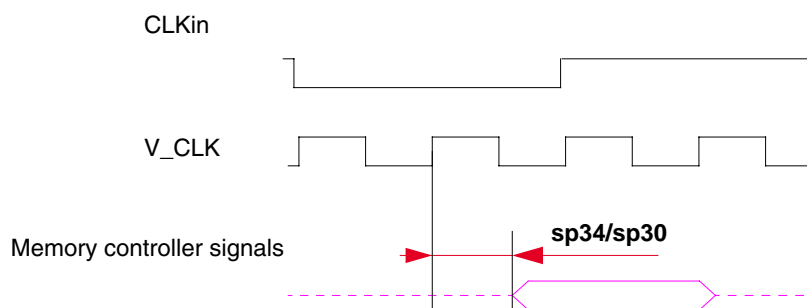
## AC Electrical Characteristics

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).



**Figure 10. Parity Mode Diagram**

Figure 11 shows signal behavior in MEMC mode.



**Figure 11. MEMC Mode Diagram**

### NOTE

Generally, all MPC8280 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 13.

Table 13. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIn)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIn	1/2 CLKIn	3/4 CLKIn
1:2.5	3/10 CLKIn	1/2 CLKIn	8/10 CLKIn
1:3.5	4/14 CLKIn	1/2 CLKIn	11/14 CLKIn

Figure 12 is a representation of the information in Table 13.

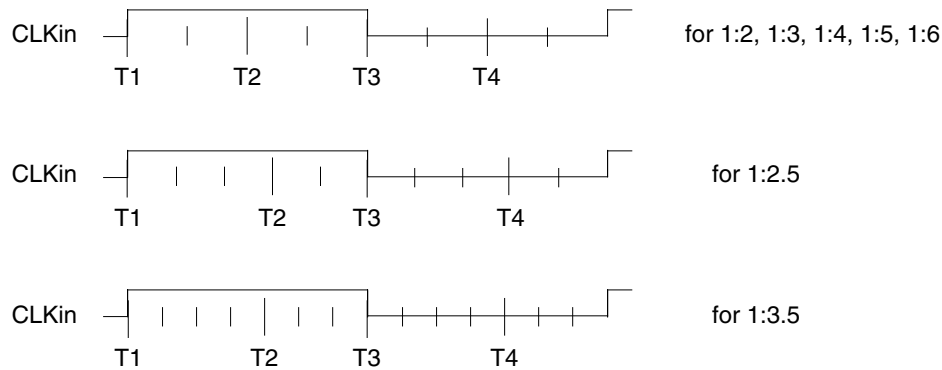


Figure 12. Internal Tick Spacing for Memory Controller Signals

#### NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKIn's rising edge.

## 7 Clock Configuration Modes

The MPC8280 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI\_MODE, PCI\_CFG[0], PCI\_MODCK—as shown in Table 14.

Table 14. MPC8280 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK <sup>1</sup>			
1	—	—	Local bus	—	Table 15
0	0	0	PCI host	50–66	Table 16
0	0	1		25–50	Table 17
0	1	0	PCI agent	50–66	Table 18
0	1	1		25–50	Table 19

<sup>1</sup> Determines PCI clock frequency range. Refer to Sections 7.2 and 7.3.

## Clock Configuration Modes

In each clocking mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-up reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK\_H). Both the PLLs and the dividers are set according to the selected MPC8280 clock operation mode as described in the following sections.

### 7.1 Local Bus Mode

Table 15 lists clock configurations for the MPC8280 in local bus mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

#### NOTE

Clock configurations change only after  $\overline{\text{PORESET}}$  is asserted.

**Table 15. Clock Configurations for Local Bus Mode<sup>1</sup>**

Mode <sup>2</sup>	Bus Clock <sup>3</sup> (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)	
	low	high		low	high		low	high
MODCK_H-MODCK[1-3]								
Default Modes (MODCK_H= 0000)								
0000_000	62.5	133.3	3	187.5	400.0	4	250.0	533.3
0000_001	50.0	133.3	3	150.0	400.0	5	250.0	666.7
0000_010	62.5	100.0	4	250.0	400.0	4	250.0	400.0
0000_011	50.0	100.0	4	200.0	400.0	5	250.0	500.0
0000_100	66.7	167.0	2	133.3	334.0	2.5	166.7	417.5
0000_101	66.7	167.0	2	133.3	334.0	3	200.0	501.0
0000_110	66.7	160.0	2.5	166.7	400.0	2.5	166.7	400.0
0000_111	55.5	160.0	2.5	138.7	400.0	3	166.7	480.0
Full Configuration Modes								
0001_000	66.7	167.0	2	133.3	334.0	4	266.7	668.0
0001_001	66.7	167.0	2	133.3	334.0	5	333.3	835.0
0001_010	66.7	167.0	2	133.3	334.0	6	396.0	1002.0
0001_011	Reserved							
0001_100	Reserved							
0001_101	62.5	133.3	3	187.5	400.0	4	250.0	533.3
0001_110	50.0	133.3	3	150.0	400.0	5	250.0	666.7
1000_111	45.5	133.3	3	136.4	400.0	5.5	250.0	733.3
0001_111	44.3	133.3	3	133.3	400.0	6	266.7	800.0
0010_000	Reserved							
0010_001	Reserved							



Table 15. Clock Configurations for Local Bus Mode<sup>1</sup> (Continued)

Mode <sup>2</sup>	Bus Clock <sup>3</sup> (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)	
	low	high		low	high		low	high
MODCK_H-MODCK[1-3]								
0010_010	62.5	100.0	4	250.0	400.0	4	250.0	400.0
0010_011	50.0	100.0	4	200.0	400.0	5	250.0	500.0
0010_100	41.7	100.0	4	166.7	400.0	6	250.0	600.0
0010_101	35.7	100.0	4	142.9	400.0	7	250.0	700.0
0010_110	33.3	100.0	4	133.3	400.0	8	266.7	800.0
0010_111	Reserved							
0011_000	50.0	80.0	5	250.0	400.0	5	250.0	400.0
0011_001	41.7	80.0	5	208.3	400.0	6	250.0	480.0
0011_010	35.7	80.0	5	178.6	400.0	7	250.0	560.0
0011_011	31.3	80.0	5	156.3	400.0	8	250.0	640.0
0011_100	Reserved							
0011_101	Reserved							
0011_110	41.7	66.7	6	250.0	400.0	6	250.0	400.0
0011_111	35.7	66.7	6	214.3	400.0	7	250.0	466.7
0100_000	31.3	66.7	6	187.5	400.0	8	250.0	533.3
0101_101	83.3	167.0	2	166.7	334.0	2	166.7	334.0
0101_110	66.7	167.0	2	133.3	334.0	2.5	166.7	417.5
0101_111	66.7	167.0	2	133.3	334.0	3	200.0	501.0
0110_000	71.4	167.0	2	142.9	334.0	3.5	250.0	584.5
0110_001	62.5	167.0	2	125.0	334.0	4	250.0	668.0
0110_010	55.6	167.0	2	111.1	334.0	4.5	250.0	751.5
0110_011	Reserved							
0110_100	66.7	160.0	2.5	166.7	400.0	2.5	166.7	400.0
0110_101	55.5	160.0	2.5	138.7	400.0	3	166.7	480.0
0110_110	71.4	160.0	2.5	133.0	400.0	3.5	250.0	560.0
0110_111	62.5	160.0	2.5	133.0.3	400.0	4	250.0	640.0
0111_000	55.6	160.0	2.5	133.0	400.0	4.5	250.0	720.0
0111_001	Reserved							
0111_010	Reserved							

Table 15. Clock Configurations for Local Bus Mode<sup>1</sup> (Continued)

Mode <sup>2</sup>	Bus Clock <sup>3</sup> (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)	
	low	high		low	high		low	high
0111_011	55.5	133.3	3	166.7	400.0	3	166.7	400.0
0111_100	71.4	133.3	3	133.0	400.0	3.5	250.0	466.7
0111_101	62.5	133.3	3	133.0	400.0	4	250.0	533.3
0111_110	55.6	133.3	3	133.0	400.0	4.5	250.0	600.0
0111_111	Reserved							
1000_000	Reserved							
1000_001	Reserved							
1000_010	71.4	114.3	3.5	250.0	400.0	3.5	250.0	400.0
1000_011	62.5	114.3	3.5	218.8	400.0	4	250.0	457.1
1000_100	55.6	114.3	3.5	194.4	400.0	4.5	250.0	514.3
1000_101	50.0	114.3	3.5	175.0	400.0	5	250.0	571.4
1000_110	45.5	114.3	3.5	159.1	400.0	5.5	250.0	628.6
1100_000	Reserved							
1100_001	Reserved							
1100_010	Reserved							
1101_000	Reserved							

<sup>1</sup> “Low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency guarantees the required minimum CPU operating frequency. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor  $\leq 3$ , the minimum CPU frequency is 166 MHz. The minimum CPM frequency is 133 MHz. For modes with a CPU multiplication factor  $\geq 3.5$ , the minimum CPU frequency is 250 MHz. The minimum CPM frequency is as shown in the table. “High” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

<sup>2</sup> MODCK\_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

<sup>3</sup> 60x and local bus frequency. Identical to CLKIN.

<sup>4</sup> CPM multiplication factor = CPM clock/bus clock

<sup>5</sup> CPU multiplication factor = Core PLL multiplication factor

## 7.2 PCI Host Mode

Table 16 and Table 17 show clock configurations for PCI host mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. In addition, note the following:

**NOTE: PCI\_MODCK**

In PCI mode only, PCI\_MODCK comes from the LGPL5 pin and MODCK\_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

**NOTE: Tval (Output Hold)**

The minimum Tval = 2 when PCI\_MODCK = 1, and the minimum Tval = 1 when PCI\_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

**Table 16. Clock Configurations for PCI Host Mode (PCI\_MODCK=0)<sup>1,2</sup>**

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
Default Modes (MODCK_H=0000)											
0000_000	66.7	66.7	2	133.3	133.3	2.5	166.7	166.7	2	66.7	66.7
0000_001	66.7	66.7	2	133.3	133.3	3	200.0	200.0	2	66.7	66.7
0000_010	55.5	80.0	2.5	150.0	200.0	3	166.7	240.0	3	50.0	66.7
0000_011	71.4	80.0	2.5	178.6	200.0	3.5	250.0	280.0	3	59.5	66.7
0000_100	62.5	80.0	2.5	156.3	200.0	4	250.0	320.0	3	52.1	66.7
0000_101	55.5	66.7	3	166.7	200.0	3	166.7	200.0	3	55.5	66.7
0000_110	PCI host mode (PCI_MODCK=1) only (refer to Table 17)										
0000_111	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
Full Configuration Modes											
0001_000	50.0	66.7	3	150.0	200.0	5	250.0	333.3	3	50.0	66.7
0001_001	50.0	66.7	3	150.0	200.0	6	300.0	400.0	3	50.0	66.7
0001_010	50.0	66.7	3	150.0	200.0	7	350.0	466.6	3	50.0	66.7
0001_011	50.0	66.7	3	150.0	200.0	8	400.0	533.3	3	50.0	66.7
0010_000	50.0	66.7	4	200.0	266.6	5	250.0	333.3	4	50.0	66.7
0010_001	50.0	66.7	4	200.0	266.6	6	300.0	400.0	4	50.0	66.7
0010_010	50.0	66.7	4	200.0	266.6	7	350.0	466.6	4	50.0	66.7
0010_011	50.0	66.7	4	200.0	266.6	8	400.0	533.3	4	50.0	66.7
0010_100	75.0	100.0	4	300.0	400.0	5	375.0	500.0	6	50.0	66.7
0010_101	75.0	100.0	4	300.0	400.0	5.5	412.5	549.9	6	50.0	66.7
0010_110	75.0	100.0	4	300.0	400.0	6	450.0	599.9	6	50.0	66.7
0011_000	50.0	66.7	5	250.0	333.3	5	250.0	333.3	5	50.0	66.7

## Clock Configuration Modes

**Table 16. Clock Configurations for PCI Host Mode (PCI\_MODCK=0)<sup>1,2</sup> (Continued)**

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
0011_001	50.0	66.7	5	250.0	333.3	6	300.0	400.0	5	50.0	66.7
0011_010	50.0	66.7	5	250.0	333.3	7	350.0	466.6	5	50.0	66.7
0011_011	50.0	66.7	5	250.0	333.3	8	400.0	533.3	5	50.0	66.7
0100_000	Reserved										
0100_001	50.0	66.7	6	300.0	400.0	6	300.0	400.0	6	50.0	66.7
0100_010	50.0	66.7	6	300.0	400.0	7	350.0	466.6	6	50.0	66.7
0100_011	50.0	66.7	6	300.0	400.0	8	400.0	533.3	6	50.0	66.7
0101_000	66.7	66.7	2	133.3	133.3	2.5	166.7	166.7	2	66.7	66.7
0101_001	66.7	66.7	2	133.3	133.3	3	200.0	200.0	2	66.7	66.7
0101_010	PCI host mode (PCI_MODCK=1) only (refer to Table 17)										
0101_011	66.7	66.7	2	133.3	133.3	4	266.7	266.6	2	66.7	66.7
0101_100	66.7	66.7	2	133.3	133.3	4.5	300.0	300.0	2	66.7	66.7
0110_000	66.7	80.0	2.5	166.7	200.0	2.5	166.7	200.0	3	55.5	66.7
0110_001	60.0	80.0	2.5	150.0	200.0	3	180.0	240.0	3	50.0	66.7
0110_010	71.4	80.0	2.5	178.6	200.0	3.5	250.0	280.0	3	59.5	66.7
0110_011	62.5	80.0	2.5	156.3	200.0	4	250.0	320.0	3	52.1	66.7
0110_100	60.0	80.0	2.5	150.0	200.0	4.5	270.0	360.0	3	50.0	66.7
0110_101	60.0	80.0	2.5	150.0	200.0	5	300.0	400.0	3	50.0	66.7
0110_110	60.0	80.0	2.5	150.0	200.0	6	360.0	480.0	3	50.0	66.7
0111_000	Reserved										
0111_001	55.5	66.7	3	166.7	200.0	3	166.7	200.0	3	55.5	66.7
0111_010	PCI host mode (PCI_MODCK=1) only (refer to Table 17)										
0111_011	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
0111_100	55.6	66.7	3	166.7	200.0	4.5	250.0	300.0	3	55.6	66.7
1000_000	Reserved										
1000_001	66.7	88.9	3	200.0	266.6	3	200.0	266.6	4	50.0	66.7
1000_010	71.4	88.9	3	214.3	266.6	3.5	250.0	311.1	4	53.6	66.7
1000_011	66.7	88.9	3	200.0	266.6	4	266.7	355.5	4	50.0	66.7

Table 16. Clock Configurations for PCI Host Mode (PCI\_MODCK=0)<sup>1,2</sup> (Continued)

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H- MODCK[1-3]											
1000_100	66.7	88.9	3	200.0	266.6	4.5	300.0	400.0	4	50.0	66.7
1000_101	66.7	88.9	3	200.0	266.6	6	400.0	533.3	4	50.0	66.7
1000_110	66.7	88.9	3	200.0	266.6	6.5	433.3	577.7	4	50.0	66.7
1001_000	66.7	76.2	3.5	233.3	266.6	2.5	166.7	190.5	4	58.3	66.7
1001_001	57.1	76.2	3.5	200.0	266.6	3	171.4	228.5	4	50.0	66.7
1001_010	71.4	76.2	3.5	250.0	266.6	3.5	250.0	266.6	4	62.5	66.7
1001_011	62.5	76.2	3.5	218.8	266.6	4	250.0	304.7	4	54.7	66.7
1001_100	57.1	76.2	3.5	200.0	266.6	4.5	257.1	342.8	4	50.0	66.7
1001_101	85.7	114.3	3.5	300.0	400.0	5	428.6	571.4	6	50.0	66.7
1001_110	85.7	114.3	3.5	300.0	400.0	5.5	471.4	628.5	6	50.0	66.7
1001_111	85.7	114.3	3.5	300.0	400.0	6	514.3	685.6	6	50.0	66.7
1010_000	83.4	100.0	2	166.7	200.0	2	166.7	200.0	3	55.5	66.7
1010_001	75.0	100.0	2	150.0	200.0	2.5	187.5	250.0	3	50.0	66.7
1010_010	75.0	100.0	2	150.0	200.0	3	225.0	300.0	3	50.0	66.7
1010_011	75.0	100.0	2	150.0	200.0	3.5	262.5	350.0	3	50.0	66.7
1010_100	75.0	100.0	2	150.0	200.0	4	300.0	400.0	3	50.0	66.7
1011_000	Reserved										
1011_001	80.0	106.7	2.5	200.0	266.6	2.5	200.0	266.6	4	50.0	66.7
1011_010	80.0	106.7	2.5	200.0	266.6	3	240.0	320.0	4	50.0	66.7
1011_011	80.0	106.7	2.5	200.0	266.6	3.5	280.0	373.3	4	50.0	66.7
1011_100	80.0	106.7	2.5	200.0	266.6	4	320.0	426.6	4	50.0	66.7
1011_101	80.0	106.7	2.5	200.0	266.6	4.5	360.0	480.0	4	50.0	66.7
1101_000	100.0	133.3	2.5	250.0	333.3	3	300.0	400.0	5	50.0	66.7
1101_001	100.0	133.3	2.5	250.0	333.3	3.5	350.0	466.6	5	50.0	66.7
1101_010	100.0	133.3	2.5	250.0	333.3	4	400.0	533.3	5	50.0	66.7
1101_011	100.0	133.3	2.5	250.0	333.3	4.5	450.0	599.9	5	50.0	66.7
1101_100	100.0	133.3	2.5	250.0	333.3	5	500.0	666.6	5	50.0	66.7

## Clock Configuration Modes

**Table 16. Clock Configurations for PCI Host Mode (PCI\_MODCK=0)<sup>1,2</sup> (Continued)**

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
	low	high		low	high		low	high		low	high
1101_101	125.0	166.7	2	250.0	333.3	3	375.0	500.0	5	50.0	66.7
1101_110	125.0	166.7	2	250.0	333.3	4	500.0	666.6	5	50.0	66.7
1110_000	100.0	133.3	3	300.0	400.0	3.5	350.0	466.6	6	50.0	66.7
1110_001	100.0	133.3	3	300.0	400.0	4	400.0	533.3	6	50.0	66.7
1110_010	100.0	133.3	3	300.0	400.0	4.5	450.0	599.9	6	50.0	66.7
1110_011	100.0	133.3	3	300.0	400.0	5	500.0	666.6	6	50.0	66.7
1110_100	100.0	133.3	3	300.0	400.0	5.5	550.0	733.3	6	50.0	66.7
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

<sup>1</sup> “Low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency guarantees the required minimum CPU operating frequency. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor  $\leq 3$ , the minimum CPU frequency is 166 MHz. The minimum CPM frequency is 133 MHz.

For modes with a CPU multiplication factor  $\geq 3.5$ , the minimum CPU frequency is 250 MHz. The minimum CPM frequency is as shown in the table.

“High” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

<sup>2</sup> As Table 14 shows, PCI\_MODCK determines the PCI clock frequency range. Refer to Table 17 for lower configurations.

<sup>3</sup> MODCK\_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

<sup>4</sup> 60x and local bus frequency. Identical to CLKIN.

<sup>5</sup> CPM multiplication factor = CPM clock/bus clock

<sup>6</sup> CPU multiplication factor = Core PLL multiplication factor

**Table 17. Clock Configurations for PCI Host Mode (PCI\_MODCK=1)<sup>1,2</sup>**

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
Default Modes (MODCK_H=0000)											
0000_000	66.7	100.0	2	133.3	200.0	2.5	166.7	250.0	4	33.3	50.0
0000_001	66.7	100.0	2	133.3	200.0	3	200.0	300.0	4	33.3	50.0
0000_010	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0000_011	71.4	120.0	2.5	178.6	300.0	3.5	250.0	420.0	6	29.8	50.0
0000_100	62.5	120.0	2.5	156.3	300.0	4	250.0	480.0	6	26.0	50.0

Table 17. Clock Configurations for PCI Host Mode (PCI\_MODCK=1)<sup>1,2</sup> (Continued)

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
0000_101	55.5	100.0	3	166.7	300.0	3	166.7	300.0	6	27.8	50.0
0000_110	71.4	100.0	3	214.3	300.0	3.5	250.0	350.0	6	35.7	50.0
0000_111	62.5	100.0	3	187.5	300.0	4	250.0	400.0	6	31.3	50.0
Full Configuration Modes											
0001_000	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
0001_001	50.0	100.0	3	150.0	300.0	6	300.0	600.0	6	25.0	50.0
0001_010	50.0	100.0	3	150.0	300.0	7	350.0	700.0	6	25.0	50.0
0001_011	50.0	100.0	3	150.0	300.0	8	400.0	800.0	6	25.0	50.0
0010_000	50.0	100.0	4	200.0	400.0	5	250.0	500.0	8	25.0	50.0
0010_001	50.0	100.0	4	200.0	400.0	6	300.0	600.0	8	25.0	50.0
0010_010	50.0	100.0	4	200.0	400.0	7	350.0	700.0	8	25.0	50.0
0010_011	50.0	100.0	4	200.0	400.0	8	400.0	800.0	8	25.0	50.0
0010_100	50.0	75.0	4	200.0	300.0	5	250.0	375.0	6	33.3	50.0
0010_101	45.5	75.0	4	181.8	300.0	5.5	250.0	412.5	6	30.3	50.0
0010_110	41.7	75.0	4	166.7	300.0	6	250.0	450.0	6	27.8	50.0
0011_000	50.0	50.0	5	250.0	250.0	5	250.0	250.0	5	50.0	50.0
0011_001	41.7	50.0	5	208.3	250.0	6	250.0	300.0	5	41.7	50.0
0011_010	35.7	50.0	5	178.6	250.0	7	250.0	350.0	5	35.7	50.0
0011_011	31.3	50.0	5	156.3	250.0	8	250.0	400.0	5	31.3	50.0
0100_000	Reserved										
0100_001	41.7	50.0	6	250.0	300.0	6	250.0	300.0	6	41.7	50.0
0100_010	35.7	50.0	6	214.3	300.0	7	250.0	350.0	6	35.7	50.0
0100_011	31.3	50.0	6	187.5	300.0	8	250.0	400.0	6	31.3	50.0
0101_000	66.7	100.0	2	133.3	200.0	2.5	166.7	250.0	4	33.3	50.0
0101_001	66.7	100.0	2	133.3	200.0	3	200.0	300.0	4	33.3	50.0
0101_010	71.4	100.0	2	142.9	200.0	3.5	250.0	350.0	4	35.7	50.0
0101_011	66.7	100.0	2	133.3	200.0	4	266.7	400.0	4	33.3	50.0
0101_100	66.7	100.0	2	133.3	200.0	4.5	300.0	450.0	4	33.3	50.0

## Clock Configuration Modes

**Table 17. Clock Configurations for PCI Host Mode (PCI\_MODCK=1)<sup>1,2</sup> (Continued)**

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
0110_000	66.7	120.0	2.5	166.7	300.0	2.5	166.7	300.0	6	27.8	50.0
0110_001	60.0	120.0	2.5	150.0	300.0	3	180.0	360.0	6	25.0	50.0
0110_010	71.4	120.0	2.5	178.6	300.0	3.5	250.0	420.0	6	29.8	50.0
0110_011	62.5	120.0	2.5	156.3	300.0	4	250.0	480.0	6	26.0	50.0
0110_100	60.0	120.0	2.5	150.0	300.0	4.5	270.0	540.0	6	25.0	50.0
0110_101	60.0	120.0	2.5	150.0	300.0	5	300.0	600.0	6	25.0	50.0
0110_110	60.0	120.0	2.5	150.0	300.0	6	360.0	720.0	6	25.0	50.0
0111_000	Reserved										
0111_001	55.5	100.0	3	166.7	300.0	3	166.7	300.0	6	27.8	50.0
0111_010	71.4	100.0	3	214.3	300.0	3.5	250.0	350.0	6	35.7	50.0
0111_011	62.5	100.0	3	187.5	300.0	4	250.0	400.0	6	31.3	50.0
0111_100	55.6	100.0	3	166.7	300.0	4.5	250.0	450.0	6	27.8	50.0
1000_000	Reserved										
1000_001	66.7	133.3	3	200.0	400.0	3	200.0	400.0	8	25.0	50.0
1000_010	71.4	133.3	3	214.3	400.0	3.5	250.0	466.7	8	26.8	50.0
1000_011	66.7	133.3	3	200.0	400.0	4	266.7	533.3	8	25.0	50.0
1000_100	66.7	133.3	3	200.0	400.0	4.5	300.0	600.0	8	25.0	50.0
1000_101	66.7	133.3	3	200.0	400.0	6	400.0	800.0	8	25.0	50.0
1000_110	66.7	133.3	3	200.0	400.0	6.5	433.3	866.7	8	25.0	50.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	71.4	114.3	3.5	250.0	400.0	3.5	250.0	400.0	8	31.3	50.0
1001_011	62.5	114.3	3.5	218.8	400.0	4	250.0	457.1	8	27.3	50.0
1001_100	57.1	114.3	3.5	200.0	400.0	4.5	257.1	514.3	8	25.0	50.0
1001_101	50.0	85.7	3.5	175.0	300.0	5	250.0	428.6	6	29.2	50.0
1001_110	45.5	85.7	3.5	159.1	300.0	5.5	250.0	471.4	6	26.5	50.0
1001_111	42.9	85.7	3.5	150.0	300.0	6	257.1	514.3	6	25.0	50.0



Table 17. Clock Configurations for PCI Host Mode (PCI\_MODCK=1)<sup>1,2</sup> (Continued)

Mode <sup>3</sup>	Bus Clock <sup>4</sup> (MHz)		CPM Multiplication Factor <sup>5</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>6</sup>	CPU Clock (MHz)		PCI Division Factor	PCI Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
1010_000	75.0	150.0	2	150.0	300.0	2	150.0	300.0	6	25.0	50.0
1010_001	75.0	150.0	2	150.0	300.0	2.5	187.5	375.0	6	25.0	50.0
1010_010	75.0	150.0	2	150.0	300.0	3	225.0	450.0	6	25.0	50.0
1010_011	75.0	150.0	2	150.0	300.0	3.5	262.5	525.0	6	25.0	50.0
1010_100	75.0	150.0	2	150.0	300.0	4	300.0	600.0	6	25.0	50.0
1011_000	Reserved										
1011_001	80.0	160.0	2.5	200.0	400.0	2.5	200.0	400.0	8	25.0	50.0
1011_010	80.0	160.0	2.5	200.0	400.0	3	240.0	480.0	8	25.0	50.0
1011_011	80.0	160.0	2.5	200.0	400.0	3.5	280.0	560.0	8	25.0	50.0
1011_100	80.0	160.0	2.5	200.0	400.0	4	320.0	640.0	8	25.0	50.0
1011_101	80.0	160.0	2.5	200.0	400.0	4.5	360.0	720.0	8	25.0	50.0
1101_000	55.5	100.0	2.5	138.5	250.0	3	166.7	300.0	5	27.8	50.0
1101_001	71.4	100.0	2.5	178.6	250.0	3.5	250.0	350.0	5	35.7	50.0
1101_010	62.5	100.0	2.5	156.3	250.0	4	250.0	400.0	5	31.3	50.0
1101_011	55.6	100.0	2.5	138.9	250.0	4.5	250.0	450.0	5	27.8	50.0
1101_100	50.0	100.0	2.5	125.0	250.0	5	250.0	500.0	5	25.0	50.0
1101_101	66.7	125.0	2	133.3	250.0	3	200.0	375.0	5	26.6	50.0
1101_110	66.7	125.0	2	133.3	250.0	4	266.7	500.0	5	26.6	50.0
1110_000	71.4	100.0	3	214.3	300.0	3.5	250.0	350.0	6	35.7	50.0
1110_001	62.5	100.0	3	187.5	300.0	4	250.0	400.0	6	31.3	50.0
1110_010	55.6	100.0	3	166.7	300.0	4.5	250.0	450.0	6	27.8	50.0
1110_011	50.0	100.0	3	150.0	300.0	5	250.0	500.0	6	25.0	50.0
1110_100	50.0	100.0	3	150.0	300.0	5.5	275.0	550.0	6	25.0	50.0
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

## Clock Configuration Modes

- <sup>1</sup> “Low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency guarantees the required minimum CPU operating frequency. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor  $\leq 3$ , the minimum CPU frequency is 166 MHz. The minimum CPM frequency is 133 MHz. For modes with a CPU multiplication factor  $\geq 3.5$ , the minimum CPU frequency is 250 MHz. The minimum CPM frequency is as shown in the table. “High” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.
- <sup>2</sup> As Table 14 shows, PCI\_MODCK determines the PCI clock frequency range. Refer to Table 16 for higher configurations.
- <sup>3</sup> MODCK\_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
- <sup>4</sup> 60x and local bus frequency. Identical to CLKIN.
- <sup>5</sup> CPM multiplication factor = CPM clock/bus clock
- <sup>6</sup> CPU multiplication factor = Core PLL multiplication factor

## 7.3 PCI Agent Mode

Table 18 and Table 19 show configurations for PCI agent mode. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device. In addition, note the following:

### NOTE: PCI\_MODCK

In PCI mode only, PCI\_MODCK comes from the LGPL5 pin and MODCK\_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

### NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI\_MODCK = 1, and the minimum Tval = 1 when PCI\_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

**Table 18. Clock Configurations for PCI Agent Mode (PCI\_MODCK=0)<sup>1,2</sup>**

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H- MODCK[1-3]	low	high		low	high		low	high		low	high
Default Modes (MODCK_H=0000											
0000_000	66.7	66.7	2	133.3	133.3	2.5	166.7	166.7	2	66.7	66.7
0000_001	66.7	66.7	2	133.3	133.3	3	200.0	200.0	2	66.7	66.7
0000_010	55.5	66.7	3	166.7	200.0	3	166.7	200.0	3	55.5	66.7
0000_011	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
0000_100	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0000_101	59.5	66.7	3	178.6	200.0	3.5	250.0	280.0	2.5	71.4	80.0
0000_110	53.6	66.7	4	214.3	266.6	3.5	250.0	311.1	3	71.4	88.9
0000_111	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
Full Configuration Modes											
0001_001	Reserved										

Table 18. Clock Configurations for PCI Agent Mode (PCI\_MODCK=0)<sup>1,2</sup> (Continued)

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	low	high		low	high		low	high		low	high
0001_010	Reserved										
0001_011	Reserved										
0001_100	66.7	66.7	2	133.3	133.3	8	266.6	266.6	4	33.3	33.3
0010_001	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
0010_010	59.5	66.7	3	178.6	200.0	3.5	250.0	280.0	2.5	71.4	80.0
0010_011	52.1	66.7	3	156.3	200.0	4	250.0	320.0	2.5	62.5	80.0
0010_100	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0
0011_000	Reserved										
0011_001	Reserved										
0011_010	Reserved										
0011_011	Reserved										
0011_100	Reserved										
0100_000	Reserved										
0100_001	50.0	66.7	3	166.7	200.0	3	166.7	200.0	3	66.7	66.7
0100_010	Reserved										
0100_011	62.5	66.7	3	187.5	200.0	4	250.0	266.6	3	62.5	66.7
0100_100	55.6	66.7	3	166.7	200.0	4.5	250.0	300.0	3	55.6	66.7
0101_000	50.0	66.7	5	250.0	333.3	2.5	250.0	333.3	2.5	100.0	133.3
0101_001	50.0	66.7	5	250.0	333.3	3	300.0	400.0	2.5	100.0	133.3
0101_010	50.0	66.7	5	250.0	333.3	3.5	350.0	466.6	2.5	100.0	133.3
0101_011	50.0	66.7	5	250.0	333.3	4	400.0	533.3	2.5	100.0	133.3
0101_100	50.0	66.7	5	250.0	333.3	4.5	450.0	599.9	2.5	100.0	133.3
0101_101	50.0	66.7	5	250.0	333.3	5	500.0	666.6	2.5	100.0	133.3
0101_110	50.0	66.7	5	250.0	333.3	5.5	550.0	733.3	2.5	100.0	133.3
0110_000	Reserved										
0110_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
0110_010	53.6	66.7	4	214.3	266.6	3.5	250.0	311.1	3	71.4	88.9
0110_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9

## Clock Configuration Modes

**Table 18. Clock Configurations for PCI Agent Mode (PCI\_MODCK=0)<sup>1,2</sup> (Continued)**

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	low	high		low	high		low	high		low	high
0110_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
0111_000	55.5	66.7	3	166.7	200.0	2	166.7	200.0	2	83.3	100.0
0111_001	50.0	66.7	3	150.0	200.0	2.5	187.5	250.0	2	75.0	100.0
0111_010	50.0	66.7	3	150.0	200.0	3	225.0	300.0	2	75.0	100.0
0111_011	50.0	66.7	3	150.0	200.0	3.5	262.5	350.0	2	75.0	100.0
1000_000	Reserved										
1000_001	66.7	66.7	3	200.0	200.0	2.5	166.7	166.7	2.5	80.0	80.0
1000_010	50.0	66.7	3	150.0	200.0	3	180.0	240.0	2.5	60.0	80.0
1000_011	59.5	66.7	3	178.6	200.0	3.5	250.0	280.0	2.5	71.4	80.0
1000_100	52.1	66.7	3	156.3	200.0	4	250.0	320.0	2.5	62.5	80.0
1000_101	50.0	66.7	3	150.0	200.0	4.5	270.0	360.0	2.5	60.0	80.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	62.5	66.7	4	250.0	266.6	4	250.0	266.6	4	62.5	66.7
1001_100	55.6	66.7	4	222.2	266.6	4.5	250.0	300.0	4	55.6	66.7
1010_000	Reserved										
1010_001	50.0	66.7	4	200.0	266.6	3	200.0	266.6	3	66.7	88.9
1010_010	53.6	66.7	4	214.3	266.6	3.5	250.0	311.1	3	71.4	88.9
1010_011	50.0	66.7	4	200.0	266.6	4	266.7	355.5	3	66.7	88.9
1010_100	50.0	66.7	4	200.0	266.6	4.5	300.0	400.0	3	66.7	88.9
1011_000	Reserved										
1011_001	50.0	66.7	4	200.0	266.6	2.5	200.0	266.6	2.5	80.0	106.7
1011_010	50.0	66.7	4	200.0	266.6	3	240.0	320.0	2.5	80.0	106.7
1011_011	50.0	66.7	4	200.0	266.6	3.5	280.0	373.3	2.5	80.0	106.7
1011_100	50.0	66.7	4	200.0	266.6	4	320.0	426.6	2.5	80.0	106.7
1100_101	50.0	66.7	6	300.0	400.0	4	400.0	533.3	3	100.0	133.3

Table 18. Clock Configurations for PCI Agent Mode (PCI\_MODCK=0)<sup>1,2</sup> (Continued)

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	low	high		low	high		low	high		low	high
MODCK_H-MODCK[1-3]											
1100_110	50.0	66.7	6	300.0	400.0	4.5	450.0	599.9	3	100.0	133.3
1100_111	50.0	66.7	6	300.0	400.0	5	500.0	666.6	3	100.0	133.3
1101_000	50.0	66.7	6	300.0	400.0	5.5	550.0	733.3	3	100.0	133.3
1101_001	50.0	66.7	6	300.0	400.0	3.5	420.0	559.9	2.5	120.0	160.0
1101_010	50.0	66.7	6	300.0	400.0	4	480.0	639.9	2.5	120.0	160.0
1101_011	50.0	66.7	6	300.0	400.0	4.5	540.0	719.9	2.5	120.0	160.0
1101_100	50.0	66.7	6	300.0	400.0	5	600.0	799.9	2.5	120.0	160.0
1110_000	50.0	66.7	5	250.0	333.3	2.5	312.5	416.6	2	125.0	166.7
1110_001	50.0	66.7	5	250.0	333.3	3	375.0	500.0	2	125.0	166.7
1110_010	50.0	66.7	5	250.0	333.3	3.5	437.5	583.3	2	125.0	166.7
1110_011	50.0	66.7	5	250.0	333.3	4	500.0	666.6	2	125.0	166.7
1110_100	50.0	66.7	5	250.0	333.3	4	333.3	444.4	3	83.3	111.1
1110_101	50.0	66.7	5	250.0	333.3	4.5	375.0	500.0	3	83.3	111.1
1110_110	50.0	66.7	5	250.0	333.3	5	416.7	555.5	3	83.3	111.1
1110_111	50.0	66.7	5	250.0	333.3	5.5	458.3	611.1	3	83.3	111.1
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										

<sup>1</sup> “Low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency guarantees the required minimum CPU operating frequency. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor  $\leq 3$ , the minimum CPU frequency is 166 MHz. The minimum CPM frequency is 133 MHz.

For modes with a CPU multiplication factor  $\geq 3.5$ , the minimum CPU frequency is 250 MHz. The minimum CPM frequency is as shown in the table.

“High” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

<sup>2</sup> As shown in Table 14, PCI\_MODCK determines the PCI clock frequency range. Refer to Table 19 for lower configurations.

<sup>3</sup> MODCK\_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.

<sup>4</sup> CPM multiplication factor = CPM clock/PCI clock

<sup>5</sup> CPU multiplication factor = Core PLL multiplication factor

## Clock Configuration Modes

**Table 19. Clock Configurations for PCI Agent Mode (PCI\_MODCK=1)<sup>1,2</sup>**

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
MODCK_H-MODCK[1-3]	low	high		low	high		low	high		low	high
Default Modes (MODCK_H=0000)											
0000_000	33.3	50.0	4	133.3	200.0	2.5	166.7	250.0	2	66.7	100.0
0000_001	33.3	50.0	4	133.3	200.0	3	200.0	300.0	2	66.7	100.0
0000_010	27.8	50.0	6	166.7	300.0	3	166.7	300.0	3	55.5	100.0
0000_011	31.3	50.0	6	187.5	300.0	4	250.0	400.0	3	62.5	100.0
0000_100	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0000_101	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
0000_110	26.8	50.0	8	214.3	400.0	3.5	250.0	466.7	3	71.4	133.3
0000_111	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
Full Configuration Modes											
0001_001	50.0	50.0	4	200.0	200.0	5	250.0	250.0	4	50.0	50.0
0001_010	41.7	50.0	4	166.7	200.0	6	250.0	300.0	4	41.7	50.0
0001_011	35.7	50.0	4	142.9	200.0	7	250.0	350.0	4	35.7	50.0
0001_100	33.3	50.0	4	133.3	200.0	8	266.7	400.0	4	33.3	50.0
0010_001	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
0010_010	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
0010_011	26.0	50.0	6	156.3	300.0	4	250.0	480.0	2.5	62.5	120.0
0010_100	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
0011_000	Reserved										
0011_001	50.0	50.0	4	200.0	200.0	2.5	166.7	166.7	3	66.7	66.7
0011_010	Reserved										
0011_011	46.9	50.0	4	187.5	200.0	4	250.0	266.7	3	62.5	66.7
0011_100	41.7	50.0	4	166.7	200.0	4.5	250.0	300.0	3	55.6	66.7
0100_000	Reserved										
0100_001	27.8	50.0	6	166.7	300.0	3	166.7	300.0	3	55.5	100.0
0100_010	35.7	50.0	6	214.3	300.0	3.5	250.0	350.0	3	71.4	100.0
0100_011	31.3	50.0	6	187.5	300.0	4	250.0	400.0	3	62.5	100.0
0100_100	27.8	50.0	6	166.7	300.0	4.5	250.0	450.0	3	55.6	100.0
0101_000	27.8	50.0	5	166.7	250.0	2.5	166.7	250.0	2.5	55.5	100.0

Table 19. Clock Configurations for PCI Agent Mode (PCI\_MODCK=1)<sup>1,2</sup> (Continued)

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	low	high		low	high		low	high		low	high
0101_001	27.8	50.0	5	139.0	250.0	3	167.7	300.0	2.5	55.5	100.0
0101_010	35.7	50.0	5	178.6	250.0	3.5	250.0	350.0	2.5	71.4	100.0
0101_011	31.3	50.0	5	156.3	250.0	4	250.0	400.0	2.5	62.5	100.0
0101_100	27.8	50.0	5	138.9	250.0	4.5	250.0	450.0	2.5	55.6	100.0
0101_101	27.8	50.0	5	133.3	250.0	5	266.7	500.0	2.5	55.5	100.0
0101_110	27.8	50.0	5	133.3	250.0	5.5	305.3	550.0	2.5	55.5	100.0
0110_000	Reserved										
0110_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3
0110_010	26.8	50.0	8	214.3	400.0	3.5	250.0	466.7	3	71.4	133.3
0110_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
0110_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
0111_000	41.6	50.0	6	166.7	300.0	2	166.7	300.0	2	83.2	150.0
0111_001	25.0	50.0	6	150.0	300.0	2.5	187.5	375.0	2	75.0	150.0
0111_010	25.0	50.0	6	150.0	300.0	3	225.0	450.0	2	75.0	150.0
0111_011	25.0	50.0	6	150.0	300.0	3.5	262.5	525.0	2	75.0	150.0
1000_000	Reserved										
1000_001	27.8	50.0	6	166.7	300.0	2.5	166.7	300.0	2.5	66.7	120.0
1000_010	25.0	50.0	6	150.0	300.0	3	180.0	360.0	2.5	60.0	120.0
1000_011	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
1000_100	26.0	50.0	6	156.3	300.0	4	250.0	480.0	2.5	62.5	120.0
1000_101	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1001_000	Reserved										
1001_001	Reserved										
1001_010	Reserved										
1001_011	31.3	50.0	8	250.0	400.0	4	250.0	400.0	4	62.5	100.0
1001_100	27.8	50.0	8	222.2	400.0	4.5	250.0	450.0	4	55.6	100.0
1010_000	Reserved										
1010_001	25.0	50.0	8	200.0	400.0	3	200.0	400.0	3	66.7	133.3

## Clock Configuration Modes

**Table 19. Clock Configurations for PCI Agent Mode (PCI\_MODCK=1)<sup>1,2</sup> (Continued)**

Mode <sup>3</sup>	PCI Clock (MHz)		CPM Multiplication Factor <sup>4</sup>	CPM Clock (MHz)		CPU Multiplication Factor <sup>5</sup>	CPU Clock (MHz)		Bus Division Factor	Bus Clock (MHz)	
	low	high		low	high		low	high		low	high
1010_010	26.8	50.0	8	214.3	400.0	3.5	250.0	466.7	3	71.4	133.3
1010_011	25.0	50.0	8	200.0	400.0	4	266.7	533.3	3	66.7	133.3
1010_100	25.0	50.0	8	200.0	400.0	4.5	300.0	600.0	3	66.7	133.3
1011_000	Reserved										
1011_001	25.0	50.0	8	200.0	400.0	2.5	200.0	400.0	2.5	80.0	160.0
1011_010	25.0	50.0	8	200.0	400.0	3	240.0	480.0	2.5	80.0	160.0
1011_011	25.0	50.0	8	200.0	400.0	3.5	280.0	560.0	2.5	80.0	160.0
1011_100	25.0	50.0	8	200.0	400.0	4	320.0	640.0	2.5	80.0	160.0
1100_101	31.3	50.0	6	187.5	300.0	4	250.0	400.0	3	62.5	100.0
1100_110	27.8	50.0	6	166.7	300.0	4.5	250.0	450.0	3	55.6	100.0
1100_111	25.0	50.0	6	150.0	300.0	5	250.0	500.0	3	50.0	100.0
1101_000	25.0	50.0	6	150.0	300.0	5.5	275.0	550.0	3	50.0	100.0
1101_001	29.8	50.0	6	178.6	300.0	3.5	250.0	420.0	2.5	71.4	120.0
1101_010	26.0	50.0	6	156.3	300.0	4	250.0	480.0	2.5	62.5	120.0
1101_011	25.0	50.0	6	150.0	300.0	4.5	270.0	540.0	2.5	60.0	120.0
1101_100	25.0	50.0	6	150.0	300.0	5	300.0	600.0	2.5	60.0	120.0
1110_000	33.3	50.0	5	133.3	250.0	2.5	166.7	312.5	2	66.7	125.0
1110_001	25.0	50.0	5	125.0	250.0	3	187.5	375.0	2	62.5	125.0
1110_010	28.6	50.0	5	142.9	250.0	3.5	250.0	437.5	2	71.4	125.0
1110_011	25.0	50.0	5	125.0	250.0	4	250.0	500.0	2	62.5	125.0
1110_100	37.5	50.0	5	187.5	250.0	4	250.0	333.3	3	62.5	83.3
1110_101	33.3	50.0	5	166.7	250.0	4.5	250.0	375.0	3	55.6	83.3
1110_110	30.0	50.0	5	150.0	250.0	5	250.0	416.7	3	50.0	83.3
1110_111	27.3	50.0	5	136.4	250.0	5.5	250.0	458.3	3	45.5	83.3
1100_000	Reserved										
1100_001	Reserved										
1100_010	Reserved										



- <sup>1</sup> “Low” values are the minimum allowable frequencies for a given clock mode. The minimum bus frequency guarantees the required minimum CPU operating frequency. Minimum CPU frequency is determined by the clock mode. For modes with a CPU multiplication factor  $\leq 3$ , the minimum CPU frequency is 166 MHz. The minimum CPM frequency is 133 MHz. For modes with a CPU multiplication factor  $\geq 3.5$ , the minimum CPU frequency is 250 MHz. The minimum CPM frequency is as shown in the table. “High” values are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.
- <sup>2</sup> As shown in Table 14, PCI\_MODCK determines the PCI clock range. Refer to Table 18 for higher range configurations.
- <sup>3</sup> MODCK\_H = hard reset configuration word [28–31]. MODCK[1-3] = three hardware configuration pins.
- <sup>4</sup> CPM multiplication factor = CPM clock/PCI clock
- <sup>5</sup> CPU multiplication factor = Core PLL multiplication factor

## 8 Pinout

This section provides the pin assignments and pinout lists for both HiP7 PowerQUICC II packages.

### 8.1 ZU Package—MPC8280 and MPC8270

The following figures and table represent the standard 480 TBGA package. For information on the alternate package, refer to Section 8.2, “VR and ZQ Packages—MPC8275 and MPC8270” on page 56.

Figure 13 shows the pinout of the ZU package as viewed from the top surface.

Pinout

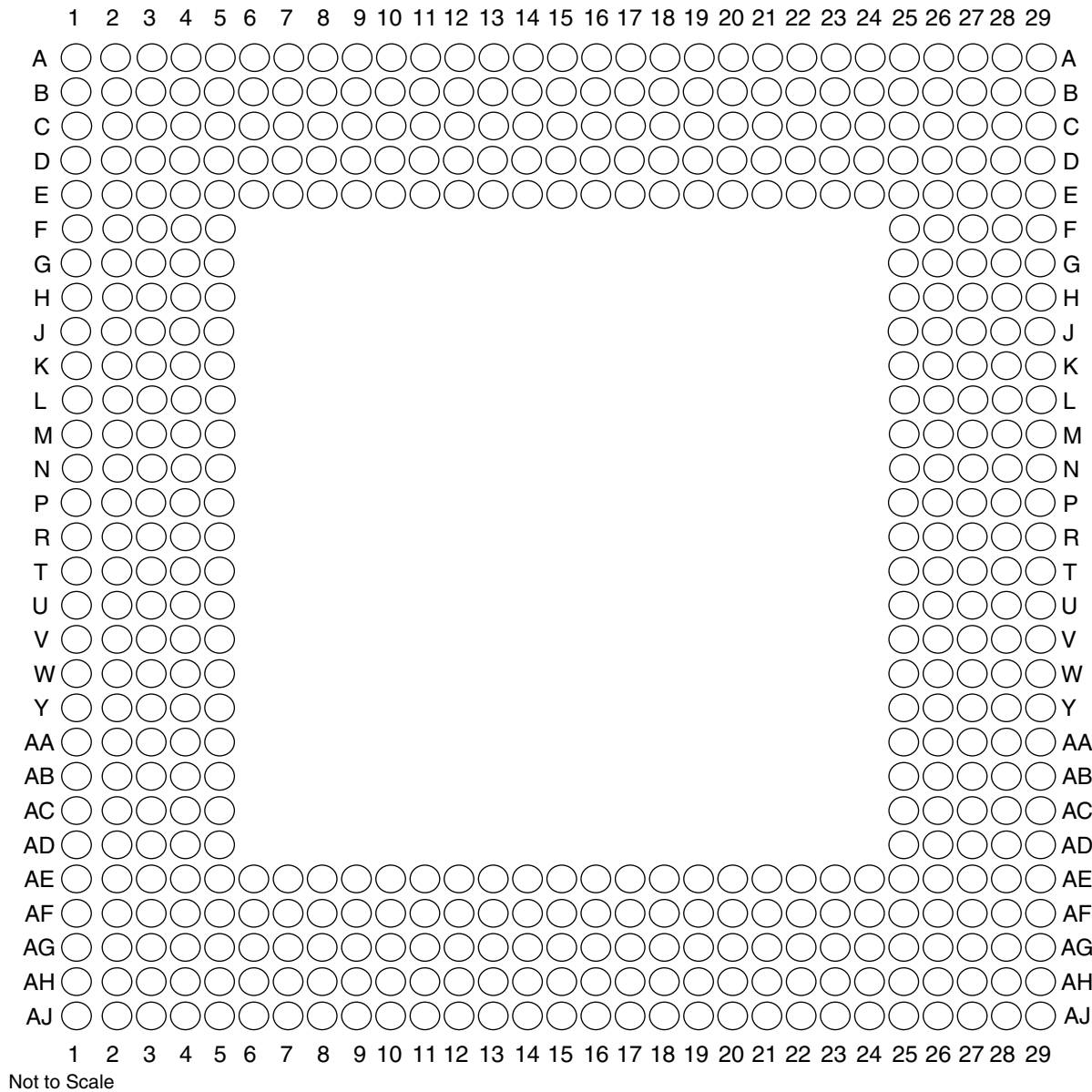


Figure 13. Pinout of the 480 TBGA Package (View from Top)

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

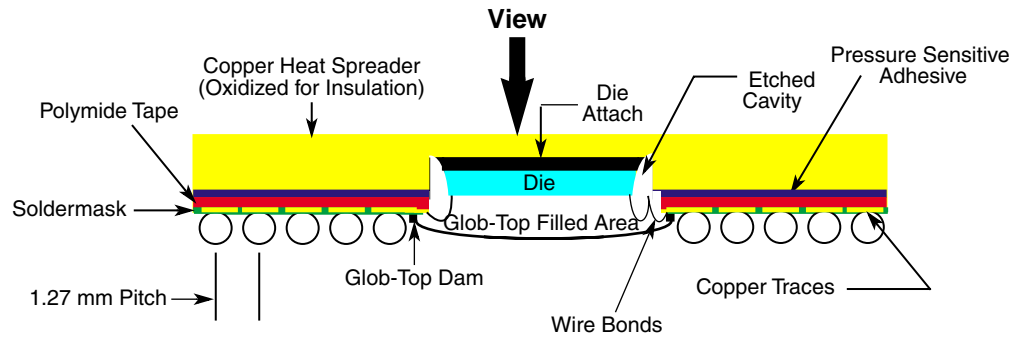


Figure 14. Side View of the TBGA Package

Table 20 shows the pinout list of the MPC8280 and MPC8270. Table 21 defines conventions and acronyms used in Table 20.

**Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List**

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
$\overline{\text{BR}}$		W5
$\overline{\text{BG}}$		F4
$\overline{\text{ABB/IRQ2}}$		E2
$\overline{\text{TS}}$		E3
A0		G1
A1		H5
A2		H2
A3		H1
A4		J5
A5		J4
A6		J3
A7		J2
A8		J1
A9		K4
A10		K3
A11		K2
A12		K1
A13		L5
A14		L4
A15		L3
A16		L2
A17		L1
A18		M5
A19		N5
A20		N4
A21		N3
A22		N2
A23		N1
A24		P4
A25		P3
A26		P2
A27		P1

## Pinout

**Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)**

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
A28		R1
A29		R3
A30		R5
A31		R4
TT0		F1
TT1		G4
TT2		G3
TT3		G2
TT4		F2
TBST		D3
TSIZ0		C1
TSIZ1		E4
TSIZ2		D2
TSIZ3		F5
AACK		F3
ARTRY		E1
DBG		V1
DBB/IRQ3		V2
D0		B20
D1		A18
D2		A16
D3		A13
D4		E12
D5		D9
D6		A6
D7		B5
D8		A20
D9		E17
D10		B15
D11		B13
D12		A11
D13		E9
D14		B7
D15		B4

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
D16		D19
D17		D17
D18		D15
D19		C13
D20		B11
D21		A8
D22		A5
D23		C5
D24		C19
D25		C17
D26		C15
D27		D13
D28		C11
D29		B8
D30		A4
D31		E6
D32		E18
D33		B17
D34		A15
D35		A12
D36		D11
D37		C8
D38		E7
D39		A3
D40		D18
D41		A17
D42		A14
D43		B12
D44		A10
D45		D8
D46		B6
D47		C4
D48		C18
D49		E16

## Pinout

**Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)**

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
D50		B14
D51		C12
D52		B10
D53		A7
D54		C6
D55		D5
D56		B18
D57		B16
D58		E14
D59		D12
D60		C10
D61		E8
D62		D6
D63		C2
DP0/RSRV/EXT_BR2		B22
IRQ1/DP1/EXT_BG2		A22
IRQ2/DP2/TLBISYNC/EXT_DBG2		E21
IRQ3/DP3/CKSTP_OUT/EXT_BR3		D21
IRQ4/DP4/CORE_SRESET/EXT_BG3		C21
IRQ5/CINT/DP5/TBEN/EXT_DBG3		B21
IRQ6/DP6/CSE0		A21
IRQ7/DP7/CSE1		E20
PSDVAL		V3
TA		C22
TEA		V5
GBL/IRQ1		W1
CI/BADDR29/IRQ2		U2
WT/BADDR30/IRQ3		U3
L2_HIT/IRQ4		Y4
CPU_BG/BADDR31/IRQ5/CINT		U4
CPU_DBG		R2
CPU_BR		Y3
CS0		F25
CS1		C29

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
CS2		E27
CS3		E28
CS4		F26
CS5		F27
CS6		F28
CS7		G25
CS8		D29
CS9		E29
CS10/BCTL1		F29
CS11/AP0		G28
BADDR27		T5
BADDR28		U1
ALE		T2
BCTL0		A27
PWE0/PSDDQM0/PBS0		C25
PWE1/PSDDQM1/PBS1		E24
PWE2/PSDDQM2/PBS2		D24
PWE3/PSDDQM3/PBS3		C24
PWE4/PSDDQM4/PBS4		B26
PWE5/PSDDQM5/PBS5		A26
PWE6/PSDDQM6/PBS6		B25
PWE7/PSDDQM7/PBS7		A25
PSDA10/PGPL0		E23
PSDWE/PGPL1		B24
POE/PSDRAS/PGPL2		A24
PSDCAS/PGPL3		B23
PGTA/PUPMWAIT/PGPL4/PPBS		A23
PSDAMUX/PGPL5		D22
LWE0/LSDDQM0/LBS0/PCI_CFG0		H28
LWE1/LSDDQM1/LBS1/PCI_CFG1		H27
LWE2/LSDDQM2/LBS2/PCI_CFG2		H26
LWE3/LSDDQM3/LBS3/PCI_CFG3		G29
LSDA10/LGPL0/PCI_MODCKH0		D27
LSDWE/LGPL1/PCI_MODCKH1		C28

## Pinout

**Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)**

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LOE/LSDRAS/LGPL2/PCI_MODCKH2		E26
LSDCAS/LGPL3/PCI_MODCKH3		D25
LGTA/LUPMWAIT/LGPL4/LPBS		C26
LGPL5/LSDAMUX/PCI_MODCK		B27
LWR		D28
L_A14/PAR		N27
L_A15/FRAME/SMI		T29
L_A16/TRDY		R27
L_A17/IRDY/CKSTP_OUT		R26
L_A18/STOP		R29
L_A19/DEVSEL		R28
L_A20/IDSEL		W29
L_A21/PERR		P28
L_A22/SERR		N26
L_A23/REQ0		AA27
L_A24/REQ1/HSEJSW		P29
L_A25/GNT0		AA26
L_A26/GNT1/HSELED		N25
L_A27/GNT2/HSENUM		AA25
L_A28/RST/CORE_SRESET		AB29
L_A29/INTA		AB28
L_A30/REQ2		P25
L_A31/DLLOUT		AB27
LCL_D0/AD0		H29
LCL_D1/AD1		J29
LCL_D2/AD2		J28
LCL_D3/AD3		J27
LCL_D4/AD4		J26
LCL_D5/AD5		J25
LCL_D6/AD6		K25
LCL_D7/AD7		L29
LCL_D8/AD8		L27
LCL_D9/AD9		L26
LCL_D10/AD10		L25



Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
LCL_D11/AD11		M29
LCL_D12/AD12		M28
LCL_D13/AD13		M27
LCL_D14/AD14		M26
LCL_D15/AD15		N29
LCL_D16/AD16		T25
LCL_D17/AD17		U27
LCL_D18/AD18		U26
LCL_D19/AD19		U25
LCL_D20/AD20		V29
LCL_D21/AD21		V28
LCL_D22/AD22		V27
LCL_D23/AD23		V26
LCL_D24/AD24		W27
LCL_D25/AD25		W26
LCL_D26/AD26		W25
LCL_D27/AD27		Y29
LCL_D28/AD28		Y28
LCL_D29/AD29		Y25
LCL_D30/AD30		AA29
LCL_D31/AD31		AA28
LCL_DP0/C0/BE $\overline{0}$		L28
LCL_DP1/C1/BE $\overline{1}$		N28
LCL_DP2/C2/BE $\overline{2}$		T28
LCL_DP3/C3/BE $\overline{3}$		W28
IRQ0/NMI_OUT		T1
IRQ7/INT_OUT/APE		D1
TRST <sup>1</sup>		AH3
TCK		AG5
TMS		AJ3
TDI		AE6
TDO		AF5
TRIS		AB4
PORESET <sup>1</sup>		AG6

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
HRESET		AH5
SRESET		AF6
QREQ		AA3
RSTCONF		AJ4
MODCK1/AP1/TC0/BNKSEL0		W2
MODCK2/AP2/TC1/BNKSEL1		W3
MODCK3/AP3/TC2/BNKSEL2		W4
CLKIN1		AH4
PA0/RESTART1/DREQ3	FCC2_UTM_TXADDR2	AC29 <sup>2</sup>
PA1/REJECT1/DONE3	FCC2_UTM_TXADDR1	AC25 <sup>2</sup>
PA2/CLK20/DACK3	FCC2_UTM_TXADDR0	AE28 <sup>2</sup>
PA3/CLK19/DACK4/L1RXD1A2	FCC2_UTM_RXADDR0	AG29 <sup>2</sup>
PA4/REJECT2/DONE4	FCC2_UTM_RXADDR1	AG28 <sup>2</sup>
PA5/RESTART2/DREQ4	FCC2_UTM_RXADDR2/FCC1_UT_RX PRTY	AG26 <sup>2</sup>
PA6/FCC2_RXADDR3	L1RSYNCA1	AE24 <sup>2</sup>
PA7/SMSYN2/FCC2_TXADDR3	L1TSYNCA1/L1GNTA1	AH25 <sup>2</sup>
PA8/SMRXD2/FCC2_TXADDR4	L1RXD0A1/L1RXDA1	AF23 <sup>2</sup>
PA9/SMTXD2	L1TXD0A1	AH23 <sup>2</sup>
PA10/MSNUM5	FCC1_UT8_RXD0/FCC1_UT16_RXD8	AE22 <sup>2</sup>
PA11/MSNUM4	FCC1_UT8_RXD1/FCC1_UT16_RXD9	AH22 <sup>2</sup>
PA12/MSNUM3	FCC1_UT8_RXD2/ FCC1_UT16_RXD10	AJ21 <sup>2</sup>
PA13/MSNUM2	FCC1_UT8_RXD3/ FCC1_UT16_RXD11	AH20 <sup>2</sup>
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT8_RXD4/ FCC1_UT16_RXD12	AG19 <sup>2</sup>
PA15/FCC1_MII_HDLC_RXD2	FCC1_UT8_RXD5/ FCC1_UT16_RXD13	AF18 <sup>2</sup>
PA16/FCC1_MII_HDLC_RXD1/ FCC1_RMII_RXD1	FCC1_UT8_RXD6/ FCC1_UT16_RXD14	AF17 <sup>2</sup>
PA17/FCC1_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/ FCC1_RMII_RXD0	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	AE16 <sup>2</sup>
PA18/FCC1_MII_HDLC_TXD0/ FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT8_TXD7/FCC1_UT16_TXD15	AJ16 <sup>2</sup>

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	AG15 <sup>2</sup>
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	AJ13 <sup>2</sup>
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	AE13 <sup>2</sup>
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12 <sup>2</sup>
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11 <sup>2</sup>
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	AH9 <sup>2</sup>
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	AJ8 <sup>2</sup>
PA26/FCC1_RMII_RX_ER	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	AH7 <sup>2</sup>
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRD_DV	FCC1_UT_RXSOC	AF7 <sup>2</sup>
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	FCC1_UTM_RXENB/ FCC1_UTS_RXENB	AD5 <sup>2</sup>
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	AF1 <sup>2</sup>
PA30/FCC1_MII_CRD/FCC1_RTS	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	AD3 <sup>2</sup>
PA31/FCC1_MII_COL	FCC1_UTM_TXENB/ FCC1_UTS_TXENB	AB5 <sup>2</sup>
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/FCC3_RTS	FCC2_UT8_RXD0	AD28 <sup>2</sup>
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD26 <sup>2</sup>
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AD25 <sup>2</sup>
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26 <sup>2</sup>
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3/L1RSYNCD1	AH27 <sup>2</sup>
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2/L1TSYNCD1/ L1GNTD1	AG24 <sup>2</sup>
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1/L1RXDD1	AH24 <sup>2</sup>
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0/L1TXDD1	AJ24 <sup>2</sup>
PB12/FCC3_MII_CRD/TXD2	L1CLKOB1/L1RSYNCC1	AG22 <sup>2</sup>
PB13/FCC3_MII_COL/L1TXD1A2	L1RQB1/L1TSYNCC1/L1GNTC1	AH21 <sup>2</sup>
PB14/FCC3_MII_RMII_TX_EN//RXD3	L1RXDC1	AG20 <sup>2</sup>
PB15/FCC3_MII_TX_ER/RXD2	L1TXDC1	AF19 <sup>2</sup>

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PB16/FCC3_MII_RMII_RX_ER/CLK18	L1CLKOA1	AJ18 <sup>2</sup>
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRS_DV	L1RQA1	AJ17 <sup>2</sup>
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	AE14 <sup>2</sup>
PB19/FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	AF13 <sup>2</sup>
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6/L1TXD1A1	AG12 <sup>2</sup>
PB21/FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7/L1TXD2A1	AH11 <sup>2</sup>
PB22/FCC2_MII_HDLC_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7/L1RXD1A1	AH16 <sup>2</sup>
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6/L1RXD2A1	AE15 <sup>2</sup>
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5/L1RXD3A1	AJ9 <sup>2</sup>
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNCC2	FCC2_UT8_TXD4/L1TXD3A1	AE9 <sup>2</sup>
PB26/FCC2_MII_CRS/L1RXDC2	FCC2_UT8_TXD1	AJ7 <sup>2</sup>
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	AH6 <sup>2</sup>
PB28/FCC2_MII_RX_ER/ FCC2_RMII_RX_ER/FCC2_RTS/ L1TSYNCB2/L1GNTB2/TXD1		AE3 <sup>2</sup>
PB29/L1RSYNCB2/FCC2_MII_TX_EN/ FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	AE2 <sup>2</sup>
PB30/FCC2_MII_RX_DV/ FCC2_RMII_CRS_DV/L1RXDB2	FCC2_UT_TXSOC	AC5 <sup>2</sup>
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	AC4 <sup>2</sup>
PC0/DREQ1/BRGO7/SMSYN2/ L1CLKOA2		AB26 <sup>2</sup>
PC1/DREQ2/BRGO6/L1RQA2/ SPISEL		AD29 <sup>2</sup>
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AE29 <sup>2</sup>
PC3/FCC3_CTS/DACK2/CTS4/ USB_RP	FCC2_UT8_TXD2	AE27 <sup>2</sup>
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AF27 <sup>2</sup>

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AF24 <sup>2</sup>
PC6/FCC1_CD	L1CLKOC1/FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AJ26 <sup>2</sup>
PC7/FCC1_CTS	L1RQC1/FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AJ25 <sup>2</sup>
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USBRN	FCC1_UT16_TXD0	AF22 <sup>2</sup>
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	AE21 <sup>2</sup>
PC10/CD3/RENA3	FCC1_UT16_TXD2/SI1_L1ST4/ FCC2_UT8_RXD3	AF20 <sup>2</sup>
PC11/CTS3/CLSN3/L1TXD3A2	L1CLKOD1/FCC2_UT8_RXD2	AE19 <sup>2</sup>
PC12/CD2/RENA2	SI1_L1ST3/FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	AE18 <sup>2</sup>
PC13/CTS2/CLSN2	L1RQD1/FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	AH18 <sup>2</sup>
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	AH17 <sup>2</sup>
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	AG16 <sup>2</sup>
PC16/CLK16/TIN4		AF15 <sup>2</sup>
PC17/CLK15/TIN3/BRGO8		AJ15 <sup>2</sup>
PC18/CLK14/TGATE2		AH14 <sup>2</sup>
PC19/CLK13/BRGO7/SPICLK		AG13 <sup>2</sup>
PC20/CLK12/TGATE1/USB_OE		AH12 <sup>2</sup>
PC21/CLK11/BRGO6		AJ11 <sup>2</sup>
PC22/CLK10/DONE1/FCC1_UT_TXPRTY		AG10 <sup>2</sup>
PC23/CLK9/BRGO5/DACK1		AE10 <sup>2</sup>
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	AF9 <sup>2</sup>
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	AE8 <sup>2</sup>
PC26/CLK6/TOUT3/TMCLK		AJ6 <sup>2</sup>
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		AG2 <sup>2</sup>
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2/ FCC2_RXADDR4		AF3 <sup>2</sup>
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		AF2 <sup>2</sup>

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	AE1 <sup>2</sup>
PC31/CLK1/BRGO1		AD1 <sup>2</sup>
PD4/BRGO8/FCC3_RTS/SMRXD2	L1TSYNCD1/L1GNTD1	AC28 <sup>2</sup>
PD5/DONE1	FCC1_UT16_TXD3	AD27 <sup>2</sup>
PD6/DACK1	FCC1_UT16_TXD4	AF29 <sup>2</sup>
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AF28 <sup>2</sup>
PD8/SMRXD1/BRGO5	FCC2_UT_TXPRTY	AG25 <sup>2</sup>
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	AH26 <sup>2</sup>
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1/L1RSYNCB1	AJ27 <sup>2</sup>
PD11/L1RQB2	FCC2_UT8_RXD0/L1TSYNCB1/ L1GNTB1	AJ23 <sup>2</sup>
PD12	SI1_L1ST2/L1RXDB1	AG23 <sup>2</sup>
PD13	SI1_L1ST1/L1TXDB1	AJ22 <sup>2</sup>
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	AE20 <sup>2</sup>
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	AJ20 <sup>2</sup>
PD16/SPIMISO	FCC1_UT_TXPRTY/L1TSYNCC1/ L1GNTC1	AG18 <sup>2</sup>
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	AG17 <sup>2</sup>
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	AF16 <sup>2</sup>
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	AH15 <sup>2</sup>
PD20/RTS4/TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	AJ14 <sup>2</sup>
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	AH13 <sup>2</sup>
PD22/RXD4L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	AJ12 <sup>2</sup>
PD23/RTS3/TENA3	FCC1_UT16_RXD4/L1RSYNCD1	AE12 <sup>2</sup>
PD24/TXD3	FCC1_UT16_RXD5/L1RXDD1	AF10 <sup>2</sup>
PD25/RXD3	FCC1_UT16_TXD6/L1TXDD1	AG9 <sup>2</sup>

Table 20. MPC8280 and MPC8270 (ZU Package) Pinout List (Continued)

Pin Name		Ball
MPC8280/MPC8270	MPC8280 only	
PD26/RTS2/TENA2	FCC1_UT16_RXD6/L1RSYNCC1	AH8 <sup>2</sup>
PD27/TXD2	FCC1_UT16_RXD7/L1RXDC1	AG7 <sup>2</sup>
PD28/RXD2	FCC1_UT16_TXD7/L1TXDC1	AE4 <sup>2</sup>
PD29/RTS1/TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1	AG1 <sup>2</sup>
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	AD4 <sup>2</sup>
PD31/RXD1		AD2 <sup>2</sup>
VCCSYN		AB3
VCCSYN1		B9
CLKIN2		AE11
SPARE4 <sup>3</sup>		U5
PCI_MODE <sup>4</sup>		AF25
SPARE6 <sup>3</sup>		V4
No connect <sup>5</sup>		AA1, AG4
I/O power		AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core power		U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground		AA5, AB1 <sup>6</sup> , AB2 <sup>7</sup> , AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

<sup>1</sup> Should be tied to VDDH via a 2K  $\Omega$  external pull-up resistor.

<sup>2</sup> The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

<sup>3</sup> Must be pulled down or left floating.

<sup>4</sup> If PCI is not desired, must be pulled up or left floating.

<sup>5</sup> Sphere is not connected to die.

## Pinout

<sup>6</sup> GNDSYN (AB1): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8280. New designs must connect AB1 to GND and follow the suggestions in Section 4.3, “Layout Practices.” Old designs in which the MPC8280 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.

<sup>7</sup> XFC (AB2) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8280 because there is no need for external capacitor to operate the PLL. New designs should connect AB2 (XFC) pin to GND. Old designs in which the MPC8280 is used as a drop-in replacement can leave the pin connected to the current capacitor.

Symbols used in Table 20 are described in Table 21.

**Table 21. Symbol Legend**

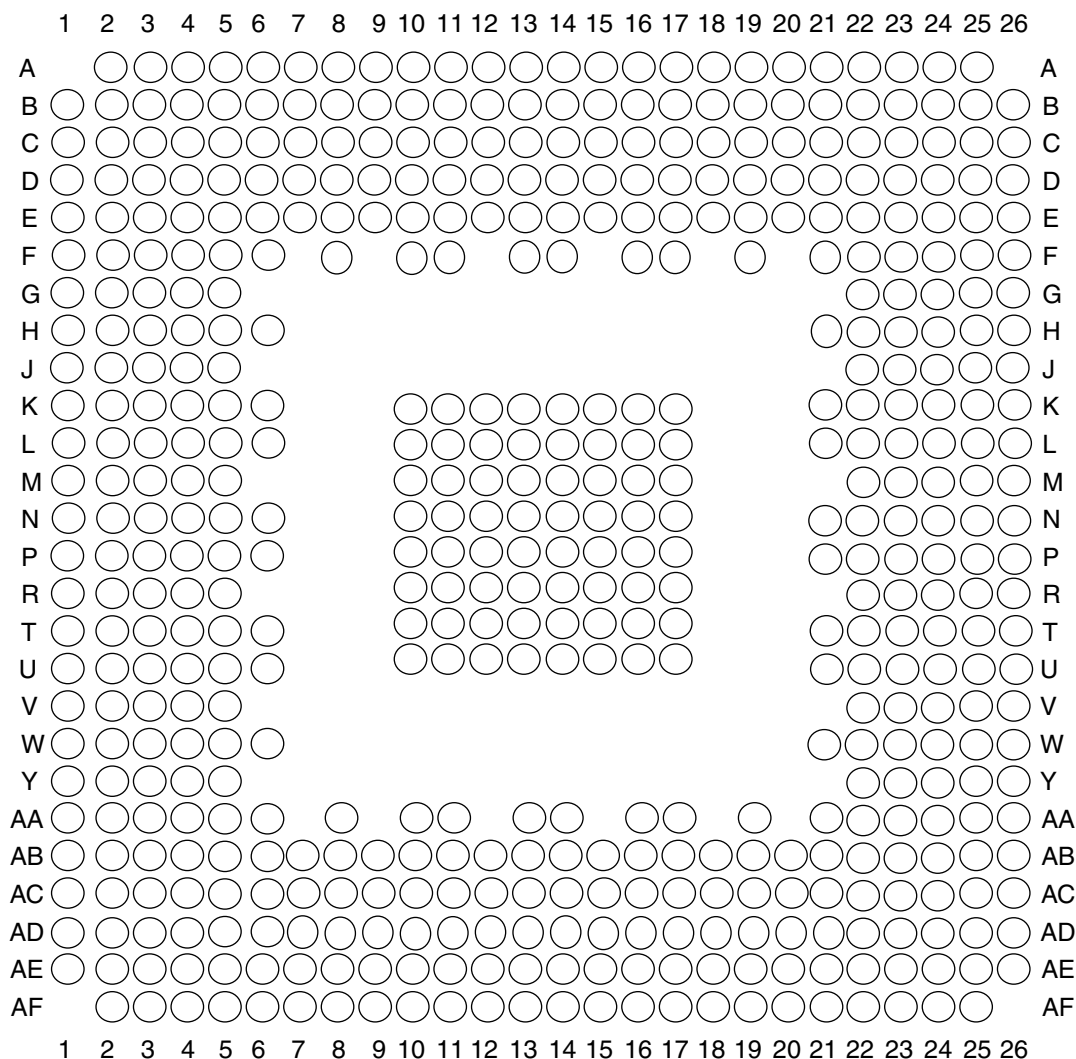
Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$ , are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.
RMII	Indicates that a signal is part of the reduced media independent interface.

## 8.2 VR and ZQ Packages—MPC8275 and MPC8270

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8280 and the MPC8270, refer to Section 8.1, “ZU Package—MPC8280 and MPC8270” on page 41.

Figure 15 shows the pinout of the VR and ZQ packages as viewed from the top surface.

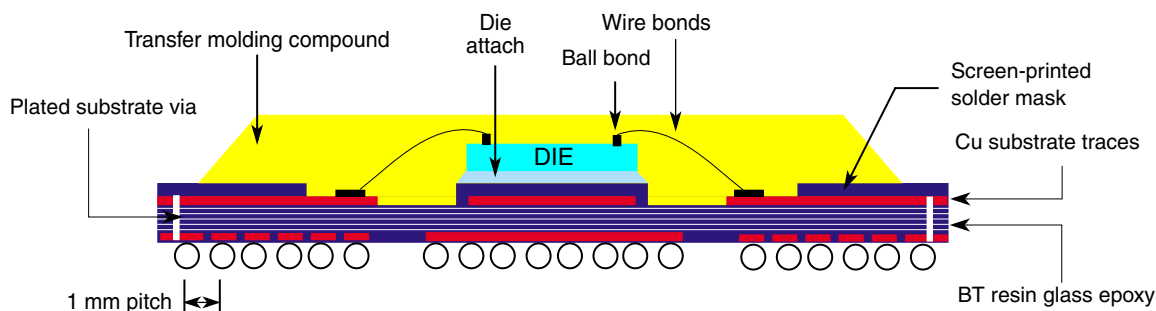




Not to Scale

**Figure 15. Pinout of the 516 PBGA Package (View from Top)**

Figure 16 shows the side profile of the PBGA package to indicate the direction of the top surface view.



**Figure 16. Side View of the PBGA Package**

**NOTE: Temperature Reflow for the VR Package**

In the VR package, sphere composition is lead-free (refer to Table 2). This requires higher temperature reflow than what is required for other PowerQUICC II packages. Users should consult “Motorola PowerQUICC II™ Pb-Free Packaging Information” (MPC8250PBFREEPKG) available at [www.motorola.com/semiconductors](http://www.motorola.com/semiconductors).

Table 22 shows the pinout list of the MPC8275 and MPC8270. Table 21 defines conventions and acronyms used in Table 22.

**Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List**

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
BR		C16
BG		D2
ABB/IRQ2		C1
TS		D1
A0		D5
A1		E8
A2		C4
A3		B4
A4		A4
A5		D7
A6		D8
A7		C6
A8		B5
A9		B6
A10		C7
A11		C8
A12		A6
A13		D9
A14		F11
A15		B7
A16		B8
A17		C9
A18		A7
A19		B9
A20		E11
A21		A8

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
A22		D11
A23		B10
A24		C11
A25		A9
A26		B11
A27		C12
A28		D12
A29		A10
A30		B12
A31		B13
TT0		E7
TT1		B3
TT2		F8
TT3		A3
TT4		C3
TBST		F5
TSIZ0		E3
TSIZ1		E2
TSIZ2		E1
TSIZ3		E4
AACK		D3
ARTRY		C2
DBG		A14
DBB/IRQ3		C15
D0		W4
D1		Y1
D2		V1
D3		P4
D4		N3
D5		K5
D6		J4
D7		G1
D8		AB1
D9		U4

## Pinout

**Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)**

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D10		U2
D11		N6
D12		N1
D13		L1
D14		J5
D15		G3
D16		AA2
D17		W1
D18		T3
D19		T1
D20		M2
D21		K2
D22		J1
D23		G4
D24		U5
D25		T5
D26		P5
D27		P3
D28		M3
D29		K3
D30		H2
D31		G5
D32		AA1
D33		V2
D34		U1
D35		P2
D36		M4
D37		K4
D38		H3
D39		F2
D40		Y2
D41		U3
D42		T2
D43		N2

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
D44		M5
D45		K1
D46		H4
D47		F1
D48		W2
D49		T4
D50		R3
D51		N4
D52		M1
D53		J2
D54		H5
D55		F3
D56		V3
D57		R5
D58		R2
D59		N5
D60		L2
D61		J3
D62		H1
D63		F4
DP0/RSRV/EXT_BR2		AB3
IRQ1/DP1/EXT_BG2		W5
IRQ2/DP2/TLBISYNC/EXT_DBG2		AC2
IRQ3/DP3/CKSTP_OUT/EXT_BR3		AA3
IRQ4/DP4/CORE_SRESET/EXT_BG3		AD1
IRQ5/CINT/DP5/TBEN/EXT_DBG3		AC1
IRQ6/DP6/CSE0		AB2
IRQ7/DP7/CSE1		Y3
PSDVAL		D15
TA		Y4
TEA		D16
GBL/IRQ1		E15
CI/BADDR29/IRQ2		D14
WT/BADDR30/IRQ3		E14

## Pinout

**Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)**

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
L2_HIT/IRQ4		A17
CPU_BG/BADDR31/IRQ5/CINT		B14
CPU_DBG		F13
CPU_BR		B17
CS0		AC6
CS1		AD6
CS2		AE6
CS3		AB7
CS4		AF7
CS5		AC7
CS6		AD7
CS7		AF8
CS8		AE8
CS9		AD8
CS10/BCTL1		AC8
CS11/AP0		AB8
BADDR27		C13
BADDR28		A12
ALE		D13
BCTL0		AF4
PWE0/PSDDQM0/PBS0		AA5
PWE1/PSDDQM1/PBS1		AE4
PWE2/PSDDQM2/PBS2		AD4
PWE3/PSDDQM3/PBS3		AF3
PWE4/PSDDQM4/PBS4		AB4
PWE5/PSDDQM5/PBS5		AE3
PWE6/PSDDQM6/PBS6		AF2
PWE7/PSDDQM7/PBS7		AD3
PSDA10/PGPL0		AE2
PSDWE/PGPL1		AD2
POE/PSDRAS/PGPL2		AE1
PSDCAS/PGPL3		AC3
PGTA/PUPMWAIT/PGPL4/PPBS		W6
PSDAMUX/PGPL5		AA4

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
LWE0/LSDDQM0/LBS0/PCI_CFG0		AC9
LWE1/LSDDQM1/LBS1/PCI_CFG1		AD9
LWE2/LSDDQM2/LBS2/PCI_CFG2		AE9
LWE3/LSDDQM3/LBS3/PCI_CFG3		AF9
LSDA10/LGPL0/PCI_MODCKH0		AB6
LSDW $\overline{E}$ /LGPL1/PCI_MODCKH1		AF5
LO $\overline{E}$ /LSDRAS/LGPL2/PCI_MODCKH2		AE5
LSDCAS/LGPL3/PCI_MODCKH3		AD5
LGTA/LUPMWAIT/LGPL4/LPBS		AC5
LGPL5/LSDAMUX/PCI_MODCK		AB5
LWR		AF6
L_A14/PAR		AE13
L_A15/FRAME/SM $\overline{I}$		AD15
L_A16/TRDY		AF16
L_A17/IRDY/CKSTP_OUT		AF15
L_A18/STOP		AE15
L_A19/DEVSEL		AE14
L_A20/IDSEL		AC17
L_A21/PERR		AD14
L_A22/SERR		AF13
L_A23/REQ0		AE20
L_A24/REQ1/HSEJSW		AC14
L_A25/GNT0		AC19
L_A26/GNT1/HSLED		AD13
L_A27/GNT2/HSENUM		AF21
L_A28/RST/CORE_SRESET		AF22
L_A29/INTA		AE21
L_A30/REQ2		AB14
L_A31/DLLOUT		AD20
LCL_D0/AD0		AB9
LCL_D1/AD1		AB10
LCL_D2/AD2		AC10
LCL_D3/AD3		AD10
LCL_D4/AD4		AE10

## Pinout

**Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)**

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
LCL_D5/AD5		AF10
LCL_D6/AD6		AF11
LCL_D7/AD7		AB12
LCL_D8/AD8		AB11
LCL_D9/AD9		AF12
LCL_D10/AD10		AE11
LCL_D11/AD11		AC13
LCL_D12/AD12		AC12
LCL_D13/AD13		AB13
LCL_D14/AD14		AD12
LCL_D15/AD15		AF14
LCL_D16/AD16		AF17
LCL_D17/AD17		AE16
LCL_D18/AD18		AD16
LCL_D19/AD19		AC16
LCL_D20/AD20		AB16
LCL_D21/AD21		AF18
LCL_D22/AD22		AE17
LCL_D23/AD23		AD17
LCL_D24/AD24		AB17
LCL_D25/AD25		AE18
LCL_D26/AD26		AD18
LCL_D27/AD27		AC18
LCL_D28/AD28		AE19
LCL_D29/AD29		AF20
LCL_D30/AD30		AD19
LCL_D31/AD31		AB18
LCL_DP0/C0/BE $\overline{0}$		AE12
LCL_DP1/C1/BE $\overline{1}$		AA13
LCL_DP2/C2/BE $\overline{2}$		AC15
LCL_DP3/C3/BE $\overline{3}$		AF19
IRQ0/NMI_OUT		A11
IRQ7/INT_OUT/APE		E5
TRST <sup>†</sup>		F22



Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
TCK		A24
TMS		C24
TDI		A25
TDO		B24
TRIS		C19
PORESET <sup>1</sup>		B25
HRESET		D24
SRESET		E23
QREQ		D18
RSTCONF		E24
MODCK1/AP1/TC0/BNKSEL0		B16
MODCK2/AP2/TC1/BNKSEL1		F16
MODCK3/AP3/TC2/BNKSEL2		A15
CLKIN1		G22
PA0/RESTART1/DREQ3	FCC2_UTM_TXADDR2	AC20 <sup>2</sup>
PA1/REJECT1/DONE3	FCC2_UTM_TXADDR1	AC21 <sup>2</sup>
PA2/CLK20/DACK3	FCC2_UTM_TXADDR0	AF25 <sup>2</sup>
PA3/CLK19/DACK4/L1RXD1A2	FCC2_UTM_RXADDR0	AE24 <sup>2</sup>
PA4/REJECT2/DONE4	FCC2_UTM_RXADDR1	AA21 <sup>2</sup>
PA5/RESTART2/DREQ4	FCC2_UTM_RXADDR2	AD25 <sup>2</sup>
PA6	FCC2_UT_RXADDR3	AC24 <sup>2</sup>
PA7/SMSYN2	FCC2_UT_TXADDR3	AA22 <sup>2</sup>
PA8/SMRXD2	FCC2_UT_TXADDR4	AA23 <sup>2</sup>
PA9/SMTXD2		Y26 <sup>2</sup>
PA10/MSNUM5	FCC1_UT8_RXD0/FCC1_UT16_RXD8	W22 <sup>2</sup>
PA11/MSNUM4	FCC1_UT8_RXD1/FCC1_UT16_RXD9	W23 <sup>2</sup>
PA12/MSNUM3	FCC1_UT8_RXD2/ FCC1_UT16_RXD10	V26 <sup>2</sup>
PA13/MSNUM2	FCC1_UT8_RXD3/ FCC1_UT16_RXD11	V25 <sup>2</sup>
PA14/FCC1_MII_HDLC_RXD3	FCC1_UT8_RXD4/ FCC1_UT16_RXD12	T22 <sup>2</sup>
PA15/FCC1_MII_HDLC_RXD2	/FCC1_UT8_RXD5/ FCC1_UT16_RXD13	T25 <sup>2</sup>
PA16/FCC1_MII_HDLC_RXD1/ FCC1_RMII_RXD1	FCC1_UT8_RXD6/ FCC1_UT16_RXD14	R24 <sup>2</sup>

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PA17/FCC_MII_HDLC_RXD0/ FCC1_MII_TRAN_RXD/ FCC1_RMII_RXD0	FCC1_UT8_RXD7/ FCC1_UT16_RXD15	P22 <sup>2</sup>
PA18/FCC1_MII_HDLC_TXD0/ FCC1_MII_TRAN_TXD/ FCC1_RMII_TXD0	FCC1_UT8_TXD7/FCC1_UT16_TXD15	N26 <sup>2</sup>
PA19/FCC1_MII_HDLC_TXD1/ FCC1_RMII_TXD1	FCC1_UT8_TXD6/FCC1_UT16_TXD14	N23 <sup>2</sup>
PA20/FCC1_MII_HDLC_TXD2	FCC1_UT8_TXD5/FCC1_UT16_TXD13	K26 <sup>2</sup>
PA21/FCC1_MII_HDLC_TXD3	FCC1_UT8_TXD4/FCC1_UT16_TXD12	L23 <sup>2</sup>
PA22	FCC1_UT8_TXD3/FCC1_UT16_TXD11	K23 <sup>2</sup>
PA23	FCC1_UT8_TXD2/FCC1_UT16_TXD10	H26 <sup>2</sup>
PA24/MSNUM1	FCC1_UT8_TXD1/FCC1_UT16_TXD9	F25 <sup>2</sup>
PA25/MSNUM0	FCC1_UT8_TXD0/FCC1_UT16_TXD8	D26 <sup>2</sup>
PA26/FCC1_MII_RMII_RX_ER/ FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	FCC1_UTM_RXCLAV/ FCC1_UTS_RXCLAV	D25 <sup>2</sup>
PA27/FCC1_MII_RX_DV/ FCC1_RMII_CRD_DV	FCC1_UT_RXSOC	C25 <sup>2</sup>
PA28/FCC1_MII_TX_EN/ FCC1_RMII_TX_EN	FCC1_UTM_RXENB/ FCC1_UTS_RXENB	C22 <sup>2</sup>
PA29/FCC1_MII_TX_ER	FCC1_UT_TXSOC	B21 <sup>2</sup>
PA30/FCC1_MII_CRD/FCC1_RTS	FCC1_UTM_TXCLAV/ FCC1_UTS_TXCLAV	A20 <sup>2</sup>
PA31/FCC1_MII_COL	FCC1_UTM_TXENB/ FCC1_UTS_TXENB	A19 <sup>2</sup>
PB4/FCC3_MII_HDLC_TXD3/ L1RSYNCA2/FCC3_RTS	FCC2_UT8_RXD0	AD21 <sup>2</sup>
PB5/FCC3_MII_HDLC_TXD2/ L1TSYNCA2/L1GNTA2	FCC2_UT8_RXD1	AD22 <sup>2</sup>
PB6/FCC3_MII_HDLC_TXD1/ FCC3_RMII_TXD1/ L1RXDA2/L1RXD0A2	FCC2_UT8_RXD2	AC22 <sup>2</sup>
PB7/FCC3_MII_HDLC_TXD0/ FCC3_RMII_TXD0/ FCC3_TXD/L1TXDA2/L1TXD0A2	FCC2_UT8_RXD3	AE26 <sup>2</sup>
PB8/FCC3_MII_HDLC_RXD0/ FCC3_RMII_RXD0/ FCC3_RXD/TXD3	FCC2_UT8_TXD3	AB23 <sup>2</sup>
PB9/FCC3_MII_HDLC_RXD1/ FCC3_RMII_RXD1/L1TXD2A2	FCC2_UT8_TXD2	AC26 <sup>2</sup>
PB10/FCC3_MII_HDLC_RXD2	FCC2_UT8_TXD1	AB26 <sup>2</sup>

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PB11/FCC3_MII_HDLC_RXD3	FCC2_UT8_TXD0	AA25 <sup>2</sup>
PB12/FCC3_MII_CRD/TXD2		W26 <sup>2</sup>
PB13/FCC3_MII_COL/L1TXD1A2		W25 <sup>2</sup>
PB14/FCC3_MII_RMII_TX_EN/RXD3		V24 <sup>2</sup>
PB15/FCC3_MII_TX_ER/RXD2		U24 <sup>2</sup>
PB16/FCC3_MII_RMII_RX_ER/CLK18		R22 <sup>2</sup>
PB17/FCC3_MII_RX_DV/CLK17/ FCC3_RMII_CRD_DV		R23 <sup>2</sup>
PB18/FCC2_MII_HDLC_RXD3/ L1CLKOD2/L1RXD2A2	FCC2_UT8_RXD4	M23 <sup>2</sup>
PB19/FCC2_MII_HDLC_RXD2/ L1RQD2/L1RXD3A2	FCC2_UT8_RXD5	L24 <sup>2</sup>
PB20/FCC2_MII_HDLC_RMII_RXD1/ L1RSYNCD2	FCC2_UT8_RXD6	K24 <sup>2</sup>
PB21/FCC2_MII_HDLC_RMII_RXD0/ FCC2_TRAN_RXD/L1TSYNCD2/ L1GNTD2	FCC2_UT8_RXD7	L21 <sup>2</sup>
PB22/FCC2_MII_HDLC_RMII_TXD0/ FCC2_TXD/FCC2_RMII_TXD0/ L1RXDD2	FCC2_UT8_TXD7	P25 <sup>2</sup>
PB23/FCC2_MII_HDLC_TXD1/ L1RXD2A1/L1TXDD2/ FCC2_RMII_TXD1	FCC2_UT8_TXD6	N25 <sup>2</sup>
PB24/FCC2_MII_HDLC_TXD2/ L1RSYNCC2	FCC2_UT8_TXD5	E26 <sup>2</sup>
PB25/FCC2_MII_HDLC_TXD3/ L1TSYNCC2/L1GNTC2	FCC2_UT8_TXD4	H23 <sup>2</sup>
PB26/FCC2_MII_CRD/L1RXDC2	FCC2_UT8_TXD1	C26 <sup>2</sup>
PB27/FCC2_MII_COL/L1TXDC2	FCC2_UT8_TXD0	B26 <sup>2</sup>
PB28/FCC2_MII_RX_ER/FCC2_RMII_RX_ER/ FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1		A22 <sup>2</sup>
PB29/L1RSYNCB2/ FCC2_MII_TX_EN/FCC2_RMII_TX_EN	FCC2_UTM_RXCLAV/ FCC2_UTS_RXCLAV	A21 <sup>2</sup>
PB30/FCC2_MII_RX_DV/L1RXDB2/ FCC2_RMII_CRD_DV	FCC2_UT_TXSOC	E20 <sup>2</sup>
PB31/FCC2_MII_TX_ER/L1TXDB2	FCC2_UT_RXSOC	C20 <sup>2</sup>
PC0/DREQ1/BRG07/SMSYN2/ L1CLKOA2		AE22 <sup>2</sup>
PC1/DREQ2/SPISEL/BRG06/L1RQA2		AA19 <sup>2</sup>
PC2/FCC3_CD/DONE2	FCC2_UT8_TXD3	AF24 <sup>2</sup>

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC3/FCC3_CTS/DACK2/CTS4/ USB_RP	FCC2_UT8_TXD2	AE25 <sup>2</sup>
PC4/SI2_L1ST4/FCC2_CD	FCC2_UTM_RXENB/ FCC2_UTS_RXENB	AB22 <sup>2</sup>
PC5/SI2_L1ST3/FCC2_CTS	FCC2_UTM_TXCLAV/ FCC2_UTS_TXCLAV	AC25 <sup>2</sup>
PC6/FCC1_CD	FCC1_UTM_RXADDR2/ FCC1_UTS_RXADDR2/ FCC1_UTM_RXCLAV1	AB25 <sup>2</sup>
PC7/FCC1_CTS	FCC1_UTM_TXADDR2/ FCC1_UTS_TXADDR2/ FCC1_UTM_TXCLAV1	AA24 <sup>2</sup>
PC8/CD4/RENA4/SI2_L1ST2/CTS3/ USB_RN	FCC1_UT16_TXD0	Y24 <sup>2</sup>
PC9/CTS4/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2/USB_RP	FCC1_UT16_TXD1	U22 <sup>2</sup>
PC10/CD3/RENA3	FCC1_UT16_TXD2/FCC2_UT8_RXD3	V23 <sup>2</sup>
PC11/CTS3/CLSN3/L1TXD3A2	FCC2_UT8_RXD2	U23 <sup>2</sup>
PC12/CD2/RENA2	FCC1_UTM_RXADDR1/ FCC1_UTS_RXADDR1	T26 <sup>2</sup>
PC13/CTS2/CLSN2	FCC1_UTM_TXADDR1/ FCC1_UTS_TXADDR1	R26 <sup>2</sup>
PC14/CD1/RENA1	FCC1_UTM_RXADDR0/ FCC1_UTS_RXADDR0	P26 <sup>2</sup>
PC15/CTS1/CLSN1/SMTXD2	FCC1_UTM_TXADDR0/ FCC1_UTS_TXADDR0	P24 <sup>2</sup>
PC16/CLK16/TIN4		M26 <sup>2</sup>
PC17/CLK15/TIN3/BRGO8		L26 <sup>2</sup>
PC18/CLK14/TGATE2		M24 <sup>2</sup>
PC19/CLK13/BRGO7/SPICLK		L22 <sup>2</sup>
PC20/CLK12/TGATE1/USB_OE		K25 <sup>2</sup>
PC21/CLK11/BRGO6		J25 <sup>2</sup>
PC22/CLK10/DONE1	FCC1_UT_TXPRTY	G26 <sup>2</sup>
PC23/CLK9/BRGO5/DACK1		F26 <sup>2</sup>
PC24/CLK8/TOUT4	FCC2_UT8_TXD3	G24 <sup>2</sup>
PC25/CLK7/BRGO4	FCC2_UT8_TXD2	E25 <sup>2</sup>
PC26/CLK6/TOUT3/TMCLK		G23 <sup>2</sup>
PC27/FCC3_TXD/FCC3_MII_TXD0/ FCC3_RMII_TXD0/CLK5/BRGO3		B23 <sup>2</sup>

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	FCC2_UT_RXADDR4	E22 <sup>2</sup>
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1		E21 <sup>2</sup>
PC30/CLK2/TOUT1	FCC2_UT8_TXD3	D21 <sup>2</sup>
PC31/CLK1/BRGO1		B20 <sup>2</sup>
PD4/BRGO8/FCC3_RTS/SMRDX2		AF23 <sup>2</sup>
PD5/DONE1	FCC1_UT16_TXD3	AE23 <sup>2</sup>
PD6/DACK1	FCC1_UT16_TXD4	AB21 <sup>2</sup>
PD7/SMSYN1/FCC1_TXCLAV2	FCC1_UTM_TXADDR3/ FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4 FCC2_UTS_TXADDR1	AD23 <sup>2</sup>
PD8/SMRDX1/BRGO5	FCC2_UT_TXPRTY	AD26 <sup>2</sup>
PD9/SMTXD1/BRGO3	FCC2_UT_RXPRTY	Y22 <sup>2</sup>
PD10/L1CLKOB2/BRGO4	FCC2_UT8_RXD1	AB24 <sup>2</sup>
PD11/L1RQB2	FCC2_UT8_RXD0 L1GNTB1	Y23 <sup>2</sup>
PD12		AA26 <sup>2</sup>
PD13		W24 <sup>2</sup>
PD14/L1CLKOC2/I2CSCL	FCC1_UT16_RXD0	V22 <sup>2</sup>
PD15/L1RQC2/I2CSDA	FCC1_UT16_RXD1	U26 <sup>2</sup>
PD16/SPIMISO	FCC1_UT_TXPRTY	T23 <sup>2</sup>
PD17/BRGO2/SPIMOSI	FCC1_UT_RXPRTY	R25 <sup>2</sup>
PD18/SPICLK	FCC1_UTM_RXADDR4/ FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/ FCC2_UTM_RXADDR3/ FCC2_UTS_RXADDR0	P23 <sup>2</sup>
PD19/SPISEL/BRGO1	FCC1_UTM_TXADDR4/ FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/ FCC2_UTM_TXADDR3/ FCC2_UTS_TXADDR0	N22 <sup>2</sup>
PD20/RTS4/TENA4/L1RSYNCA2/ USB_TP	FCC1_UT16_RXD2	M25 <sup>2</sup>
PD21/TXD4/L1RXD0A2/L1RXDA2/ USB_TN	FCC1_UT16_RXD3	L25 <sup>2</sup>
PD22/RXD4L1TXD0A2/L1TXDA2/ USB_RXD	FCC1_UT16_TXD5	J26 <sup>2</sup>
PD23/RTS3/TENA3	FCC1_UT16_RXD4	K22 <sup>2</sup>
PD24/TXD3	FCC1_UT16_RXD5	G25 <sup>2</sup>

Table 22. MPC8275 and MPC8270 (VR and ZQ Packages) Pinout List (Continued)

Pin Name		Ball
MPC8275/MPC8270	MPC8275 only	
PD25/RXD3	FCC1_UT16_TXD6	H24 <sup>2</sup>
PD26/RTS2/TENA2	FCC1_UT16_RXD6	F24 <sup>2</sup>
PD27/TXD2	FCC1_UT16_RXD7	H22 <sup>2</sup>
PD28/RXD2	FCC1_UT16_TXD7	B22 <sup>2</sup>
PD29/RTS1/TENA1	FCC1_UTM_RXADDR3/ FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/ FCC2_UTM_RXADDR4/ FCC2_UTS_RXADDR1	D22 <sup>2</sup>
PD30/TXD1	FCC2_UTM_TXENB/ FCC2_UTS_TXENB	C21 <sup>2</sup>
PD31/RXD1		E19 <sup>2</sup>
VCCSYN		D19
VCCSYN1		K6
CLKIN2		K21
SPARE4 <sup>3</sup>		C14
PCI_MODE <sup>4</sup>		AD24
SPARE6 <sup>3</sup>		B15
No connect <sup>5</sup>		E17, C23
I/O power		E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9
Core Power		L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10
Ground		B18 <sup>6</sup> , A18 <sup>7</sup> , A2, B1, B2, A5, C5, C18, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17

- <sup>1</sup> Should be tied to VDDH via a 2K  $\Omega$  external pull-up resistor.
- <sup>2</sup> The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.
- <sup>3</sup> Must be pulled down or left floating.
- <sup>4</sup> If PCI is not desired, must be pulled up or left floating.
- <sup>5</sup> Sphere is not connected to die.
- <sup>6</sup> GNDSYN (B18): This pin exists as a separate ground signal in MPC826x(A) devices; it does not exist as a separate ground signal on the MPC8275/MPC8270. New designs must connect B18 to GND and follow the suggestions in Section 4.3, “Layout Practices.” Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to GND with the noise filtering capacitors.
- <sup>7</sup> XFC (A18) pin: This pin is used in MPC826x(A) devices; it is not used in MPC8275/MPC8270 because there is no need for external capacitor to operate the PLL. New designs should connect A18 (XFC) pin to GND. Old designs in which the MPC8275/MPC8270 is used as a drop-in replacement can leave the pin connected to the current capacitor.

## 9 Package Description

The following sections provide the package parameters and mechanical dimensions.

### 9.1 Package Parameters

Package parameters are provided in Table 23.

**Table 23. Package Parameters**

Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8280 MPC8270	37.5 x 37.5	TBGA	480	1.27	1.55
VR	MPC8275VR MPC8270VR	27 x 27	PBGA	516	1	2.25
ZQ	MPC8275ZQ MPC8270ZQ	27 x 27	PBGA	516	1	2.25

9.2 Mechanical Dimensions

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA (ZU) package. Refer to Table 2.

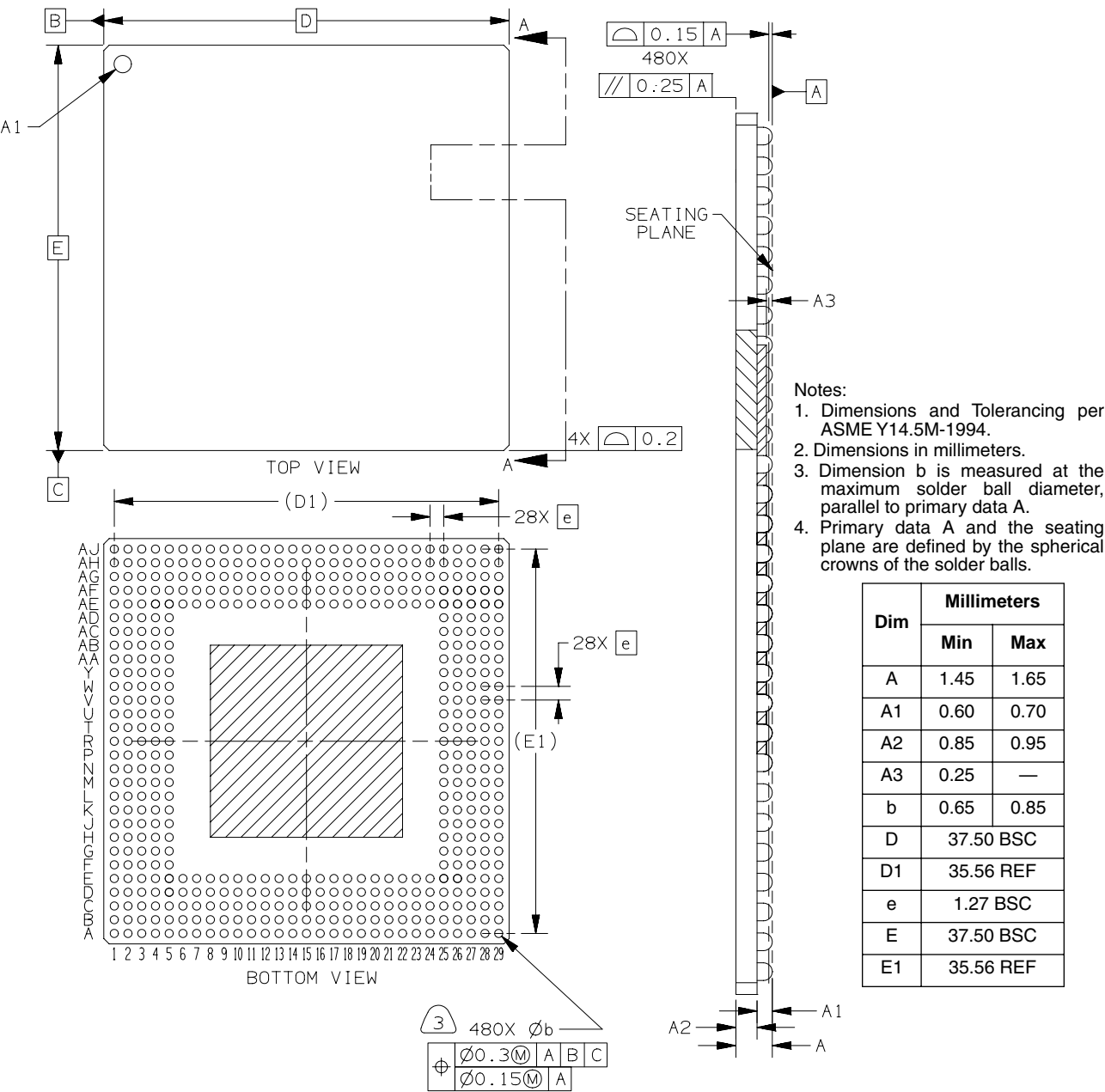


Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

Figure 18 provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA (VR/ZQ) packages.



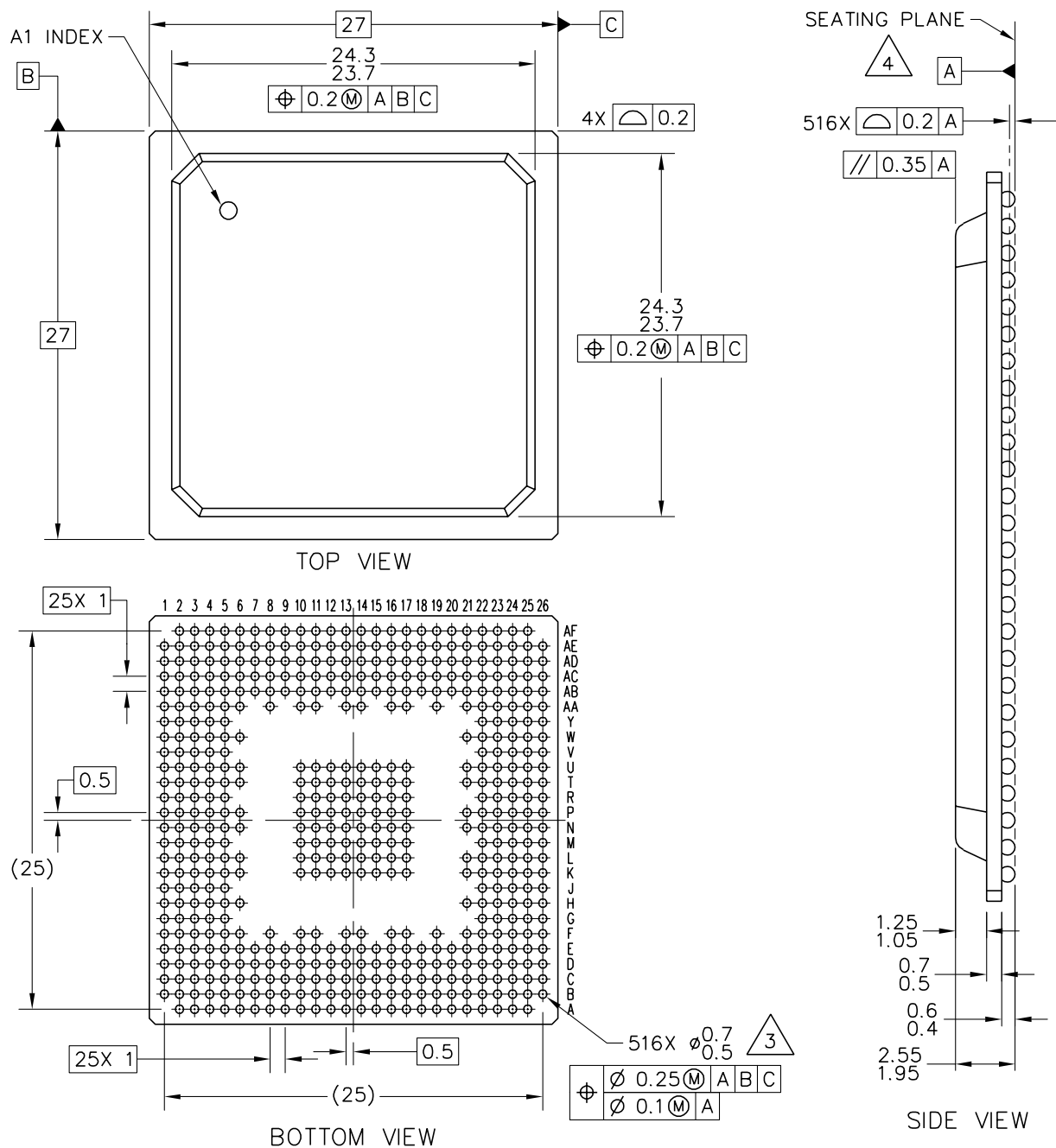


Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

## 10 Ordering Information

Figure 19 provides an example of the Motorola part numbering nomenclature for the MPC8280. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Motorola sales office.

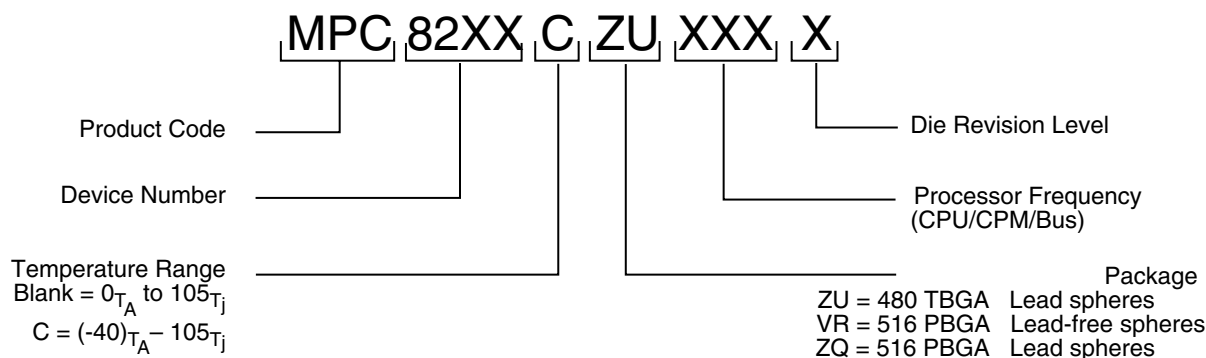


Figure 19. Motorola Part Number Key

## 11 Document Revision History

Table 24. Document Revision History

Revision	Date	Substantive Changes
0.1	—	Initial public release
0.2	11/2002	Table 22, "VR Pinout": Addition of C18 to the Ground (GND) pin list (page 63)
0.3	6/2003	<ul style="list-style-type: none"> <li>Removal of notes stating "no local bus" on VR-package devices. The MPC8270VR and the MPC8275VR have local bus support.</li> <li>References to "G2 core" changed to "G2_LE core." Refer to the <i>G2 Core Reference Manual</i> (G2CORERM/D).</li> <li>Addition of VCCSYN to "Note" below Table 4, and to note 3 of Table 5</li> <li>Figure 2: New</li> <li>Table 5: Addition of note 1</li> <li>Table 6: Addition of <math>\theta_{JB}</math> and <math>\theta_{JC}</math>. Modifications to ZU package values.</li> <li>Table 7: Addition of various configurations, Modification of values. Addition of note 3.</li> <li>Table 9: Addition of 66 MHz and 100 MHz values. Addition of sp42a/sp43a.</li> <li>Table 10: Addition of 66 MHz and 100 MHz values</li> <li>Table 12: sp30 values. sp33b @ 100 MHz value. Removal of previous note 2. Modification of current note 2.</li> <li>Figure 5, Figure 6, Figure 7, and Figure 8: Addition of notes</li> <li>Section 6.2: Addition of note on PCI timing</li> <li>Table 15, Table 16, Table 17, Table 18, Table 19: Addition of note 1 concerning minimum operating frequencies</li> <li>Addition of statement before clock tables about selection of clock configuration and input frequency</li> <li>Table 20 and Table 22: Addition of note 1 to CPM pins</li> </ul>

Table 24. Document Revision History

Revision	Date	Substantive Changes
1.0	2/2004	<ul style="list-style-type: none"> <li>Removal of "Advance Information" and "Preliminary." The MPC8280 is fully qualified.</li> <li>Table 1: New</li> <li>Figure 1: Modification to note 2</li> <li>Section 1.1: Core frequency range is 166–450 MHz</li> <li>Addition of ZQ (516 PBGA with Lead spheres) package references</li> <li>Table 4: VDD and VCCSYN modified to 1.45–1.60 V</li> <li>Note following Table 4: Modified</li> <li>Table 5: Addition of note 2 regarding <math>\overline{\text{TRST}}</math> and <math>\overline{\text{PORESET}}</math> (see VIH row of Table 5)</li> <li>Table 5: Changed <math>I_{OL}</math> for 60x signals to 6.0 mA</li> <li>Table 5: Moved QREQ to <math>V_{OL}</math>: <math>I_{OL} = 3.2</math> mA</li> <li>Table 5: Addition of critical interrupt (<math>\overline{\text{CINT}}</math>) to <math>\overline{\text{IRQ5}}</math> for <math>V_{OL}</math> (<math>I_{OL} = 6.0</math> mA)</li> <li>Table 6: Addition of <math>\Psi_{JT}</math> and note 4</li> <li>Sections 4.1–4.2: New</li> <li>Table 7: Modified power values (+ 150mW to each)</li> <li>Table 8: Addition of note 2. Changed PCI impedance to 27 <math>\Omega</math>.</li> <li>Table 9: Changes to sp36b, SP38a, sp38b, sp37a, sp39a, sp40 and sp41</li> <li>Table 10: Changes to sp16a, sp18a, sp20 and sp21</li> <li>Section 6.2: Addition of Note: CLKIN Jitter and Duty Cycle</li> <li>Table 11: Changes to sp13 @ 66 and 83 MHz, sp14 @ 83 MHz</li> <li>Table 12: Change to sp30 (data bus signals). Changes to sp33b. Removal of note 2.</li> <li>Table 15 through Table 19: Modification of note 1 regarding CPU and CPM Fmin. Modification to corresponding values in tables.</li> <li>Table 20: Addition of note 1 to <math>\overline{\text{TRST}}</math> (AH3) and <math>\overline{\text{PORESET}}</math> (AG6)</li> <li>Table 20: Addition of RXD3 to CPM port pin PB14. Previously omitted.</li> <li>Table 20: Addition of critical interrupt (<math>\overline{\text{CINT}}</math>) to B21 and U4. Previously omitted.</li> <li>Table 20: Addition of note 5 to 'No connect' (AA1, AG4)</li> <li>Addition of "Note: Temperature Reflow for the VR Package" on page 58</li> <li>Table 22: Addition of note 1 to <math>\overline{\text{TRST}}</math> (F22) and <math>\overline{\text{PORESET}}</math> (B25)</li> <li>Table 22: Addition of previously omitted signals that are multiplexed with CPM port pins: <ul style="list-style-type: none"> <li>PA6—FCC2_UT_RXADDR3</li> <li>PA7—FCC2_UT_TXADDR3</li> <li>PA8—FCC2_UT_TXADDR4</li> <li>PB14—RXD3</li> <li>PC19—SPICLK</li> <li>PC22—FCC1_UT_TXPRTY</li> <li>PC28—FCC2_UT_RXADDR4</li> </ul> </li> <li>Table 22: Removal of serial interface 1 (SI1) signals from port pins (see note 2 in Figure 1): <ul style="list-style-type: none"> <li>PA[6–9], PB[8–17, 20–25], PC[6–7, 10–13], PD[4, 10–13, 16, 23–28]</li> </ul> </li> <li>Table 22: Addition of critical interrupt (<math>\overline{\text{CINT}}</math>) to AC1 and B14. Previously omitted.</li> <li>Table 22: Addition of note 5 to 'No connect' (E17, C23)</li> </ul>

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