



# MOTOROLA

## QUAD DUAL-IN-LINE SILICON ANNULAR<sup>†</sup> COMPLEMENTARY PAIR TRANSISTORS

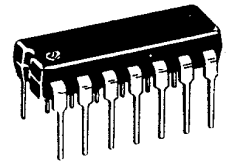
... designed for high-speed switching circuits, DC to VHF amplifier applications and complementary circuitry.

- Maximum Power Dissipation @  $T_A = 25^\circ\text{C}$   
 $P_D = 1.25$  Watts — MPQ6001, MPQ6002, MPQ6501, MPQ6502  
 $= 0.9$  Watts — MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N
- DC Current Gain Specified — 1.0 to 300 mAdc
- High Current-Gain-Bandwidth Product —  
 $f_T = 400$  MHz (Typ) @  $I_C = 50$  mAdc
- NPN Transistor Similar to 2N2218 or 2N2219
- PNP Transistor Similar to 2N2904 or 2N2905
- Compact Size Compatible with IC Automatic Insertion Equipment

# MPQ6001,N MPQ6002,N MPQ6501,N MPQ6502,N

## QUAD DUAL-IN-LINE SILICON COMPLEMENTARY PAIR TRANSISTORS

CASE 646  
PLASTIC PACKAGE



### MAXIMUM RATINGS

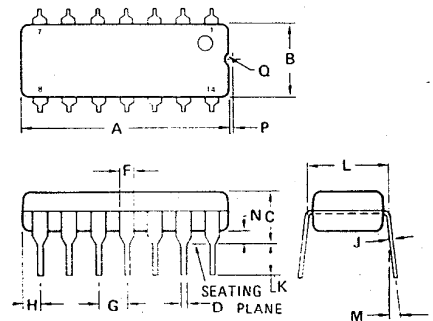
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	30	Vdc
Collector-Base Voltage	$V_{CB}$	60	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current — Continuous	$I_C$	500	mAdc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (1) MPQ6001, MPQ6002, MPQ6501, MPQ6502 MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N Derate above $25^\circ\text{C}$		$P_D$	Watts
MPQ6001, MPQ6002, MPQ6501, MPQ6502		0.65	1.25
MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N		0.5	0.9
MPQ6001, MPQ6002, MPQ6501, MPQ6502		5.18	10
MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N		4.0	7.2
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ MPQ6001, MPQ6002, MPQ6501, MPQ6502 MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N Derate above $25^\circ\text{C}$		$P_D$	Watts
MPQ6001, MPQ6002, MPQ6501, MPQ6502		1.0	3.0
MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N		0.825	2.4
MPQ6001, MPQ6002, MPQ6501, MPQ6502		8.0	24
MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N		6.7	19.2
Operating and Storage Junction Temperature Range		$T_J, T_{stg}$	$-55$ to $+150$ $^\circ\text{C}$

(1) Second Breakdown occurs at power levels greater than 3 times the power dissipation rating.

### THERMAL CHARACTERISTICS

Characteristic	Junction to Case	Junction to Ambient	Unit
Thermal Resistance			
Each Die			$^\circ\text{C/W}$
MPQ6001, MPQ6002, MPQ6501, MPQ6502	125	193	
MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N	151	250	
Effective, 4 Die			
MPQ6001, MPQ6002, MPQ6501, MPQ6502	41.6	100	
MPQ6001N, MPQ6002N, MPQ6501N, MPQ6502N	52	134	
Coupling Factors			
Q1-Q4 or Q2-Q3	30	60	%
Q1-Q2 or Q3-Q4	34	70	
	2.0	24	
	2.0	26	

<sup>†</sup> Annular Semiconductors Patented by Motorola Inc.

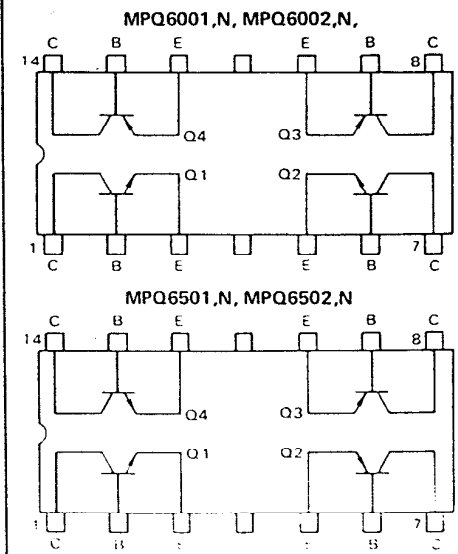


DIM	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54	BSC	0.100	BSC
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	—	10 <sup>0</sup>	—	10 <sup>0</sup>
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

### CONNECTION DIAGRAM



## THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

$$(1) \Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$$

Where  $\Delta T_{J1}$  is the change in junction temperature of die 1  
 $R_{\theta 1}$  thru 4 is the thermal resistance of die 1 through 4  
 $P_{D1}$  thru 4 is the power dissipated in die 1 through 4  
 $K_{\theta 2}$  thru 4 is the thermal coupling between die 1 and die 2 through 4.

An effective package thermal resistance can be defined as follows:

$$(2) R_{\theta(EFF)} = \Delta T_{J1} / P_{DT}$$

where:  $P_{DT}$  is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to

$$(3) \Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$$

For the conditions where  $P_{D1} = P_{D2} = P_{D3} = P_{D4}$ ,  $P_{DT} = 4 P_D$ , equation (3) can be further simplified and by substituting into equation (2) results in

$$(4) R_{\theta(EFF)} = R_{\theta 1} (1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4}) / 4$$

Values for the coupling factors when either the case or the ambient is used as a reference are given in the table on page 1. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest possible junction temperatures will result.

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Breakdown Voltage (1) ( $I_C = 10 \text{ mA}$ , $I_B = 0$ )	$BV_{CEO}$	30	—	—	Vdc
Collector-Base Breakdown Voltage ( $I_C = 10 \text{ mA}$ , $I_E = 0$ )	$BV_{CBO}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 10 \text{ mA}$ , $I_C = 0$ )	$BV_{EBO}$	5.0	—	—	Vdc
Collector Cutoff Current ( $V_{CB} = 50 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	—	—	30	nA
Emitter Cutoff Current ( $V_{EB} = 3.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	—	30	nA
<b>ON CHARACTERISTICS</b>					
DC Current Gain (1) ( $I_C = 1.0 \text{ mA}$ , $V_{CE} = 10 \text{ Vdc}$ )	$h_{FE}$	25	—	—	—
( $I_C = 10 \text{ mA}$ , $V_{CE} = 10 \text{ Vdc}$ )		50	—	—	—
( $I_C = 150 \text{ mA}$ , $V_{CE} = 10 \text{ Vdc}$ )		35	—	—	—
( $I_C = 300 \text{ mA}$ , $V_{CE} = 10 \text{ Vdc}$ )		75	—	—	—
Collector-Emitter Saturation Voltage (1) ( $I_C = 150 \text{ mA}$ , $I_B = 15 \text{ mA}$ )	$V_{CE(sat)}$	—	—	0.4	Vdc
( $I_C = 300 \text{ mA}$ , $I_B = 30 \text{ mA}$ )		—	—	1.4	Vdc
Base-Emitter Saturation Voltage (1) ( $I_C = 150 \text{ mA}$ , $I_B = 15 \text{ mA}$ )	$V_{BE(sat)}$	—	—	1.3	Vdc
( $I_C = 300 \text{ mA}$ , $I_B = 30 \text{ mA}$ )		—	—	2.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Current-Gain-Bandwidth Product (1) ( $I_C = 50 \text{ mA}$ , $V_{CE} = 20 \text{ Vdc}$ , $f = 100 \text{ MHz}$ )	$f_T$	200	350	—	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 100 \text{ kHz}$ )	$C_{ob}$	—	6.0	8.0	pF
Input Capacitance ( $V_{EB} = 2.0 \text{ Vdc}$ , $I_C = 0$ , $f = 100 \text{ kHz}$ )	$C_{ib}$	—	20	30	pF
<b>SWITCHING CHARACTERISTICS</b>					
Turn-On Time ( $V_{CC} = 30 \text{ Vdc}$ , $V_{BE(on)} = 0.5 \text{ Vdc}$ , $I_C = 150 \text{ mA}$ , $I_{B1} = 15 \text{ mA}$ , Figure 1)	$t_{on}$	—	30	—	ns
Turn-Off Time ( $V_{CC} = 30 \text{ Vdc}$ , $I_C = 150 \text{ mA}$ , $I_{B1} = I_{B2} = 15 \text{ mA}$ , Figure 2)	$t_{off}$	—	225	—	ns

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle = 2%.

### NPN SATURATED SWITCHING TIME TEST CIRCUITS

For PNP Switching Tests, reverse the diodes, voltage polarities, and input pulses.

FIGURE 1 — NPN TURN-ON TIME

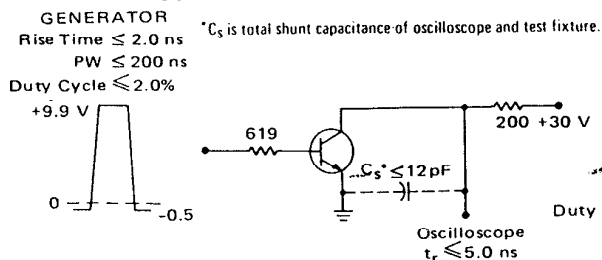
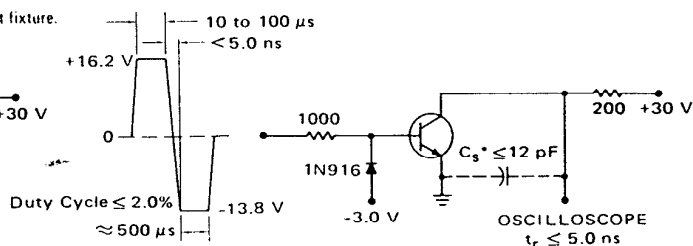


FIGURE 2 — NPN TURN-OFF TIME



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## NPN DATA

FIGURE 3 – NORMALIZED DC CURRENT GAIN

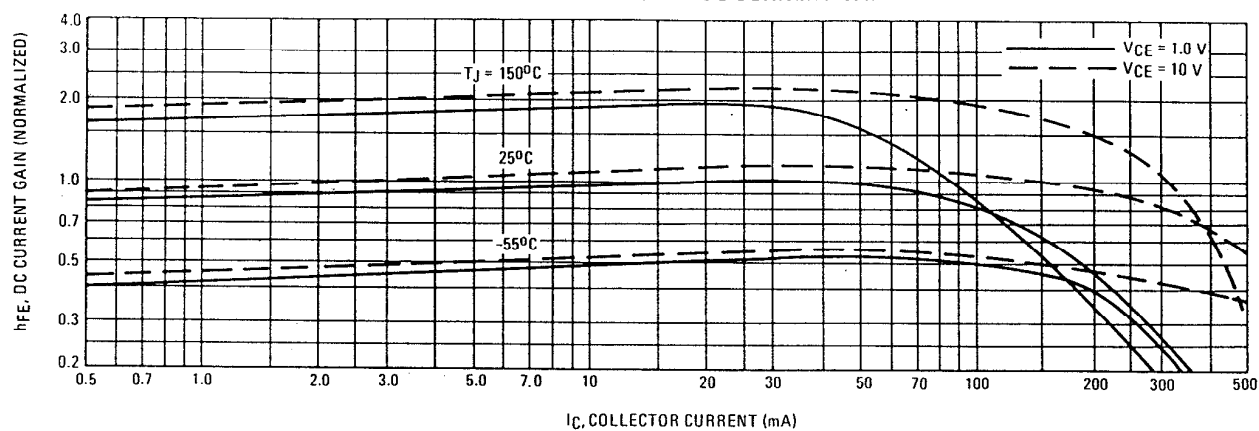


FIGURE 4 – "ON" VOLTAGES

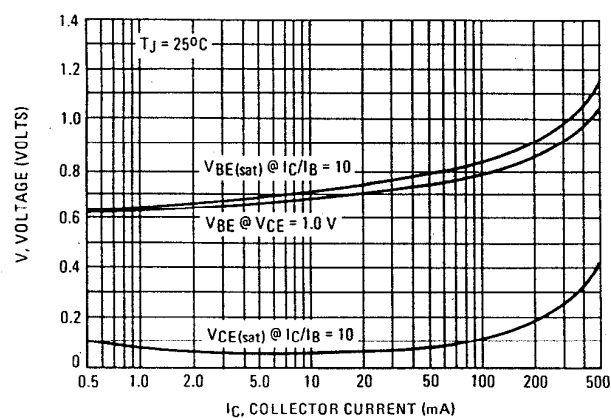


FIGURE 5 – TEMPERATURE COEFFICIENTS

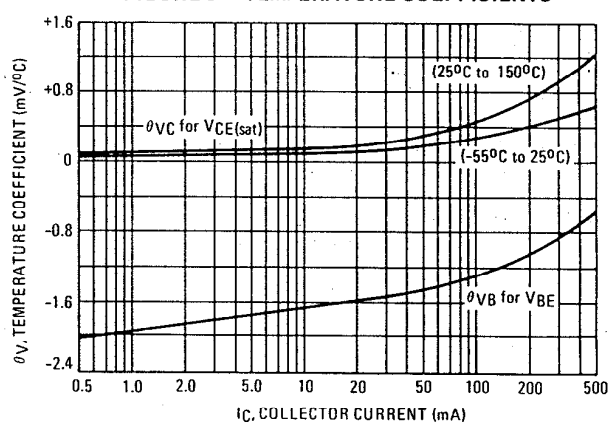
NOISE FIGURE  
( $V_{CE} = 10 \text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ )

FIGURE 6 – FREQUENCY EFFECTS

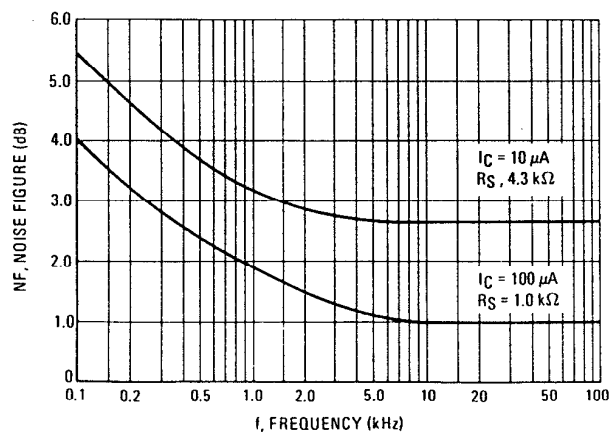
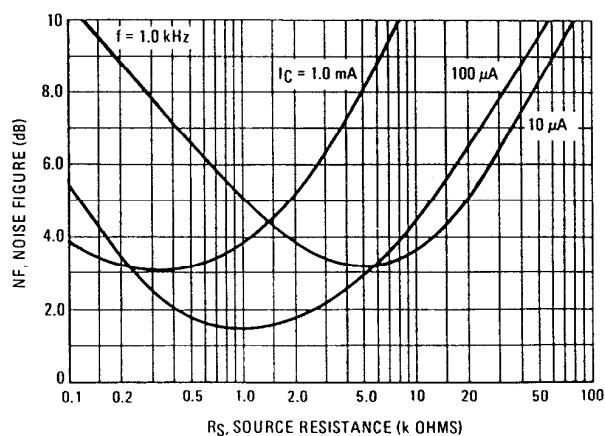


FIGURE 7 – SOURCE RESISTANCE EFFECTS



NPN DATA

FIGURE 8 — CURRENT-GAIN — BANDWIDTH PRODUCT

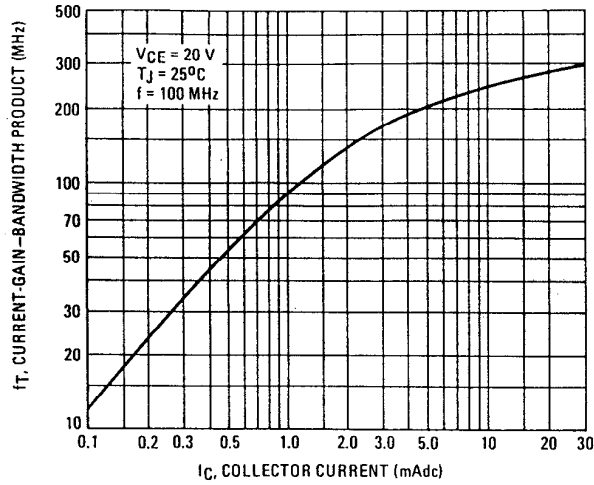
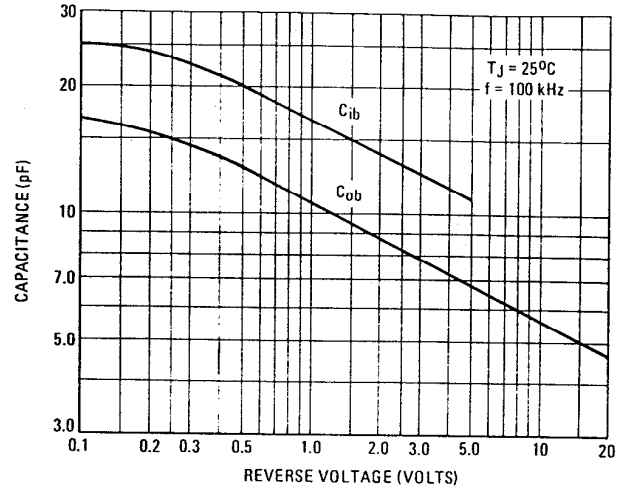


FIGURE 9 — CAPACITANCE



SWITCHING TIME CHARACTERISTICS

FIGURE 10 — TURN-ON TIME

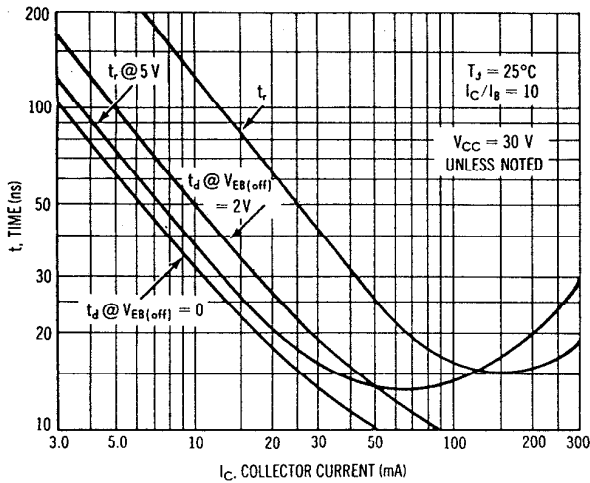


FIGURE 11 — CHARGE DATA

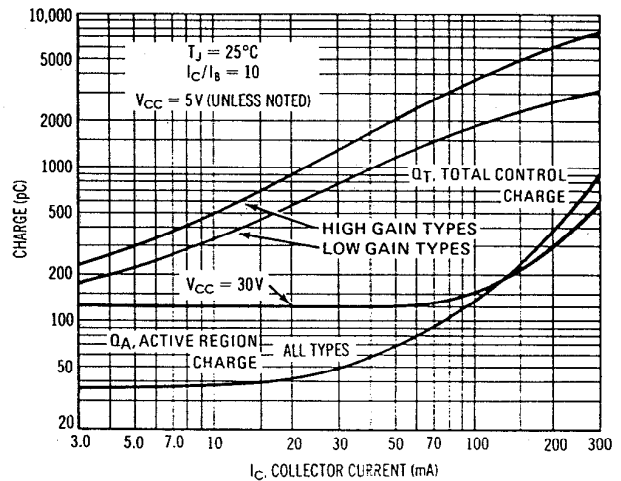
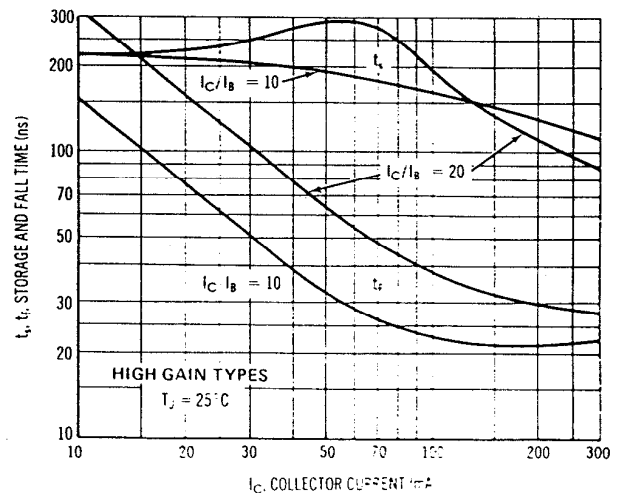
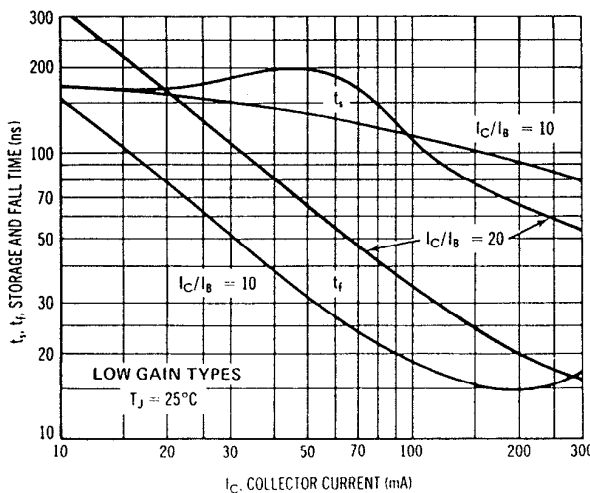


FIGURE 12 — TURN-OFF TIME



# PNP DATA

FIGURE 13 – DC CURRENT GAIN

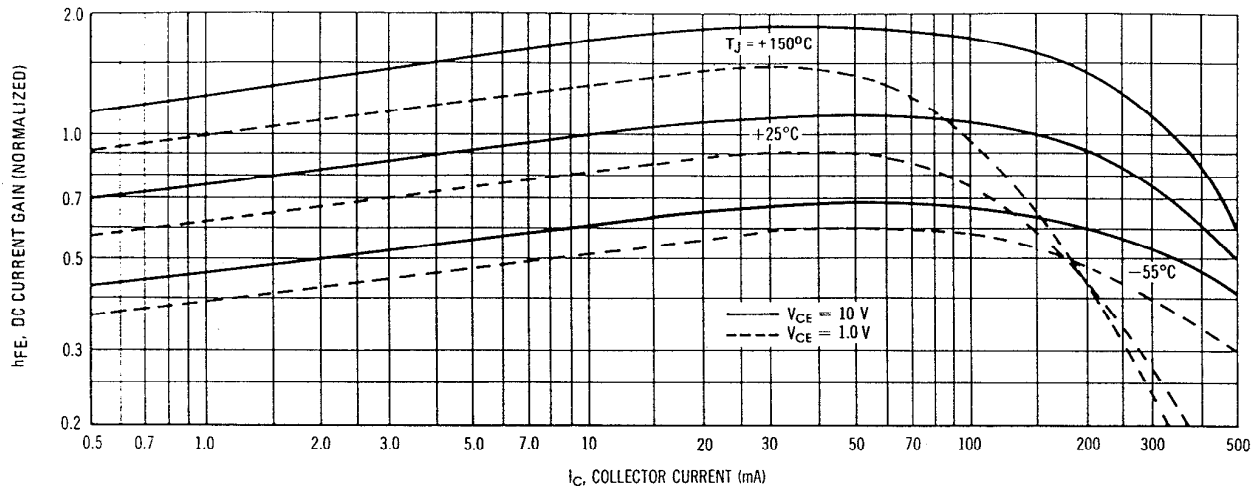


FIGURE 14 – "ON" VOLTAGES

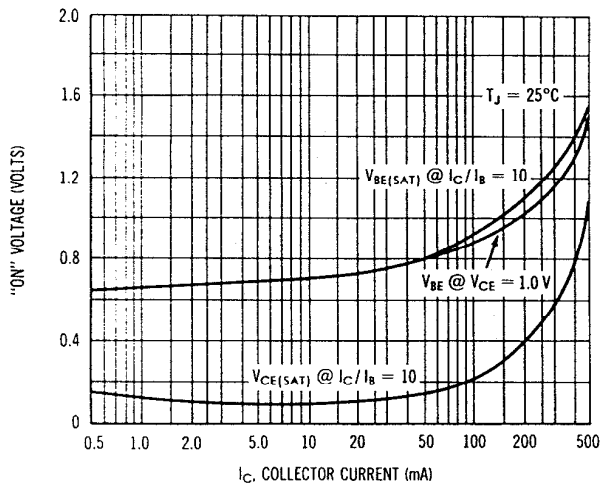
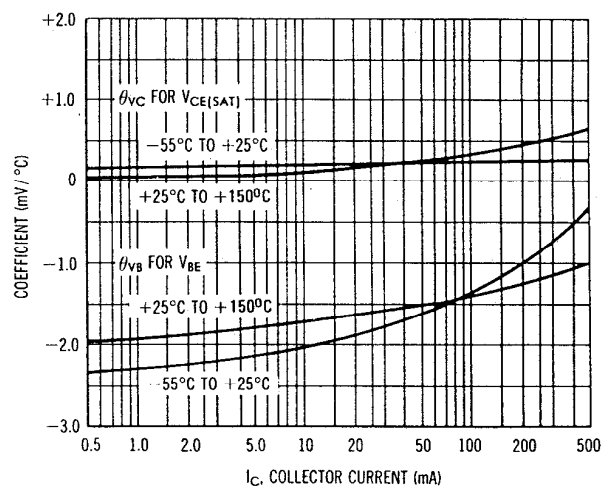


FIGURE 15 – TEMPERATURE COEFFICIENTS



## NOISE FIGURE ( $V_{CE} = 10\text{ V}$ , $T_A = 25^\circ\text{C}$ )

FIGURE 16 – FREQUENCY EFFECTS

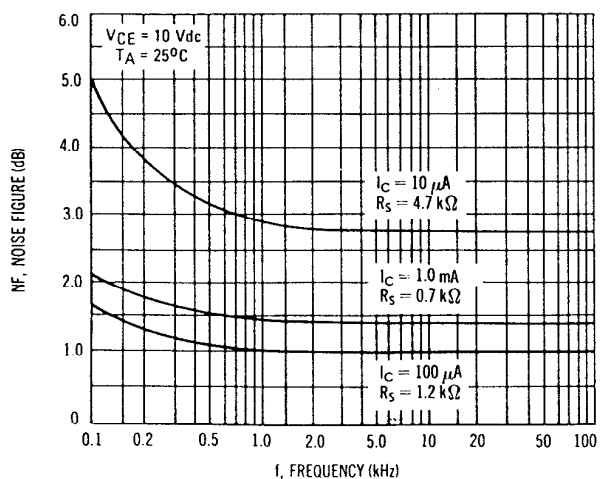
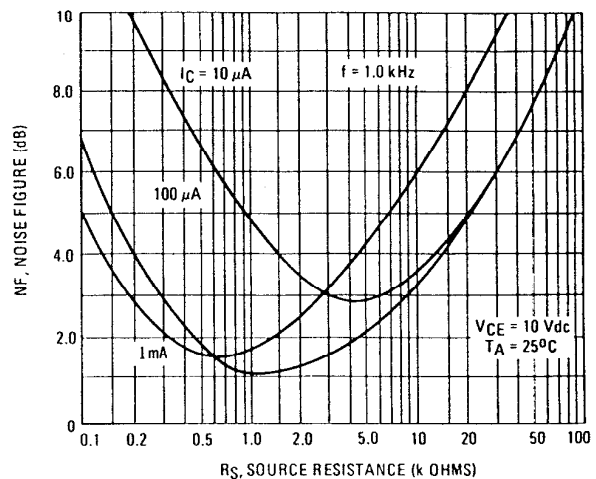


FIGURE 17 – SOURCE RESISTANCE EFFECTS



## PNP DATA

FIGURE 18 – CURRENT-GAIN BANDWIDTH PRODUCT

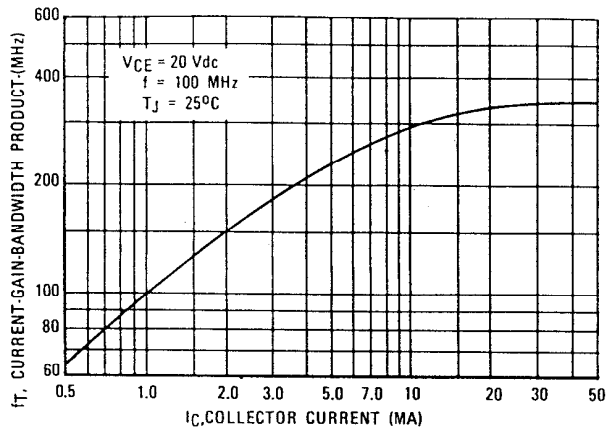


FIGURE 19 – CAPACITANCE

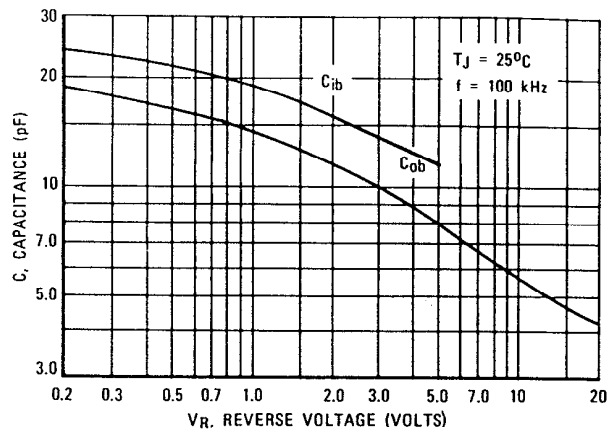


FIGURE 20 – TURN ON TIME

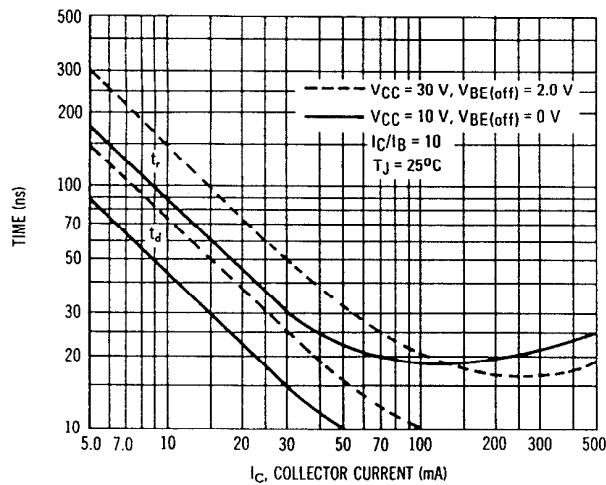


FIGURE 21 – CHARGE DATA

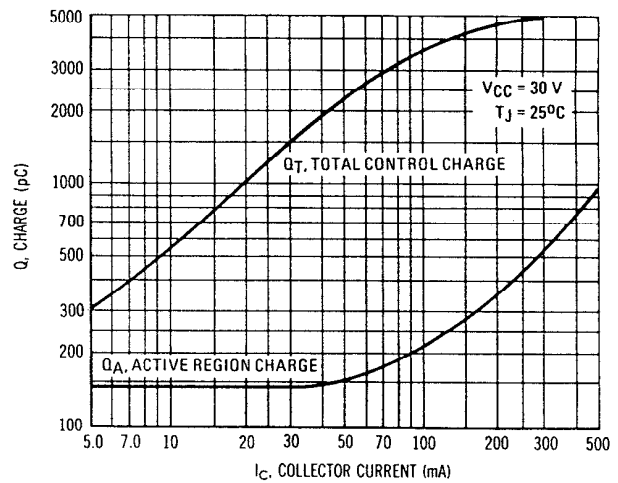


FIGURE 22 – STORAGE TIME

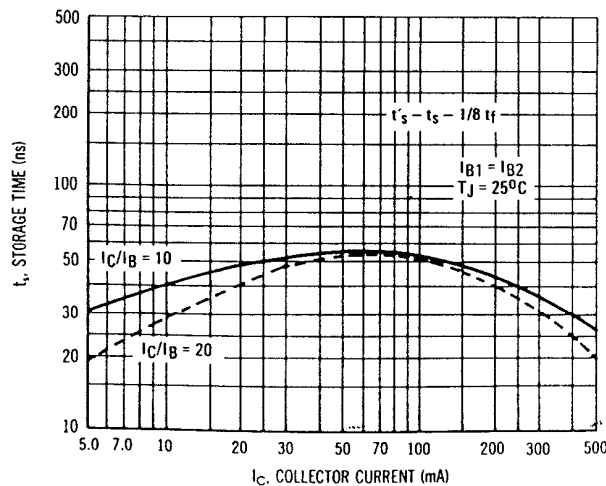
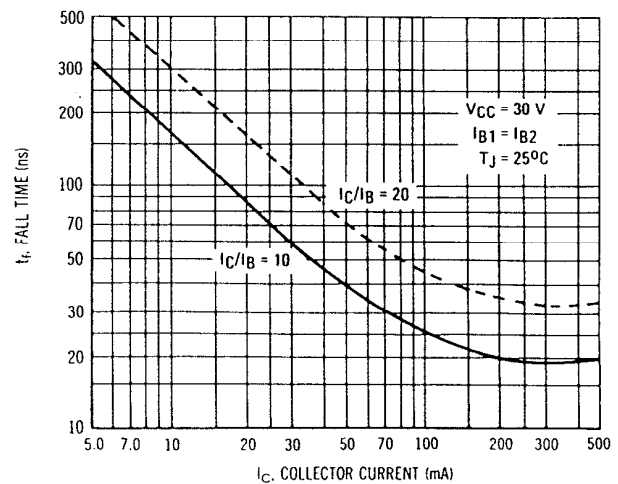


FIGURE 23 – FALL TIME


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