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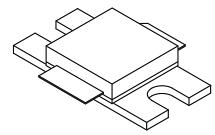
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF19045R3
MRF19045SR3

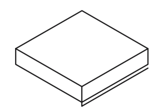
Designed for PCN and PCS base station applications with frequencies from 1.9 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications.

- Typical CDMA Performance @ 1960 MHz, 26 Volts, I_{DQ} = 550 mA
  Multi–carrier CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
  - Output Power — 9.5 Watts Avg.
  - Power Gain — 14.9 dB
  - Efficiency — 23.5%
  - Adjacent Channel Power —
    885 kHz: –50 dBc @ 30 kHz BW
  - IM3 — –37 dBc
- 100% Tested Under 2–Carrier N–CDMA
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 1.93 GHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

1990 MHz, 45 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465E–03, STYLE 1
NI–400
MRF19045R3



CASE 465F–03, STYLE 1
NI–400S
MRF19045SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

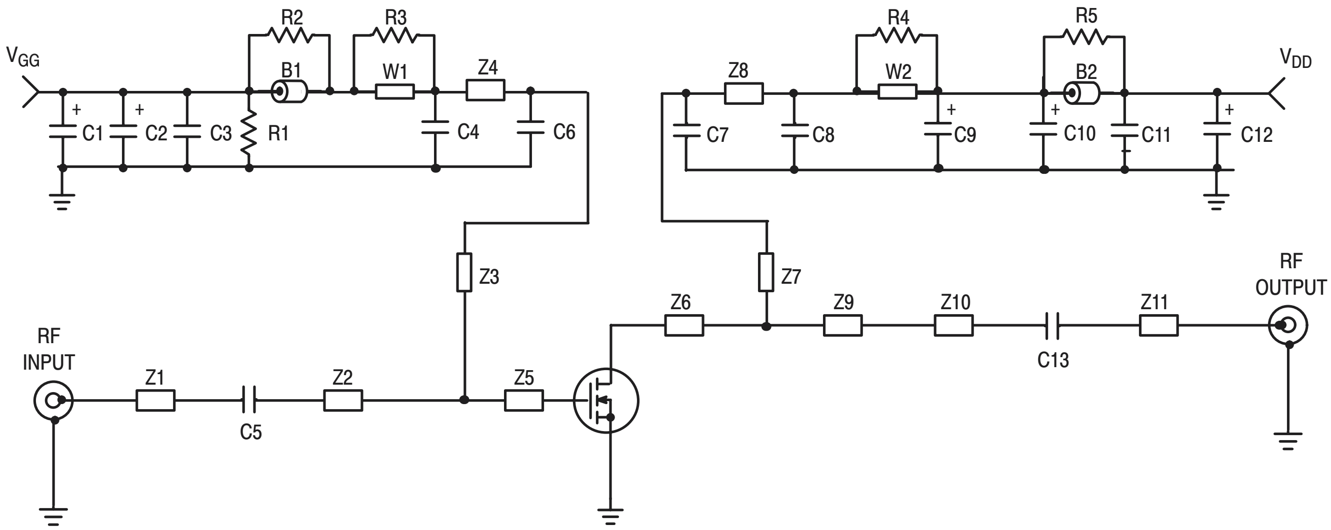
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 550 mAdc)	$V_{GS(Q)}$	3	3.8	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.19	0.21	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	4.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	1.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier N–CDMA, 1.2288 MHz Channel Bandwidth, IM3 measured in 1.2288 MHz Integrated Bandwidth. ACPR measured in 30 kHz Integrated Bandwidth.					
Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz)	G_{ps}	13	14.5	—	dB
Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz)	η	21	23.5	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz; IM3 Measured in a 1.2288 MHz Integrated Bandwidth Centered at f1 –2.5 Mhz and f2 +2.5 MHz, Referenced to the Carrier Channel Power)	IM3	—	–37	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 = 1987.5 MHz, f2 = 1990 MHz; ACPR measured in a 30 kHz Integrated Bandwith Centered at f1 –885 kHz and f2 +885 kHz)	ACPR	—	–51	–45	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 9.5 W Avg, 2–Carrier N–CDMA, I_{DQ} = 550 mA, f1 = 1930 MHz, f2 = 1932.5 MHz and f1 =1987.5 MHz, f2 = 1990 MHz)	IRL	—	–16	–9	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 550 mA, f = 1990 MHz)	P1dB	—	45	—	W
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 45 W CW, I_{DQ} = 550 mA, f = 1930 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



Z1	1.336″ x 0.081″ Microstrip	Z9	0.519″ x 0.254″ Microstrip
Z2	0.693″ x 0.081″ Microstrip	Z10	0.874″ x 0.081″ Microstrip
Z3	1.033″ x 0.047″ Microstrip	Z11	0.645″ x 0.081″ Microstrip
Z4	0.468″ x 0.047″ Microstrip	Board	3″ x 5″ Copper Clad PCB, Arlon GX0300-55-22, ε_r = 2.55
Z5	0.271″ x 0.460″ Microstrip		
Z6	0.263″ x 0.930″ Microstrip	Printed Circuit Board	CMR Part Number 19045PC5.SKF
Z7	1.165″ x 0.047″ Microstrip		
Z8	0.216″ x 0.047″ Microstrip		

NOTE: Z3, Z4, Z7, Z8 lengths and component placement tolerances are ±0.050″.
Zx lengths are microstrip lengths between components, center-line to center-line.
All component and z-length tolerances are ±0.015″, except as noted.

Figure 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Schematic

Table 1. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Designations and Values

Designators	Description
B1, B2	0.120″ x 0.333″ x 0.100″, Surface Mount Ferrite Beads, Fair Rite #2743019446
C1, C2	10 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T495X106K035AS4394
C3, C11	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C4, C8	24 pF Chip Capacitors, B Case, ATC #100B240JP500X
C5	470 pF Chip Capacitor, B Case, ATC #100B471JP200X
C6, C7	11 pF Chip Capacitors, B Case, ATC #100B110JP500X
C9, C10, C12	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet #T491X226K035AS4394
C13	8.2 pF Chip Capacitor, B Case, ATC #100B8R2CP500X
R1	560 kΩ, 1/4 W Chip Resistor (0.08″ x 0.13″)
R2, R3, R4, R5	8.2 Ω, 1/4 W Chip Resistors (0.08″ x 0.13″), Garrett Instruments #RM73B2B110JT
W1, W2	Solid Copper Buss Wire, 16 AWG
WS1, WS2	Beryllium Copper Wear Blocks (0.005″ x 0.150″ x 0.350″) Nominal
	Brass Banana Jack and Nut
	Red Banana Jack and Nut
	Green Banana Jack and Nut
	Type “N” Jack Connectors, Omni-Spectra #3052-1648-10
	4-40 Ph Head Screws, 0.125″ long
	4-40 Ph Head Screws, 0.312″ long
	4-40 Ph Head Screws, 0.625″ long
	4-40 Ph Rec. Hd. Screws, 0.625″ long

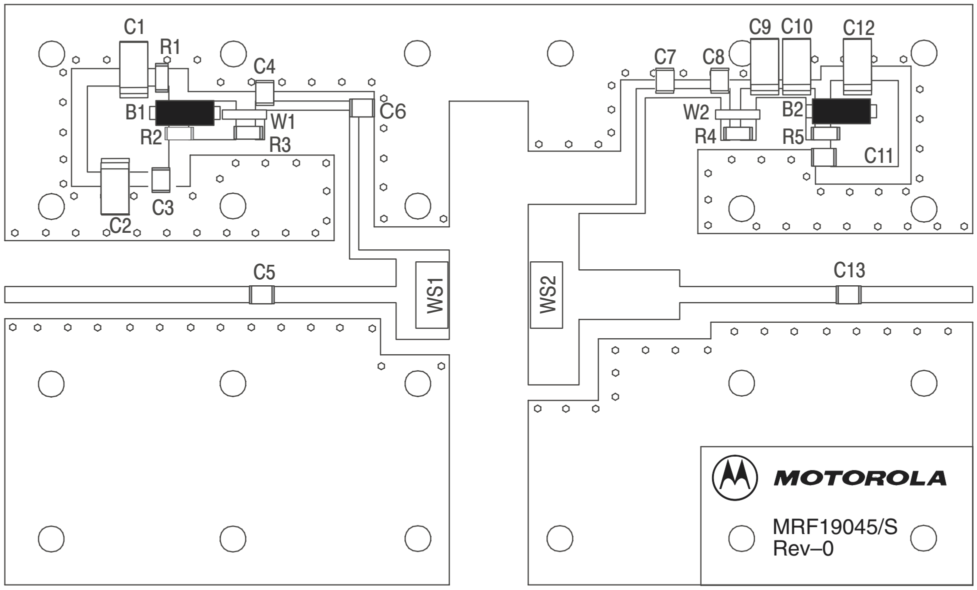


Figure 2. 1930 – 1990 MHz 2-Carrier N-CDMA Test Circuit Component Layout

TYPICAL CHARACTERISTICS

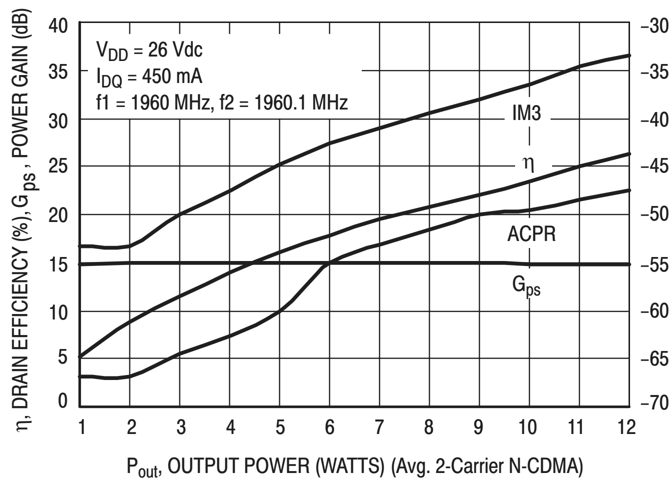


Figure 3. 2-Carrier N–CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

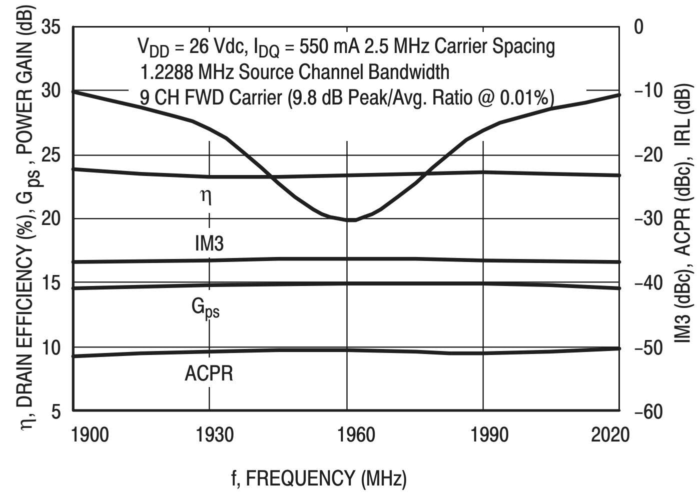


Figure 4. 2-Carrier N-CDMA ACPR, IM3, Power Gain, IRL and Drain Efficiency versus Output Power

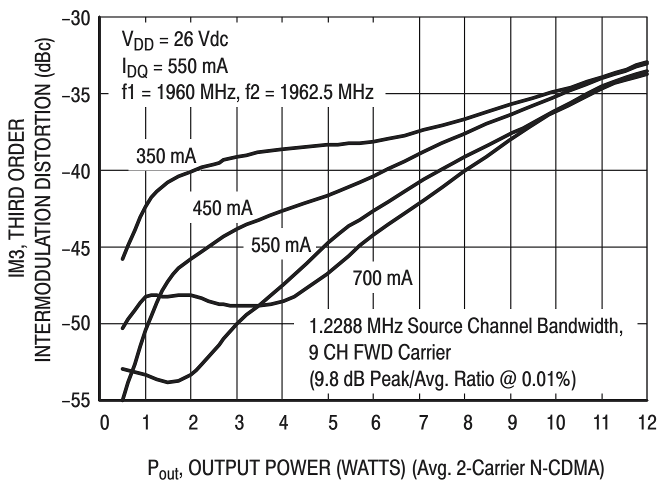


Figure 5. 2-Carrier N-CDMA IM3 versus Output Power

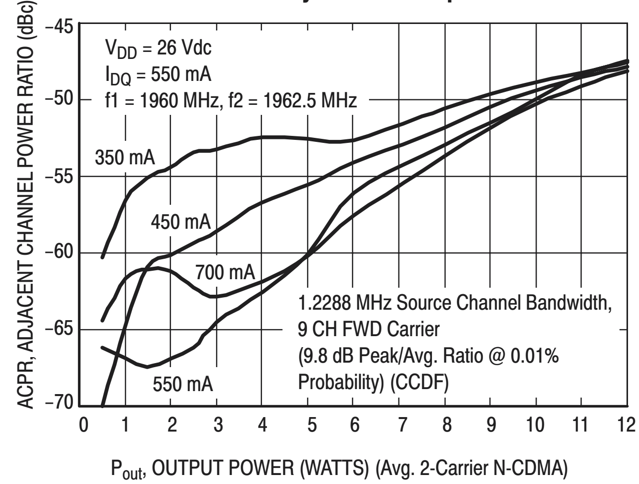


Figure 6. 2-Carrier N-CDMA ACPR versus Output Power

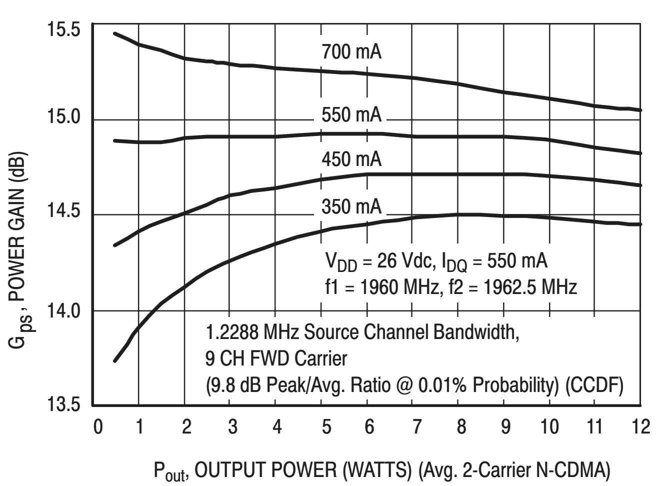


Figure 7. 2-Carrier N-CDMA Power Gain versus Output Power

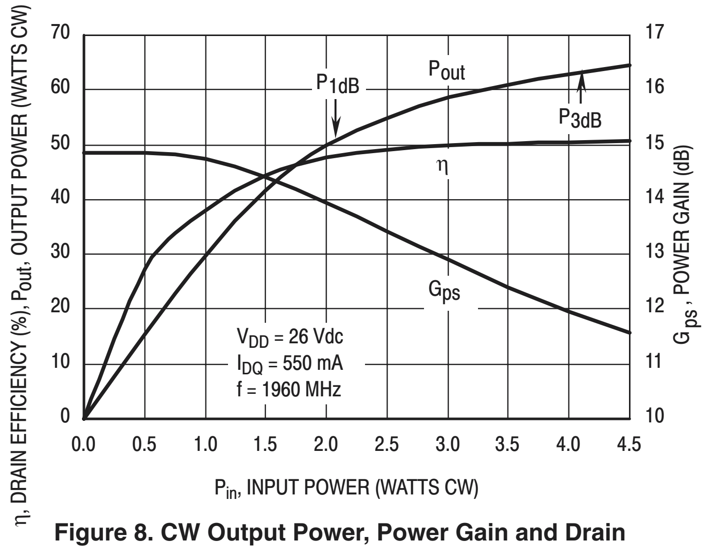


Figure 8. CW Output Power, Power Gain and Drain Efficiency versus Input Power

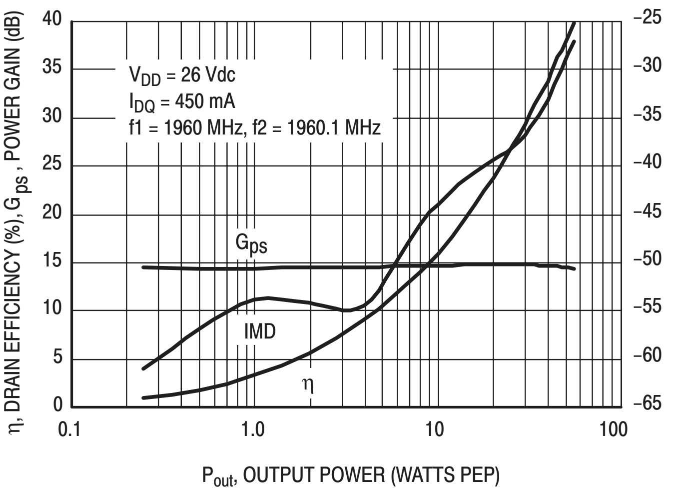


Figure 9. CW Two-Tone Power Gain, IMD and Drain Efficiency versus Output Power

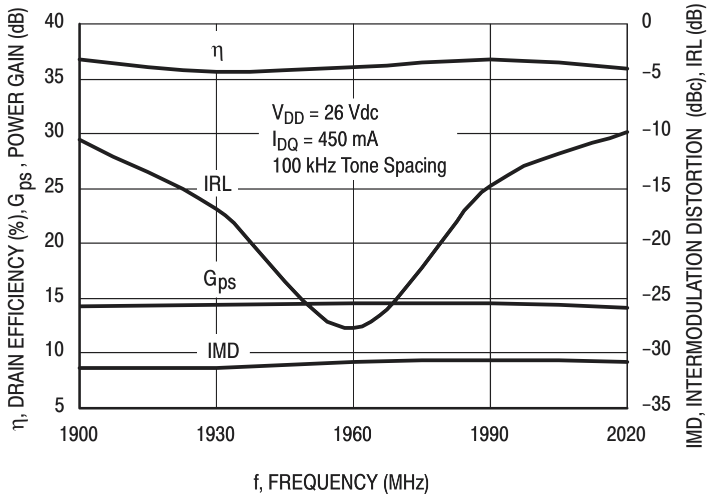


Figure 10. CW Two-Tone Power Gain, Input Return Loss, IMD and Drain Efficiency versus Frequency

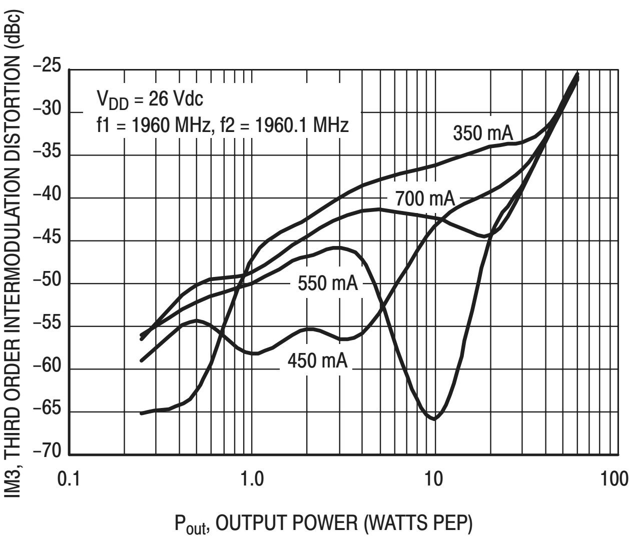


Figure 11. CW Two-Tone Intermodulation Distortion versus Output Power

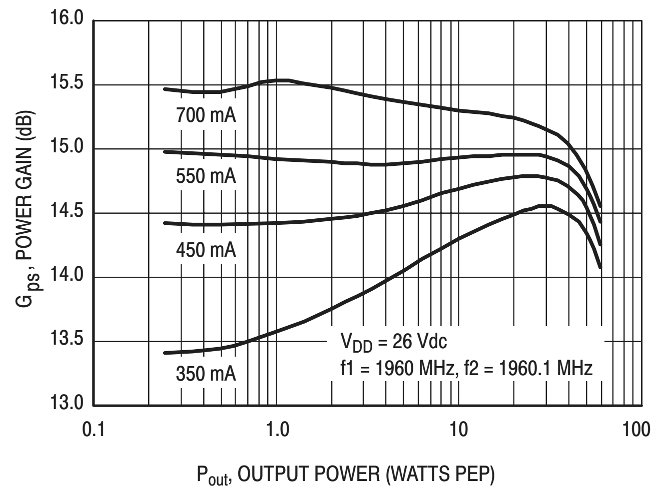


Figure 12. CW Two-Tone Power Gain versus Output Power

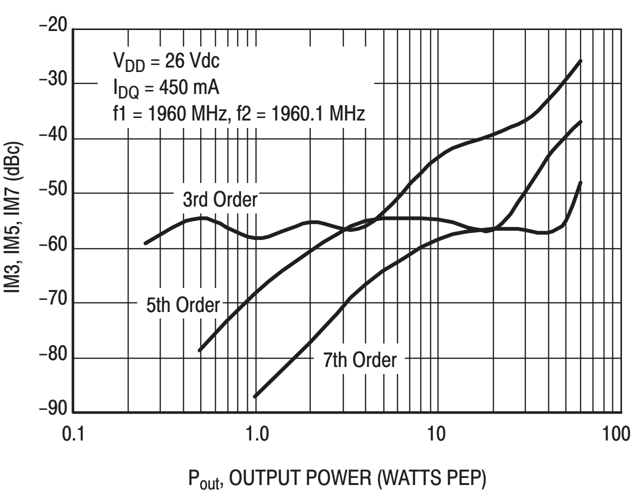


Figure 13. CW Two-Tone Intermodulation Distortion Products versus Output Power

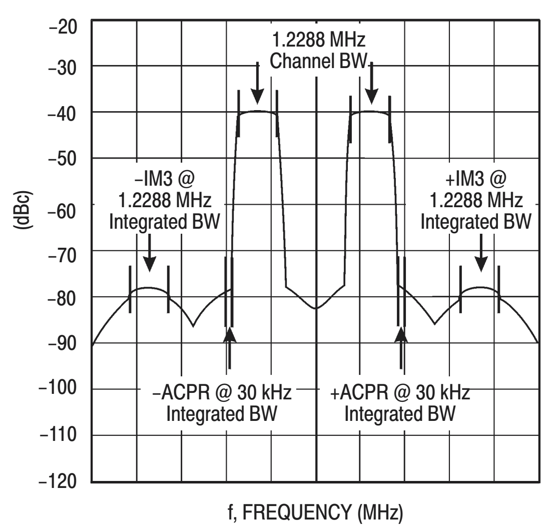
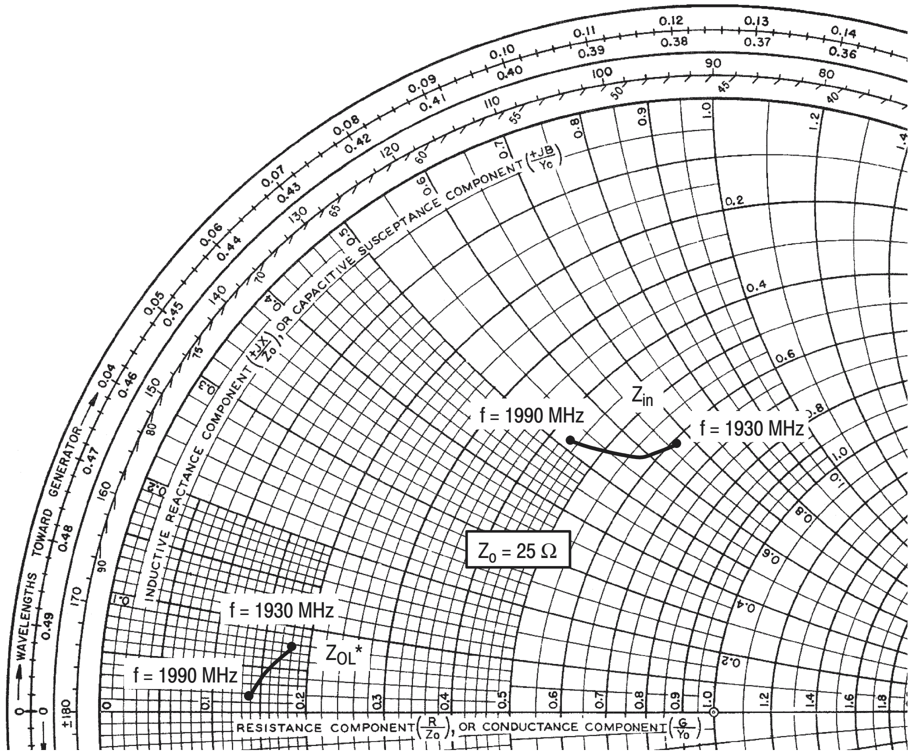


Figure 14. 2-Carrier N-CDMA Spectrum



V_{DD} = 26 V, I_{DQ} = 550 mA, P_{out} = 9 W Avg., 2-Carrier N-CDMA

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	15.52 + j16.5	4.52 + j1.86
1960	14.24 + j14.44	3.85 + j1.04
1990	11.11 + j13.01	3.44 + j0.69

Z_{in} = Complex conjugate of the optimum source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note 1: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Note 2: Measurements were taken on the MRF19045 2-carrier N-CDMA test circuit, with SMA Launchers.

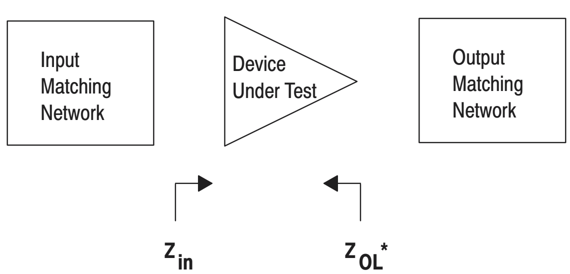


Figure 15. Series Equivalent Input and Output Impedance

NOTES

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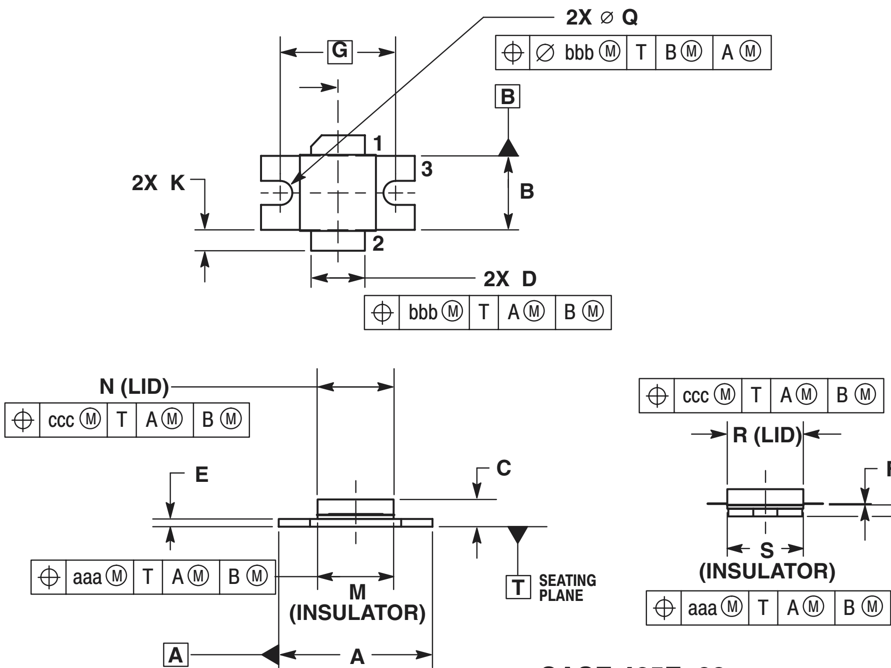
NOTES

PACKAGE DIMENSIONS

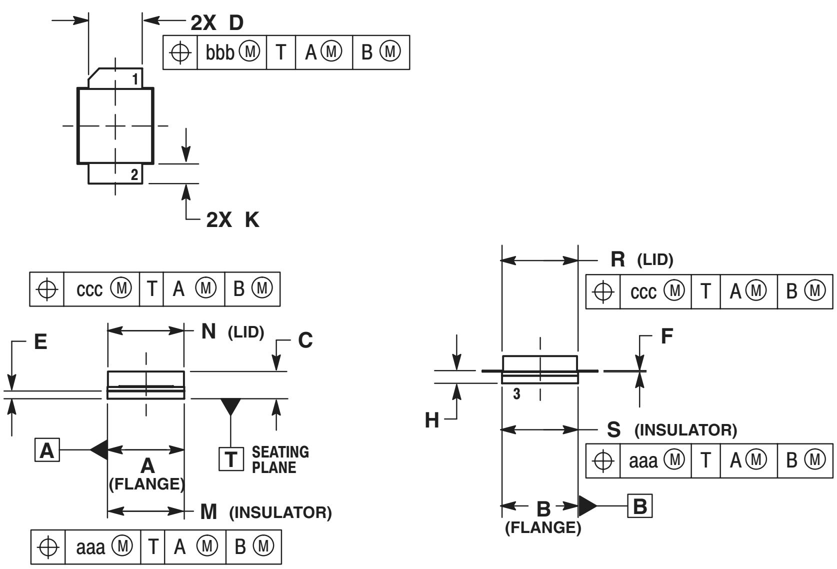


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.07	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	∅ .110	∅ .130	∅ 2.79	∅ 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E–03
ISSUE D
NI–400
MRF19045R3



NOTES:
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3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.08	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F–03
ISSUE B
NI–400S
MRF19045SR3

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