

The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and EDGE base station applications with frequencies from 921 to 960 MHz, the high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 26 volt base station equipment.

- On-Die Integrated Input Match
- Typical Performance @ Full GSM Band, 921 to 960 MHz, 26 Volts
Output Power, P1dB — 110 Watts (Typ)
Power Gain @ P1dB — 16.5 dB (Typ)
Efficiency @ P1dB — 53% (Typ)
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 921 MHz, 100 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF9100
MRF9100R3
MRF9100SR3

GSM/EDGE 900 MHz, 110 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs

CASE 465-06, STYLE 1
(NI-780)
(MRF9100)

CASE 465A-06, STYLE 1
(NI-780S)
(MRF9100SR3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	175 1.0	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, 50 ohm system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 500\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 800\text{ mAdc}$)	$V_{GS(Q)}$	3	—	5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	$V_{DS(on)}$	—	0.19	0.5	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	g_{fs}	—	8	—	S
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1.0	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Output Power, 1 dB Compression Point, CW ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 800\text{ mA}$, $f = 960\text{ MHz}$)	P_{1dB}	100	110	—	W
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 100\text{ W CW}$, $I_{DQ} = 800\text{ mA}$, $f = 960\text{ MHz}$)	G_{ps}	16	17	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 100\text{ W CW}$, $I_{DQ} = 800\text{ mA}$, $f = 960\text{ MHz}$)	η	47	51	—	%
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 100\text{ W CW}$, $I_{DQ} = 800\text{ mA}$, $f_1 = 921\text{ MHz}$ and 960 MHz , $f_2 = 940\text{ MHz}$)	IRL	— —	— –20	–10 —	dB
Third Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 100\text{ W PEP}$, $I_{DQ} = 800\text{ mA}$, $f = \text{Full GSM Band } 921\text{--}960\text{ MHz}$, Tone Spacing = 100 kHz)	IMD	—	–30	—	dBc
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 800\text{ mA}$, $P_{out} = 100\text{ W CW}$, $f = 921\text{ MHz}$, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

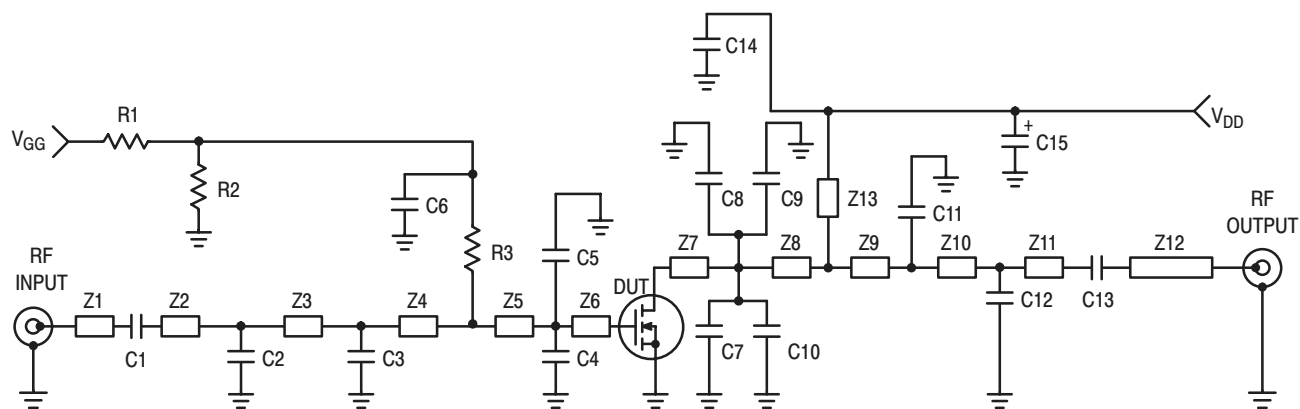


Figure 1. MRF9100 Test Circuit Schematic

Table 1. MRF9100 Test Circuit Component Designations and Values

Designators	Description
C1, C13	22 pF, 100B Chip Capacitors, ATC #100B220GW
C2, C12	2.2 pF, 100B Chip Capacitors, ATC #100B2R2BW
C3	6.8 pF, 100B Chip Capacitor, ATC #100B6R8CW
C4, C5	10 pF, 100B Chip Capacitors, ATC #100B100GW
C6, C14	33 pF, 100B Chip Capacitors, ATC #100B330JW
C7, C8, C9, C10	4.7 pF, 100B Chip Capacitors, ATC #100B4R7BW
C11	2.7 pF, 100B Chip Capacitor, ATC #100B2R7BW
C15	10 μ F, 35 V Tantalum Chip Capacitor, Vishay–Sprague #293D106X9035D
R1, R2	10 k Ω , 1/8 W Chip Resistors (0805)
R3	1 k Ω , 1/8 W Chip Resistor (0805)
Z1	0.495" x 0.087" Microstrip
Z2	0.657" x 0.087" Microstrip
Z3	0.324" x 0.087" Microstrip
Z4	0.429" x 0.087" Microstrip
Z5	0.250" x 0.790" Microstrip
Z6	0.535" x 0.790" Microstrip
Z7	0.312" x 0.790" Microstrip
Z8	0.409" x 0.790" Microstrip
Z9	0.432" x 0.087" Microstrip
Z10	0.220" x 0.087" Microstrip
Z11	0.828" x 0.087" Microstrip
Z12	0.485" x 0.087" Microstrip
Z13	1.602" x 0.087" Microstrip
Substrate	Taconic TLX8, Thickness 0.8 mm

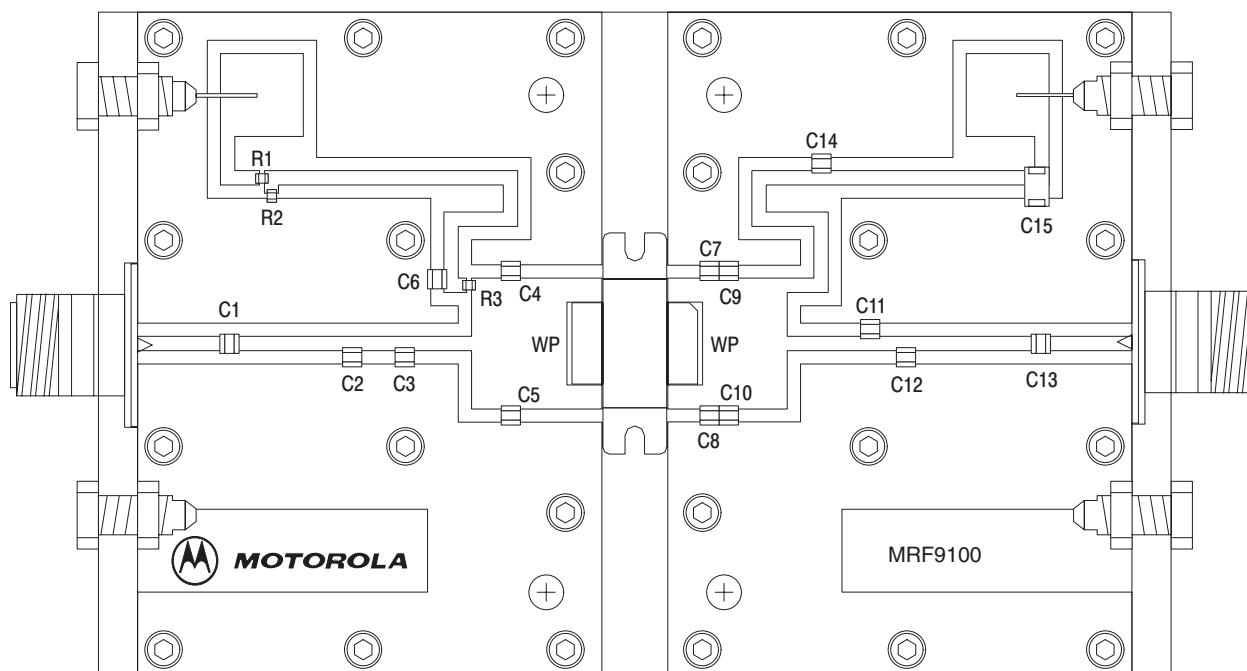


Figure 2. MRF9100 Test Circuit Component Layout

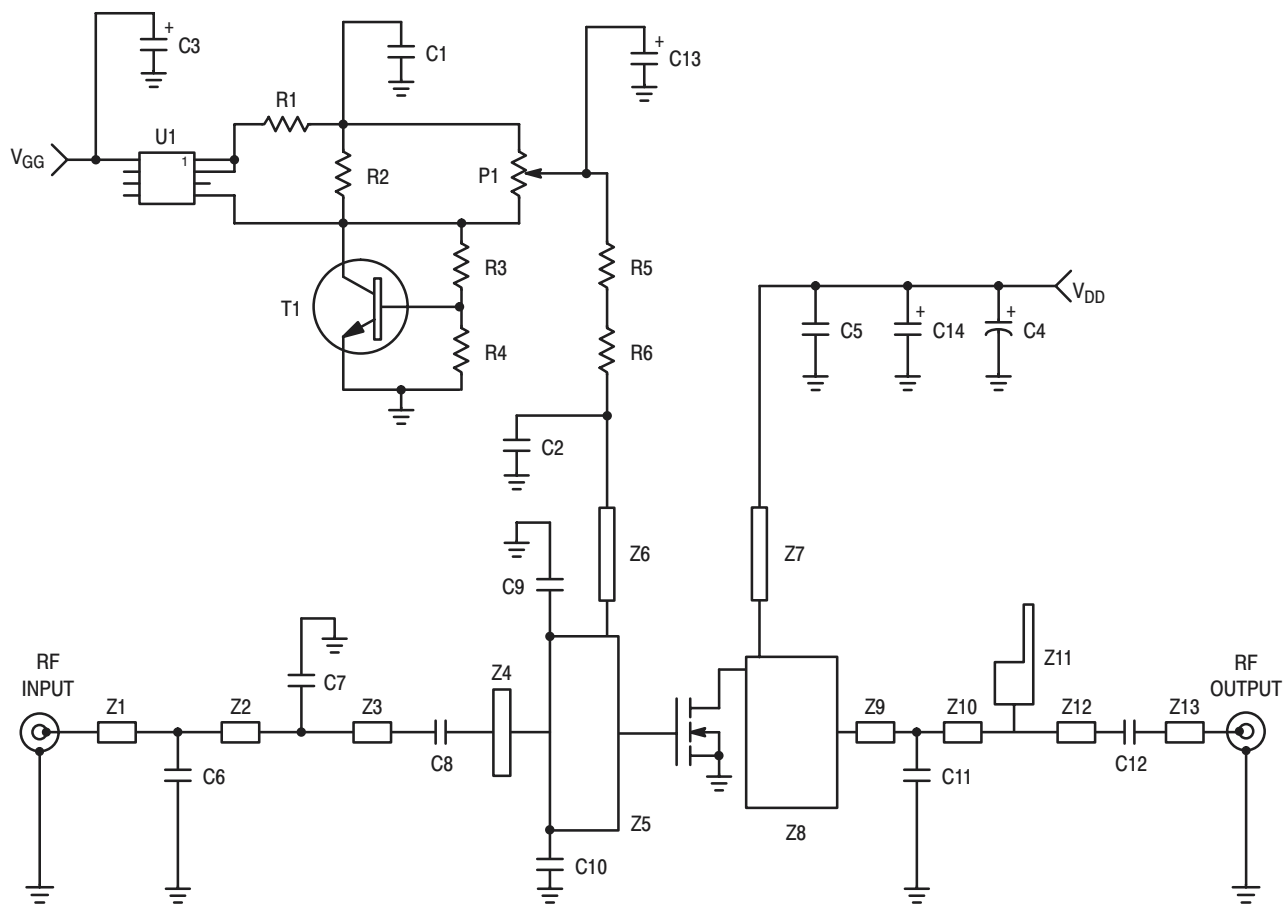


Figure 3. MRF9100 Demo Board Schematic

Table 2. GSM 900 Optimized Demo Board Component Designations and Values

Designators	Description
C1	1.0 μ F Chip Capacitor, AVX #08053G105ZATEA (0805)
C2, C5	33 pF Chip Capacitors, AVX #08051J330GBT, ACCU-P (0805)
C3, C13, C14	22 μ F, 35 V Tantalum Chip Capacitors, Kemet #T491x226K035AS4394
C4	220 μ F, 63 V Electrolytic Capacitor Radial, Philips #13668221
C6	5.6 pF Chip Capacitor, AVX #08051J5R6CBT, ACCU-P (0805)
C7	4.7 pF Chip Capacitor, AVX #08051J4R7CBT, ACCU-P (0805)
C8	22 pF Chip Capacitor, AVX #08051J220GBT, ACCU-P (0805)
C9, C10	3.9 pF Chip Capacitors, AVX #08051J3R9BBT, ACCU-P (0805)
C11	2.2 pF Chip Capacitor, AVX #08051J2R2BBT, ACCU-P (0805)
C12	33 pF, 100B Chip Capacitor, ATC #100B330JW
P1	5.0 k Ω Potentiometer CMS Cermet multi-turn, Bourns #3224W
R1	10 Ω , 1/8 W Chip Resistor (0805)
R2	1.0 k Ω , 1/8 W Chip Resistor (0805)
R3	1.2 k Ω , 1/8 W Chip Resistor (0805)
R4	2.2 k Ω , 1/8 W Chip Resistor (0805)
R5	100 Ω , 1/8 W Chip Resistor (0805)
R6	1.0 Ω , 1/8 W Chip Resistor (0805)
T1	NPN Bipolar Transistor, SOT-23, Motorola #BC847
U1	Voltage Regulator, Micro-8, Motorola #LP2951
Z1	0.916" x 0.042" Microstrip
Z2	0.169" x 0.042" Microstrip
Z3	0.212" x 0.042" Microstrip
Z4	0.090" x 0.465" Microstrip
Z5	0.465" x 0.842" Microstrip
Z6	1.776" x 0.059" Microstrip
Z7	1.802" x 0.059" Microstrip
Z8	1.094" x 0.592" Microstrip
Z9	0.085" x 0.042" Microstrip
Z10	0.198" x 0.042" Microstrip
Z11	0.253" x 0.191" + 0.292" x 0.061" Microstrip
Z12	0.181" x 0.042" Microstrip
Z13	0.282" x 0.042" Microstrip
Substrate	Taconic RF35, Thickness 0.5 mm, $\epsilon_r = 3.5$

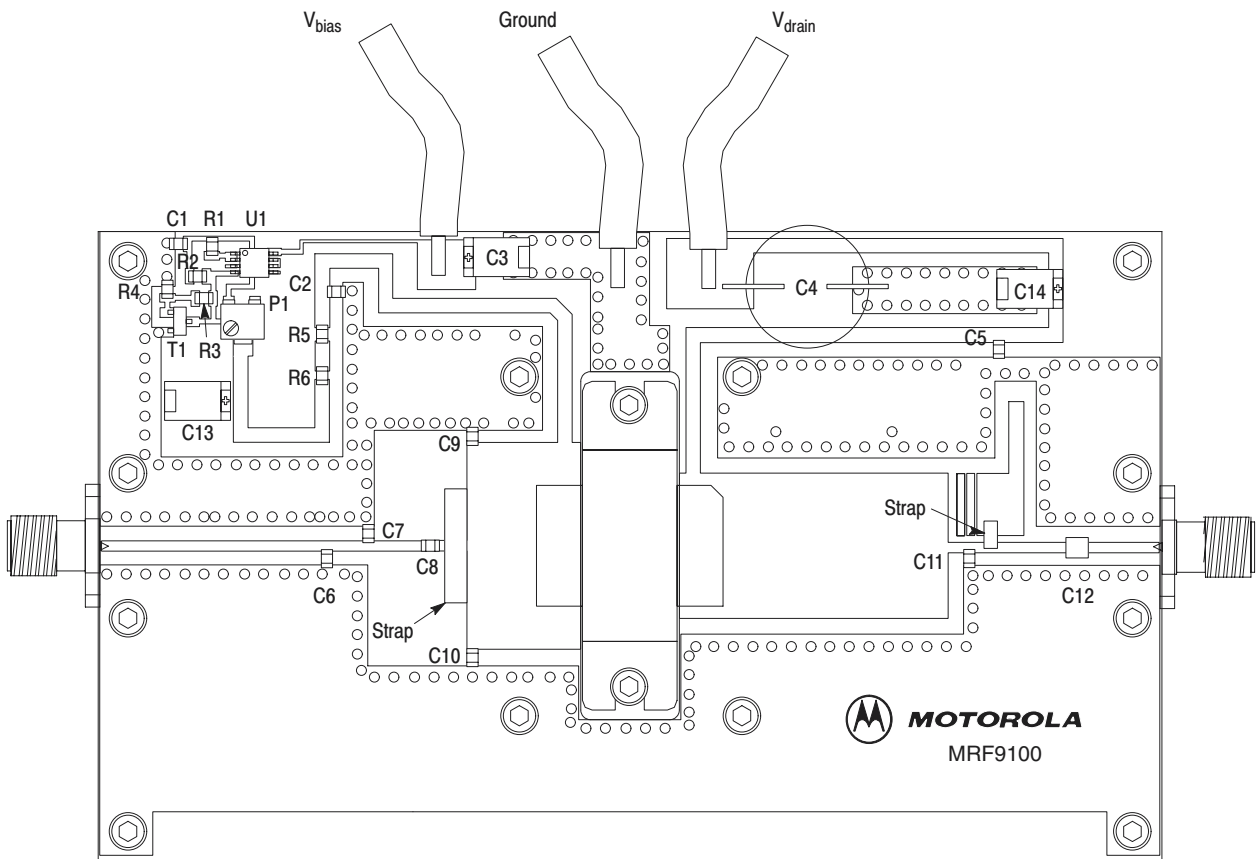


Figure 4. MRF9100 Demo Board Component Layout

TYPICAL CHARACTERISTICS

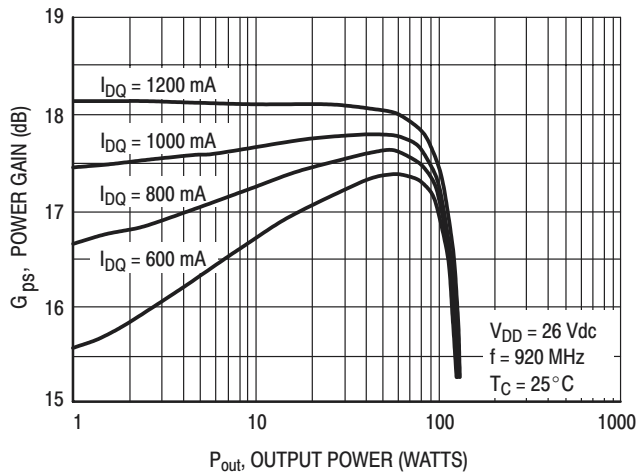


Figure 5. Power Gain versus Output Power

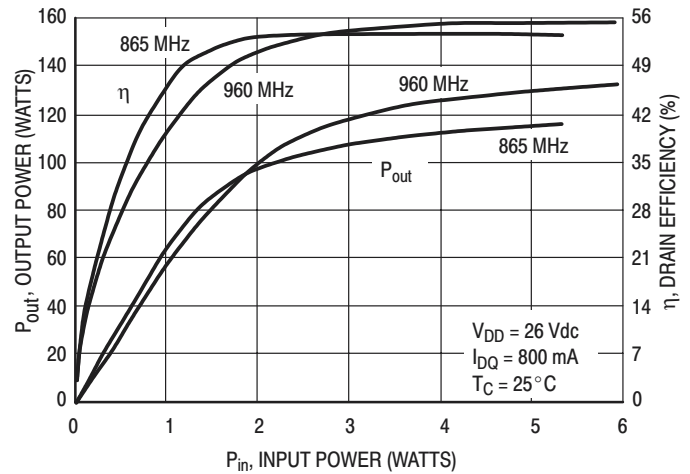


Figure 6. Output Power and Efficiency versus Input Power

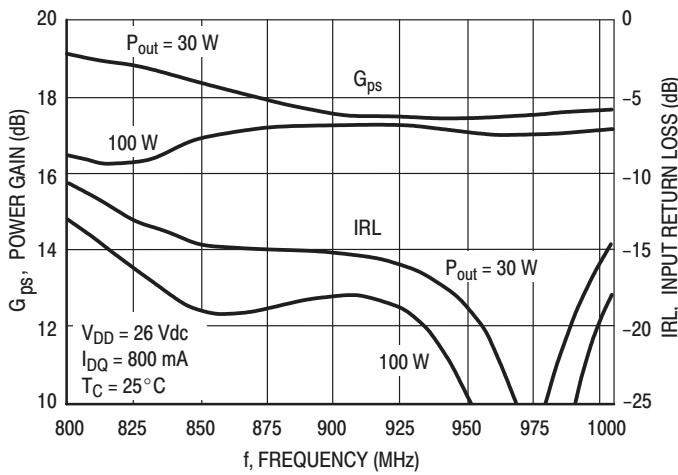


Figure 7. Power Gain and Input Return Loss versus Frequency

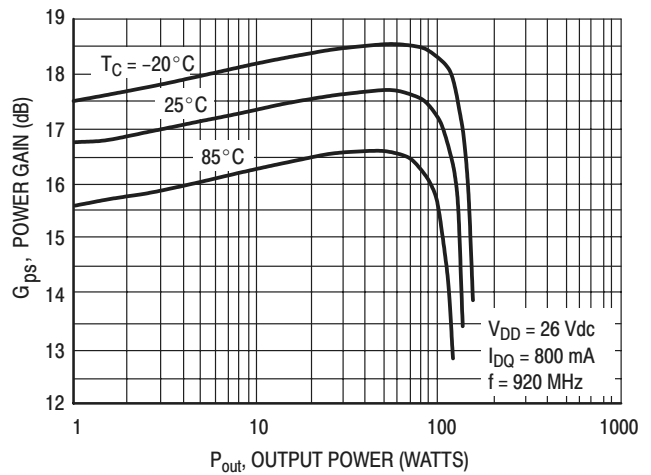


Figure 8. Power Gain versus Output Power

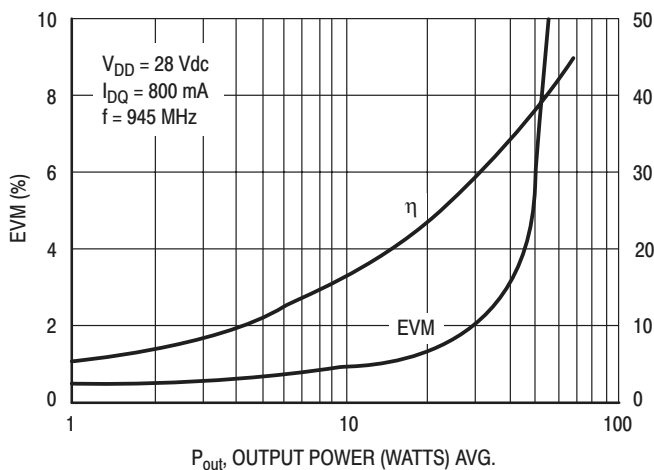


Figure 9. EVM and Efficiency versus Output Power

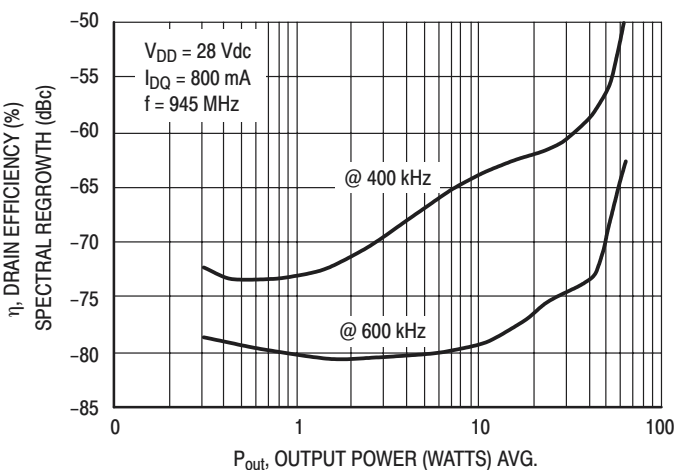
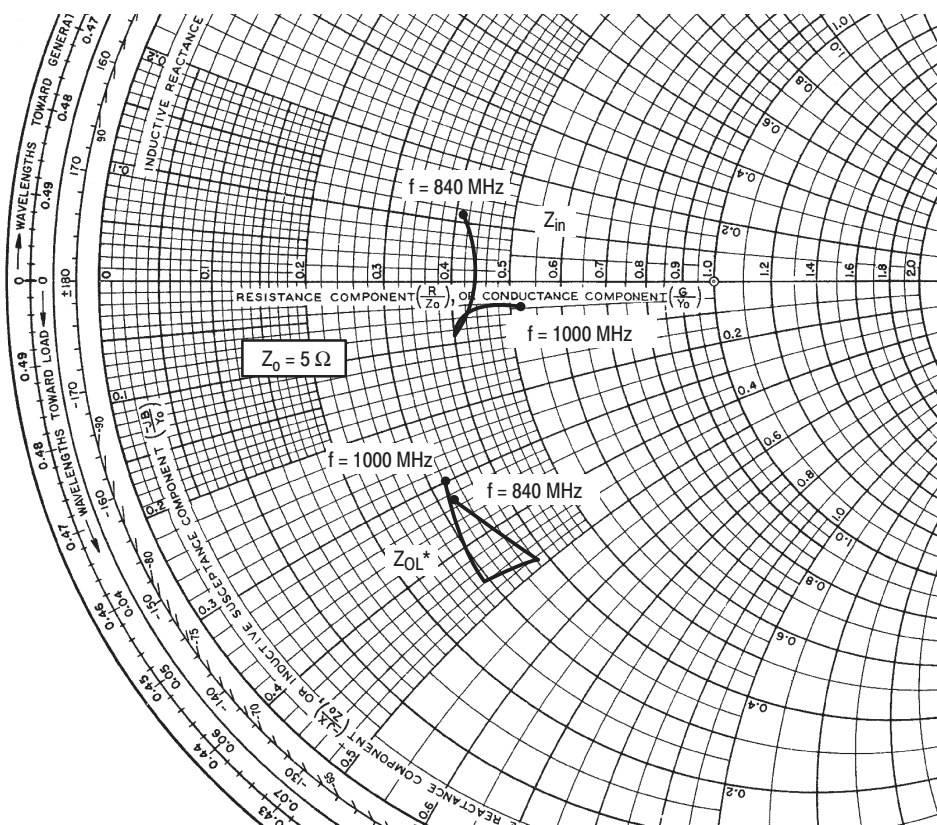


Figure 10. Spectral Regrowth versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 800 \text{ mA}$, $P_{out} = 110 \text{ W (CW)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
840	$2.04 + j0.57$	$1.62 - j1.65$
880	$2.20 + j0.16$	$1.88 - j2.45$
920	$2.00 - j0.44$	$1.79 - j2.40$
960	$2.16 - j0.25$	$1.47 - j1.82$
1000	$2.62 - j0.25$	$1.58 - j1.52$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

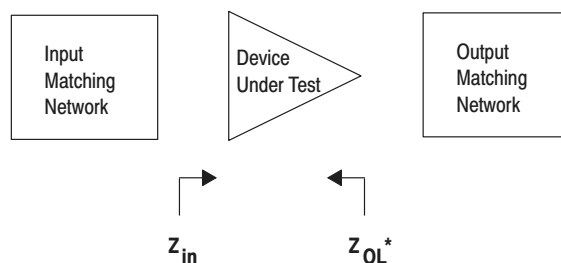
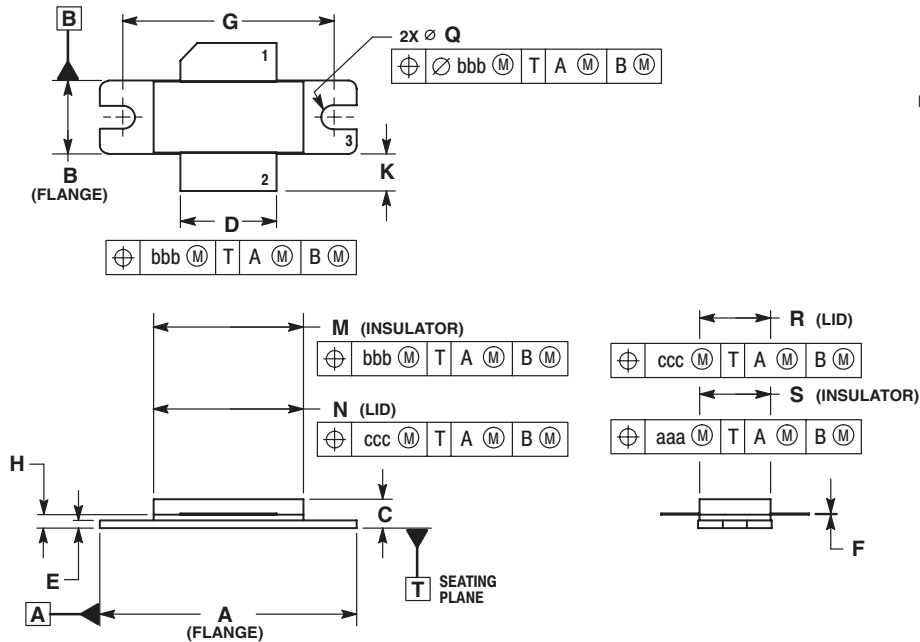


Figure 11. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS



NOTES:

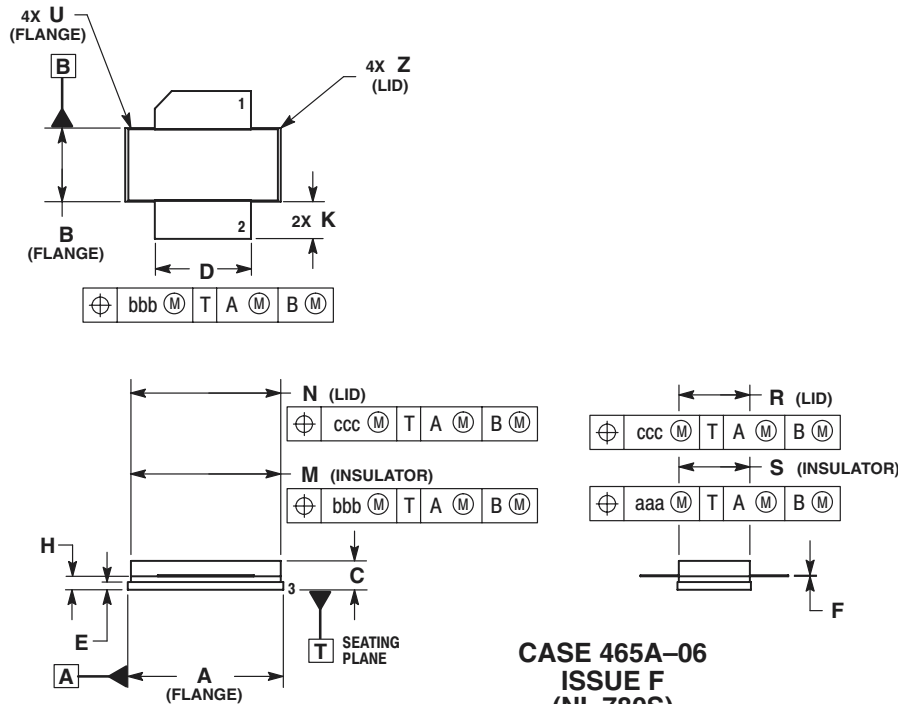
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100	BSC	27.94	BSC
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	Ø 0.118	Ø 0.138	Ø 3.00	Ø 3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005	REF	0.127	REF
bbb	0.010	REF	0.254	REF
ccc	0.015	REF	0.381	REF

STYLE 1:

- PIN 1. DRAIN
- PIN 2. GATE
- PIN 3. SOURCE

**CASE 465-06
ISSUE F
(NI-780)
(MRF9100)**



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005	REF	0.127	REF
bbb	0.010	REF	0.254	REF
ccc	0.015	REF	0.381	REF

STYLE 1:

- PIN 1. DRAIN
- PIN 2. GATE
- PIN 5. SOURCE

**CASE 465A-06
ISSUE F
(NI-780S)
(MRF9100SR3)**

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MRF9100/D