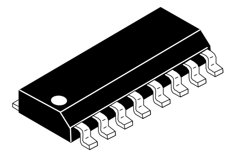
The MRFIC Line
2.4 GHz GaAs Downconverter

MRFIC2401

**2.4 GHz
DOWNCONVERTER
GaAs MONOLITHIC
INTEGRATED CIRCUIT**



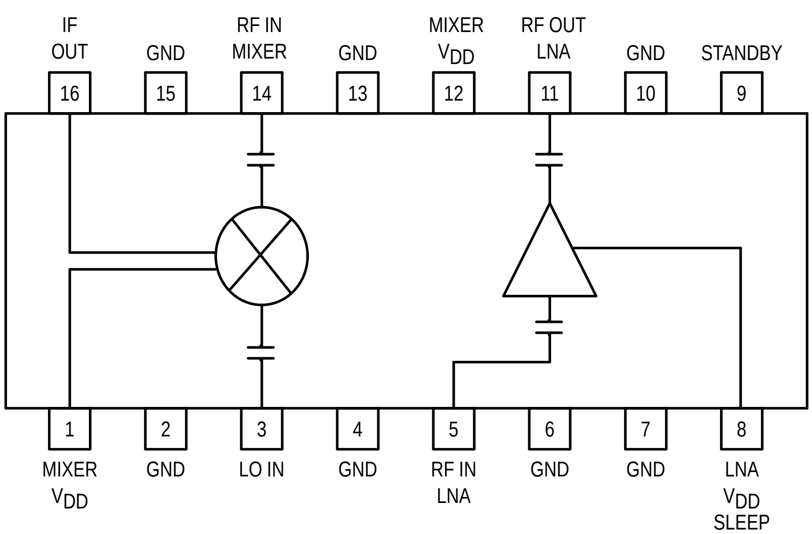
**CASE 751B-05
(SO-16)**

The MRFIC2401 is a GaAs low–noise amplifier and downmixer in a low–cost 16 lead plastic package designed for use in the 2.4 to 2.5 GHz Industrial–Scientific–Medical (ISM) band. The design is optimized for efficiency at 5.0 Volt operation at 2.45 GHz but is usable from 2.0 to 3.0 GHz in applications such as telemetry and Multichannel Multipoint Distribution System (MMDS) wireless cable TV systems. Performance is suitable for frequency hopping or direct sequence spread spectrum as well as single–frequency applications. LNA output and mixer input are available to allow image filtering.

- Single Supply Voltage = 5.0 Volts
- High Conversion Gain = 21 dB Typical Less Image Filter
- Low Supply Current = 9.5 mA Typical
- Low–Cost, Low Profile Plastic SOIC Package
- Available in Tape and Reel by Adding R2 Suffix to Part Number.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M2401

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	Vdc
Input Power, RF IN Ports	P_{RF}	+5.0	dBm
Input Power, LO IN Port	P_{LO}	+5.0	dBm
Ambient Operating Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C
Bias Control Voltage	STANDBY	6.0	Vdc



Pin Connections and Functional Block Diagram

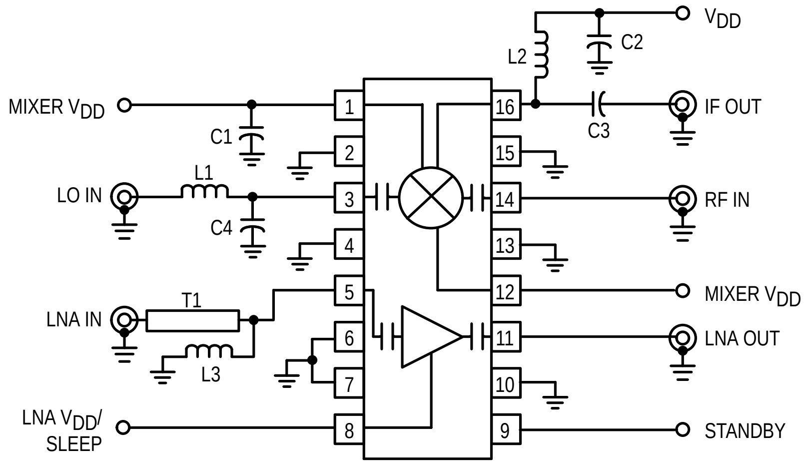
MOTOROLA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	4.75 to 5.25	Vdc
IF Frequency Range	f_{IF}	100 to 350	MHz
LO Drive Power Level	P_{LO}	–10 to 0	dBm
LO Frequency Range	f_{LO}	2050 to 2400	MHz
RF Frequency Range	f_{RF}	2400 to 2500	MHz
STANDBY Mode ON	STANDBY	V_{DD}	Vdc
STANDBY Mode OFF	STANDBY	0	Vdc
SLEEP Mode OFF	SLEEP	V_{DD}	Vdc
SLEEP Mode ON	SLEEP	0	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 Vdc, T_A = 25°C, RF = 2.45 GHz, LO = 2.125 GHz @ –5.0 dBm, STANDBY = 0 Vdc)

Characteristic	Min	Typ	Max	Unit
Conversion Gain – Downconverter (Less Image Filter Loss)	19	21	–	dB
Gain – LNA	–	17	–	dB
Conversion Gain – Mixer	–	4.0	–	dB
Noise Figure – LNA	–	1.9	–	dB
Noise Figure – Mixer	–	11	–	dB
Return Loss – Mixer Input, LO Input, LNA Output	–	10	–	dB
Input Third Order Intercept – Downconverter (Less Image Filter Loss)	–	–18	–	dBm
Input Third Order Intercept – LNA	–	–13	–	dBm
Input Third Order Intercept – Mixer	–	0	–	dBm
Reverse Isolation – Downconverter (Less Image Filter Loss)	–	30	–	dB
Isolation – LO to RF, LO to IF	–	20	–	dB
Supply Current – Downconverter	–	9.5	11	mA
SLEEP Mode Supply Current – Downconverter (No LO, STANDBY= 5 Vdc, V_{DD}/SLEEP = 5 Vdc)	–	600	–	μA
Turn On, Turn Off Time – LNA	–	1.0	–	μs



325 MHz IF:
C1, C2 – 100 pF
C3 – 5.6 pF
C4 – 0.5 pF
L1 – 4.7 nH
L2 – 8.2nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92 MILS

240 MHz IF:
C1, C2 – 100 pF
C3 – 5.6 pF
C4 – 0.5 pF
L1 – 8.2 nH
L2 – 18 nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92mils

Board Material – FR4

110 MHz IF:
C1 – 100 pF
C2 – 1000 pF
C3 – 8.2 pF
C4 – 0.3 pF
L1 – 8.2 nH
L2 – 82 nH
L3 – 6.8 nH
T1 – 100 Ω Line, 92 mils

Figure 1. Applications Circuit Configuration

f	LO Z_{in}	
Frequency (GHz)	**R**	**jX**
2.0	39.7	23.9
2.1	35.7	22.1
2.2	32.1	19.8
2.3	29.1	17.1
2.4	26.5	14.0
2.5	24.4	10.7

Table 1. Selected Port Impedances (from Conjugate Match)

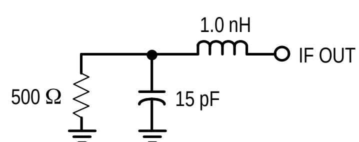


Figure 2. Equivalent IF Output Circuit

Table 2. LNA Scattering Parameters
(VDD = 5 V, T_A = 25°C, 50 Ω System)

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\lvert S_{11} \rvert$	∠ φ	$\lvert S_{21} \rvert$	∠ φ	$\lvert S_{12} \rvert$	∠ φ	$\lvert S_{22} \rvert$	∠ φ
2000	0.823	–50.8	5.35	14.3	0.0373	164.2	0.609	–64.1
2050	0.783	–62.9	6.13	–0.3	0.0425	154.3	0.558	–78.7
2100	0.752	–76.8	6.56	–18.3	0.0477	138	0.497	–94.3
2150	0.713	–89.8	6.8	–34	0.05	121	0.425	–110.7
2200	0.656	–104.2	7.14	–50.2	0.0511	106.4	0.343	–129.6
2250	0.583	–119	7.44	–66.4	0.0527	91.8	0.25	–152.3
2300	0.509	–134.1	7.8	–84.2	0.0554	78.1	0.155	176.2
2350	0.425	–148.2	7.86	–102.6	0.0579	59.89	0.088	120.7
2400	0.34	–163.6	7.84	–119.4	0.0552	42.31	0.111	43.8
2450	0.261	–177.8	7.78	–138.1	0.0528	28.27	0.191	2.2
2500	0.175	173.4	7.43	–154.6	0.0514	13.37	0.269	–21.9
2550	0.103	170.4	7.15	–170.6	0.0484	–0.842	0.338	–41.8
2600	0.056	–160.5	6.72	173	0.0455	–15.4	0.393	–59.4
2650	0.067	–130.7	6.47	159.1	0.0422	–28.11	0.436	–76.2
2700	0.102	–117.8	6.25	142.3	0.039	–41.5	0.472	–92.2
2750	0.132	–119.5	5.53	127.1	0.0353	–53.47	0.496	–107.5
2800	0.166	–125.2	5.26	117.5	0.0329	–63.28	0.513	–121.3
2850	0.19	–134.8	5.15	102.4	0.0309	–75.04	0.533	–135
2900	0.219	–144.8	4.71	87.6	0.0283	–87.86	0.547	–148.8
2950	0.235	–155.9	4.43	76.1	0.025	–95.83	0.559	–162.4
3000	0.262	–165.9	4.08	62.3	0.0235	–108.4	0.57	–175.7

TYPICAL CHARACTERISTICS

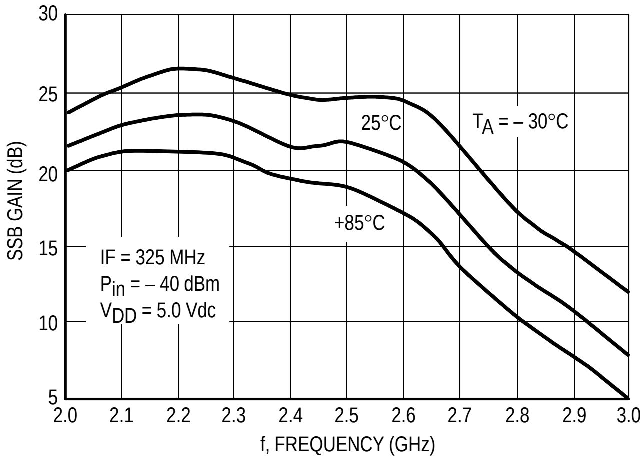


Figure 3. Downconverter Gain versus Frequency

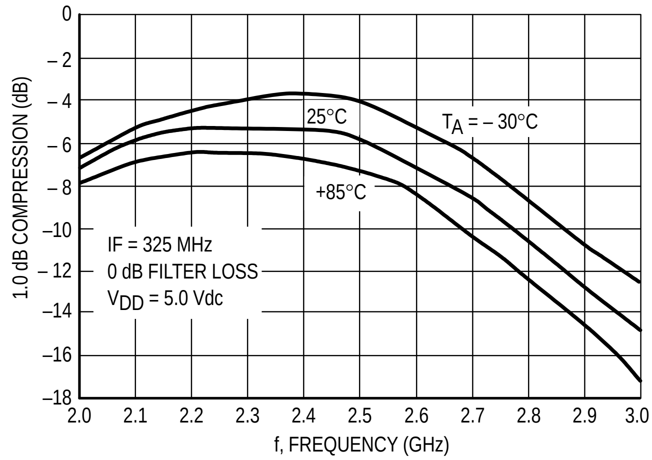


Figure 4. Downconverter 1.0 dB Compression versus Frequency

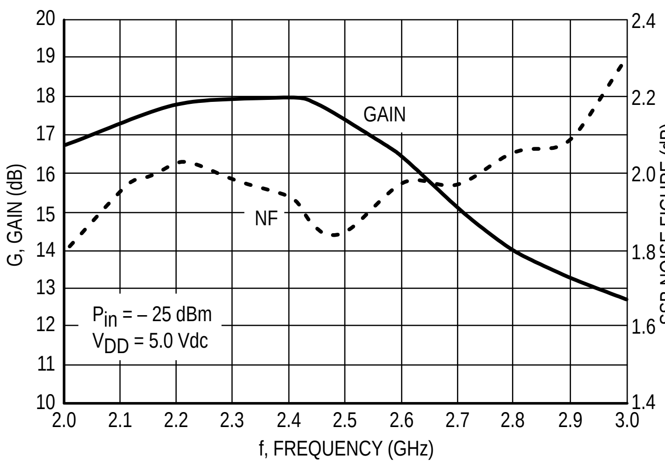


Figure 5. LNA Gain and Noise Figure versus Frequency

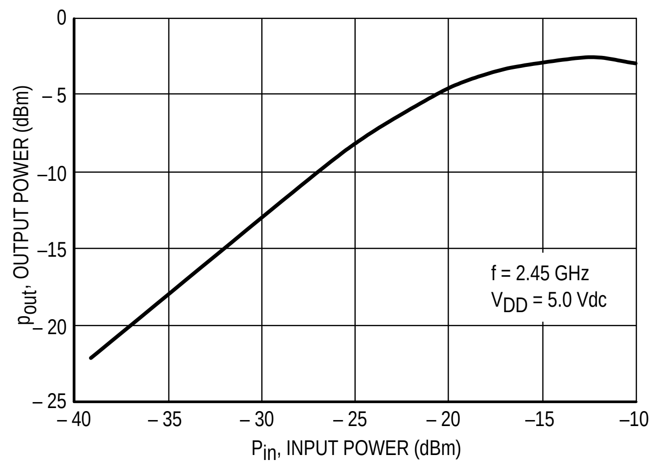


Figure 6. LNA Output Power versus Input Power

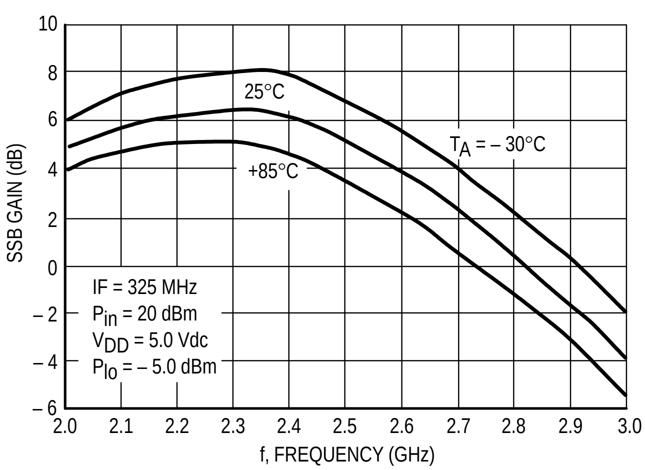


Figure 7. Mixer Conversion Gain versus Frequency

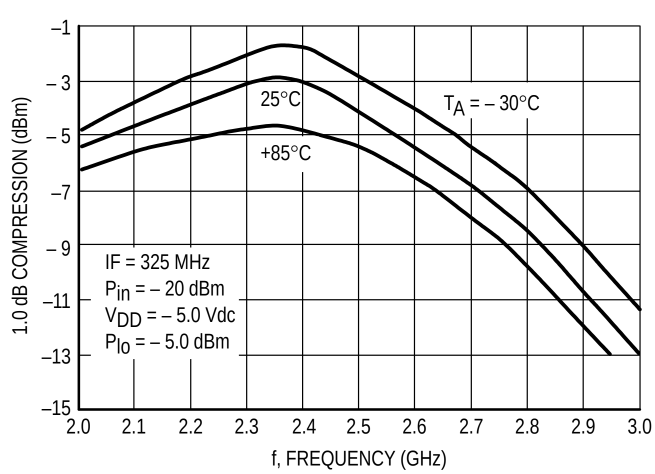


Figure 8. Mixer 1.0 dB Compression versus Frequency

TYPICAL CHARACTERISTICS

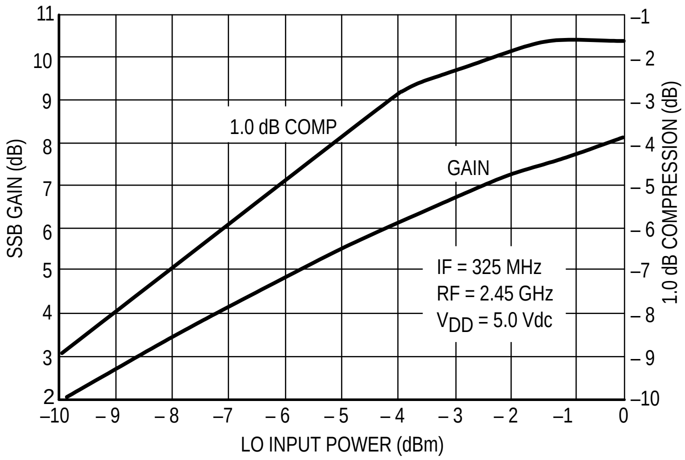


Figure 9. Mixer 1.0 dB Compression and Gain versus LO Power

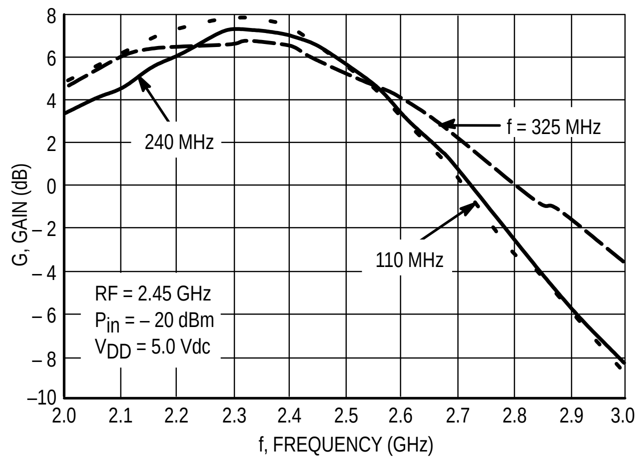


Figure 10. Mixer Gain versus Frequency

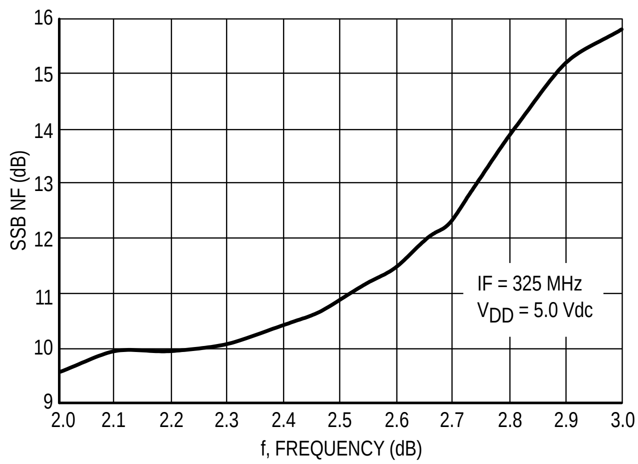


Figure 11. Mixer Noise Figure versus Frequency

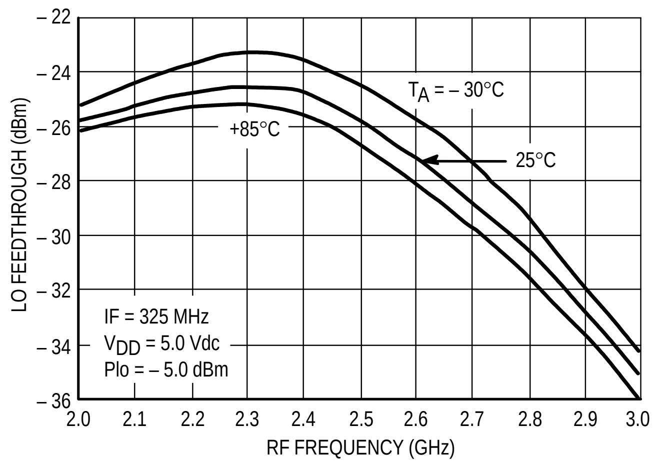


Figure 12. Mixer LO Feedthrough versus RF Frequency

DESIGN AND APPLICATIONS INFORMATION

The MRFIC2401 consists of a two–stage GaAs MESFET low noise amplifier and a single ended MESFET mixer. The LNA design conserves bias current through stacking of the two FETs, thus reusing the current. The mixer consists of a common gate stage driving a common source stage with the IF output being the drain of the common source stage shunted with 15 pF. The LNA output and mixer input have been separated to allow the addition of an external image filter. Such a filter, usually ceramic, is useful in improving the mixer noise figure and third order intercept performance. It also provides LO rejection to reduce the amount of LO power which may leak to the antenna. Alternatively, image trapping can be implemented at the LNA input or output with discrete or distributed components.

The design has been optimized for best performance from 2.4 to 2.5 GHz, but the device is usable with reduced performance from 2.0 to 3.0 GHz as shown in the performance curves. These curves were generated using the circuit shown in Figure 1 and performance above 2.5 GHz can be enhanced by rematching the LO input port. Matching circuit details are shown for IFs of 110 MHz, 240 MHz, and 325 MHz matched to 50 Ω and LO frequencies consistent with an RF frequency of 2.45 GHz. Customized IF matching can be accomplished by using the Equivalent IF Output circuit model shown in Figure 2. The best gain/noise figure tradeoff match is shown in the LNA input impedance column of Table 1. The LO input impedance is shown in the same table. These numbers are derived from conjugate match measurements of the applications circuit. The LNA output and mixer input are matched to 50 Ω.

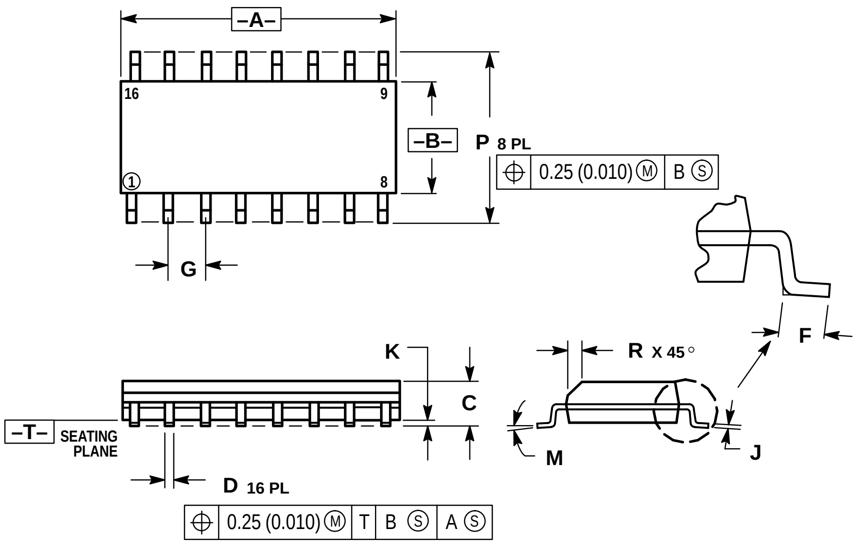
As with all RF circuitry, layout is important. Controlled impedance lines should be used at all RF ports. RF bypassing of power supply connections as close to the part as possible, while not always shown in the applications circuit, are recommended. Additional power supply “stiffening” and digital transient bypassing should be accomplished with electrolytic or tantalum capacitors.

The device can be placed in a reduced current “standby” mode by applying 5.0 Vdc to the STANDBY pin and removing the LO drive. Further current reduction “sleep” mode, is enabled by applying 0 Vdc to V_{DD}/SLEEP. This sleep mode can also be used to disable the LNA under high signal level conditions and give higher input intercept point if V_{DD} is still applied to the mixer.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced poduct, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B–05
ISSUE J

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