

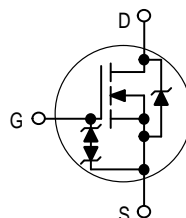
## Advance Information

### TMOS E-FET™

## High Energy Power FET D2PAK for Surface Mount N-Channel Enhancement-Mode Silicon Gate

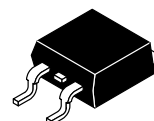
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor-Absorbs High Energy in the Avalanche Mode
- ESD Protected. Designed to Typically Withstand 400 V Machine Model and 4000 V Human Body Model.



**MTB55N06Z**

TMOS POWER FET  
55 AMPERES  
60 VOLTS  
RDS(on) = 18 mΩ



CASE 418B-02, Style 2  
D2PAK

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DS</sub>	60	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 1.0 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage — Continuous — Non-Repetitive (t <sub>p</sub> ≤ 10 ms)	V <sub>GS</sub> V <sub>GSM</sub>	±20 ±40	Vdc Vpk
Drain Current — Continuous @ T <sub>C</sub> = 25°C — Continuous @ T <sub>C</sub> = 100°C — Single Pulse (t <sub>p</sub> ≤ 10 μs)	I <sub>D</sub> I <sub>D</sub> I <sub>DM</sub>	55 35.5 165	Adc Adc Apk
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C Total Power Dissipation @ T <sub>A</sub> = 25°C (1)	P <sub>D</sub>	113 0.91 2.5	Watts W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	– 55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy — Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 25 Vdc, V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 10 Vdc, Peak I <sub>L</sub> = 55 Apk, L = 0.3 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	454	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	R <sub>θJC</sub> R <sub>θJC</sub> R <sub>θJA</sub>	1.1 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

E-FET is a trademark of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.



**MTB55N06Z****ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\text{ }\mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 —	— 53	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current ( $V_{DS} = 60\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ) ( $V_{DS} = 60\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$I_{DSS}$	— —	— —	1.0 10	$\mu\text{Adc}$	
Gate-Body Leakage Current ( $V_{GS} = \pm 20\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	100	nAdc	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{Adc}$ ) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	3.0 6.0	4.0 —	Vdc mV/°C	
Static Drain-to-Source On-Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 27.5\text{ Adc}$ )	$R_{DS(on)}$	—	14	18	m $\Omega$	
Drain-to-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ ) ( $I_D = 55\text{ Adc}$ ) ( $I_D = 27.5\text{ Adc}$ , $T_J = 125^\circ\text{C}$ )	$V_{DS(on)}$	— —	0.825 0.74	1.2 1.0	Vdc	
Forward Transconductance ( $V_{DS} = 4.0\text{ Vdc}$ , $I_D = 27.5\text{ Adc}$ )	gFS	12	15	—	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	$(V_{DS} = 25\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , f = 1.0 MHz)	$C_{iss}$	—	1390	pF	
Output Capacitance		$C_{oss}$	—	520		
Transfer Capacitance		$C_{rss}$	—	119		
SWITCHING CHARACTERISTICS (2)						
Turn-On Delay Time	$(V_{DD} = 30\text{ Vdc}$ , $I_D = 55\text{ Adc}$ , $V_{GS(on)} = 10\text{ Vdc}$ , $R_G = 9.1\text{ }\Omega$ )	$t_{d(on)}$	—	27	ns	
Rise Time		$t_r$	—	157		
Turn-Off Delay Time		$t_{d(off)}$	—	116		
Fall Time		$t_f$	—	126		
Gate Charge (See Figure 8)	$(V_{DS} = 48\text{ Vdc}$ , $I_D = 55\text{ Adc}$ , $V_{GS} = 10\text{ Vdc}$ )	$Q_T$	—	40	nC	
		$Q_1$	—	7.0		
		$Q_2$	—	18		
		$Q_3$	—	15		
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	$(I_S = 55\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ ) $(I_S = 55\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$V_{SD}$	— —	0.93 0.82	1.1 —	Vdc
Reverse Recovery Time	$(I_S = 55\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $dI_S/dt = 100\text{ A}/\mu\text{s}$ )	$t_{rr}$	—	57	—	ns
		$t_a$	—	32	—	
		$t_b$	—	25	—	
Reverse Recovery Stored Charge		$Q_{RR}$	—	0.11	—	$\mu\text{C}$
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from drain lead 0.25" from package to center of die)	$L_D$	— —	3.5 4.5	— —	nH	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	$L_S$	—	7.5	—		

(1) Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

(2) Switching characteristics are independent of operating junction temperature.

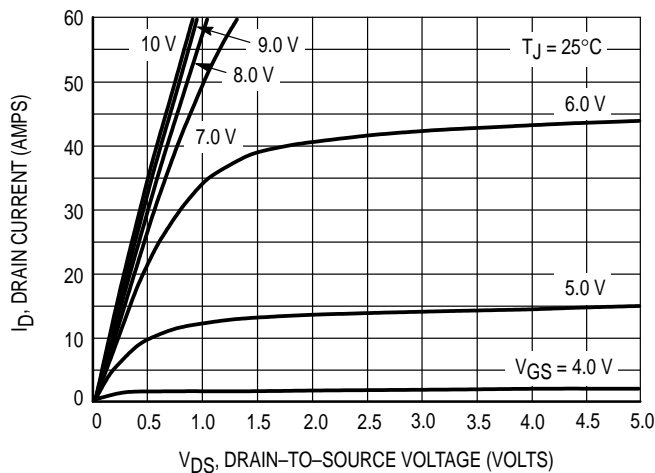


Figure 1. On-Region Characteristics

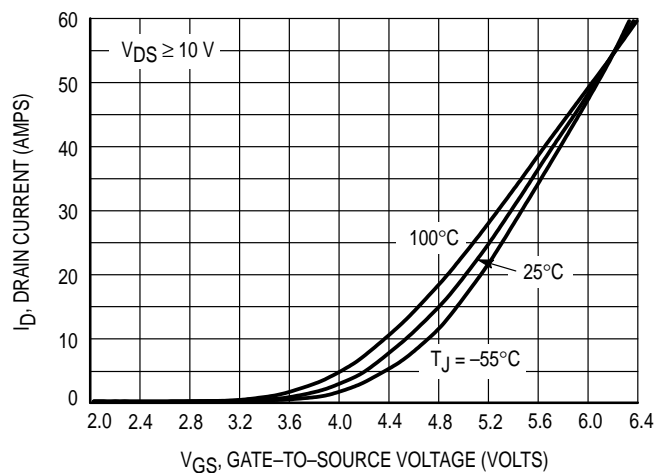


Figure 2. Transfer Characteristics

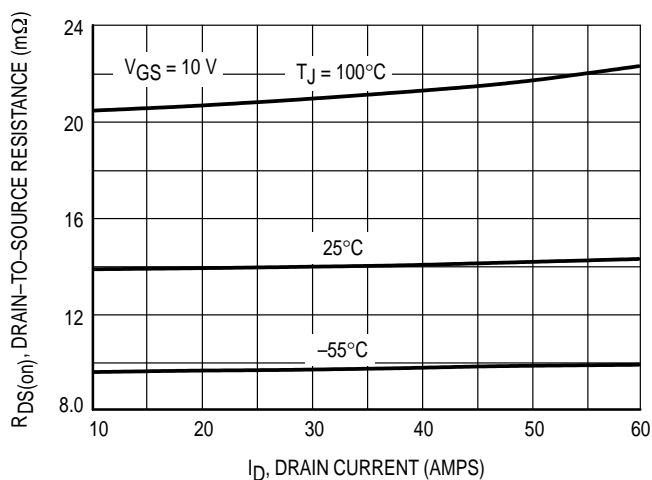


Figure 3. On-Resistance versus Drain Current and Temperature

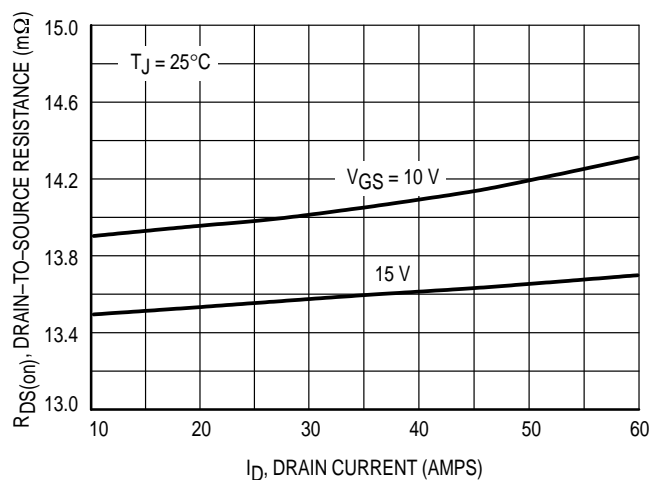


Figure 4. On-Resistance versus Drain Current and Gate Voltage

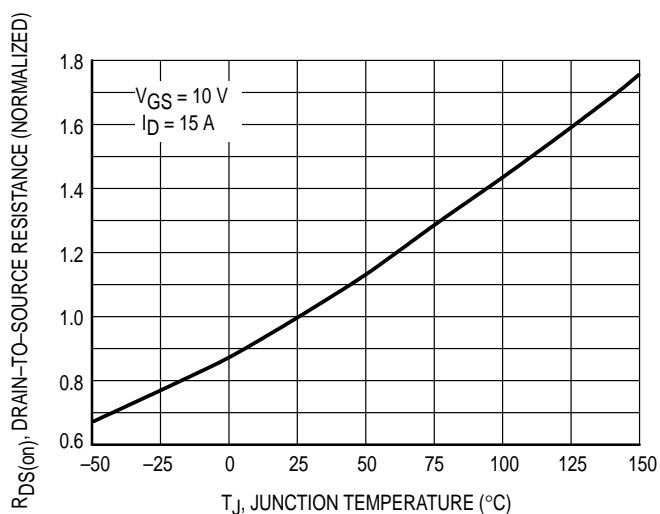


Figure 5. On-Resistance Variation with Temperature

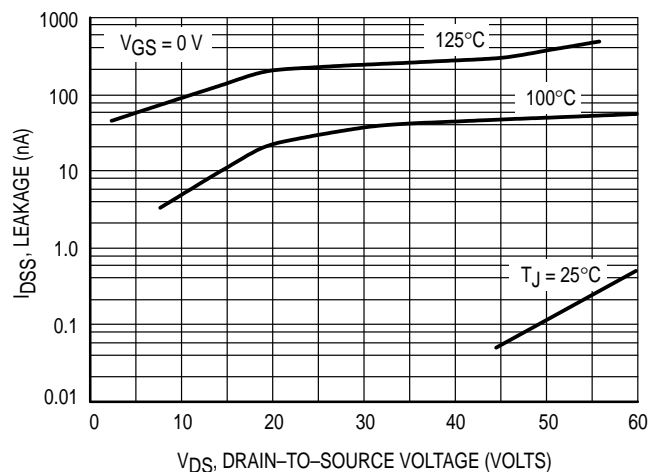
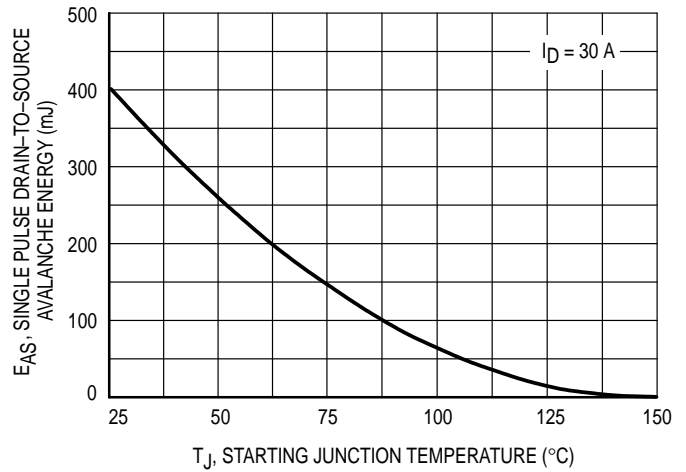
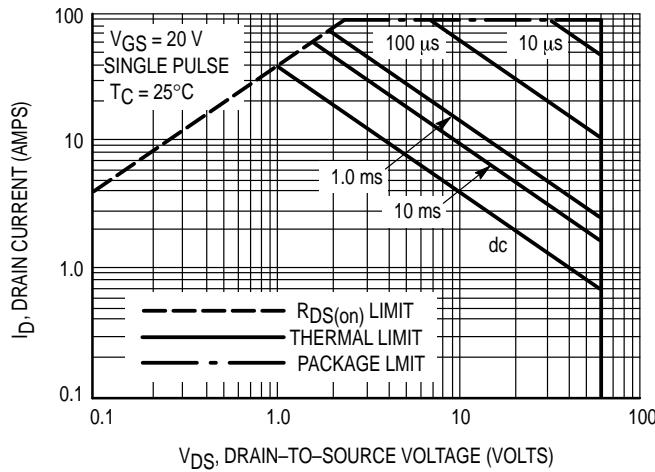
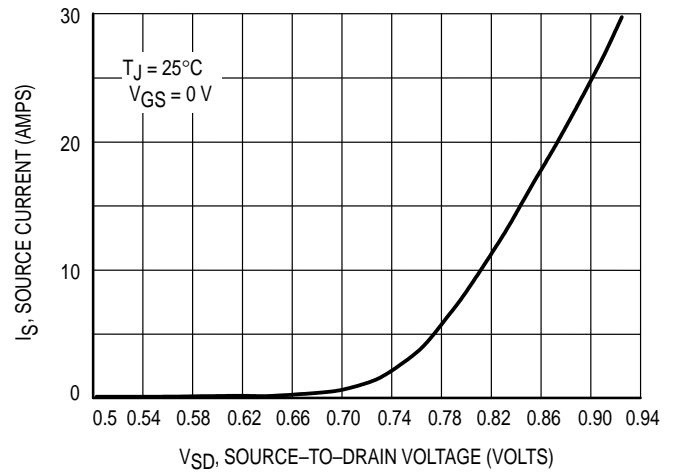
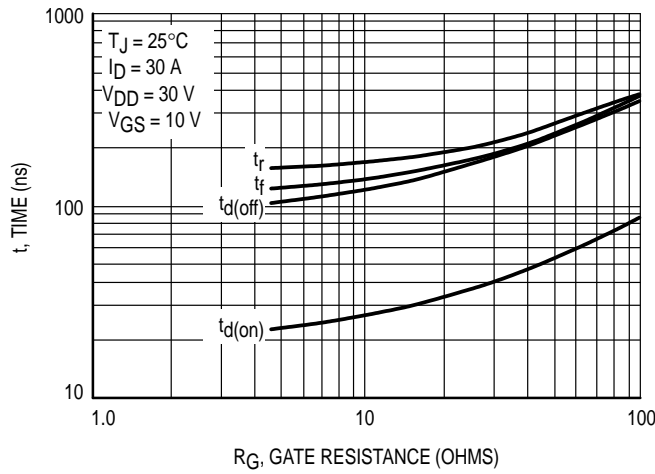
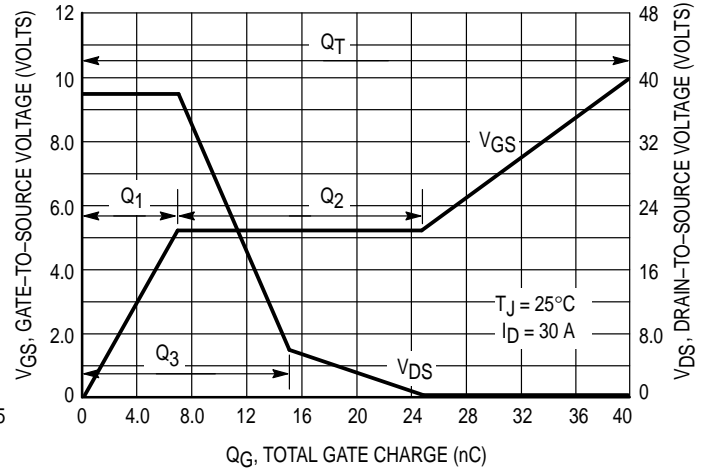
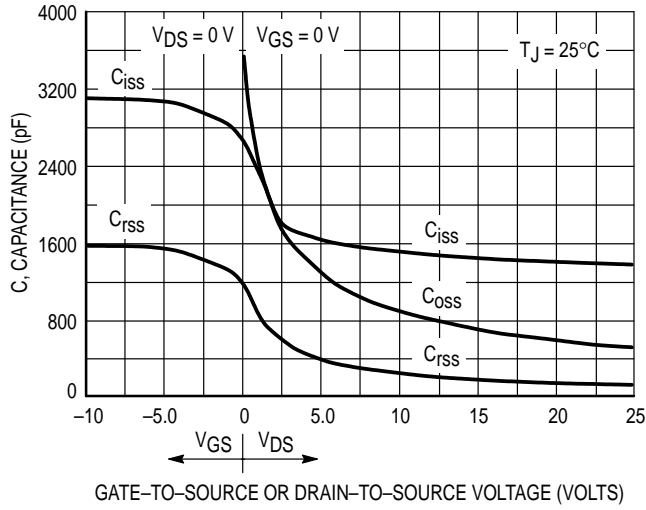


Figure 6. Drain-to-Source Leakage Current versus Voltage



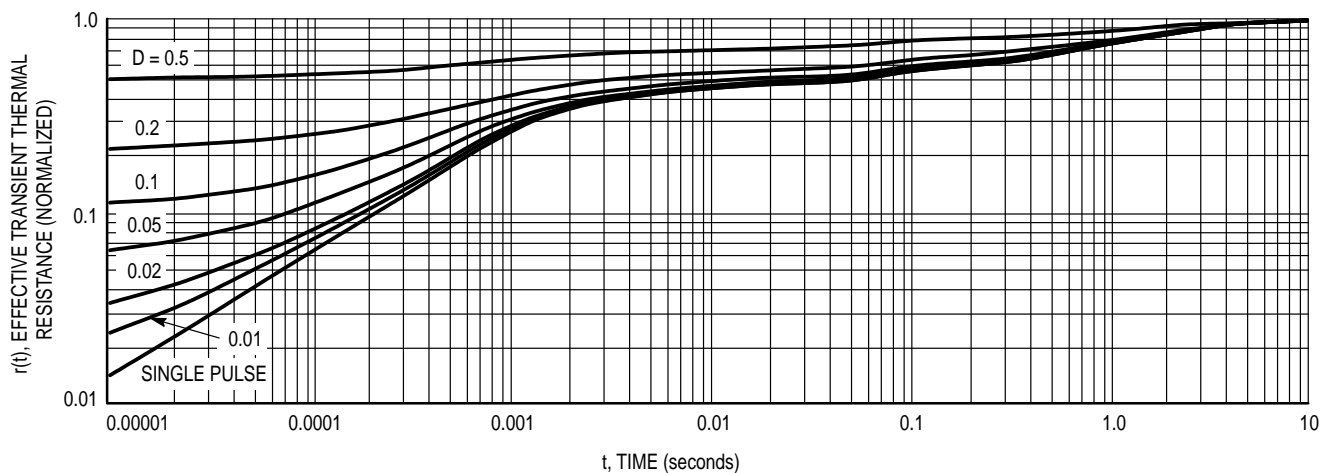
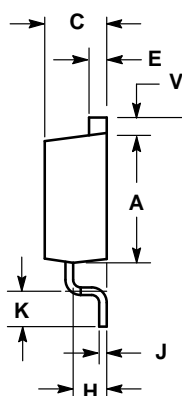
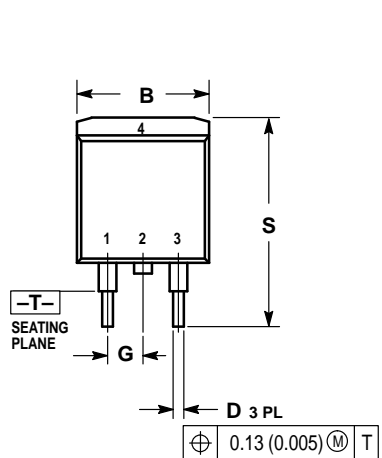


Figure 13. Thermal Response

## PACKAGE DIMENSIONS




STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

CASE 418B-02  
ISSUE B

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**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,  
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

**Mfax™:** RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609  
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**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

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