

## Preliminary Information

# Adjustable Dual Output Switching Power Supply

The 34710 is a dual-output power regulator IC that integrates a switching regulator, a linear regulator, supervisor circuitry, and a power supply sequencer. With a wide operating input voltage range of 12 V to 32 V and robust temperature limits, the 34710 is applicable in many commercial and industrial applications that use an MCU.

A user-selectable 5.0 V/3.3 V buck switching regulator is provided for board-level I/Os and user circuitry. The regulator is capable of delivering up to 1.0 A. The MCU core voltage is an adjustable 3.3 V/2.5 V/1.8 V/1.5 V linear voltage regulator that can supply up to 500 mA.

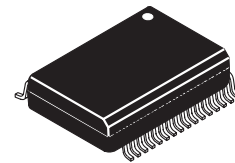
The switching and linear regulator output voltage are determined through three digital input mode terminals that can be controlled by an MCU.

### Features

- High-Current Adjustable 5.0 V/3.3 V Switching Regulator
- Low Noise User-Selectable 3.3 V/2.5 V/1.8 V/1.5 V Linear Regulator
- On-Chip Thermal Shutdown and Error Reset Circuitry
- Supervisory Functions (Power-ON Reset and Error Reset Circuitry)
- Sequenced I/O and Core Voltages
- Pb-Free Packaging Designated by Suffix Code EW

**34710**

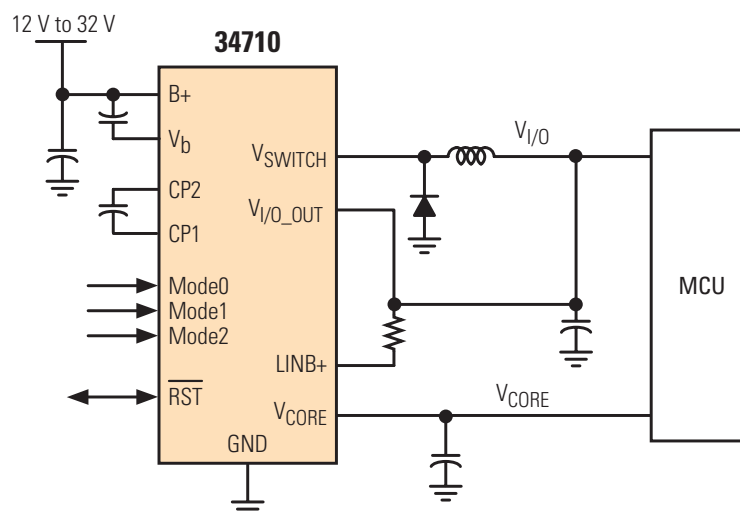
## ADJUSTABLE DUAL OUTPUT SWITCHING POWER SUPPLY



EW (Pb-FREE) SUFFIX  
CASE 1324-02  
32-LEAD SOICW-EP

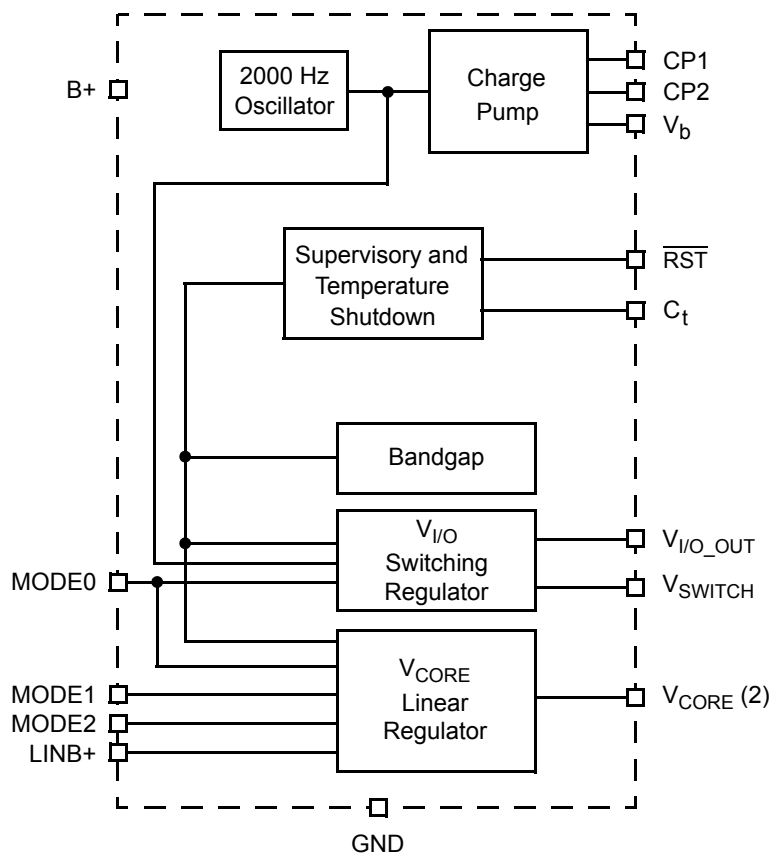
### ORDERING INFORMATION

Device	Temperature Range (T <sub>A</sub> )	Package
PC34710EW/R2	0°C to 85°C	32 SOICW-EP

**34710 Simplified Application Diagram**

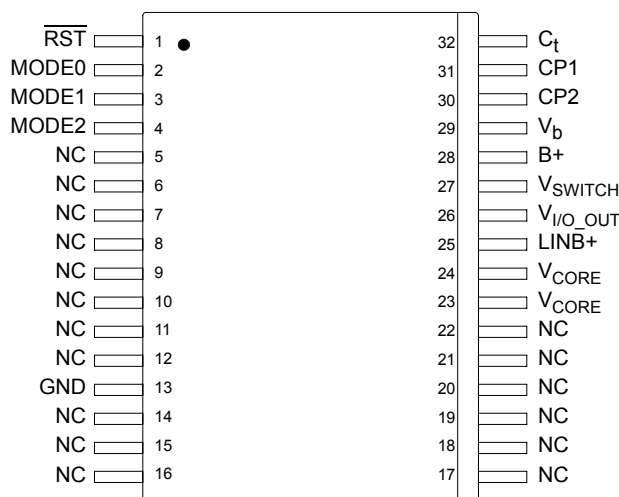
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**Figure 1. 34710 Simplified Internal Block Diagram**

# Freescale Semiconductor, Inc.



## TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1	$\overline{\text{RST}}$	Reset	Reset input and output. This terminal is open drain.
2 3 4	MODE0 MODE1 MODE2	Mode Control	These input terminals control $V_{I/O\_OUT}$ and $V_{CORE}$ output voltages.
5–12, 14–22	NC	No Connects	No internal connection to this terminal.
13	GND	Ground	Ground.
23, 24	$V_{CORE}$	Core Voltage Regulator Output	Core regulator output voltage.
25	LINB+	Core Voltage Regulator Input	Core regulator input voltage.
26	$V_{I/O\_OUT}$	$V_{I/O}$ Switching Regulator Feedback	Feedback terminal for $V_{I/O}$ switching regulator and internal logic supply.
27	$V_{SWITCH}$	$V_{I/O}$ Switching Regulator Switch Output	$V_{I/O}$ switching regulator switching output.
28	B+	Power Supply Input	Regulator input voltage.
29	$V_b$	Boost Voltage	Boost voltage storage node.
30	CP2	Switching Capacitor 2	Charge pump capacitor connection 2.
31	CP1	Switching Capacitor 1	Charge pump capacitor connection 1.
32	$C_t$	Reset Delay Capacitor	Reset delay adjustment capacitor.

## MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Max	Unit
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### GLOBAL ABSOLUTE MAXIMUM RATINGS

Input Power Supply Voltage $I_{B+} = 0 \text{ A}$	$V_{B+}$	-0.3 to 36	V
Terminal Soldering Temperature (Note 1)	$T_{\text{SOLDER}}$	260	°C
Power Dissipation (Note 2)	$P_D$	3.0	W
ESD Standoff Voltage Non-Operating, Unbiased, Human Body Model (Note 3)	$V_{\text{ESD1}}$	±2000	V
Thermal Resistance Junction-to-Ambient (Note 4) Junction-to-Ambient (Note 2) Junction-to-Case	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JC}$	45 25 2.0	°C/W

### GLOBAL OPERATING RATINGS

Operating Ambient Temperature	$T_A$	0 to 85	°C
Operating Device Junction Temperature	$T_J$	105	°C
Input Power Supply Voltage $I_{B+} = 0 \text{ A}$ to 3.0 A	$V_{B+}$	12 to 32	V
Quiescent Bias Current from B+ (Note 5) $V_{B+} = 12 \text{ V}$ to 32 V	$I_{B+(q)}$	7.5	mA
Operating Junction Temperature	$T_J$	-0 to 105	°C

### $V_{I/O}$ SWITCHING REGULATOR (Note 6)

Maximum Output Voltage Startup Overshoot ( $C_{OUT} = 330 \mu\text{F}$ ) MODE0 = 0 MODE0 = Open	$V_{I/O}(\text{STARTUP})$	5.4 3.6	V
Maximum Output Current $T_A = 0^\circ\text{C}$ to $105^\circ\text{C}$	$I_{V/I/O}$	1.2	A

#### Notes

- Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- With 2.0 in<sup>2</sup> of copper heatsink.
- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100 \text{ pF}$ ,  $R_{ZAP} = 1500 \Omega$ ).
- With no additional heatsinking.
- Maximum quiescent power dissipation is 0.25 W.
- $12 \text{ V} \leq V_{B+} \leq 32 \text{ V}$  and  $-20^\circ\text{C} \leq T_J \leq 145^\circ\text{C}$  unless otherwise noted.

## MAXIMUM RATINGS (continued)

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Max	Unit
<b>V<sub>CORE</sub> LINEAR REGULATOR (Note 7)</b>			
Maximum Output Voltage Startup Overshoot ( $C_{OUT} = 10 \mu F$ ) (Note 8) MODE[2:0] = [0, x, 0] MODE[2:0] = [0, x, Open] MODE[2:0] = [Open, x, 0] MODE[2:0] = [Open, x, Open]	$V_{CORE(STARTUP)}$	3.6 2.7 2.0 1.65	V
Maximum Output Current $T_J = 0^\circ C$ to $105^\circ C$ , $V_{LINB+} \leq V_{CORE(NOM)} + 0.8 V$ (Note 9)	$I_{VCORE}$	500	mA

### Notes

7.  $12 V \leq V_{B+} \leq 32 V$  and  $-20^\circ C \leq T_J \leq 145^\circ C$  unless otherwise noted.
8. Refer to [Table 1](#), page 10.
9. Pulse testing with low duty cycle used.

## STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions  $4.75\text{ V} \leq V_{IO} \leq 5.25\text{ V}$ ,  $12\text{ V} \leq V_{B+} \leq 32\text{ V}$ , and  $0^\circ\text{C} \leq T_J \leq 105^\circ\text{C}$  unless otherwise noted.

Typical values noted reflect the approximate parameter mean at  $T_A = 25^\circ\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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### $V_{IO}$ SWITCHING REGULATOR

Logic Supply Voltage ( $I_{VIO} = 25\text{ mA to } 1.0\text{ A}$ ) MODE0 = 0 MODE0 = Open	$V_{IO}$	4.8 3.15	– –	5.2 3.45	V
Logic Supply Current $V_{IO} = \text{Nominal}$ , Power Dissipation in Switching Regulator = 0.45 W	$I_{VIO}$	0.025	–	1.0	A
Output On Resistance $V_{B+} = 12\text{ V to } 32\text{ V}$	$R_{DS(ON)}$	0.5	TBD	2.0	$\Omega$
Soft Start Threshold Voltage MODE0 = X	$V_{IO}(\text{SOFT})$	–	–	2.5	V
Current Limit Threshold ( $T_J = 25^\circ\text{C to } 100^\circ\text{C}$ ) Normal Operation Soft Start, $V_{IO} \leq 2.5\text{ V}$	$I_{LIMIT(OP)}$ $I_{LIMIT(SOFT)}$	2.1 1.3	– –	3.2 1.8	A
Minimum Voltage Allowable on $V_{SWITCH}$ Terminal $T_J = 25^\circ\text{C to } 100^\circ\text{C}$	$V_{VSWITCH(MIN)}$	-0.5	–	–	V

### $V_{CORE}$ LINEAR REGULATOR

Supply Voltage ( $I_{VCORE} = 5.0\text{ mA to } 500\text{ mA}$ ) (Note 10) MODE[2:0] = [0, x, 0] MODE[2:0] = [0, x, Open] MODE[2:0] = [Open, x, 0] MODE[2:0] = [Open, x, Open]	$V_{CORE(NOM)}$	3.15 2.35 1.71 1.425	– – – –	3.45 2.65 1.89 1.575	V
Supply Current $V_{CORE} = V_{CORE(NOM)}$	$I_{VCORE}$	1.0	–	500	mA
$V_{CORE}$ Dropout Voltage $V_{CORE} = V_{CORE(NOM)}$ , $I_{VCORE} = 0.5\text{ A}$	$I_{VCORE(DROPOUT)}$	0.8	–	–	V
Regulator Input Voltage $V_{CORE} = V_{CORE(NOM)}$ , $I_{VCORE} = 0.5\text{ A}$	$V_{LINB+}$	$V_{CORE(NOM)} + 1.0$	–	10	V
Normal Current Limit Threshold $T_J = 25^\circ\text{C to } 100^\circ\text{C}$ , $V_{LINB+} = V_{CORE(NOM)} + 1.0\text{ V}$	$I_{LIMIT}$	800	–	1000	mA

#### Notes

10. Refer to [Table 1](#), page 10.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions  $4.75\text{ V} \leq V_{IO} \leq 5.25\text{ V}$ ,  $12\text{ V} \leq V_{B+} \leq 32\text{ V}$ , and  $0^\circ\text{C} \leq T_J \leq 105^\circ\text{C}$  unless otherwise noted.

Typical values noted reflect the approximate parameter mean at  $T_A = 25^\circ\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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### MODE TERMINALS OPERATING VOLTAGES

MODE Control Terminals Low Voltage $T_J = 0^\circ\text{C}$ to TBD $^\circ\text{C}$ , $V_{B+} = 12\text{ V}$ to $32\text{ V}$	$V_{IL}(\text{MODEn})$	–	–	0.825	V
MODE Control Terminals High Voltage $T_J = 0^\circ\text{C}$ to TBD $^\circ\text{C}$ , $V_{B+} = 12\text{ V}$ to $32\text{ V}$	$V_{IH}(\text{MODEn})$	2.6	–	–	V
MODE Control Terminals Voltage with Input Floating $T_J = 0^\circ\text{C}$ to TBD $^\circ\text{C}$ , $V_{B+} = 12\text{ V}$ to $14\text{ V}$ $T_J = 0^\circ\text{C}$ to TBD $^\circ\text{C}$ , $V_{B+} = 14\text{ V}$ to $32\text{ V}$	$V_{\text{MODE}}(\text{FLOAT})$	7.0 8.0	– –	12 13.2	V

### SUPERVISOR CIRCUITRY

Minimum Function $V_{B+}$ for Charge Pump and Oscillator Running	$V_{B+}(\text{MIN})$	9.0	–	–	V
Minimum $V_{B+}$ for $\overline{\text{RST}}$ Assertion, $V_{B+}$ Rising	$V_{B+}(\text{ASSERT})$	2.0	–	–	V
$\overline{\text{RST}}$ Low Voltage $V_{B+} = 2.0\text{ V}$ , $I_{\overline{\text{RST}}} \leq 5.0\text{ mA}$	$V_{OL}$	–	–	0.4	V
$\overline{\text{RST}}$ $V_{IO}$ Threshold $V_{IO}$ Rising $V_{IO}$ Falling	$V_{IOt+}$ $V_{IOt-}$	– $V_{IO}(\text{NOM})$ – 225 mV	– –	$V_{IO}(\text{NOM})$ – 80 mV –	V
$\overline{\text{RST}}$ Hysteresis for $V_{IO}$	$V_{\text{HYS}V_{IO}}$	10	–	100	mV
$\overline{\text{RST}}$ $V_{\text{CORE}}$ Threshold $V_{\text{CORE}}$ Rising $V_{\text{CORE}}$ Falling	$V_{\text{CORE}t+}$ $V_{\text{CORE}t-}$	– $V_{\text{CORE}}(\text{NOM})$ – 225 mV	– –	$V_{\text{CORE}}(\text{NOM})$ – 80 mV –	V
$\overline{\text{RST}}$ Hysteresis for $V_{\text{CORE}}$ $V_{B+} = 12\text{ V}$ to $32\text{ V}$	$V_{\text{HYS CORE}}$	10	–	100	mV
$V_{\text{CORE}} - V_{IO}$ for $V_{\text{CORE}}$ Shutdown $V_{B+} = 12\text{ V}$ to $32\text{ V}$	$V_{\text{CORE}}(\text{SHUTDOWN})$	–	–	TBD	V
Thermal Shutdown Temperature $T_J$ Rising	$T_J(\text{TSD})$	170	–	–	$^\circ\text{C}$
Overtemperature Hysteresis	$T_J(\text{HYSTERESIS})$	20	–	TBD	$^\circ\text{C}$

### $V_b$ CHARGE PUMP

Boost Voltage (Note 11) $V_{B+} = 12\text{ V}$ to $32\text{ V}$ , $I_{Vb} = 0.5\text{ mA}$	$V_b$	$V_{B+} + 10\text{ V}$	–	$V_{B+} + 12\text{ V}$	V
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#### Notes

11. Bulk capacitor ESR  $\leq 10\ \Omega$ .

## DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions  $4.75\text{ V} \leq V_{IO} \leq 5.25\text{ V}$ ,  $12\text{ V} \leq V_{B+} \leq 32\text{ V}$ , and  $0^\circ\text{C} \leq T_J \leq 105^\circ\text{C}$  unless otherwise noted.

Typical values noted reflect the approximate parameter mean at  $T_A = 25^\circ\text{C}$  under nominal conditions unless otherwise noted

Characteristic	Symbol	Min	Typ	Max	Unit
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### $V_{IO}$ SWITCHING REGULATOR

Duty Cycle	D	45	—	55	%
Switching Rise and Fall Time Load Resistance = $100\ \Omega$ , $V_{B+} = 30\text{ V}$	$t_r, t_f$	25	—	—	ns
Switching Rise and Fall Time Load Resistance = $100\ \Omega$ , $V_{B+} = 30\text{ V}$	$t_r + t_f$	—	—	50	ns

### SUPERVISOR CIRCUITRY

$\overline{\text{RST}}$ Delay $C_{\text{delay}} = 0.1\ \mu\text{F}$	$t_{\text{delay}}$	48	—	82	ms
$\overline{\text{RST}}$ Filter Time $V_{B+} = 9.0\text{ V}$	$t_{\text{filter}}$	1.0	—	6.0	$\mu\text{s}$
$\overline{\text{RST}}$ Fall Time $C_L = 100\text{ pF}$ , $R_{\text{PULLUP}} = 4.7\text{ k}\Omega$ , 90% to 10%	$t_f$	—	—	125	ns
External Low (Note 12) $V_{IO} = 5.0\text{ V}$	$t_{\text{slpl}}$ (Note 13)	30	—	—	ns
$\overline{\text{RST}}$ Recovery Time Before Next $\overline{\text{RST}}$ Input (Note 12) $V_{IO} = 5.0\text{ V}$	$t_{\text{phsl}}$	—	—	10	$\mu\text{s}$

### INTERNAL OSCILLATOR

Charge Pump and $V_{IO}$ Switching Regulator Operating Frequency $V_{B+} = 9.0\text{ V}$ to $32\text{ V}$	$f_{\text{OP}}$	140	—	260	kHz
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#### Notes

12. See [Figure 2. RST Timing](#), page 9.
13.  $t_{\text{slpl}}$  is an input.



# Timing Diagram

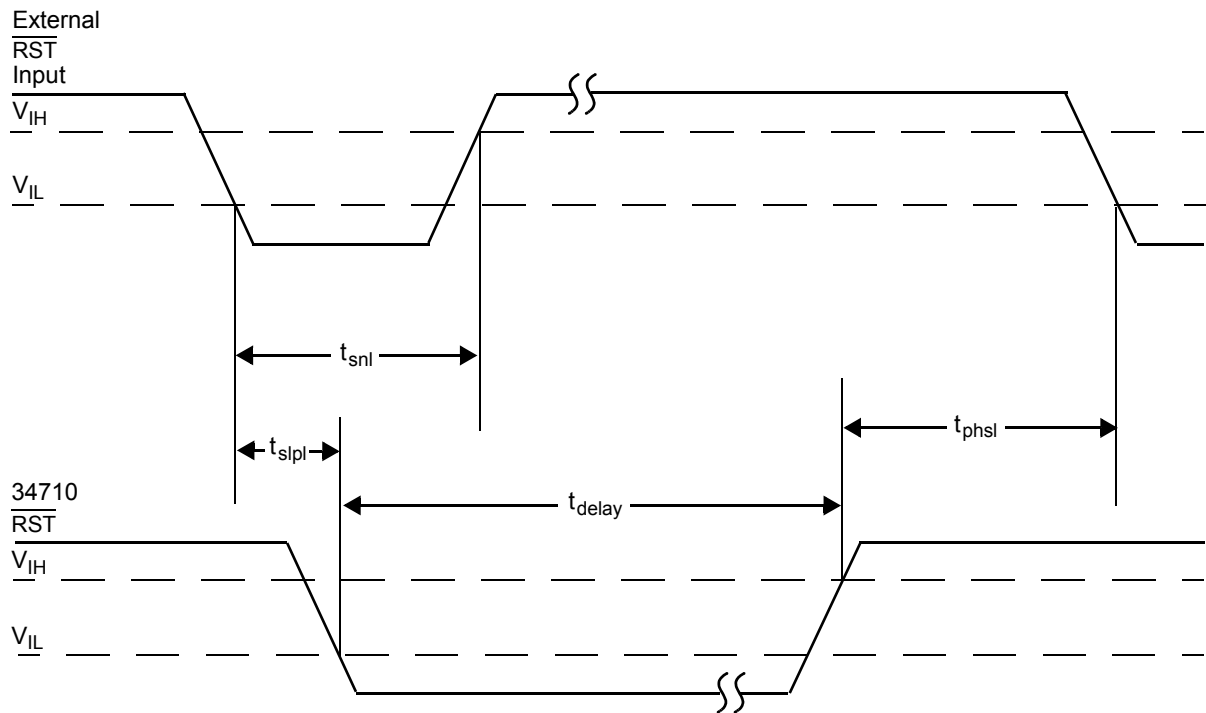


Figure 2.  $\overline{\text{RST}}$  Timing

## SYSTEM/APPLICATION INFORMATION

### INTRODUCTION

#### $V_{I/O}$ Switching Regulator

The  $V_{I/O}$  switching regulator output voltage is determined by the MODE digital input terminals. The 34710's MODE[2:0] select the output voltage (Table 1). For example, if MODE[2:0] = 0, 0, 0, then  $V_{I/O}$  = 5.0 V; if MODE[2:0] = Open, Open, Open, then  $V_{I/O}$  = 3.3 V. The MODE0 terminal controls the output voltage of both regulators.

The topology of the regulator is a bang-bang buck regulator operating from the internal ~200 kHz oscillator.

#### $V_{CORE}$ Linear Regulator

The  $V_{CORE}$  linear regulator can produce a +3.3 V, 2.5 V, 1.8 V, or 1.5 V output voltage at 500 mA. The input to the  $V_{CORE}$  regulator is a terminal that may be connected to the  $V_{I/O}$  regulator output. The minimum input voltage must be  $V_{CORE}(NOM) + 0.8$  V.

The MODE[2:0] terminals select the output voltage as depicted in Table 1.

**Table 1.  $V_{I/O}$  and  $V_{CORE}(NOM)$  Regulator Output Voltage Selection**

MODE2	MODE1	MODE0	$V_{I/O}$ (V)	$V_{CORE}(NOM)$ (V)
0	0	0	5.0	3.3
0	0	Open	3.3	2.5
0	Open	0	5.0	1.8
0	Open	Open	3.3	1.8
Open	0	0	5.0	2.5
Open	0	Open	3.3	2.5
Open	Open	0	5.0	1.5
Open	Open	Open	3.3	1.5

Open indicates terminal is not connected externally.

### SUPERVISORY AND MISCELLANEOUS FUNCTIONS

#### Introduction

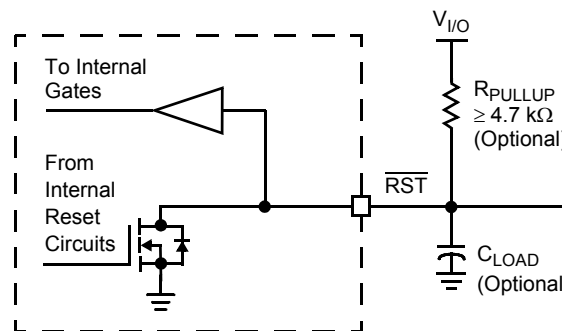
The supervisor circuitry provides control of the  $\overline{RST}$  line, an open drain signal, based on system operating conditions monitored by the 34710.  $V_{I/O}$ ,  $V_{CORE}$ ,  $V_{B+}$ , and thermal shutdown (TSD) detectors in various parts of the chip are monitored for error conditions. Because other devices in the system may trigger a reset, the  $\overline{RST}$  line itself is also monitored, but the supervisor circuitry controls all reset timing, including externally generated resets. Driving the  $\overline{RST}$  line low causes the system to be held in the reset state.  $V_{I/O}$ ,  $V_{CORE}$ ,  $V_{B+}$ , and thermal shutdown have both positive- and negative-going thresholds.

The supervisor circuitry also ensures that the power supplies sequence properly. Specifically, that  $V_{I/O}$  is never less than TBD V below  $V_{CORE}$ . This means that  $V_{CORE} - V_{I/O}$  will be clamped at 0.5 V, and that the  $V_{CORE}$  regulator operation will be suppressed during startup and shutdown to ensure that  $V_{CORE} - V_{I/O} = TBD$  V.

#### Static Operating Specifications

The  $\overline{RST}$  output is an I/O device with an open drain output driver with a pullup and a CMOS digital input gate (Figure 3). This I/O structure allows wired OR connection to the MCU's  $\overline{RST}$  I/O terminal, as well as allowing the MCU to initiate a reset cycle by driving its  $\overline{RST}$  terminal low. When responding to a MCU request for a reset cycle, the 34710 must respond rapidly enough to prevent a glitch. Figure 2, page 9, shows the timing

parameters for responding to an externally applied  $\overline{RST}$  signal. The rise time may be relatively slow, depending on the load capacitance, and the internal  $\overline{RST}$  input gate must operate reliably (no oscillations during the transition) under these conditions, i.e., the  $\overline{RST}$  input can be inhibited for up to  $t_{phs1}(MAX)$ . Error conditions must be present for a minimum time,  $t_{filter}$ , before the 34710 responds to them. Once all error conditions are cleared,  $\overline{RST}$  is held low for an additional time of  $t_{delay}$ . If any monitored item falls below its negative-going threshold for  $t_{filter}$ , 1.0  $\mu s$  to 6.0  $\mu s$ , the  $t_{delay}$  will be restarted when system operating conditions are met. The trigger for the  $t_{delay}$  retriggerable one shot should be  $([V_{I/O}(LOW) + V_{CORE}(LOW) + V_{B+}(LOW) + T_J(TSD)] \& t_{filter})$ , where  $t_{filter}$  is the 1.0  $\mu s$  to 6.0  $\mu s$  delay.



**Figure 3.  $\overline{RST}$  Terminal Interface**

## $V_b$ Charge Pump

The high-side MOSFETs in the H-Bridge motor drivers and voltage regulators switch require a gate voltage in excess of  $V_{B+}$ , which is provided by the  $V_b$  supply. The  $V_b$  regulator is a charge pump, switching directly off the  $V_{B+}$  supply, and uses an internal oscillator operating at 200 kHz.

## Internal Oscillator

The internal oscillator provides timing for the charge pump and switching regulators.

## APPLICATIONS

### Power Dissipation

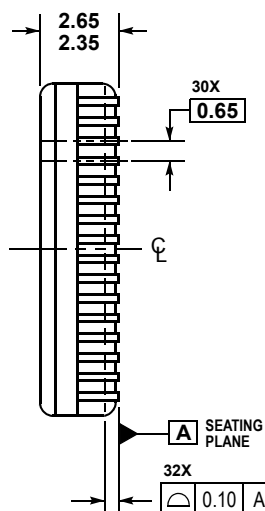
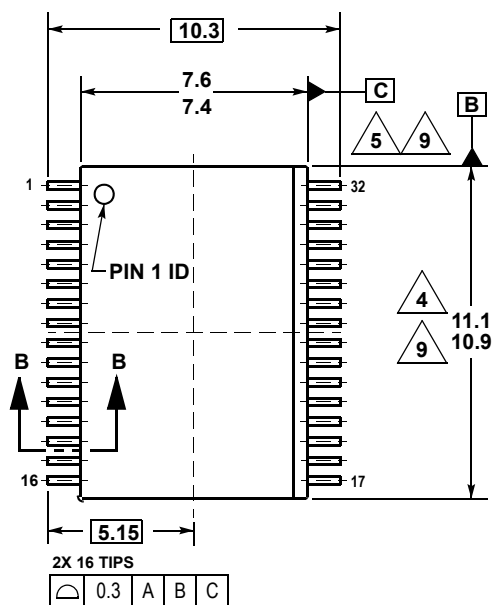
The power budget is described in [Table 2](#). The maximum dissipation for this device is 1.0 W continuous.

**Table 2. Power Budget**

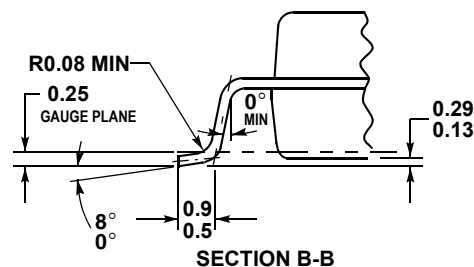
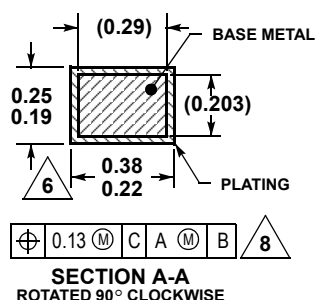
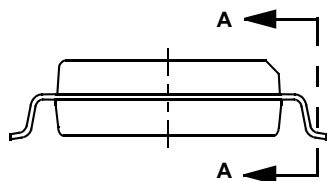
Functional Block	Watt
Bias	0.00
Charge Pump	0.15
Switching Regulator	0.45
Linear Regulator	0.35
<b>Total</b>	<b>0.95</b>

## PACKAGE DIMENSIONS

**EW (Pb-FREE) SUFFIX**  
**32-LEAD SOICW-EXPOSED PAD**  
**PLASTIC PACKAGE**  
**CASE 1324-02**  
**ISSUE A**



- NOTES:
- ALL DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  - DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  - THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  - THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
  - THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 MM PER SIDE. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
  - EXACT SHAPE OF EACH CORNER IS OPTIONAL.
  - THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.3 MM FROM THE LEAD TIP.
  - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.



**NOTES**

**NOTES**

**NOTES**

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