

SCF5250 Integrated ColdFire® Microprocessor Data Sheet

1 Introduction

This document provides an overview of the SCF5250 ColdFire® processor and general descriptions of SCF5250 features and its various modules.

The SCF5250 was designed as a system controller/decoder for compressed audio music players, especially portable and automotive CD and hard disk drive players. The 32-bit ColdFire core with Enhanced Multiply Accumulate (EMAC) unit provides optimum performance and code density for the combination of control code and signal processing required for audio decoding and post processing, file management, and system control.

Low power features include a hardwired CD ROM decoder, advanced 0.13um CMOS process technology, 1.2V core power supply, and on-chip 128KByte SRAM that enables Windows Media Audio (WMA) decoding without the need for external DRAM in CD applications.

The SCF5250 is also an excellent general purpose system controller with over 110 Dhrystone 2.1 MIPS @ 120MHz performance at a very competitive price. The integrated peripherals and enhanced MAC unit allow the

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SCF5250 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can also be remapped as General Purpose I/O pins.

1.1 Orderable Part Numbers

1.1.1 Orderable Part Table

Table 1. Orderable Part Numbers

| Orderable Part Number | Maximum Clock Frequency | Package Type | Operating Temperature Range | Part Status |
|-----------------------|-------------------------|-----------------|-----------------------------|-------------|
| SCF5250PV120 | 120 MHz | 144 pin QFP | -20°C to 70°C | Leaded |
| SCF5250AG120 | 120 MHz | 144 pin QFP | -20°C to 70°C | Lead Free |
| SCF5250CPV120 | 120 MHz | 144 pin QFP | -40°C to 85°C | Leaded |
| SCF5250CAG120 | 120 MHz | 144 pin QFP | -40°C to 85°C | Lead Free |
| SCF5250VM120 | 120 MHz | 196 ball MAPBGA | -20°C to 70°C | Lead Free |

1.2 SCF5250 Features

1.2.1 ColdFire V2 Core

The ColdFire processor Version 2 core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size. The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, which minimizes time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register file feeding an arithmetic/logic unit (ALU).

1.2.2 DMA Controller

The SCF5250 provides four fully programmable DMA channels for quick data transfer. Single and dual address mode is supported with the ability to program bursting and cycle stealing. Data transfer is selectable as 8, 16, 32, or 128-bits. Packing and unpacking is supported.

Two internal audio channels and the dual UART can be used with the DMA channels. All channels can perform memory to memory transfers. The DMA controller has a user-selectable, 24- or 16-bit counter and a programmable DMA exception handler.

External requests are not supported.

1.2.3 Enhanced Multiply and Accumulate Module (EMAC)

The integrated EMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture. The EMAC provides functionality in three related areas:

1. Faster signed and unsigned integer multiplies
2. New multiply-accumulate operations supporting signed and unsigned operands
3. New miscellaneous register operations

Multiplies of 16x16 and 32x32 with 48-bit accumulates are supported in addition to a full set of extensions for signed and unsigned integers plus signed, fixed-point fractional input operands. The EMAC has a single-clock issue for 32x32-bit multiplication instructions and implements a four-stage execution pipeline.

1.2.4 Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The SCF5250 processor uses a 8K-byte, direct-mapped instruction cache to achieve 107 MIPS at 120 MHz. The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16-bit and 8-bit port sizes to quickly fill cache lines.

1.2.5 Internal 128-KByte SRAM

The 128-KByte on-chip SRAM is available in two banks, SRAM0 (64K) and SRAM1 (64K). It provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance. Memory in SRAM1 can be accessed under DMA.

1.2.6 SDRAM Controller

The SCF5250 SDRAM controller provides a glueless interface for one bank of SDRAM up to 32 MB (256 Mbits). The controller supports a 16-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMs.

1.2.7 System Interface

The SCF5250 provides a glueless interface to 16-bit port size SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-select and write-enable signals.

The SCF5250 also supports bursting ROMs.

1.2.8 External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides 23 bits of address bus

space, a 16-bit data bus, Output Enable, and Read/Write signals. This interface implements an extended synchronous protocol that supports bursting operations.

1.2.9 Serial Audio Interfaces

The SC5250 digital audio interface provides three serial Philips IIS/Sony EIAJ interfaces. One interface is a 4-pin (1 bit clock, 1 word clock, 1 data in, 1 data out), the other two interfaces are 3-pin (1 bit clock, 1 word clock, 1 data in or out). The serial interfaces have no limit on minimum sampling frequency. Maximum sampling frequency is determined by maximum frequency on bit clock input. This is 1/3 the frequency of the internal system clock.

1.2.10 IEC958 Digital Audio Interfaces

The SCF5250 has one digital audio input interface, and one digital audio output interface. The single output carries the consumer “c” channel.

1.2.11 Audio Bus

The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission. Each transmitter has a source select register.

In addition to the audio interfaces, there are six CPU accessible registers connected to the audio bus. Three of these registers allow data reads from the audio bus and allow selection of the audio source. The other three register provide a write path to the audio bus and can be selected by transmitters as the audio source. Through these registers, the CPU has access to the audio samples for processing.

Audio can be routed from a receiver to a transmitter without the data being processed by the core so the audio bus can be used as a digital audio data switch. The audio bus can also be used for audio format conversion.

1.2.12 CD-ROM Encoder/Decoder

The SCF5250 is capable of processing CD-ROM sectors in hardware. Processing is compliant with CD-ROM and CD-ROM XA standards.

The CD-ROM decoder performs following functions in hardware:

- Sector sync recognition
- Descrambling of sectors
- Verification of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors
- Third-layer error correction is not performed

The CD-ROM encoder performs following functions in hardware:

- Sector sync recognition
- Scrambling of sectors

- Insertion of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors.
- Third-layer error encoding needs to be done in software. This can use approximately 5-10 Mhz of performance for single-speed.

1.2.13 Dual UART Module

Two full-duplex UARTs with independent receive and transmit buffers are in this module. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The Dual UART module also provides several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{\text{RTS}}$) and clear-to-send ($\overline{\text{CTS}}$) lines.

The system clock provides the clocking function from a programmable prescaler. You can select full duplex, auto-echo loopback, local loopback, and remote loopback modes. The programmable Dual UARTs can interrupt the CPU on various normal or error-condition events.

1.2.14 Queued Serial Peripheral Interface QSPI

The QSPI module provides a serial peripheral interface with queued transfer capability. It supports up to 16 stacked transfers at a time, making CPU intervention between transfers unnecessary. Transfers of up to 15 Mbits/second are possible at a CPU clock of 120 MHz. The QSPI supports master mode operation only.

1.2.15 Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer. Timer0 has an external pin TOUT0, which can be used in Output Compare mode. This mode triggers an external signal or interrupts the CPU when the timer reaches a set value, and can also generate waveforms on TOUT0.

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. In addition to the $\div 1$ and $\div 16$ clock derived from the bus clock (CPU clock / 2), the programmable timer-output pins either generate an active-low pulse or toggle the outputs.

1.2.16 IDE and SmartMedia Interfaces

The SCF5250 system bus allows connection of an IDE hard disk drive or SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the SCF5250.

1.2.17 Analog/Digital Converter (ADC)

The six channel ADC is based on the Sigma-Delta concept with 12-bit resolution. Both the analogue comparator and digital sections of the ADC are provided internally. An external integrator circuit (resistor/capacitor) is required, which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

1.2.18 I²C Module

The two-wire I²C bus interface, which is compliant with the Philips I²C bus standard, is a bidirectional serial bus that exchanges data between devices. The I²C bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

1.2.19 Chip-Selects

Up to four programmable chip-select outputs provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.

CS0 is active after reset to provide boot-up from external FLASH/ROM.

1.2.20 GPIO Interface

A total of 60 General Purpose inputs and 57 General Purpose outputs are available. These are multiplexed with various other signals. Seven of the GPIO inputs have edge sensitive interrupt capability.

1.2.21 Interrupt Controller

The interrupt controller provides user-programmable control of a total of 57 interrupts. There are 49 internal interrupt sources. In addition, there are 7 GPIOs where interrupts can be generated on the rising or falling edge of the pin. All interrupts are autovectored and interrupt levels are programmable.

1.2.22 JTAG

To help with system diagnostics and manufacturing testing, the SCF5250 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1A standard. Freescale provides BSDL files for JTAG testing.

1.2.23 System Debug Interface

The ColdFire processor core debug interface supports real-time instruction trace and debug, plus background-debug mode. A background-debug mode (BDM) interface provides system debug.

In real-time instruction trace, four status lines provide information on processor activity in real time (PST pins). A four-bit wide debug data bus (DDATA) displays operand data and change-of-flow addresses, which helps track the machine's dynamic execution path.

1.2.24 Crystal and On-chip PLL

Typically, an external 16.92 Mhz or 33.86 Mhz clock input is used for CD R/W applications, while an 11.2896 MHz clock is more practical for Portable CD player applications. However, the on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5-35 Mhz).

Two clock outputs (MCLK1 and MCLK2) are provided for use as Audio Master Clock. The output frequencies of both outputs are programmable to Fxtal, Fxtal/2, Fxtal/3, and Fxtal/4. The Fxtal/3 option is only available when the 33.86 Mhz crystal is connected.

The SCF5250 supports VCO operation of the oscillator by means of a 16-bit pulse density modulation output. Using this mode, it is possible to lock the oscillator to the frequency of an incoming IEC958 or IIS signal. The maximum trim depends on the type and design of the oscillator. Typically a trim of +/- 100 ppm can be achieved with a crystal oscillator and over +/- 1000 ppm with an LC oscillator.

1.2.25 Boot ROM

The boot ROM on the SCF5250 serves to boot the CPU in designs which do not have external Flash memory or ROM. Typically this occurs in systems which have a separate MCU to control the system, and/or the SCF5250 is used as a stand-alone decoder.

The SCF5250 can be booted in one of three modes:

- External ROM
- Internal ROM Master mode – boots from I2C, SPI, or IDE
- Internal ROM Slave mode – boots from I2C or UART

1.2.26 Voltage Regulator

The SCF5250 contains an on-chip linear regulator that generates 1.2V from a 3.3V input. The regulator is self-contained and drives the 1.2V core voltage out on one pin that can be used to power the core supply pins at the board level. In battery powered portable applications, it is recommended that an external dc-dc converter be used to generate the 1.2V core voltage to minimize power consumption.

2 SCF5250 Block Diagram

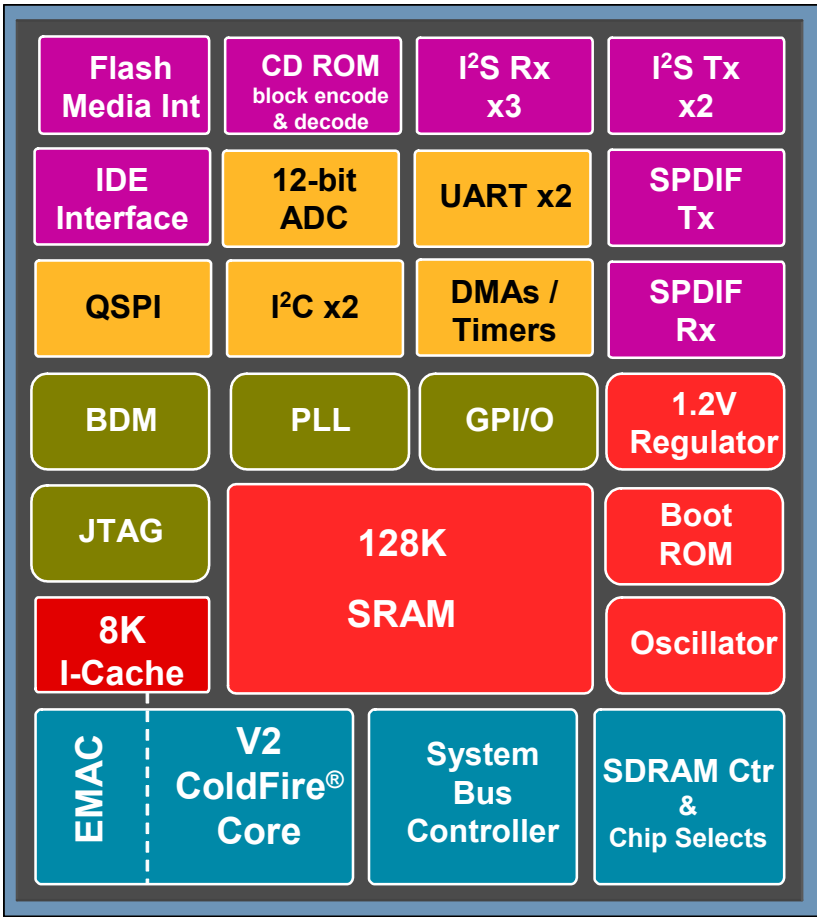


Figure 1. SCF5250 Block Diagram

3 Documentation

Table 2 lists the documents that provide a complete description of the SCF5250 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet; <http://e-www.Freescale.com/> (the source for the latest information).

Table 2. SCF5250 Documentation

| Document Name | Description | Order Number |
|---------------|---|-----------------|
| CFPRM/D | ColdFire Family Programmer's Reference Manual | CFPRM/D |
| ColdFire2UM | Version 2/2M ColdFire Core Processor User's Manual | ColdFire2UM/D |
| ColdFire2UMAD | Version 2/2M ColdFire Core Processor User's Manual Addendum | ColdFire2UMAD/D |
| SCF5250UM | SCF5250 User's Manual | SCF5250UM/D |

4 Signal Descriptions

4.1 Introduction

This section describes the SCF5250 input and output signals. The signal descriptions as shown in Table 2-A are grouped according to relevant functionality.

Table 3. SCF5250 Signal Index

| Signal Name | Mnemonic | Function | Input/Output | Reset State |
|-----------------------------------|------------------------------|--|--------------|-------------|
| Address | A[24:1] A[23]/GPO54 | 24 address lines, address line 23 multiplexed with GPO54 and address 24 is multiplexed with A20 (SDRAM access only). | Out | X |
| Read-write control | R/ \overline{W} | Bus write enable - indicates if read or write cycle in progress | Out | H |
| Output enable | OE | Output enable for asynchronous memories connected to chip selects | Out | negated |
| Data | D[31:16] | Data bus used to transfer word data | In/Out | Hi-Z |
| Synchronous row address strobe | \overline{SDRAS} /GPIO59 | Row address strobe for external SDRAM. | Out | negated |
| Synchronous column address strobe | \overline{SDCAS} /GPIO39 | Column address strobe for external SDRAM | Out | negated |
| SDRAM write enable | \overline{SDWE} /GPIO38 | Write enable for external SDRAM | Out | negated |
| SDRAM upper byte enable | \overline{SDUDQM} /GPO53 | Indicates during write cycle if high byte is written | Out | |
| SDRAM lower byte enable | \overline{SDLDQM} /GPO52 | Indicates during write cycle if low byte is written | Out | |
| SDRAM chip selects | $\overline{SD_CS0}$ /GPIO60 | SDRAM chip select | In/Out | negated |
| SDRAM clock enable | BCLKE/GPIO63 | SDRAM clock enable | Out | |
| System clock | BCLK/GPIO40 | SDRAM clock output | In/Out | |

Table 3. SCF5250 Signal Index (continued)

| Signal Name | Mnemonic | Function | Input/ Output | Reset State |
|----------------------|--|--|------------------|----------------|
| ISA bus read strobe | IDE-DIOR/GPIO31 (CS2) | There is 1 ISA bus read strobe and 1 ISA bus write strobe. They allow connection of one independent ISA bus peripherals, e.g. an IDE slave device. | In/Out | |
| ISA bus write strobe | IDE-DIOW/GPIO32 (CS2) | | In/Out | |
| ISA bus wait signal | IDE-IORDY/GPIO33 | ISA bus wait line - available for both busses | In/Out | |
| Chip Selects[2:0] | CS0/CS4 CS1/QSPI_CS3/GPIO28 | Enables peripherals at programmed addresses. CS[0] provides boot ROM selection | Out In/Out | negated |
| Buffer enable 1 | BUFENB1/GPIO29 | Two programmable buffer enables allow seamless steering of external buffers to split data and address bus in sections. | In/Out | |
| Buffer enable 2 | BUFENB2/GPIO30 | | In/Out | |
| Transfer acknowledge | TĀ/GPIO12 | Transfer Acknowledge signal | In/Out | |
| Wake Up | WAKE_UP/GPIO21 | Wake-up signal input | In | |
| Serial Clock Line | SCL0/SDATA1_BS1/GPIO41 SCL1/TXD1/GPIO10 | Clock signal for Dual I ² C module operation | In/Out | |
| Serial Data Line | SDA0/SDATA3/GPIO42 SDA1/RXD1/GPIO44 | Serial data port for second I ² C module operation | In/Out | |
| Receive Data | SDA1/RXD1/GPIO44 RXD0/GPIO46 | Signal is receive serial data input for DUART | In | |
| Transmit Data | SCL1/TXD1/GPIO10 TXD0/GPIO45 | Signal is transmit serial data output for DUART | Out | |
| Request-To-Send | DDATA3/RTS0/GPIO4 DDATA1/RTS1/SDATA2_BS2/GPIO2 | DUART signals a ready to receive data query | Out | |
| Clear-To-Send | DDATA2/CTS0/GPIO3 DDATA0/CTS1/SDATA0_SDIO1/GPIO1 | Signals to DUART that data can be transmitted to peripheral | In | |
| Timer Output | SDATA01/TOUT0/GPIO18 | Capable of output waveform or pulse generation | Out | |
| IEC958 inputs | EBUIN1/GPIO36 EBUIN2/SCLK_OUT/GPIO13 EBUIN3/CMD_SDIO2/GPIO14 QSPI_CS0/EBUIN4/GPIO15 | audio interfaces IEC958 inputs | In | |
| IEC958 outputs | EBUOUT1/GPIO37 QSPI_CS1/EBUOUT2/GPIO16 | audio interfaces IEC958 outputs | Out | |
| Serial data in | SDATAI1/GPIO17 SDATAI3/GPIO8 | audio interfaces serial data inputs | In | |
| Serial data out | SDATA01/TOUT0/GPIO18 SDATA02/GPIO34 | audio interfaces serial data outputs | In/Out Out | |
| Word clock | LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/GPIO43/AUDIO_CLOCK | audio interfaces serial word clocks | In/Out | |
| Bit clock | SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35 | audio interfaces serial bit clocks | In/Out | |

Table 3. SCF5250 Signal Index (continued)

| Signal Name | Mnemonic | Function | Input/ Output | Reset State |
|-------------------------------------|--|---|------------------|----------------|
| Serial input | EF/GPIO6 | error flag serial in | In/Out | |
| Serial input | CFLG/GPIO5 | C-flag serial in | In/Out | |
| Subcode clock | RCK/QSPI_DIN/QSPI_DOUT/ GPIO26 | audio interfaces subcode clock | In/Out | |
| Subcode sync | QSPI_DOUT/SFSY/GPIO27 | audio interfaces subcode sync | In/Out | |
| Subcode data | QSPI_CLK/SUBR/GPIO25 | audio interfaces subcode data | In/Out | |
| Clock frequency trim | XTRIM/GPIO0 | clock trim control | Out | |
| Audio clocks out | MCLK1/GPIO11 QSPI_CS2/MCLK2/GPIO24 | DAC output clocks | Out | |
| Audio clock in | LRCK3/GPIO43/AUDIO_CLOCK | Optional Audio clock Input | | |
| MemoryStick/SecureDigital interface | EBUIN3/CMD_SDIO2/GPIO14 | Secure Digital command lane MemoryStick interface 2 data i/o | In/Out | |
| | EBUIN2/SCLK_OUT/GPIO13 | Clock out for both MemoryStick interfaces and for Secure Digital | In/Out | |
| | DDATA0/ $\overline{\text{CTS1}}$ /SDATA0_SDIO1/GPIO1 | SecureDigital serial data bit 0 MemoryStick interface 1 data i/o | In/Out | |
| | SCL0/SDATA1_BS1/GPIO41 | SecureDigital serial data bit 1 MemoryStick interface 1 strobe | In/Out | |
| | DDATA1/ $\overline{\text{RTS1}}$ /SDATA2_BS2/GPIO2 | SecureDigital serial data bit 2 MemoryStick interface 2 strobe Reset output signal | In/Out | |
| | SDA0/SDATA3/GPIO42 | SecureDigital serial data bit 3 | In/Out | |
| ADC IN | ADIN0/GPI52 ADIN1/GPI53 ADIN2/GPI54 ADIN3/GPI55 ADIN4/GPI56 ADIN5/GPI57 | Analog to Digital converter input signals | In | |
| ADC OUT | ADREF ADOUT/SCLK4/GPIO58 | Analog to digital convertor output signal. Connect to ADREF via integrator network. | In/Out | |
| QSPI clock | QSPI_CLK/SUBR/GPIO25 | QSPI clock signal | In/Out | |
| QSPI data in | RCK/QSPI_DIN/QSPI_DOUT/GPIO26 | QSPI data input | In/Out | |
| QSPI data out | RCK/QSPI_DIN/QSPI_DOUT/GPIO26 QSPI_DOUT/SFSY/GPIO27 | QSPI data out | In/Out | |
| QSPI chip selects | QSPI_CS0/EBUIN4/GPIO15 QSPI_CS1/EBUOUT2/GPIO16 QSPI_CS2/MCLK2/GPIO24 $\overline{\text{CS1}}$ /QSPI_CS3/GPIO28 | QSPI chip selects | In/Out | |
| Crystal in | CRIN | Crystal input | In | |
| Crystal out | CROUT | Crystal Out | Out | |
| Reset In | RSTI | Processor Reset Input | In | |
| Freescale Test Mode | TEST[2:0] | TEST pins. | In | |
| Linear regulator output | LINOUT | outputs 1.2 V to supply core | Out | |

Table 3. SCF5250 Signal Index (continued)

| Signal Name | Mnemonic | Function | Input/ Output | Reset State |
|--|--|--|------------------|----------------|
| Linear regulator input | LININ | Input, typically I/O supply (3.3V) | In | |
| Linear regulator ground | LINGND | | | |
| High Impedance | HI-Z | Assertion Tri-states all output signal pins. | In | |
| Debug Data | DDATA0/ $\overline{\text{CTS1}}$ /SDATA0_SDIO1/GPIO1 DDATA1/ $\overline{\text{RTS1}}$ /SDATA2_BS2/GPIO2 DDATA2/ $\overline{\text{CTS0}}$ /GPIO3 DDATA3/ $\overline{\text{RTS0}}$ /GPIO4 | Displays captured processor data and break-point status. | In/Out | Hi-Z |
| Processor Status | PST0/GPIO50 PST1/GPIO49 PST2/INTMON2/GPIO48 PST3/INTMON1/GPIO47 | Indicates internal processor status. | In/Out | Hi-Z |
| Processor clock | PSTCLK/GPIO51 | processor clock output | Out | |
| Test Clock | TCK | Clock signal for IEEE 1149.1A JTAG. | In | |
| Test Reset/Development Serial Clock | $\overline{\text{TRST}}$ /DSCLK | Multiplexed signal that is asynchronous reset for JTAG controller. Clock input for debug module. | In | |
| Test Mode Select/ Break Point | TMS/ $\overline{\text{BKPT}}$ | Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode. | In | |
| Test Data Input / Development Serial Input | TDI/DSI | Multiplexed serial input for the JTAG or background debug module. | In | |
| Test Data Output/Development Serial Output | TDO/DSO | Multiplexed serial output for the JTAG or background debug module. | Out | |

4.2 GPIO

Many pins have an optional GPIO function.

- General purpose input is always active, regardless of state of pin.
- General purpose output or primary output is determined by the appropriate setting of the Pin Multiplex Control Registers, GPIO-FUNCTION, GPIO1-FUNCTION and PIN-CONFIG.
- At Power-on reset, all pins are set to their primary function.

4.3 SCF5250 Bus Signals

These signals provide the external bus interface to the SCF5250.

4.3.1 Address Bus

- The address bus provides the address of the byte or most significant byte of the word or longword being transferred. The address lines also serve as the DRAM address pins, providing multiplexed row and column address signals.
- Bits 23 down to 1 and 24 of the address are available. A24 is intended to be used with 256 Mbit DRAM's. Signals are named:
 - A[23:1]
 - A20/24

4.3.2 Read-Write Control

This signal indicates during any bus cycle whether a read or write is in progress. A low is write cycle and a high is a read cycle.

4.3.3 Output Enable

The \overline{OE} signal is intended to be connected to the output enable of asynchronous memories connected to chip selects. During bus read cycles, the ColdFire processor will drive \overline{OE} low.

4.3.4 Data Bus

The data bus (D[31:16]) is bi-directional and non-multiplexed. Data is registered by the SCF5250 on the rising clock edge. The data bus uses a default configuration if none of the chip-selects or DRAM bank match the address decode. All 16 bits of the data bus are driven during writes, regardless of port width or operand size.

4.3.5 Transfer Acknowledge

The \overline{TA} /GPIO12 pin is the transfer acknowledge signal.

4.4 SDRAM Controller Signals

The following SDRAM signals provide a glueless interface to external SDRAM. An SDRAM width of 16 bits is supported and can access as much as 32MB of memory. ADRAMs are not supported.

Table 4. SDRAM Controller Signals

| SDRAM Signal | Description |
|--|--|
| Synchronous DRAM row address strobe | The \overline{SDRAS} /GPIO59 active low pin provides a seamless interface to the RAS input on synchronous DRAM |
| Synchronous DRAM Column Address Strobe | The \overline{SDCAS} /GPIO39 active low pin provides a seamless interface to CAS input on synchronous DRAM. |
| Synchronous DRAM Write | The \overline{SDWE} /GPIO38 active-low pin is asserted to signify that a SDRAM write cycle is underway. This pin outputs logic '1' during read bus cycles. |

Table 4. SDRAM Controller Signals (continued)

| SDRAM Signal | Description |
|--|--|
| Synchronous DRAM Chip Enable | The $\overline{SD_CS0}$ /GPIO60 active-low output signal is used during synchronous mode to route directly to the chip select of a SDRAM device. |
| Synchronous DRAM UDQM and LDQM signals | The DRAM byte enables UDMQ and LDQM are driven by the \overline{SDUDQM} /GPO53 and \overline{SDLDQM} /GPO52 byte enable outputs. |
| Synchronous DRAM clock | The DRAM clock is driven by the BCLK/GPIO40 signal |
| Synchronous DRAM Clock Enable | The BCLKE active high output signal is used during synchronous mode to route directly to the SCKE signal of external SDRAMs. This signal provides the clock enable to the SDRAM. |

4.5 Chip Selects

There are three chip select outputs on the SCF5250 device. $\overline{CS0/CS4}$ and $\overline{CS1/QSPI_CS3}$ /GPIO28 and CS2 which is associated with the IDE interface read and write strobes - IDE-DIOR and IDE-DIOW.

CS0 and CS4 are multiplexed. The SCF5250 has the option to boot from an internal Boot Rom. The function of the CS0/CS4 pin is determined by the boot mode. When the device is booted from internal ROM, the internal ROM is accessed with CS0 (required for boot) and the CS0/CS4 pin is driven by CS4. When the device is booted from external ROM / Flash, the CS0/CS4 pin is driven by CS0 and the internal ROM is disabled.

The active low chip selects can be used to access asynchronous memories. The interface is glueless.

4.6 ISA bus

The SCF5250 supports an ISA bus. Using the ISA bus protocol, reads and writes for one ISA bus peripheral is possible. $\overline{IDE-DIOR}$ /GPIO31 and $\overline{IDE-DIOW}$ /GPIO32 are the read and write strobe. The peripheral can insert wait states by pulling IDE-IORDY/GPIO33.

CS2 is associated with the IDE-DIOR and IDE-DIOW.

4.7 Bus Buffer Signals

As the SCF5250 has a complicated slave bus, which allows SDRAM, asynchronous memories, and ISA peripherals on the bus, it may become necessary to introduce a buffer on the bus in certain applications. The SCF5250 has a glueless interface to steer these bus buffers with two bus buffer output signals $\overline{BUFENB1}$ /GPIO29 and $\overline{BUFENB2}$ /GPIO30.

4.8 I²C Module Signals

There are two I²C interfaces on this device.

The I²C module acts as a two-wire, bidirectional serial interface between the SCF5250 processor and peripherals with an I²C interface (e.g., LED controller, A-to-D converter, D-to-A converter). When

devices connected to the I²C bus drive the bus, they will either drive logic-0 or high-impedance. This can be accomplished with an open-drain output.

Table 5. I²C Module Signals

| I ² C Module Signal | Description |
|--------------------------------|--|
| I ² C Serial Clock | The SCL0/SDATA1_BS1/GPIO41 and SCL1/TXD1/GPIO10 bidirectional signals are the clock signal for first and second I ² C module operation. The I ² C module controls this signal when the bus is in master mode; all I ² C devices drive this signal to synchronize I ² C timing. Signals are multiplexed |
| I ² C Serial Data | The SDA0/SDATA3/GPIO42 and SDA1/RXD1/GPIO44 bidirectional signals are the data input/output for the first and second serial I ² C interface. Signals are multiplexed |

4.9 Serial Module Signals

The following signals transfer serial data between the two UART modules and external peripherals.

Table 6. Serial Module Signals

| Serial Module Signal | Description |
|----------------------|--|
| Receive Data | The RXD0/GPIO46 and SDA1/RXD1/GPIO44 are the inputs on which serial data is received by the DUART. Data is sampled on RxD[1:0] on the rising edge of the serial clock source, with the least significant bit received first. |
| Transmit Data | The DUART transmits serial data on the TXD0/GPIO45 and SCL1/TXD1/GPIO10 output signals. Data is transmitted on the falling edge of the serial clock source, with the least significant bit transmitted (LSB) first. When no data is being transmitted or the transmitter is disabled, these two signals are held high. TxD[1:0] are also held high in local loopback mode. |
| Request To Send | The DDATA3/RTS0/GP104 and DDATA1/RTS1/SDATA2_BS2/GPIO2 request-to-send outputs indicate to the peripheral device that the DUART is ready to send data and requires a clear-to-send signal to initiate transfer. |
| Clear To Send | Peripherals drive the DDATA2/CTS0/GPIO3 and DDATA0/CTS1/SDATA0_SDIO1/GPIO1 inputs to indicate to the SCF5250 serial module that it can begin data transmission. |

4.10 Timer Module Signals

The following signal provides an external interface to Timer0.

Table 7. Timer Module Signals

| Serial Module Signal | Description |
|----------------------|---|
| Timer Output | The SDATA01/TOUT0/GPIO18 programmable output pulse or toggle on various timer events. |

4.11 Serial Audio Interface Signals

The following signals provide the external audio interface.

Table 8. Serial Audio Interface Signals

| Serial Module Signal | Description |
|-------------------------|---|
| Serial Audio Bit Clock | The SCLK1/GPIO20, SCLK2/GPIO22 and SCLK3/GPIO35, multiplexed pins can serve as general purpose I/Os or serial audio bit clocks. As bit clocks, these bidirectional pins can be programmed as outputs to drive their associated serial audio (IIS) bit clocks. Alternately, these pins can be programmed as inputs when the serial audio bit clocks are driven internally. The functionality is programmed within the Audio module. During reset, these pins are configured as input serial audio bit clocks. |
| Serial Audio Word Clock | The LRCK1/GPIO19, LRCK2/GPIO23 and LRCK3/GPIO43/AUDIO_CLOCK multiplexed pins can serve as general purpose I/Os or serial audio word clocks. As word clocks, the bidirectional pins can be programmed as inputs to drive their associated serial audio word clock. Alternately, these pins can be programmed as outputs when the serial audio word clocks are derived internally. The functionality is programmed within the Audio module. During reset, these pins are configured as input serial audio word clocks. LRCK3/GPIO43/AUDIO_CLOCK can be used as the external audio clock input. If the core clock chosen to be non-audio specific. |
| Serial Audio Data In | The SDATAI1/GPIO17 and SDATAI3/GPIO8 multiplexed pins can serve as general purpose I/Os or serial audio inputs. As serial audio inputs the data is sent to interfaces 1 and 3 respectively. During reset, the pins are configured as serial data inputs. |
| Serial Audio Data Out | SDATO1/TOUT0/GPIO18 AND SDATAO2/GPIO34 multiplexed pins can serve as general purpose I/Os or serial audio outputs. During reset, the pins are configured as serial data outputs. |
| Serial audio error flag | The EF/GPIO6 multiplexed pin can serve as general purpose I/Os or error flag input. As error flag input, this pin will input the error flag delivered by the CD-DSP. EF/GPIO6 is only relevant for serial interface SDATAI1. |
| Serial audio CFLG | The CFLG/GPIO5 multiplexed pin can serve as general purpose I/O or CFLG input. As CFLG input, the pin will input the CFLG flag delivered by the CD-DSP. CFLG/GPIO5 is only relevant for serial interface SDATAI1. |

4.12 Digital Audio Interface Signals

Table 9. Digital Audio Interface Signals

| Serial Module Signal | Description |
|----------------------|--|
| Digital Audio In | The EBUIN1/GPIO36, EBUIN2/SCLK_OUT/GPIO13, EBUIN3/CMD_SDIO2/GPIO14, and QSPI_CS0/EBUIN4/GPIO15 multiplexed signals can serve as general purpose input or can be driven by various digital audio (IEC958) input sources. Both functionalities are always active. Input chosen for IEC958 receiver is programmed within the audio module. Input value on the 4 pins can always be read from the appropriate GPIO register. |
| Digital Audio Out | The EBUOUT1/GPIO37 and QSPI_CS1/EBUOUT2/GPIO16 multiplexed pins can serve as general purpose I/O or as digital audio (IEC958) output. EBUOUT1 is digital audio out for consumer mode, EBUOUT2 is digital audio out for professional mode. During reset, the pin is configured as a digital audio output. |

4.13 Subcode Interface

There is a 3-line subcode interface on the SCF5250. This 3-line subcode interface allows the device to format and transmit subcode in EIAJ format to a CD channel encoder device. The three signals are described in [Table 10](#).

Table 10. Subcode Interface Signal

| Signal name | Description |
|-------------------------------|---|
| RCK/QSPI_DIN/QSPI_DOUT/GPIO26 | Subcode clock input. When pin is used as subcode clock, this pin is driven by the CD channel encoder. |
| QSPI_DOUT/SFSY/GPIO27 | Subcode sync output This signal is driven high if a subcode sync needs to be inserted in the EFM stream. |
| QSPI_CLK/SUBR/GPIO25 | Subcode data output This signal is a subcode data out pin. |

4.14 Analog to Digital Converter (ADC)

The ADOUT signal on the ADOUT/SCLK4/GPIO58 pin provides the reference voltage in PWM format. This output requires an external integrator circuit (resistor/capacitor) to convert it to a DC level to be input to the ADREF pin.

The six AD inputs are each fed to their own comparator. The reference input to each (ADREF) is then multiplexed as only one AD comparison can be made at any one time.

NOTE

To use the ADINx as General Purpose inputs (rather than there analogue function) it is necessary to generate a fixed comparator voltage level of $VDD/2$. This can be accomplished by a potential divider network connected to the ADREF pin. However in portable applications where stand-by power

consumption is important the current taken by the divider network (in stand-by mode) could be excessive. Therefore it is possible to generate a VDD/2 voltage by selecting SCLK4 output mode and feeding this clock signal (which is 50% duty cycle) through an external integration circuit. This would generate a voltage level equal to VDD/2 but would be disabled when stand-by mode was selected.

4.15 Secure Digital/ MemoryStick Card Interface

The device has a versatile flash card interface that supports both SecureDigital and MemoryStick cards. The interface can either support one SecureDigital or two MemoryStick cards. No mixing of card types is possible. [Table 11](#) gives the pin descriptions.

Table 11. Flash Memory Card Signals

| Flash Memory Signal | Description |
|--|--|
| EBUIN2/SCLKOUT/GPIO13 | Clock out for both MemoryStick interfaces and for SecureDigital |
| EBUIN3/CMD_SDIO2/GPIO14 | Secure Digital command line MemoryStick interface 2 data i/o |
| DDATA0/ $\overline{\text{CTS1}}$ /SDATA0_SDIO1/GPIO1 | SecureDigital serial data bit 0 MemoryStick interface 1 data i/o |
| SCL0/SDATA1_BS1/GPIO41 | SecureDigital serial data bit 1 MemoryStick interface 1 strobe |
| DDATA1/ $\overline{\text{RTS1}}$ /SDATA2_BS2/GPIO2 | SecureDigital serial data bit 2 MemoryStick interface 2 strobe Reset output signal Selection between Reset function and SDATA2_BS2 is done by programming PLLCR register. |
| SDA0/SDATA3/GPIO42 | SecureDigital serial data bit 3 |

4.16 Queued Serial Peripheral Interface (QSPI)

The QSPI interface is a high-speed serial interface allowing transmit and receive of serial data. Pin descriptions are given in [Table 12](#).

Table 12. Queued Serial Peripheral Interface (QSPI) Signals

| Serial Module Signal | Description |
|--|--|
| QSPICLK/SUBR/GPIO25 | Multiplexed signal IIC interface clock or QSPI clock output Function select is done via PLLCR register. |
| RCK/QSPIDIN/QSPI_DOUT/GPIO26 | Multiplexed signal IIC interface data or QSPI data input. Function select is done via PLLCR register. |
| RCK/QSPI_DIN/QSPI_DOUT/GPIO26 QSPI_DOUT/SFSY/GPIO27 | QSPI data output |

Table 12. Queued Serial Peripheral Interface (QSPI) Signals (continued)

| Serial Module Signal | Description |
|------------------------|-------------------------------|
| QSPICS0/EBUIN4/GPIO15 | 4 different QSPI chip selects |
| QSPICS1/EBUOUT2/GPIO16 | |
| QSPICS2/MCLK2/GPIO24 | |
| CS1/QSPICS3/GPIO28 | |

4.17 Crystal Trim

The XTRIM/GPIO0 output produces a pulse-density modulated phase/frequency difference signal to be used after low-pass filtering to control varicap-voltage to control crystal oscillation frequency. This will lock the crystal to the incoming digital audio signal.

4.18 Clock Out

The MCLK1/GPIO11 and QSPI_CS2/MCLK2/GPIO24 can serve as DAC clock outputs. When programmed as DAC clock outputs, these signals are directly derived from the crystal oscillator or clock Input (CRIN).

4.19 Debug and Test Signals

These signals interface with external I/O to provide processor debug and status signals.

4.19.1 Test Mode

The TEST[2:0] inputs are used for various manufacturing and debug tests. For normal mode TEST [2:1] should be ways be tied low. TEST0 should be set high for BDM debug mode and set low for JTAG mode.

4.19.2 High Impedance

The assertion of $\overline{\text{HI_Z}}$ will force all output drivers to a high-impedance state. The timing on $\overline{\text{HI_Z}}$ is independent of the clock.

NOTE

JTAG operation will override the $\overline{\text{HI_Z}}$ pin.

4.19.3 Processor Clock Output

The internal PLL generates this PSTCLK/GPIO51 and output signal, and is the processor clock output that is used as the timing reference for the Debug bus timing (DDATA[3:0] and PST[3:0]). The PSTCLK/GPIO51 is at the same frequency as the core processor.

4.19.4 Debug Data

The debug data pins, DDATA0/CTS1/SDATA0_SDIO1/GPIO1, DDATA1/RTS1/SDATA2_BS2/GPIO2, DDATA2/CTS0/GPIO3, and DDATA3/RTS0/GPIO4, are four bits wide. This nibble-wide bus displays captured processor data and break-point status.

4.19.5 Processor Status

The processor status pins, PST0/GPIO50, PST1/GPIO49, PST2/INTMON/GPIO48, and PST3/INTMON/GPIO47, indicate the SCF5250 processor status. During debug mode, the timing is synchronous with the processor clock (PSTCLK) and the status is not related to the current bus transfer. [Table 13](#) shows the encodings of these signals.

Table 13. Processor Status Signal Encodings

| PST[3:0] | | Definition |
|--|----------|--|
| (HEX) | (BINARY) | |
| \$0 | 0000 | Continue execution |
| \$1 | 0001 | Begin execution of an instruction |
| \$2 | 0010 | Reserved |
| \$3 | 0011 | Entry into user-mode |
| \$4 | 0100 | Begin execution of PULSE and WDDATA instructions |
| \$5 | 0101 | Begin execution of taken branch or Synch_PC ¹ |
| \$6 | 0110 | Reserved |
| \$7 | 0111 | Begin execution of RTE instruction |
| \$8 | 1000 | Begin 1-byte data transfer on DDATA |
| \$9 | 1001 | Begin 2-byte data transfer on DDATA |
| \$A | 1010 | Begin 3-byte data transfer on DDATA |
| \$B | 1011 | Begin 4-byte data transfer on DDATA |
| \$C | 1100 | Exception processing ² |
| \$D | 1101 | Emulator mode entry exception processing ² |
| \$E | 1110 | Processor is stopped, waiting for interrupt ² |
| \$F | 1111 | Processor is halted ² |
| Rev. B enhancement. These encodings are asserted for multiple cycles. | | |

4.20 BDM/JTAG Signals

The SCF5250 complies with the IEEE 1149.1A JTAG testing standard. The JTAG test pins are multiplexed with background debug pins.

4.21 Clock and Reset signals

These signals configure the SCF5250 and provide interface signals to the external system.

4.21.1 Reset In

Asserting $\overline{\text{RSTI}}$ causes the SCF5250 to enter reset exception processing. When $\overline{\text{RSTI}}$ is recognized, the data bus is tri-stated.

4.21.2 Clock Input

SCF5250 includes on-chip crystal oscillator. The crystal should be connected between CRIN and CROUT. An externally generated clock signal can also be used and should be connected directly to the CRIN pin.

4.22 Wake-Up Signal

To exit power down mode, apply a LOW level to the WAKE_UP/GPIO21 input pin.

4.23 On-chip Linear Regulator

The SCF5250 includes an on-chip linear regulator. This regulator provides an 1.2 V output which is intended to be used to power the SCF5250 core. Three pins are associated with this function. LININ, LINOUT and LINGND. Typically LININ would be fed by the I/O (PAD) supply (3.3 V) with separate filtering recommended to provide some isolation between the I/O and the core.

In portable solutions this linear regulator may not be efficient enough and in this case we would expect the 1.2 V supply to be generated externally, possibly by a highly efficient DC-DC convertor.

If not used leave pins not connected.

5 Electrical Characteristics

Table 14. Maximum Ratings

| Rating | Symbol | Value | Units |
|--------------------------------|----------|--------------|-------|
| Supply Core Voltage | V_{CC} | -0.5 to +2.5 | V |
| Maximum Core Operating Voltage | V_{CC} | +1.32 | V |
| Minimum Core Operating Voltage | V_{CC} | +1.08 | V |

Table 14. Maximum Ratings (continued)

| Rating | Symbol | Value | Units |
|-------------------------------|-----------|--------------|-------|
| Supply I/O Voltage | V_{cc} | -0.5 to +4.6 | V |
| Maximum I/O Operating Voltage | V_{cc} | +3.6 | V |
| Minimum I/O Operating Voltage | V_{cc} | +3.0 | V |
| Input Voltage | V_{in} | -0.5 to +6.0 | V |
| Storage Temperature Range | T_{stg} | -65 to 150 | °C |

Table 15. Operating Temperature

| Characteristic | Symbol | Value | Units |
|---------------------------------------|------------|-----------------|-------|
| Maximum Operating Ambient Temperature | T_{Amax} | 85 ¹ | °C |
| Minimum Operating Ambient Temperature | T_{Amin} | -40 | °C |

Note: This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature does not exceed 105°C.

Table 16. Recommended Operating Supply Voltages

| Pin Name | Min | Typ | Max |
|-------------|-------|------|-------|
| CORE-VDD | 1.08V | 1.2V | 1.32V |
| CORE-VSS | | gnd | --- |
| PAD-VDD | 3.0V | 3.3v | 3.6V |
| PAD-VSS | | gnd | |
| ADVDD | 3.0V | 3.3v | 3.6V |
| ADGND | | gnd | |
| OSCPAD-VDD | 3.0V | 3.3v | 3.6V |
| OSCPAD-GND | | gnd | |
| PLLCORE1VDD | 1.08V | 1.2V | 1.32V |
| PLLCORE1GND | | gnd | |
| PLLCORE2VDD | 1.08V | 1.2v | 1.32V |
| PLLCORE2GND | | gnd | |
| LIN | 3.0v | 3.3V | 3.6V |

Table 17. Linear Regulator Operating Specification

| Characteristic | Symbol | Min | Typ | Max |
|---|------------------|-------|-------|-------|
| Input Voltage | V _{in} | 3.0V | 3.3V | 3.6 |
| Output Voltage (LINOUT) | V _{out} | 1.14V | 1.2V | 1.26V |
| Output Current | I _{out} | | 100mA | 150mA |
| Power Dissipation | P _d | | | 436uW |
| Load Regulation 10% I _{out} -> 90% I _{out} | | 40mV | 50mV | 60mV |
| Power Supply Rejection | PSRR | | 40dB | |
| Note: A pmos regulator is employed as a current source in this Linear regulator, so a 10µF capacitor (ESR 0 ... 5 Ohm) is needed on the output pin (LINOUT) to integrate the current. Typically this will require the use of a Tantalum type capacitor. | | | | |

Table 18. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc)

| Characteristic | Symbol | Min | Max | Units |
|--|------------------|------|-----|-------|
| Operation Voltage Range for I/O | V _{CC} | 3.0 | 3.6 | V |
| Input High Voltage | V _{IH} | 2 | 5.5 | V |
| Input Low Voltage | V _{IL} | -0.3 | 0.8 | V |
| Input Leakage Current @ 0.0 V /3.3 V During Normal Operation | I _{in} | - | ±1 | μA |
| Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation | I _{TSI} | - | ±1 | μA |
| Output High Voltage I _{OH} = 8mA ¹ , 4mA ² , 2mA ³ | V _{OH} | 2.4 | - | V |
| Output Low Voltage I _{OL} = 8mA ¹ , 4mA ² , 2mA ³ | V _{OL} | - | 0.4 | V |
| Schmitt Trigger Low to High Threshold Point ⁶ | V _{T+} | 1.47 | - | V |
| Schmitt Trigger High to Low Threshold Point ⁶ | V _{T-} | - | .95 | V |
| Load Capacitance (DATA[31:16], SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[3:1], SDATAO[2:1], CFLG, EF, DDATA[3:0], PST[3:0], PSTCLK, IDE-DIOR, IDE-DIOW, IORDY) | C _L | - | 50 | pF |
| Load Capacitance (ADDR[24:9], BCLK) | C _L | - | 40 | pF |
| Load Capacitance (BCLKE, SDCAS, SDRAS, SDLDQM, SD_CS0, SDUDQM, SDWE, BUFENB[2:1]) | C _L | - | 30 | pF |
| Load Capacitance (SDA0, SDA1, SCL0, SCL1, CMD_SDIO2, SDATA2_BS2, SDATA1_BS1, SDATA0_SDIO1, CS0/CS4, CS1, OE, R/W, TA, TXD[1:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT0, QSPID_OUT, QSPICS[3:0], GP[6:5]) | C _L | - | 20 | pF |
| Capacitance ⁵ , V _{in} = 0 V, f = 1 MHz | C _{IN} | - | 6 | pF |
| DATA[31:16], ADDR[24:9], PSTCLK, BCLK SCL, SDA, PST[3:0], DDATA[3:0], TDSO, SDRAS, SDCAS, SDWE, SD_CS0, SDLDQM, SDUDQM, R/W TOUT0, RTS[1:0], TXD[1:0], SCLK[4:1] BKPT/TMS, DSI/TDI, DSCLK/TRST Capacitance C _{IN} is periodically sampled rather than 100% tested. SCLK[4:1], SCL0, SCL1, SDA0, SDA1, CRIN, RSTI | | | | |

Table 19. Clock Timing Specification

| NUM | Characteristic | | | Units |
|-----|-----------------------------|------|-------|-------|
| | | Min | Max | |
| | CRIN Frequency ¹ | 5.00 | 33.86 | MHz |
| C5 | PSTCLK cycle time | 7.1 | — | nSec |
| C6 | PSTCLK duty cycle | 40 | 60 | % |
| C7 | BCLK cycle time | 14.2 | — | nSec |
| C8 | BCLK duty cycle | 45 | 55 | % |

Note: There are only three choices for the valid Audio frequencies 11.29 MHz, 16.93 MHz, or 33.86 MHz; no other values are allowed. The System Clock is derived from one of these crystals via an internal PLL.

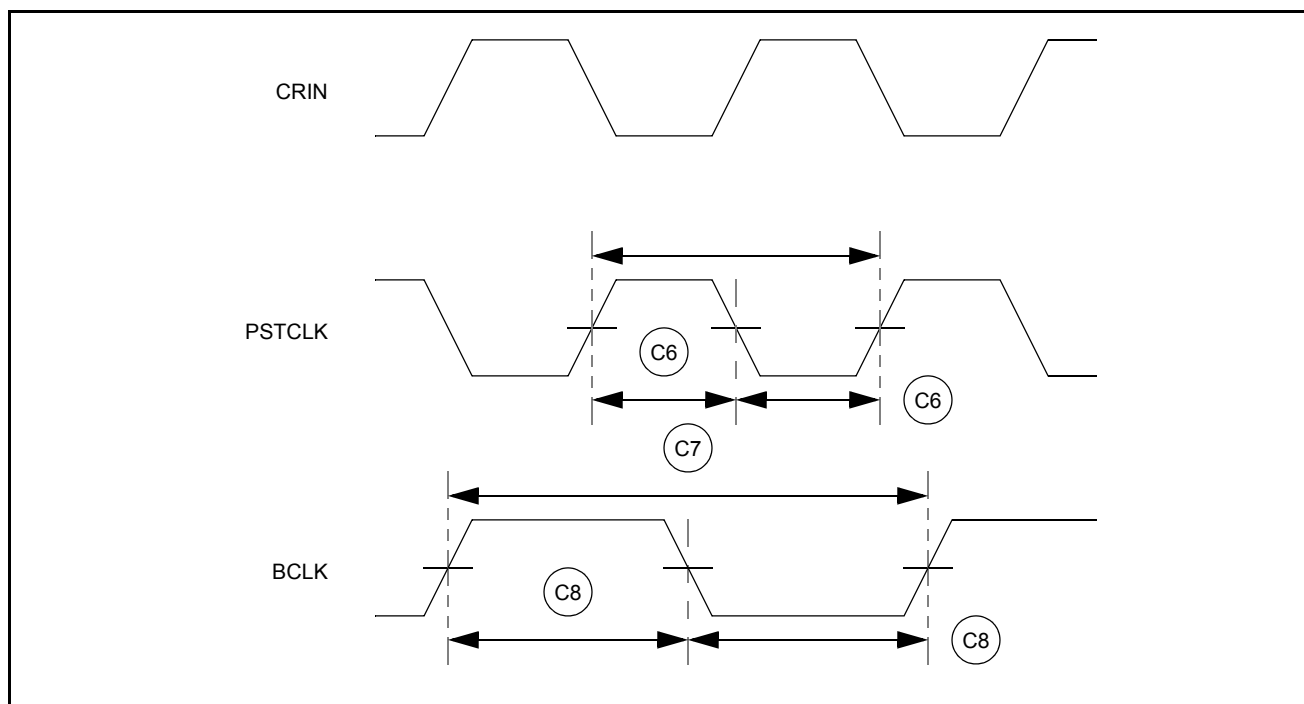


Figure 2. Clock Timing Definition

NOTE

Signals above are shown in relation to the clock. No relationship between signals is implied or intended.

Table 20. Input AC Timing Specification

| Num | Characteristic | | | Units |
|--|--------------------------------------|-----|-----|------------|
| | | Min | Max | |
| B1 ^{1,2} | Signal Valid to BCLK Rising (setup) | 3 | — | nSec |
| B2 ¹ | BCLK Rising to signal Invalid (hold) | 2 | — | nSec |
| B3 ¹ | BCLK to Input High Impedance | — | 5 | BCLK cycle |
| 1. Inputs (rising): DATA[31:16] 2. AC timing specs assume 40pF load capacitance on BCLK and 50pF load capacitance on output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load. | | | | |

Table 21. Output AC Timing Specification

| Num | Characteristic ⁵ | | | Units |
|---|--|-----|-----|-------|
| | | Min | Max | |
| • B10 ¹ | BCLK (8mA) Rising to signal Valid | --- | 10 | nSec |
| • B11 ¹ | BCLK (8mA) Rising to signal Invalid (hold) | 3.5 | — | nSec |
| • B10 ² | BCLK (4mA) Rising to signal Valid | --- | 11 | nSec |
| • B11 ² | BCLK (4mA) Rising to signal Invalid (hold) | 4 | — | nSec |
| • B12 ³ | BCLK to High Impedance (Three-State) | --- | 14 | nSec |
| • H1 | $\overline{\text{HIZ}}$ to High Impedance | — | tbd | nSec |
| • H2 | $\overline{\text{HIZ}}$ to Low Impedance | — | tbd | nSec |
| 1. Outputs (8mA): DATA[31:16], ADDR[25,23:9] 2. Outputs (4mA): SDRAS, SDCAS, SDWE, SD_CS0, SDUDQM, SDLDQM, BCLK 3. High Impedance (Three-State): DATA[31:16] 4. AC timing specs assume 40pF load capacitance on BCLK and a 50pF load capacitance on output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load. | | | | |

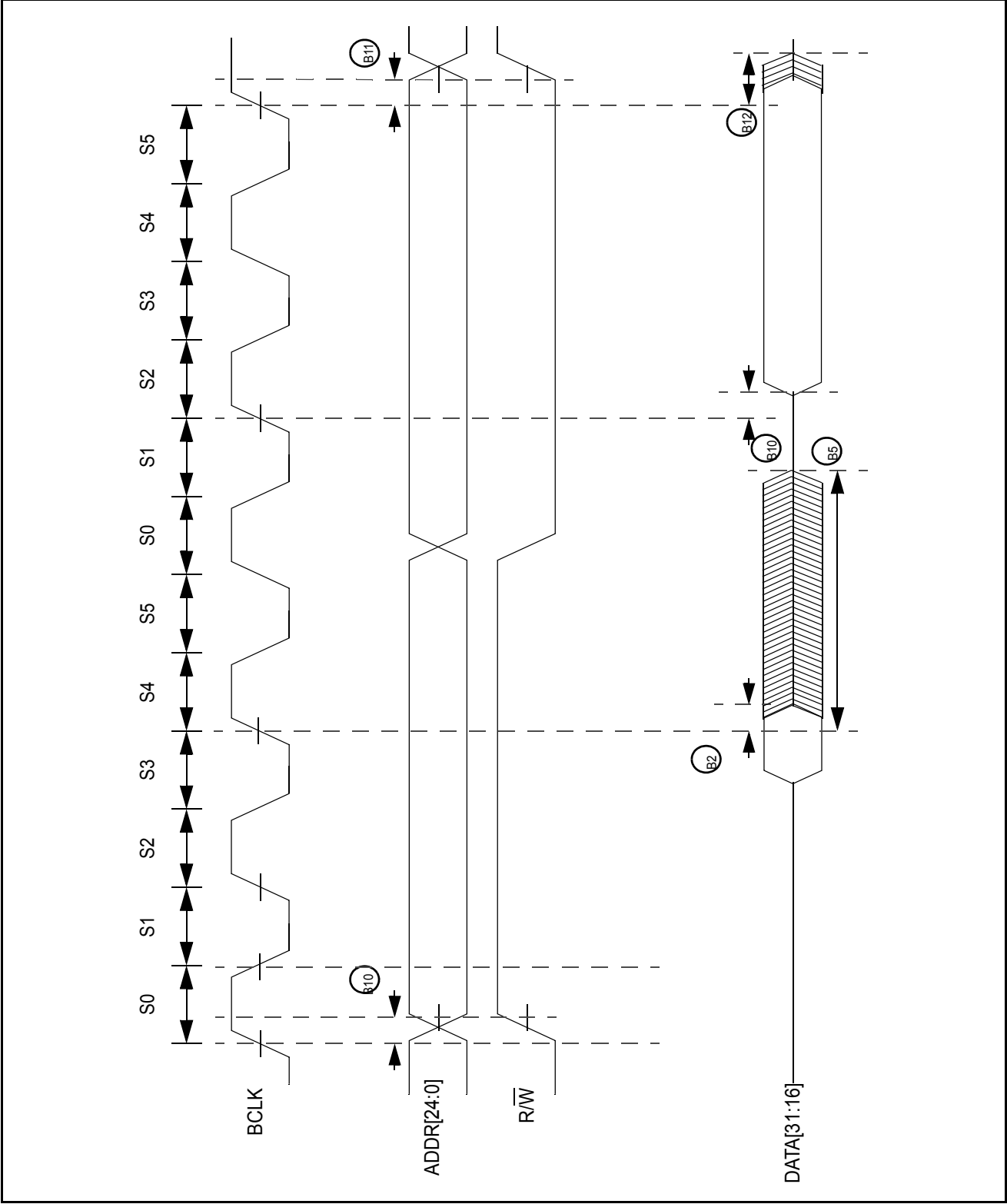


Figure 3. Input/Output Timing Definition-I

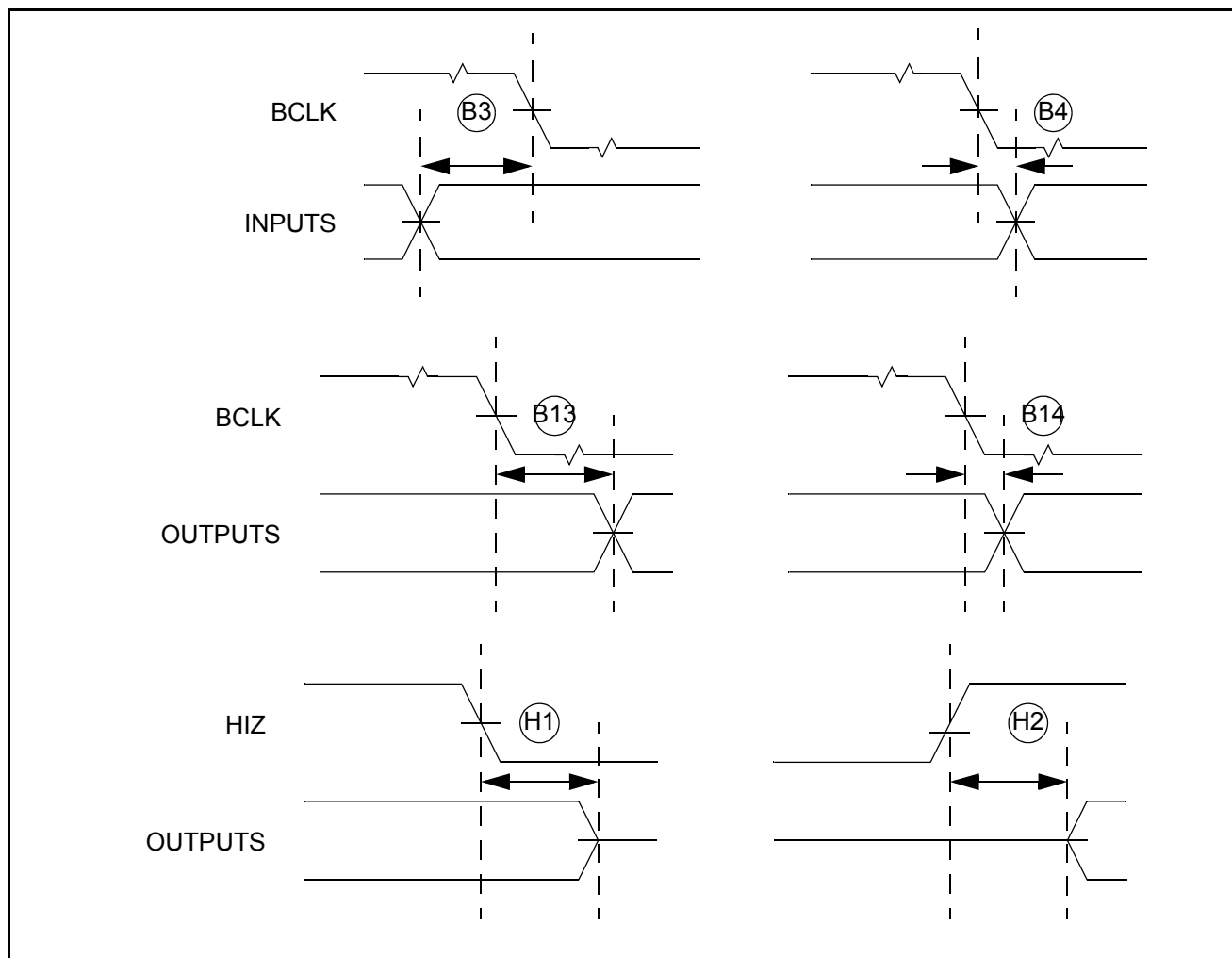


Figure 4. Input/Output Timing Definition-III

Table 22. Debug AC Timing Specification

| Num | Characteristic | | | Units |
|-----------------|--|-----|-----|-------|
| | | Min | Max | |
| D1 | PSTCLK to signal Valid (Output valid) | --- | 6 | nSec |
| D2 | PSTCLK to signal Invalid (Output hold) | 1.8 | — | nSec |
| D3 ¹ | Signal Valid to PSTCLK (Input setup) | 3 | — | nSec |
| D4 | PSTCLK to signal Invalid (Input hold) | 5 | — | nSec |

1. DSCLK and DSI are internally synchronized. This setup time must be met only if recognition on a particular clock is required.

2. AC timing specs assume 50pF load capacitance on PSTCLK and output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

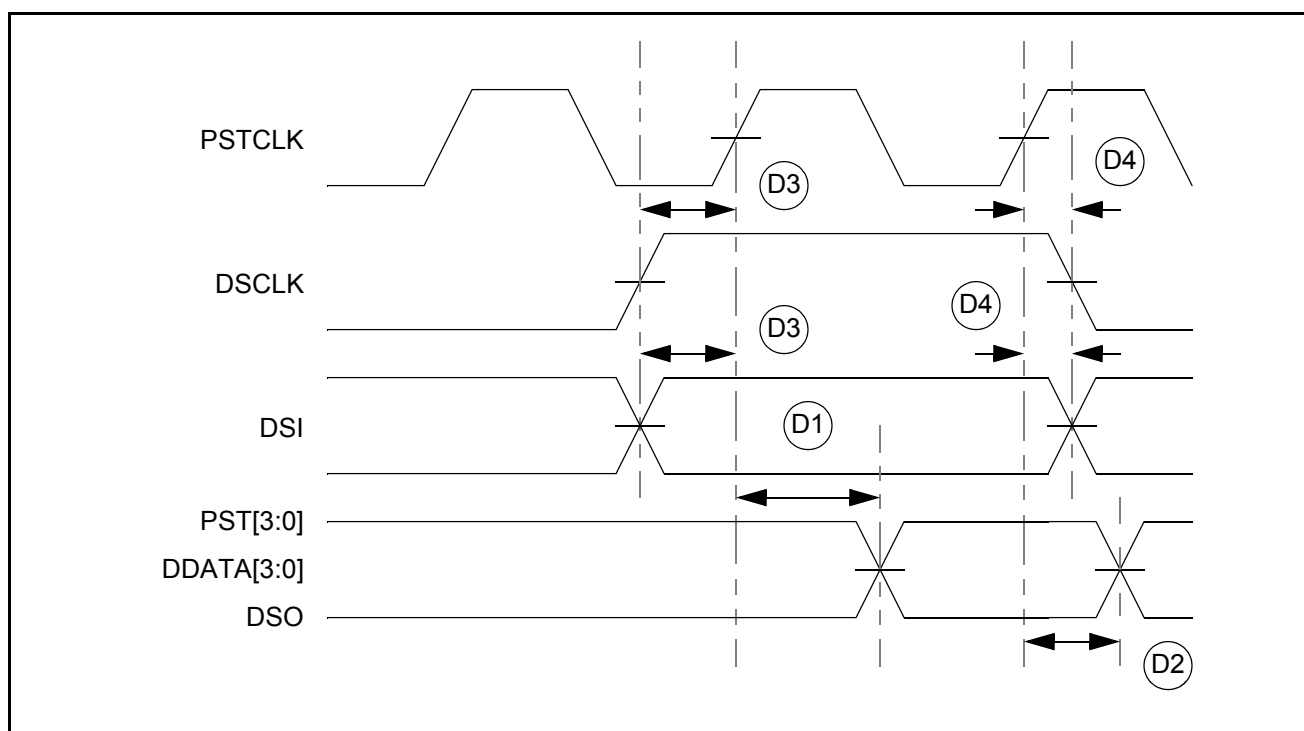


Figure 5. Debug Timing Definition

Table 23. Timer Module AC Timing Specification

| Num | Characteristic | | | Units |
|-----|------------------------------------|-----|-----|------------|
| | | Min | Max | |
| T1 | TIN Cycle time | 3T | — | bus clocks |
| T2 | TIN Valid to BCLK (input setup) | 6 | — | nSec |
| T3 | BCLK to TIN Invalid (input hold) | 0 | — | nSec |
| T4 | BCLK to TOUT Valid (output valid) | — | 10 | nSec |
| T5 | BCLK to TOUT Invalid (output hold) | tbd | — | nSec |
| T6 | TIN Pulse Width | 1T | — | bus clocks |
| T7 | TOUT Pulse Width | 1T | — | bus clocks |

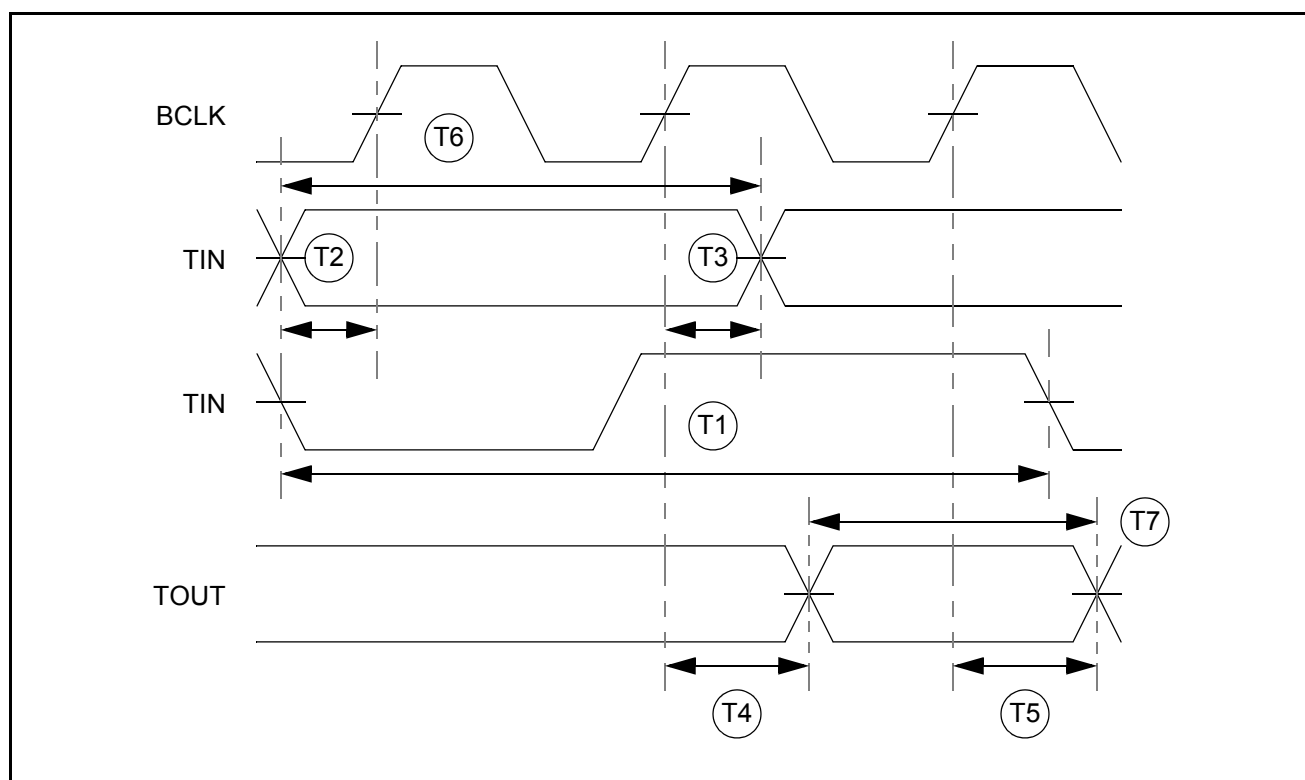


Figure 6. Timer Module Timing Definition

Table 24. UART Module AC Timing Specifications

| Num | Characteristic | | | Units |
|-----|---|-----|-----|-------|
| | | Min | Max | |
| U1 | RXD Valid to BCLK (input setup) | 6 | — | nSec |
| U2 | BCLK to RXD Invalid (input hold) | 0 | — | nSec |
| U3 | $\overline{\text{CTS}}$ Valid to BCLK (input setup) | 6 | — | nSec |
| U4 | BCLK to $\overline{\text{CTS}}$ Invalid (input hold) | 0 | — | nSec |
| U5 | BCLK to TXD Valid (output valid) | --- | tbd | nSec |
| U6 | BCLK to TXD Invalid (output hold) | 3 | — | nSec |
| U7 | BCLK to $\overline{\text{RTS}}$ Valid (output valid) | --- | tbd | nSec |
| U8 | BCLK to $\overline{\text{RTS}}$ Invalid (output hold) | 3 | — | nSec |

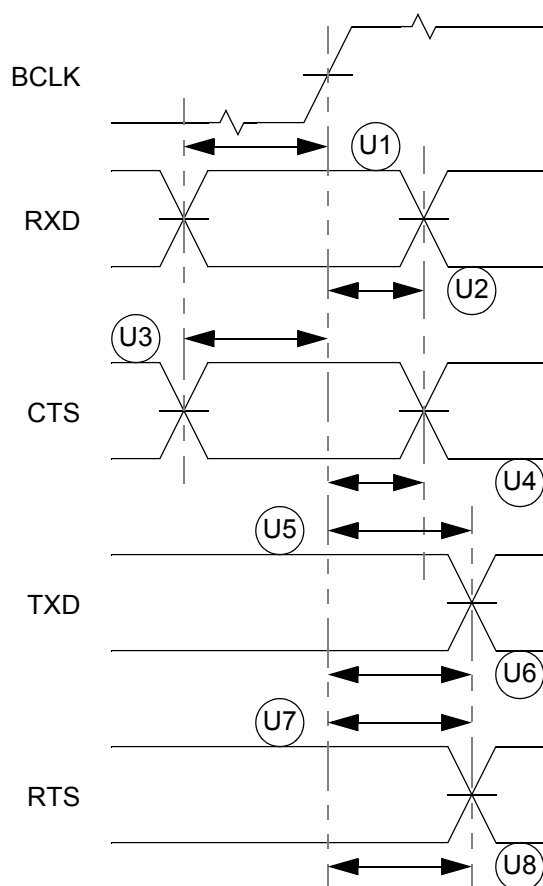


Figure 7. UART Timing Definition

Table 25. I2C-Bus Input Timing Specifications Between SCL and SDA

| Num | Characteristic | | | Units |
|-----|---|-----|-----|------------|
| | | Min | Max | |
| M1 | Start Condition Hold Time | 2 | — | bus clocks |
| M2 | Clock Low Period | 8 | — | bus clocks |
| M3 | SCL/SDA Rise Time (VIL = 0.5 V to VIH = 2.4 V) | — | 1 | mSec |
| M4 | Data Hold Time | 0 | — | nSec |
| M5 | SCL/SDA Fall Time (VIH = 2.4 V to VIL = 0.5 V) | — | 1 | mSec |
| M6 | Clock High time | 4 | — | bus clocks |
| M7 | Data Setup Time | 0 | — | nSec |
| M8 | Start Condition Setup Time (for repeated start condition only) | 2 | — | bus clocks |
| M9 | Stop Condition Setup Time | 2 | — | bus clocks |

Table 26. I2C-Bus Output Timing Specifications Between SCL and SDA

| Num | Characteristic | | | Units |
|--|---|--------|--------|------------|
| | | Min | Max | |
| M1 ¹ | Start Condition Hold Time | 6 | — | bus clocks |
| M2 ¹ | Clock Low Period | 10 | — | bus clocks |
| M3 ² | SCL/SDA Rise Time (V _{IL} = 0.5 V to V _{IH} = 2.4 V) | note 2 | note 2 | mSec |
| M4 ¹ | Data Hold Time | 7 | — | bus clocks |
| M5 ³ | SCL/SDA Fall Time (V _{IH} = 2.4 V to V _{IL} = 0.5 V) | — | 3 | nSec |
| M6 ¹ | Clock High time | 10 | — | bus clocks |
| M7 ¹ | Data Setup Time | 2 | — | bus clocks |
| M8 ¹ | Start Condition Setup Time (for repeated start condition only) | 20 | — | bus clocks |
| M9 ¹ | Stop Condition Setup Time | 10 | — | bus clocks |
| <p>1. Note: Output numbers are dependent on the value programmed into the MFDR; an MFDR programmed with the maximum frequency (MFDR = 0x20) will result in minimum output timings as shown in the above table. The MBUS interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the MFDR; however, numbers given in the above table are the minimum values.</p> <p>2. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.</p> <p>3. Specified at a nominal 20 pF load.</p> | | | | |

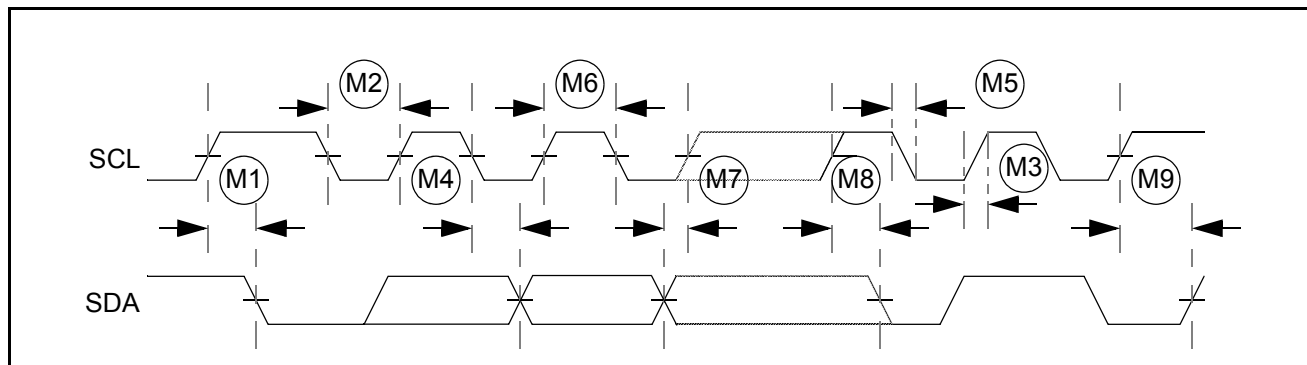


Figure 8. I2C Timing Definition

Table 27. I2C Output Bus Timings

| Num | Characteristic | 96 MHz | | Units |
|--|--|--------|-----|-------|
| | | Min | Max | |
| M10 ³ | SCL, SDA Valid to BCLK (input setup) | 2 | — | nSec |
| M11 | BCLK to SCL, SDA Invalid (input hold) | 4.5 | — | nSec |
| M12 ¹ | BCLK to SCL, SDA Low (output valid) | — | 10 | nSec |
| M13 ² | BCLK to SCL, SDA Invalid (output hold) | 3 | — | nSec |
| <ol style="list-style-type: none"> 1. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are driven low by the processor. The time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values. 2. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are actively being driven or held low by the processor. 3. SCL and SDA are internally synchronized. This setup time must be met only if recognition on a particular clock is required. | | | | |

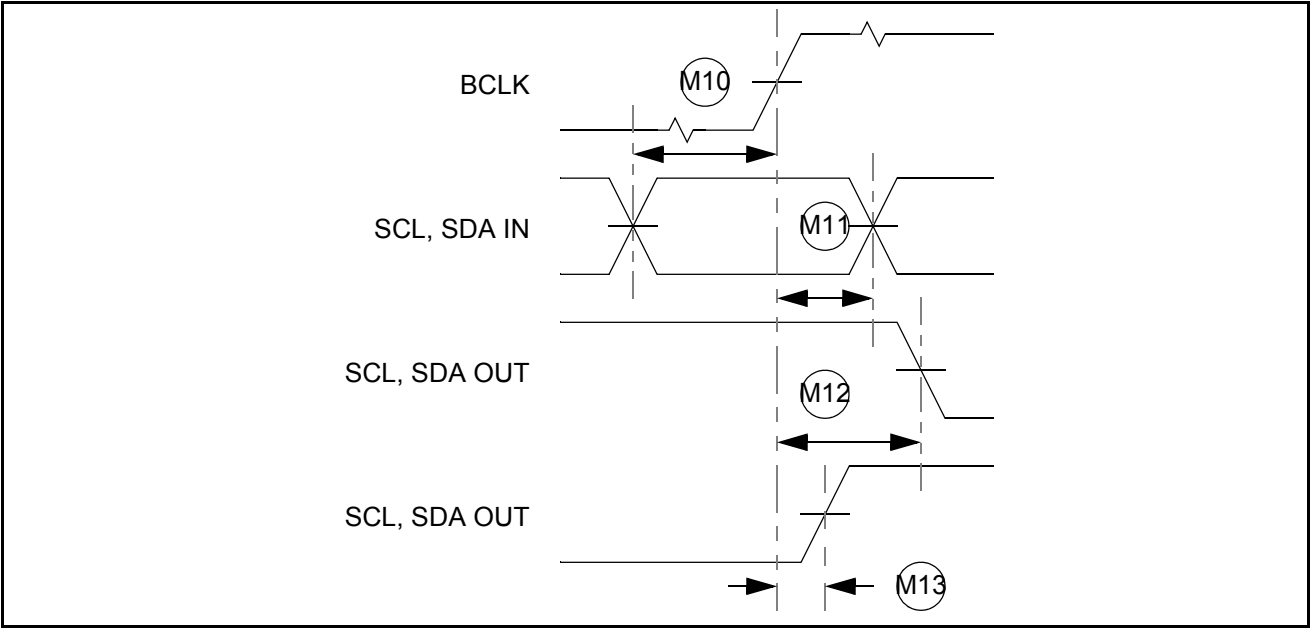


Figure 9. I2C and System Clock Timing Relationship

Table 28. General-Purpose I/O Port AC Timing Specifications

| Num | Characteristic | | | Units |
|-----|------------------------------------|-----|-----|-------|
| | | Min | Max | |
| P1 | GPIO Valid to BCLK (input setup) | 6 | — | nSec |
| P2 | BCLK to GPIO Invalid (input hold) | 0 | — | nSec |
| P3 | BCLK to GPIO Valid (output valid) | — | tbd | nSec |
| P4 | BCLK to GPIO Invalid (output hold) | 1 | — | nSec |

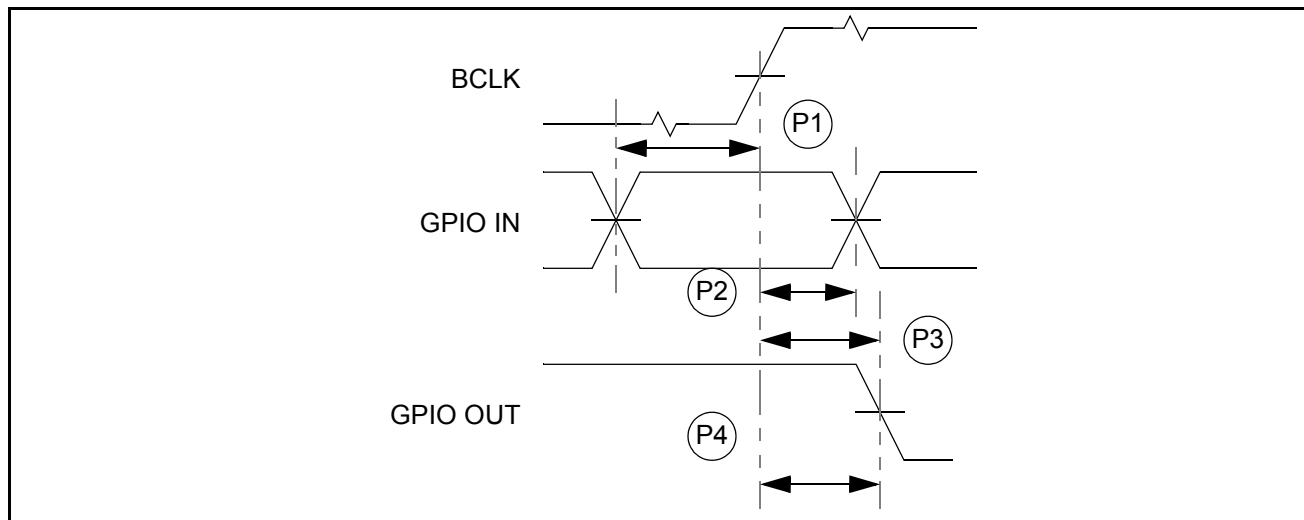


Figure 10. General-Purpose Parallel Port Timing Definition

Table 29. IEEE 1149.1 (JTAG) AC Timing Specifications

| Num | Characteristic | | | Units |
|-----|--|-----|-----|-------|
| | | Min | Max | |
| - | TCK Frequency of Operation | 0 | 10 | MHz |
| J1 | TCK Cycle Time | 100 | - | nSec |
| J2a | TCK Clock Pulse High Width | 25 | - | nSec |
| J2b | TCK Clock Pulse Low Width | 25 | - | nSec |
| J3a | TCK Fall Time ($V_{IH}=2.4$ V to $V_{IL}=0.5$ V) | — | 5 | nSec |
| J3b | TCK Rise Time ($V_{IL}=0.5$ v to $V_{IH}=2.4$ V) | — | 5 | nSec |
| J4 | TDI, TMS to TCK rising (Input Setup) | 8 | — | nSec |
| J5 | TCK rising to TDI, TMS Invalid (Hold) | 10 | — | nSec |
| J6 | Boundary Scan Data Valid to TCK (Setup) | tbd | — | nSec |
| J7 | TCK to Boundary Scan Data Invalid to rising edge (Hold) | tbd | — | nSec |
| J8 | $\overline{\text{TRST}}$ Pulse Width (asynchronous to clock edges) | 12 | — | nSec |
| J9 | TCK falling to TDO Valid (signal from driven or three-state) | — | 15 | nSec |
| J10 | TCK falling to TDO High Impedance | — | 15 | nSec |
| J11 | TCK falling to Boundary Scan Data Valid (signal from driven or three-state) | — | tbd | nSec |

Table 29. IEEE 1149.1 (JTAG) AC Timing Specifications (continued)

| Num | Characteristic | | | Units |
|-----|--|-----|------|-------|
| | | Min | Max | |
| J12 | TCK falling to Boundary Scan Data High Impedance | — | tbid | nSec |

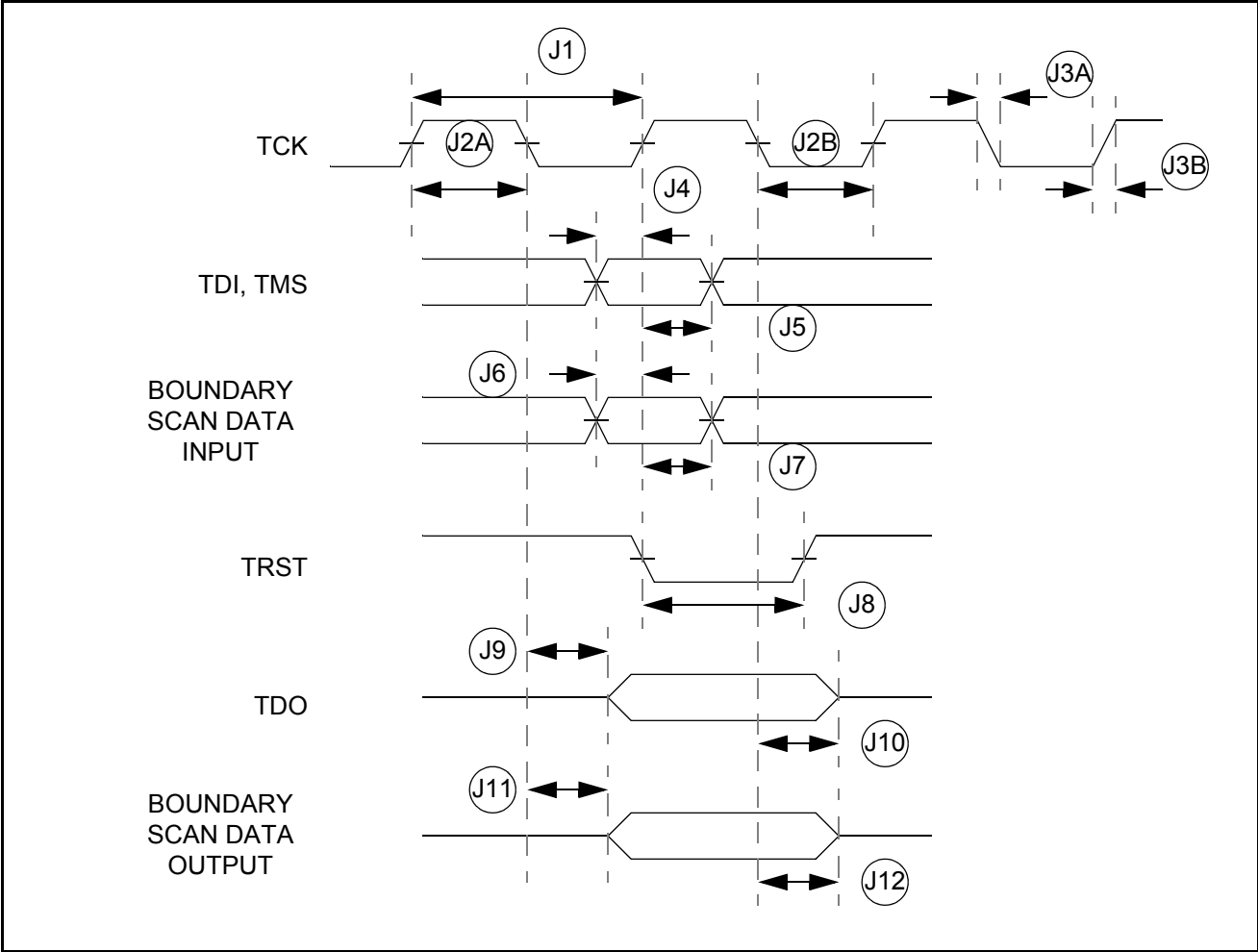


Figure 11. JTAG Timing

5.1 IIS Module AC Timing Specifications

Table 30. SCLK INPUT, SDATAO OUTPUT Timing Specifications

| Name | Characteristic | | | Unit |
|------|--------------------------|-----|-----|------|
| | | Min | Max | |
| TU | SCLK fall to SDATAO rise | --- | 25 | ns |
| TD | SCLK fall to SDATAO fall | --- | 25 | ns |

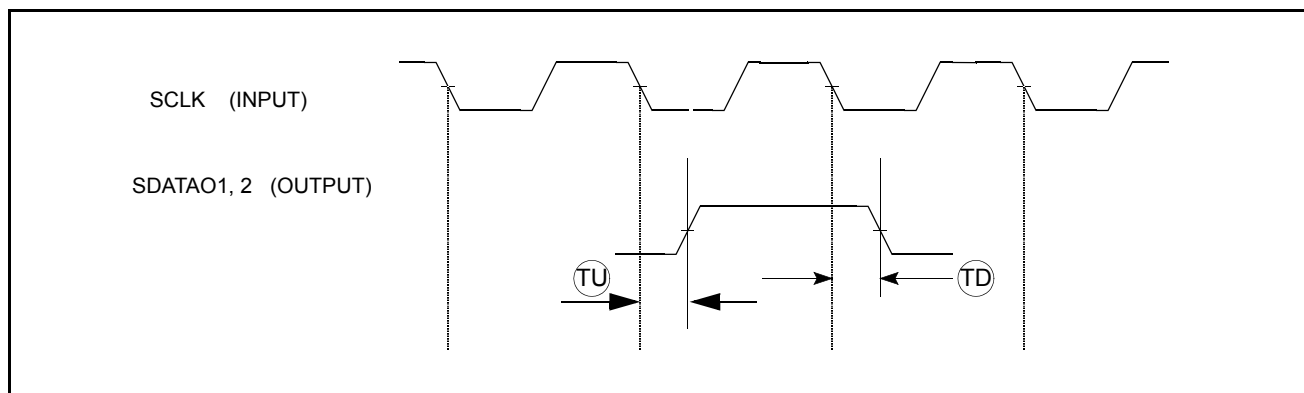


Figure 12. SCLK Input, SDATA Output Timing

Table 31. SCLK OUTPUT, SDATAO OUTPUT Timing Specifications

| Name | Characteristic | | | Unit |
|------|--------------------------|-----|-----|------|
| | | Min | Max | |
| TU | SCLK fall to SDATAO rise | --- | 3 | ns |
| TD | SCLK fall to SDATAO fall | --- | 3 | ns |

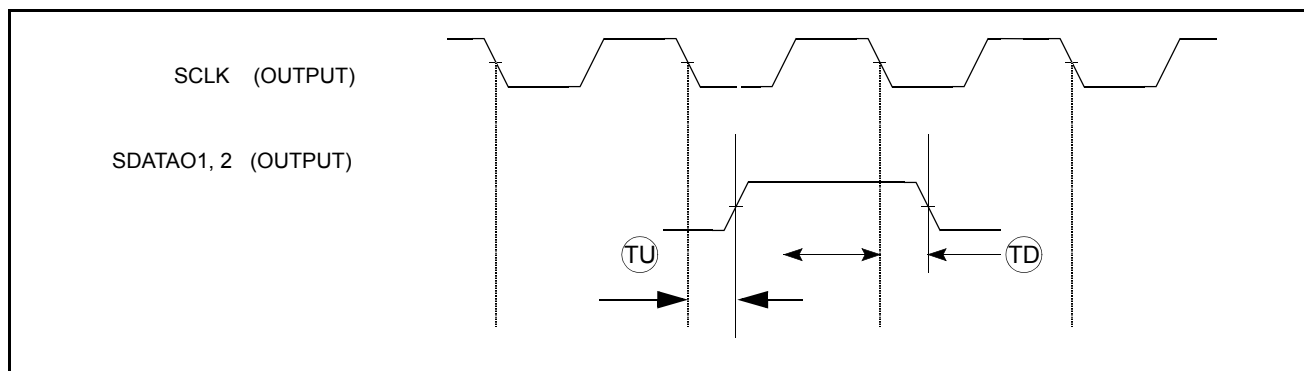


Figure 13. SCLK Output, SDATAO Output Timing Diagram

Table 32. SCLK INPUT, SDATAI INPUT Timing Specifications

| Name | Characteristic | | | Unit |
|------|---------------------|-----|-----|------|
| | | Min | Max | |
| TSU | SDATAI IN to SCLKn | -5 | — | ns |
| TH | SCLK rise to SDATAI | 3 | — | ns |

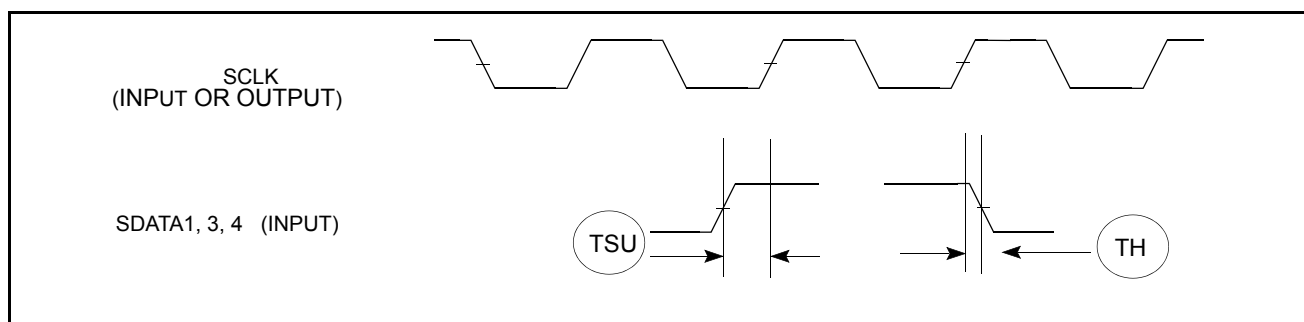


Figure 14. SCLK Input/Output, SDATAI Input Timing Diagram

6 Pin-Out and Package Information

6.1 Pinning Chart

Table 33. 144 QFP Pin Assignments

| 144 QFP Pin Number | Name | Type | Description | Pin State After Reset |
|--------------------|-----------|------|----------------------------|--|
| 01 | DATA16 | I/O | Data | X |
| 02 | A23/GPO54 | I/O | SDRAM address / static adr | Out (requires pull up /down for boot-up selection) |
| 03 | PAD-VDD | | | |
| 04 | A22 | O | SDRAM address / static adr | Out |
| 05 | A21 | O | SDRAM address / static adr | Out |
| 06 | A20/A24 | O | SDRAM address / static adr | Out |
| 07 | A19 | O | SDRAM address / static adr | Out |
| 08 | A18 | O | SDRAM address / static adr | Out |

Table 33. 144 QFP Pin Assignments (continued)

| 144 QFP Pin Number | Name | Type | Description | Pin State After Reset |
|--------------------------|-------------|------|---|--------------------------|
| 09 | PAD-GND | | | |
| 10 | A17 | O | SDRAM address / static adr | Out |
| 11 | A16 | O | SDRAM address / static adr | Out |
| 12 | A15 | O | SDRAM address / static adr | Out |
| 13 | A14 | O | SDRAM address / static adr | Out |
| 14 | A13 | O | SDRAM address / static adr | Out |
| 15 | PAD-VDD | | | |
| 16 | A12 | O | SDRAM address / static adr | Out |
| 17 | A11 | O | SDRAM address / static adr | Out |
| 18 | CORE-VDD | | | |
| 19 | CORE-GND | | | |
| 20 | A10 | O | SDRAM address / static adr | Out |
| 21 | A9 | O | SDRAM address / static adr | Out |
| 22 | A8 | O | SDRAM address / static adr | Out |
| 23 | A7 | O | SDRAM address / static adr | Out |
| 24 | A6 | O | SDRAM address / static adr | Out |
| 25 | A5 | O | SDRAM address / static adr | Out |
| 26 | PAD-GND | | PAD-GND | |
| 27 | A4 | O | SDRAM address / static adr | Out |
| 28 | A3 | o | SDRAM address / static adr | Out |
| 29 | A2 | o | SDRAM address / static adr | Out |
| 30 | A1 | o | SDRAM address / static adr | Out |
| 31 | CS0/CS4 | o | Static chip select 0 / static chip select 4 | Out |
| 32 | RW | o | Bus write enable | Out |
| 33 | OSC PAD VDD | | | |
| 34 | CRIN | I | Crystal / external clock input | X |

Table 33. 144 QFP Pin Assignments (continued)

| 144 QFP Pin Number | Name | Type | Description | Pin State After Reset |
|--------------------|---------------------------------------|------|---|--|
| 35 | CROUT | O | Crystal clock output | X |
| 36 | OSC PAD GND | | OSC_PAD_GND | |
| 37 | PLL CORE1 VDD | | | |
| 38 | PLL CORE2 VDD | | | |
| 39 | PLL CORE2 GND | | | |
| 40 | PLL CORE1 GND | | | |
| 41 | OE | O | Output Enable | Out |
| 42 | IDE-DIOW/GPIO32 | I/O | IDE DIOW | Out / HIGH |
| 43 | IDE-IORDY/GPIO33 | I/O | IDE interface IORDY | In / LOW |
| 44 | IDE-DIOR/GPIO31 | I/O | IDE interface DIOR | Out / HIGH |
| 45 | BUFENB2/GPIO30 | I/O | External buffer 2 enable | Out / HIGH |
| 46 | BUFENB1/GPIO29 | I/O | External buffer 1 enable | Out / HIGH |
| 47 | TA/GPIO12 | I/O | Transfer acknowledge | In (requires pull-up for normal operation) |
| 48 | WAKE_UP/ GPIO21 | I/O | Wake-up input | In (requires pull-up for normal operation) |
| 49 | EBUIN2/SCLK_OUT/ GPIO13 | I/O | Audio interfaces EBU in 2 / FlashMedia Clock | In / LOW |
| 50 | EBUIN3/CMD_SDIO2/ GPIO14 | I/O | Audio interfaces EBU in 3 / FlashMedia Command interface | In / LOW |
| 51 | PAD VDD | | | |
| 52 | EBUIN1/GPIO36 | I/O | Audio interfaces EBU in 1 | In / LOW |
| 53 | EBUOUT1/GPIO37 | I/O | Audio interfaces EBU out 1 | Out / LOW |
| 54 | XTRIM/GPIO0 | I/O | Audio interfaces X-tal trim | Out / clock out |
| 55 | CS1/QSPI_CS3/GPIO28 | I/O | Chip select 1/ QSPI Chip Select 3 | Out / HIGH |
| 56 | RCK/ QSPI_DIN/QSPI_DOUT/ GPIO26 | I/O | Subcode RCK interface / QSPI Data In / Data Out | Out / LOW |

Table 33. 144 QFP Pin Assignments (continued)

| 144 QFP Pin Number | Name | Type | Description | Pin State After Reset |
|--------------------|-----------------------------|------|--|-----------------------|
| 57 | QSPI_CLK/SUBR/ GPIO25 | I/O | QSPI clock pin / subcode interface | Out / LOW |
| 58 | QSPI_DOUT/SFSY/ GPIO27 | I/O | QSPI Data Output / subcode interface SFSY | Out / LOW |
| 59 | QSPI_CS1/EBUOUT2/ GPIO16 | I/O | QSPI Chip select 1 output / audio interface EBU output 2 | Out / LOW |
| 60 | QSPI_CS0/EBUIN4/ GPIO15 | I/O | QSPI chip select 0 / audio interface EBUIN 4 | Out / LOW |
| 61 | PAD GND | | | |
| 62 | SCLK1/GPIO20 | I/O | Audio interfaces serial clock 1 | In / LOW |
| 63 | LRCK1/GPIO19 | I/O | Audio interfaces word clock 1 | In / LOW |
| 64 | SDATAO1/TOUT0/ GPIO18 | I/O | Audio interfaces serial data output 1 / Timer output 0 | Out / LOW |
| 65 | SDATAI1/GPIO17 | I | Audio interfaces serial data in 1 | In / LOW |
| 66 | CFLG/GPIO5 | I/O | CFLG input | In / LOW |
| 67 | EF/GPIO6 | I/O | Error flag input | In / LOW |
| 68 | QSPI_CS2/MCLK2/ GPIO24 | I/O | QSPI Chip Select output 2 / audio master clock output 2 | Out / LOW |
| 69 | SDATAI3/GPIO8 | I/O | Audio interfaces serial data input 3 | In / LOW |
| 70 | ADIN0/GPI52 | A | AD input 0 | In only |
| 71 | ADIN1/GPI53 | A | AD input 1 | In only |
| 72 | ADIN2/GPI54 | A | AD input 2 | In only |
| 73 | ADVDD | | | |
| 74 | ADGND | | | |
| 75 | ADIN3/GPI55 | A | AD input 3 | In only |
| 76 | ADIN4/GPI56 | A | AD input 4 | In only |
| 77 | ADIN5/GPI57 | A | AD input 5 | In only |
| 78 | ADREF | A | ADC reference input | In |
| 79 | ADOUT/SCLK4/ GPIO58 | I/O | AD output / SCLK4 (for GPI function in low power applications) | Out / clock output |

Table 33. 144 QFP Pin Assignments (continued)

| 144 QFP Pin Number | Name | Type | Description | Pin State After Reset |
|--------------------|--|------|---|-----------------------|
| 80 | LRCK3/GPIO43/ AUDIO_CLOCK | I/O | Audio interface LRCK3 / Audio master clock input | In / LOW |
| 81 | SCLK3/GPIO35 | I/O | Audio interface SCLK3 | In / LOW |
| 82 | SCL0/SDATA1_BS1/ GPIO41 | I/O | I2C0 clock line / FlashMedia Data interface | Out / LOW |
| 83 | SDA0/SDATA3/ GPIO42 | I/O | I2C0 data / FlashMedia data interface | Hi-Z |
| 84 | DDATA0/CTS1/ SDATA0_SDIO1/ GPIO1 | I/O | Debug / UART1 CTS / FlashMedia data interface | Out / HIGH |
| 85 | DDATA1/RTS1/ SDATA2_BS2/GPIO2 | I/O | Debug / UART1 RTS / FlashMedia data interface | Out / HIGH |
| 86 | DDATA2/CTS0/GPIO3 | I/O | Debug / UART0 CTS | Out / HIGH |
| 87 | DDATA3/RTS0/GPIO4 | I/O | Debug / UART0 RTS | Out / HIGH |
| 88 | SCL1/TXD1/GPIO10 | I/O | I2C1 clock line / second UART transmit data output | Out / LOW |
| 89 | CORE VDD | | | |
| 90 | CORE GND | | | |
| 91 | SDA1/RXD1/GPIO44 | I/O | I2C1 data line / second UART receive data input | Hi-Z |
| 92 | PAD VDD | | | |
| 93 | TXD0/GPIO45 | I/O | First UART transmit data output | Out / HIGH |
| 94 | RXD0/GPIO46 | I/O | First UART receive data input | In / LOW |
| 95 | PST3/INTMON1/ GPIO47 | I/O | Debug / interrupt monitor output 1 | Out / HIGH |
| 96 | PST2/INTMON2/ GPIO48 | I/O | Debug / interrupt monitor output 2 | Out / HIGH |
| 97 | PAD GND | | | |
| 98 | PST1/GPIO49 | I/O | Debug | Out / HIGH |
| 99 | PST0/GPIO50 | I/O | Debug | Out / HIGH |
| 100 | PSTCLK/GPIO51 | I/O | Debug | Out / clock output |
| 101 | TDO/DSO | O | JTAG/debug | BDM |

Table 33. 144 QFP Pin Assignments (continued)

| 144 QFP Pin Number | Name | Type | Description | Pin State After Reset |
|--------------------|----------------|------|---------------------------------------|-----------------------|
| 102 | TDI/DSI | I | JTAG/debug | BDM |
| 103 | TCK | I | JTAG | BDM |
| 104 | TMS/BKPT | I | JTAG/debug | BDM |
| 105 | TRST/DSCLK | I | JTAG/Debug | BDM |
| 106 | RSTI | I | Reset | X |
| 107 | SCLK2/GPIO22 | I/O | Audio interfaces serial clock 2 | In / LOW |
| 108 | LRCK2/GPIO23 | I/O | Audio interfaces EBU out 1 | In /LOW |
| 109 | LINOUT | A | Linear regulator output | X |
| 110 | LININ | A | Linear regulator input | X |
| 111 | LINGND | | Linear regulator ground | X |
| 112 | SDATAO2/GPIO34 | I/O | Audio interfaces serial data output 2 | Out / LOW |
| 113 | MCLK1/GPIO11 | I/O | Audio master clock output 1 | Out / clock output |
| 114 | HI-Z | I | JTAG | X |
| 115 | TEST2 | I | Test | X |
| 116 | TEST1 | I | Test | X |
| 117 | TEST0 | I | Test | X |
| 118 | SDWE/GPIO38 | I/O | SDRAM write enable | Out / HIGH |
| 119 | SDCAS/GPIO39 | I/O | SDRAM CAS | Out / HIGH |
| 120 | PAD VDD | | | |
| 121 | SDRAS/GPIO59 | I/O | SDRAM RAS | Out / HIGH |
| 122 | SD_CS0/GPIO60 | I/O | SDRAM chip select out 0 | Out / HIGH |
| 123 | SDLDQM/GPO52 | O | SDRAM LDQM | Out / HIGH |
| 124 | SDUDQM/GPO53 | O | SDRAM UDQM | Out / HIGH |
| 125 | BCLKE/GPIO63 | I/O | SDRAM clock enable output | Out / HIGH |
| 126 | BCLK/GPIO40 | I/O | SDRAM clock output | Out / HIGH |
| 127 | DATA31 | I/O | Data | X |
| 128 | DATA30 | I/O | Data | X |

Table 33. 144 QFP Pin Assignments (continued)

| 144 QFP Pin Number | Name | Type | Description | Pin State After Reset |
|--------------------------|---------|------|-------------|--------------------------|
| 129 | PAD GND | | | |
| 130 | DATA29 | I/O | Data | X |
| 131 | DATA28 | I/O | Data | X |
| 132 | DATA27 | I/O | Data | X |
| 133 | DATA26 | I/O | Data | X |
| 134 | DATA25 | I/O | Data | X |
| 135 | PAD-VDD | | | |
| 136 | DATA24 | I/O | Data | X |
| 137 | DATA23 | I/O | Data | X |
| 138 | DATA22 | I/O | Data | X |
| 139 | DATA21 | I/O | Data | X |
| 140 | DATA20 | I/O | Data | X |
| 141 | PAD GND | | | |
| 142 | DATA19 | I/O | Data | X |
| 143 | DATA18 | I/O | Data | X |
| 144 | DATA17 | I/O | Data | X |

6.2 Package

The SCF5250 is assembled in 144-pin QFP package. Thermal characteristics are not available at this time.



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