



## 4 x 4 REGISTER FILE OPEN-COLLECTOR

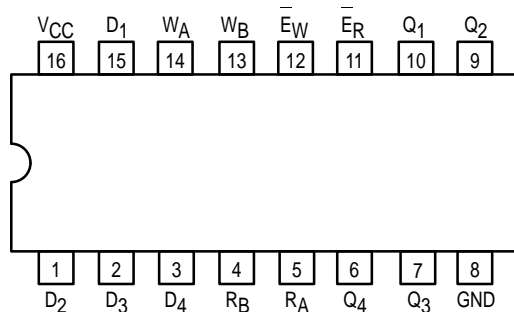
The TTL/MSI SN54/74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54/74LS670 provides a similar function to this device but it features 3-state outputs.

- Simultaneous Read/Write Operation
- Expandable to 512 Words of n-Bits
- Typical Access Time of 20 ns
- Low Leakage Open-Collector Outputs for Expansion
- Typical Power Dissipation of 125 mW

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version  
has the same pinouts  
(Connection Diagram) as  
the Dual In-Line Package.

### PIN NAMES

D <sub>1</sub> –D <sub>4</sub>	Data Inputs
W <sub>A</sub> , W <sub>B</sub>	Write Address Inputs
E <sub>W</sub>	Write Enable (Active LOW) Input
R <sub>A</sub> , R <sub>B</sub>	Read Address Inputs
E <sub>R</sub>	Read Enable (Active LOW) Input
Q <sub>1</sub> –Q <sub>4</sub>	Outputs (Note b)

### LOADING (Note a)

	HIGH	LOW
D <sub>1</sub> –D <sub>4</sub>	0.5 U.L.	0.25 U.L.
W <sub>A</sub> , W <sub>B</sub>	0.5 U.L.	0.25 U.L.
E <sub>W</sub>	1.0 U.L.	0.5 U.L.
R <sub>A</sub> , R <sub>B</sub>	0.5 U.L.	0.25 U.L.
E <sub>R</sub>	1.0 U.L.	0.5 U.L.
Q <sub>1</sub> –Q <sub>4</sub>	Open-Collector	5 (2.5) U.L.

### NOTES:

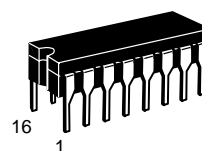
a. 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74)  
Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V<sub>CC</sub>.

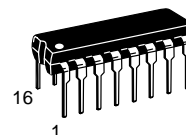
## SN54/74LS170

### 4 x 4 REGISTER FILE OPEN-COLLECTOR

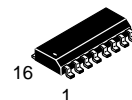
#### LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-08



**N SUFFIX**  
PLASTIC  
CASE 648-08

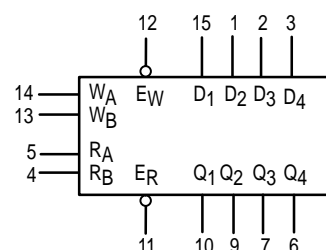


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

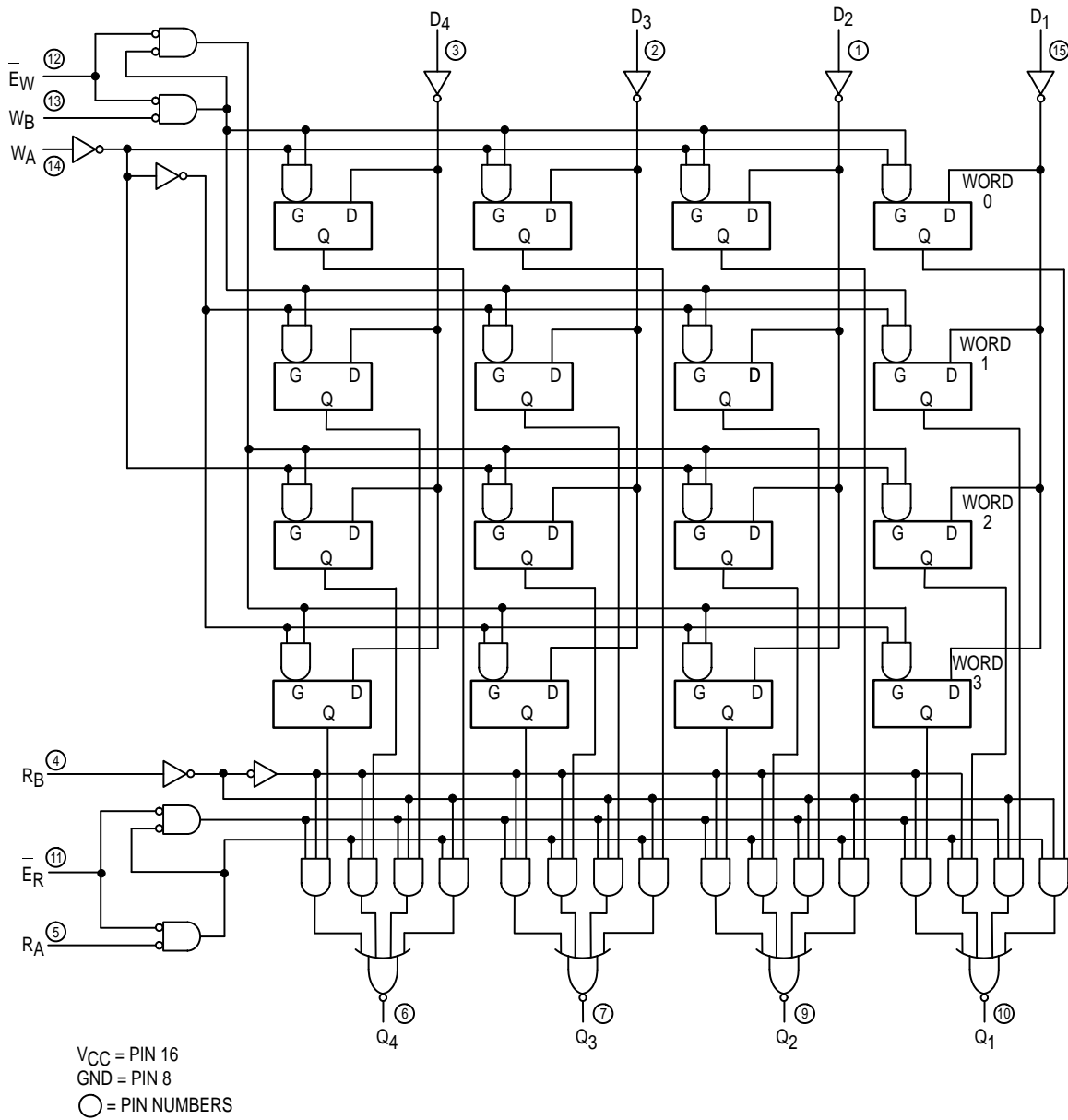
### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

# SN54/74LS170

## LOGIC DIAGRAM



# SN54/74LS170

**WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)**

WRITE INPUTS			WORD			
$W_B$	$W_A$	$E_W$	0	1	2	3
L	L	L	Q = D	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>
L	H	L	Q <sub>0</sub>	Q = D	Q <sub>0</sub>	Q <sub>0</sub>
H	L	L	Q <sub>0</sub>	Q <sub>0</sub>	Q = D	Q <sub>0</sub>
H	H	L	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q = D
X	X	H	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>

**READ FUNCTION TABLE (SEE NOTES A AND D)**

READ INPUTS			OUTPUTS			
$R_B$	$R_A$	$E_R$	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = HIGH Level, L = LOW Level, X = Irrelevant.

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q<sub>0</sub> = the level of Q before the indicated input conditions were established.

D. W<sub>0B1</sub> = The first bit of word 0, etc.

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V <sub>OH</sub>	Output Voltage — High	54, 74			5.5	V
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V <sub>IK</sub>	Input Clamp Diode Voltage			-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
I <sub>OH</sub>	Output HIGH Current	54, 74			100	μA	V <sub>CC</sub> = MIN, V <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current Any $\overline{D}$ , R, W E <sub>R</sub> , E <sub>W</sub>				20 40	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.4 V
	Any $\overline{D}$ , R, W E <sub>R</sub> , E <sub>W</sub>				0.1 0.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current Any $\overline{D}$ , R, W E <sub>R</sub> , E <sub>W</sub>				-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>CC</sub>	Power Supply Current				40	mA	V <sub>CC</sub> = MAX

# SN54/74LS170

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Negative-Going $E_R$ to Q Outputs		20 20	30 30	ns	Figure 1	$V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$ $R_L = 2.0\text{ k}\Omega$
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $R_A$ or $R_B$ to Q Outputs		25 24	40 40	ns	Figure 2	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Negative-Going $E_W$ to Q Outputs		30 26	45 40	ns	Figure 1	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Data Inputs to Q Outputs		30 22	45 35	ns	Figure 1	

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$t_W$	Pulse Width, $E_R$ , $E_W$	25			ns	$V_{CC} = 5.0\text{ V}$ $R_L = 2.0\text{ k}\Omega$	
$t_s$	Setup Time, Data to $E_W$	10			ns		
$t_s$	Setup Time, $W_A$ , $W_B$ to $E_W$	15			ns		
$t_h$	Hold Time, Data to $E_W$	15			ns		
$t_h$	Hold Time, $W_A$ , $W_B$ to $E_W$	5.0			ns		
$t_{LATCH}$	Latch Time	25			ns		

## VOLTAGE WAVEFORMS

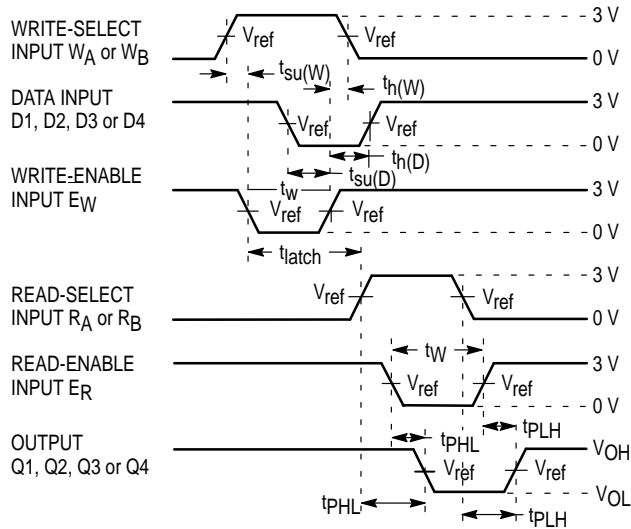


Figure 1

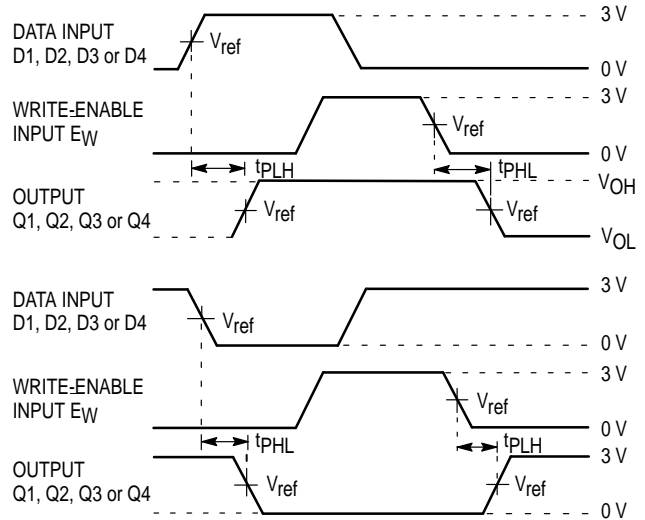


Figure 2