

## Dual Pixel LVDS Display Interface (LDI) Transmitter

### GENERAL DESCRIPTION

The CS5830 converts 48 bits (Dual pixel 24-bit color) of CMOS/TTL data into 8 LVDS (Low Voltage Differential Signalling) data streams. Control signals (VSYNC, HSYNC, DE and two user-defined signals) are sent during blanking intervals.

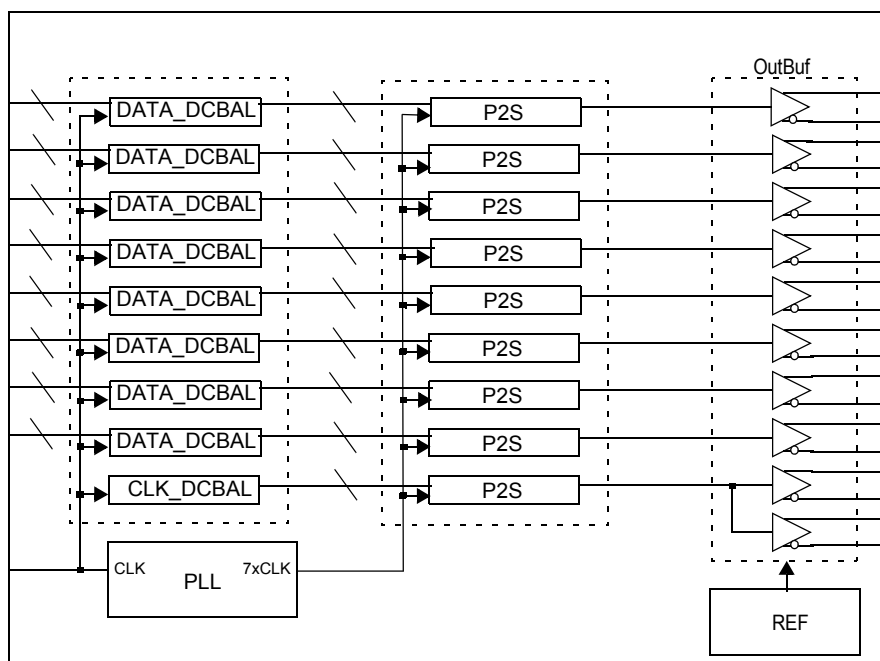
The CS5830 provides 3 operating modes: Single-In-Single-Out, Dual-In-Dual-Out and Single-In-Dual-Out. In Single-In-Single-Out and Dual-In-Dual-Out modes, single pixel data can be clocked into CS5830 at a maximum rate of 85MHz. In Single-In-Dual-Out mode, CS5830 supports a maximum clock rate of 170MHz.

DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable.

### FEATURES

- Complies with OpenLDI specification for digital display interface.
- 30 to 85 (170)MHz clock support.
- Supports SVGA through UXGA panel resolutions.
- Drives long, low cost cables.
- DC balance data transmission to reduce ISI distortion.
- Supports single and dual pixel GUI interface
- Rejects cycle-to-cycle jitter.
- 5V tolerant on data and control input pins.
- Programmable data and control strobe select (rising or falling edge strobe)
- Support for two additional user-defined control signals in DC balanced mode
- Compatible with TIA/EIA LVDS standard.
- 100-pin LQFP.

### BLOCK DIAGRAM



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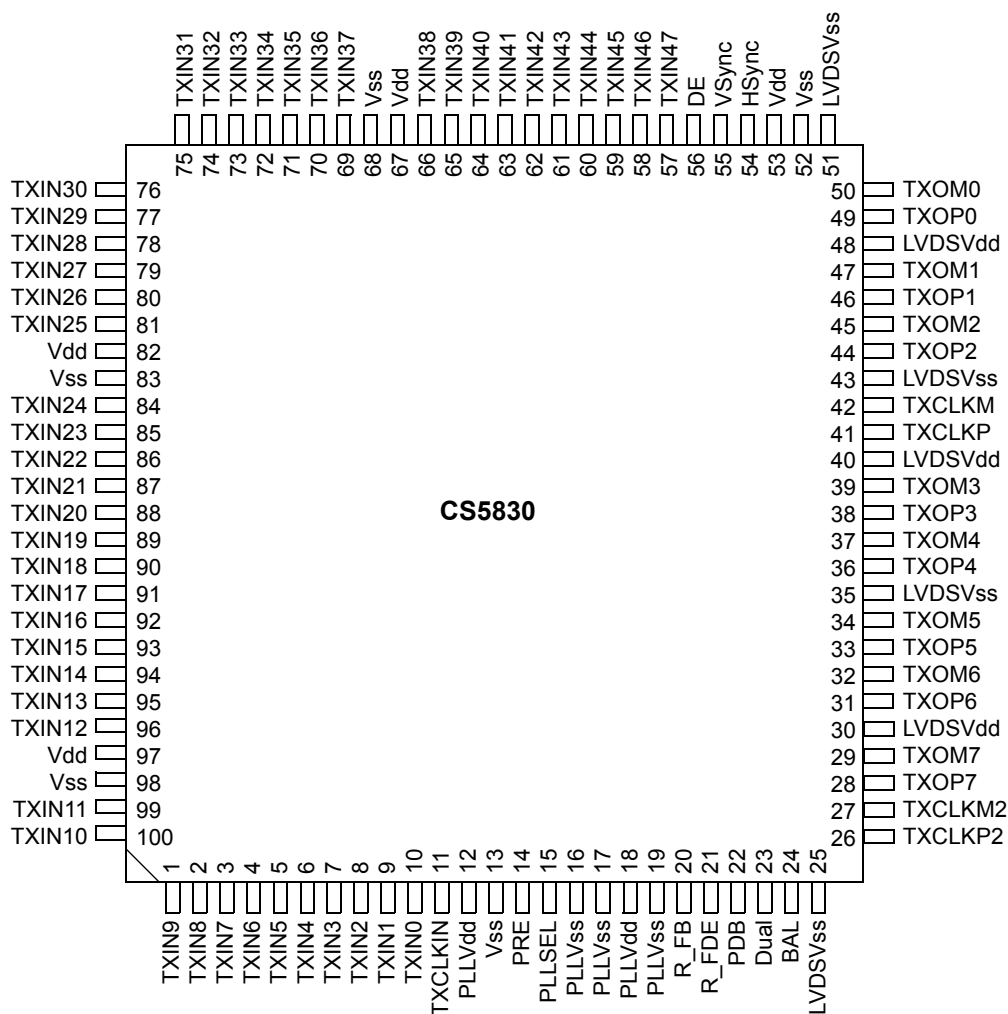
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Rev.1.0 August 2002

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**PIN CONNECTION DIAGRAM**



**PIN DESCRIPTION**

Name	I/O	Pin	Description
TXIN0	I	10	TTL level input. R10.
TXIN1	I	9	TTL level input. R11.
TXIN2	I	8	TTL level input. R12.
TXIN3	I	7	TTL level input. R13.
TXIN4	I	6	TTL level input. R14.
TXIN5	I	5	TTL level input. R15.
TXIN6	I	4	TTL level input. R16.
TXIN7	I	3	TTL level input. R17.
TXIN8	I	2	TTL level input. G10.
TXIN9	I	1	TTL level input. G11.
TXIN10	I	100	TTL level input. G12.
TXIN11	I	99	TTL level input. G13.
TXIN12	I	96	TTL level input. G14.
TXIN13	I	95	TTL level input. G15.
TXIN14	I	94	TTL level input. G16.
TXIN15	I	93	TTL level input. G17.
TXIN16	I	92	TTL level input. B10.
TXIN17	I	91	TTL level input. B11.
TXIN18	I	90	TTL level input. B12.
TXIN19	I	89	TTL level input. B13.
TXIN20	I	88	TTL level input. B14.
TXIN21	I	87	TTL level input. B15.
TXIN22	I	86	TTL level input. B16.
TXIN23	I	85	TTL level input. B17.
TXIN24	I	84	TTL level input. R20.
TXIN25	I	81	TTL level input. R21.
TXIN26	I	80	TTL level input. R22.
TXIN27	I	79	TTL level input. R23.
TXIN28	I	78	TTL level input. R24.
TXIN29	I	77	TTL level input. R25.
TXIN30	I	76	TTL level input. R26.
TXIN31	I	75	TTL level input. R27.
TXIN32	I	74	TTL level input. G20.
TXIN33	I	73	TTL level input. G21.
TXIN34	I	72	TTL level input. G22.
TXIN35	I	71	TTL level input. G23.

Name	I/O	Pin	Description
TXIN36	I	70	TTL level input. G24.
TXIN37	I	69	TTL level input. G25.
TXIN38	I	66	TTL level input. G26.
TXIN39	I	65	TTL level input. G27.
TXIN40	I	64	TTL level input. B20.
TXIN41	I	63	TTL level input. B21.
TXIN42	I	62	TTL level input. B22.
TXIN43	I	61	TTL level input. B23.
TXIN44	I	60	TTL level input. B24.
TXIN45	I	59	TTL level input. B25.
TXIN46	I	58	TTL level input. B26. CNTLF.
TXIN47	I	57	TTL level input. B27. CNTLE.
DE	I	56	Data Enable.
VSYNC	I	55	V Sync.
HSYNC	I	54	H Sync.
TXOM0	O	50	Negative LVDS differential data output.
TXOP0	O	49	Positive LVDS differential data output.
TXOM1	O	47	Negative LVDS differential data output.
TXOP1	O	46	Positive LVDS differential data output.
TXOM2	O	45	Negative LVDS differential data output.
TXOP2	O	44	Positive LVDS differential data output.
CKOM1	O	42	Negative LVDS differential clock output.
CKOP1	O	41	Positive LVDS differential clock output.
TXOM3	O	39	Negative LVDS differential data output.
TXOP3	O	38	Positive LVDS differential data output.
TXOM4	O	37	Negative LVDS differential data output.
TXOP4	O	36	Positive LVDS differential data output.
TXOM5	O	34	Negative LVDS differential data output.
TXOP5	O	33	Positive LVDS differential data output.
TXOM6	O	32	Negative LVDS differential data output.
TXOP6	O	31	Positive LVDS differential data output.
TXOM7	O	29	Negative LVDS differential data output.
TXOP7	O	28	Positive LVDS differential data output.
CKOM2	O	27	Negative LVDS differential clock output.
CKOP2	O	26	Positive LVDS differential clock output.
BAL	I	24	DC-balanced enable.

Name	I/O	Pin	Description
DUAL	I	23	Three-mode select. (Internal biasd to Vdd/2) DUAL Mode Description H dual pixel All LVDS active L single pixel TXOP/TXOM 0-3 and CKOP/CKOM 1 active F single in dual out
PDB	I	22	Power-down. Active low.
R_FDE	I	21	Programmable DE strobe select. R_FDE Mode H DE active high L DE active low
R_FB	I	20	Programmable data strobe select. R_FB Mode H TXIN strobed at TXCLKIN rising edge L TXIN strobed at TXCLKIN falling edge
PLLSEL	I	15	LVDS channel drive current select. PLLSEL Mode H 7.0mA current output L/F 3.5mA current output
PRE	I	14	Pre-emphasis level select. (CS5830 has NO pre-emphasis circuit implementation.)
TXCLKIN	I	11	Clock input.
Vdd	I	53, 67, 82 97	Power supply pins for TTL inputs and digital circuits.
Vss	I	13, 52, 68, 83, 98	Ground pins for TTL inputs and digital circuits.
PLLVdd	I	12, 18	Power supply pins for PLL and REF.
PLLVss	I	16,17,19	Ground pins for PLL and REF.
LVDSVdd	I	30, 40, 48	Power supply pins for LVDS outputs.
LVDSVss	I	25, 35, 43 51	Ground pins for LVDS outputs.

**FUNCTIONAL DESCRIPTION****PLL**

Used to generate a 7X freq. Internal clock source for Parallel-to-Serial transfer. The freq. range need to meet (30MHz X 7) min. to (85MHz X 7) max.

**REF**

A band-gap voltage reference generator used to provide one constant current source for all analog circuits. REF provides a 3.5mA current reference for OutBuf circuit to control the amplitude of output signal on LVDS channels.

**DATA\_DCBAL**

Calculates disparity and DCBAL bit value and data-word translation.

**P2S**

Parallel to serial translation block.

**OutBuf**

LVDS line driver circuit.

## ELECTRICAL CHARACTERISTICS

### Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vdd	Supply Voltage	3.0	3.3	3.6	V
T <sub>A</sub>	Operating Free Air Temperature	-10	+25	+70	C

### DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>od</sub>	Differential output voltage	250	345	450	mV
Delta (V <sub>od</sub> )				35	mV
V <sub>os</sub>	Offset Voltage	1.125	1.25	1.375	V
Delta (V <sub>os</sub> )				35	mV
I <sub>os</sub>	Output short circuit current (V <sub>od</sub> =0)		3.5	10	mA
I <sub>oz</sub>	PDB=0, V <sub>out</sub> =0 ~V <sub>cc</sub>		1	10	uA
V <sub>IH</sub>	High Level Input Voltage	1.8		5.0	V
V <sub>IL</sub>	Low Level input Voltage	GND		1.0	V

### Switching Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
LHLT/ LLHT	LVDS transition time (Figure 3), PLLSEL=L/F			0.5		ns
	LVDS transition time (Figure 3), PLLSEL=H			0.4		ns
THTC	TxIN hold to TxCLK IN (Figure 5)		0			ns
TSTC	TxIN setup to TxCLK IN (Figure 5)		2.7			ns
TCIT	TxCLK IN Transition Time (Figure 4)	DUAL=H/L	1.0	2.0	3.0	ns
		DUAL=F	1.0	1.5	1.7	ns
TCIP	TxCLK in period (Figure 5)	DUAL=H/L	11.76	T	33.33	ns
		DUAL=F	5.88		16.67	ns
TCIH	TxCLK in high time (Figure 5)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK in low time (Figure 5)		0.35T	0.5T	0.65T	ns
TXIT	TxIN transition time		1.5		6.0	ns
TBIT	Transmitter output bit width	DUAL=H/L		1/7TCIP		ns
		DUAL=F		2/7TCIP		ns
TCCS	TxOUT channel to channel skew			100		ps
TPLLS	Transmitter phase lock loop set (Figure 6)				10	ms
TPDD	Transmitter powerdown delay (Figure 7)				100	ns

Power Supply Current

Symbol	Parameter	Conditions	Freq.	Min	Typ	Max	Unit
I <sub>dd</sub>	Quiescent Supply Current (average)	Worst_case pattern Dual = High BAL = High	32MHZ 48MHZ 65MHZ 85MHZ	- - - -			mA
		Gray_scale pattern Dual = High BAL = High	32MHZ 48MHZ 65MHZ 85MHZ	- - - -			mA
		Power Down	-				uA

AC Timing Diagram

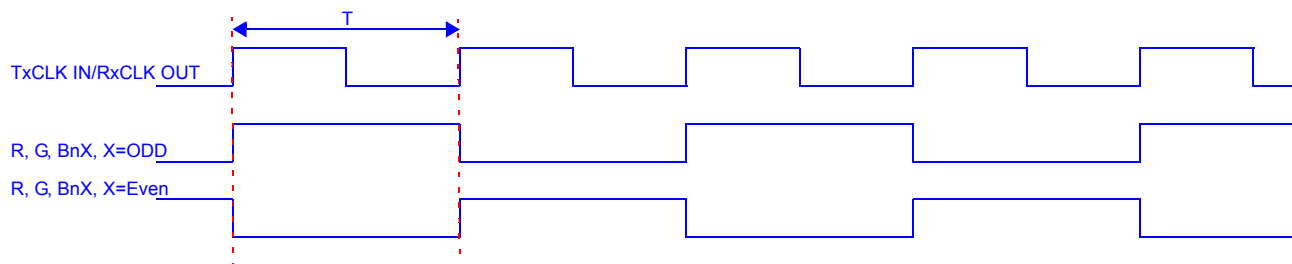


Figure-1 "Worst Case" Test Pattern



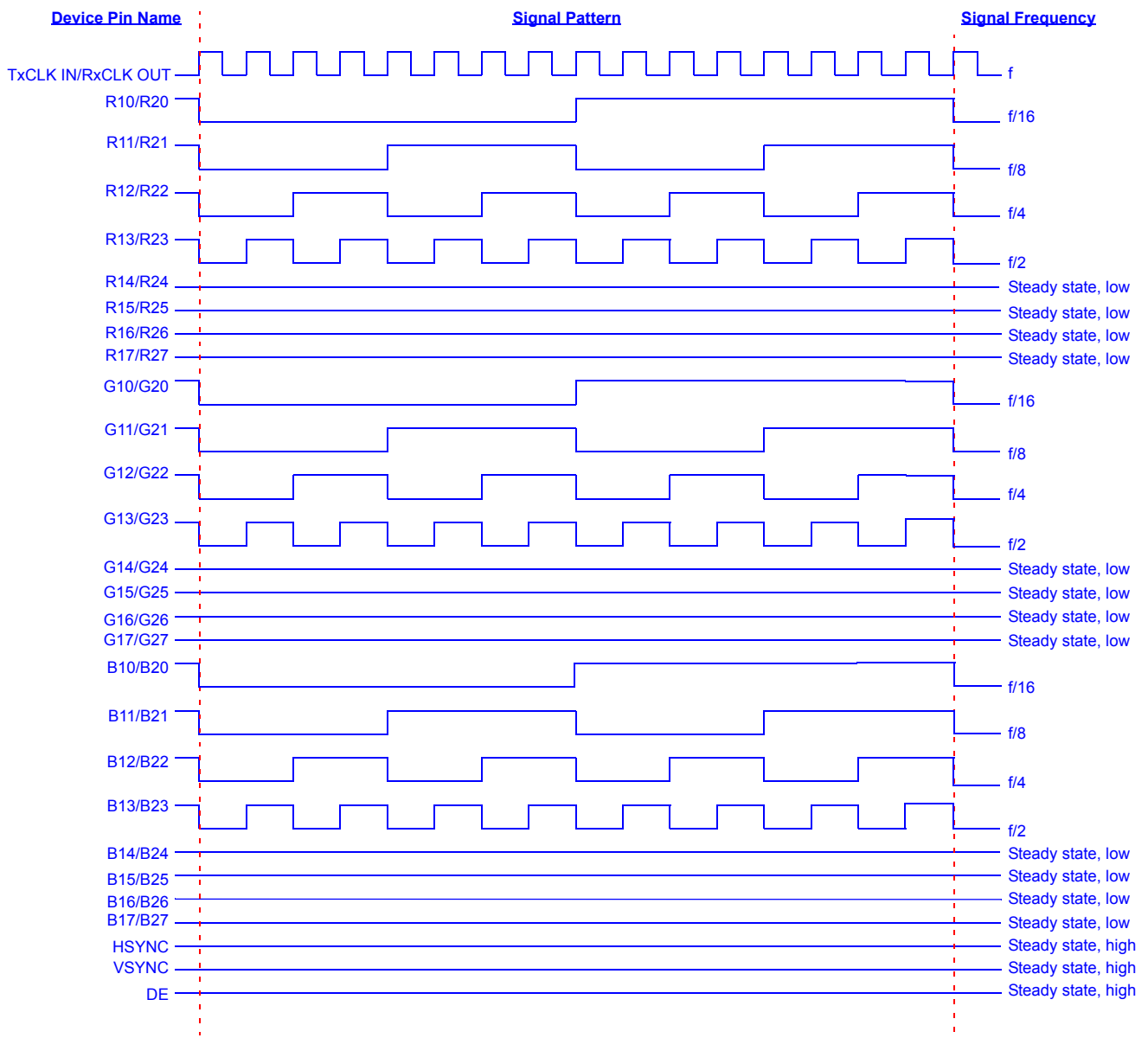


Figure-2 “16 Grayscale” Test Pattern

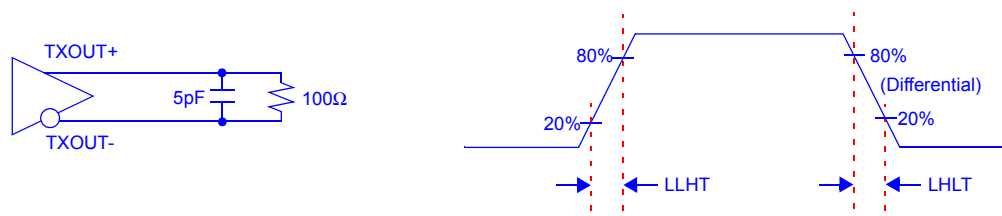


Figure-3 LVDS Output Load and Transition Times

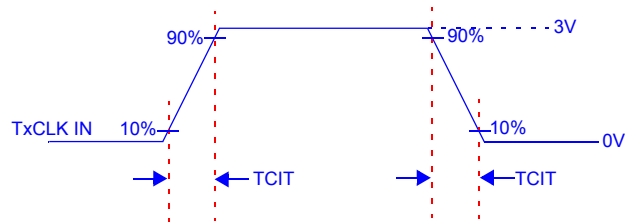


Figure-4 Input Clock Transition Time

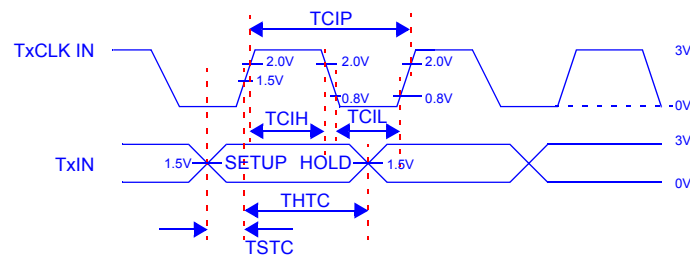


Figure-5 Setup/Hold and High/Low Times (Rising Edge Strobe)

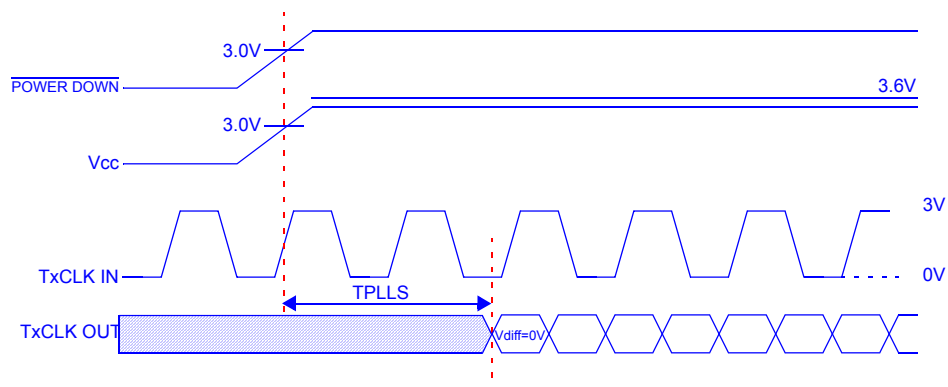


Figure-6 CS5830 (Transmitter) Phase Lock Loop Set Time

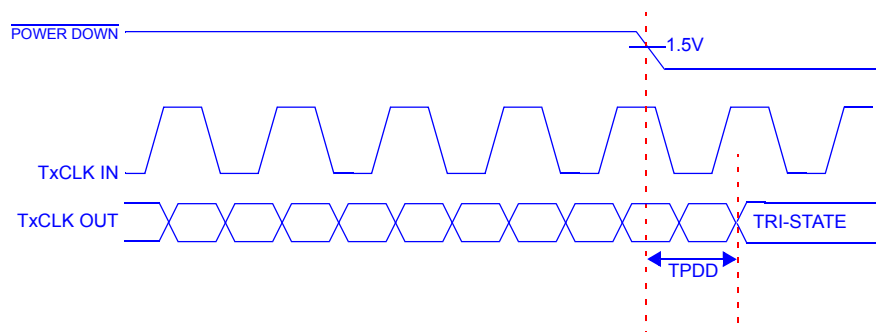


Figure-7 Transmitter Power Down Delay

## COLOR MAPPING TABLE

### Single-In-Single-Out Data Mapping

VGA - TFT Data Signals Color Bits			CS5830 Input Pin Names	TFT Panel Data Signals	
	24-bit	18-bit		24-bit	18-bit
<b>LSB</b>	R0		TXIN0	R0	
	R1		TXIN1	R1	
	R2	R0	TXIN2	R2	R0
	R3	R1	TXIN3	R3	R1
	R4	R2	TXIN4	R4	R2
	R5	R3	TXIN5	R5	R3
	R6	R4	TXIN6	R6	R4
<b>MSB</b>	R7	R5	TXIN7	R7	R5
<b>LSB</b>	G0		TXIN8	G0	
	G1		TXIN9	G1	
	G2	G0	TXIN10	G2	G0
	G3	G1	TXIN11	G3	G1
	G4	G2	TXIN12	G4	G2
	G5	G3	TXIN13	G5	G3
	G6	G4	TXIN14	G6	G4
<b>MSB</b>	G7	G5	TXIN15	G7	G5
<b>LSB</b>	B0		TXIN16	B0	
	B1		TXIN17	B1	
	B2	B0	TXIN18	B2	B0
	B3	B1	TXIN19	B3	B1
	B4	B2	TXIN20	B4	B2
	B5	B3	TXIN21	B5	B3
	B6	B4	TXIN22	B6	B4
<b>MSB</b>	B7	B5	TXIN23	B7	B5

### Dual-In-Dual-Out Data Mapping

VGA - TFT Data Signals Color Bits			CS5830 Input Pin Names	TFT Panel Data Signals	
	48-bit	36-bit		48-bit	36-bit
<b>LSB</b>	RO0		TXIN0	RO0	
	RO1		TXIN1	RO1	
	RO2	RO0	TXIN2	RO2	RO0
	RO3	RO1	TXIN3	RO3	RO1
	RO4	RO2	TXIN4	RO4	RO2
	RO5	RO3	TXIN5	RO5	RO3
	RO6	RO4	TXIN6	RO6	RO4
<b>MSB</b>	RO7	RO5	TXIN7	RO7	RO5
<b>LSB</b>	GO0		TXIN8	GO0	

VGA - TFT Data Signals Color Bits			CS5830 Input Pin Names	TFT Panel Data Signals	
	GO1		TXIN9	GO1	
	GO2	GO0	TXIN10	GO2	GO0
	GO3	GO1	TXIN11	GO3	GO1
	GO4	GO2	TXIN12	GO4	GO2
	GO5	GO3	TXIN13	GO5	GO3
	GO6	GO4	TXIN14	GO6	GO4
<b>MSB</b>	GO7	GO5	TXIN15	GO7	GO5
<b>LSB</b>	BO0		TXIN16	BO0	
	BO1		TXIN17	BO1	
	BO2	BO0	TXIN18	BO2	BO0
	BO3	BO1	TXIN19	BO3	BO1
	BO4	BO2	TXIN20	BO4	BO2
	BO5	BO3	TXIN21	BO5	BO3
	BO6	BO4	TXIN22	BO6	BO4
<b>MSB</b>	BO7	BO5	TXIN23	BO7	BO5
<b>LSB</b>	RE0		TXIN24	RE0	
	RE1		TXIN25	RE1	
	RE2	RE0	TXIN26	RE2	RE0
	RE3	RE1	TXIN27	RE3	RE1
	RE4	RE2	TXIN28	RE4	RE2
	RE5	RE3	TXIN29	RE5	RE3
	RE6	RE4	TXIN30	RE6	RE4
<b>MSB</b>	RE7	RE5	TXIN31	RE7	RE5
<b>LSB</b>	GE0		TXIN32	GE0	
	GE1		TXIN33	GE1	
	GE2	GE0	TXIN34	GE2	GE0
	GE3	GE1	TXIN35	GE3	GE1
	GE4	GE2	TXIN36	GE4	GE2
	GE5	GE3	TXIN37	GE5	GE3
	GE6	GE4	TXIN38	GE6	GE4
<b>MSB</b>	GE7	GE5	TXIN39	GE7	GE5
<b>LSB</b>	BE0		TXIN40	BE0	
	BE1		TXIN41	BE1	
	BE2	BE0	TXIN42	BE2	BE0
	BE3	BE1	TXIN43	BE3	BE1
	BE4	BE2	TXIN44	BE4	BE2
	BE5	BE3	TXIN45	BE5	BE3
	BE6	BE4	TXIN46	BE6	BE4
<b>MSB</b>	BE7	BE5	TXIN47	BE7	BE5

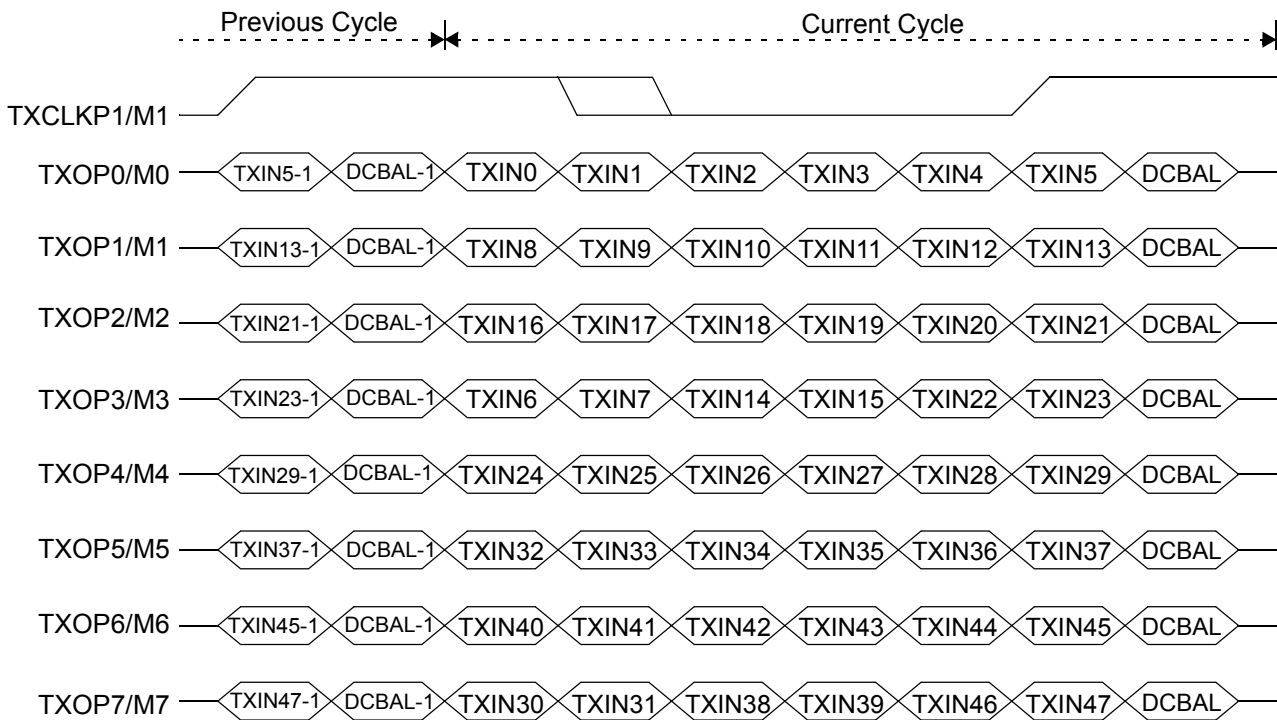
**Single-In-Dual-Out Data Mapping**

VGA - TFT Data Signals Color Bits			CS5830 Input Pin Names	TFT Panel Data Signals	
	24-bit	18-bit		48-bit	36-bit
<b>LSB</b>	R0		TXIN0	RO0	
	R1		TXIN1	RO1	
	R2	R0	TXIN2	RO2	RO0
	R3	R1	TXIN3	RO3	RO1
	R4	R2	TXIN4	RO4	RO2
	R5	R3	TXIN5	RO5	RO3
	R6	R4	TXIN6	RO6	RO4
<b>MSB</b>	R7	R5	TXIN7	RO7	RO5
<b>LSB</b>	G0		TXIN8	GO0	
	G1		TXIN9	GO1	
	G2	G0	TXIN10	GO2	GO0
	G3	G1	TXIN11	GO3	GO1
	G4	G2	TXIN12	GO4	GO2
	G5	G3	TXIN13	GO5	GO3
	G6	G4	TXIN14	GO6	GO4
<b>MSB</b>	G7	G5	TXIN15	GO7	GO5
<b>LSB</b>	B0		TXIN16	BO0	
	B1		TXIN17	BO1	
	B2	B0	TXIN18	BO2	BO0
	B3	B1	TXIN19	BO3	BO1
	B4	B2	TXIN20	BO4	BO2
	B5	B3	TXIN21	BO5	BO3
	B6	B4	TXIN22	BO6	BO4
<b>MSB</b>	B7	B5	TXIN23	BO7	BO5
			TXIN0	RE0	
			TXIN1	RE1	
			TXIN2	RE2	RE0
			TXIN3	RE3	RE1
			TXIN4	RE4	RE2
			TXIN5	RE5	RE3
			TXIN6	RE6	RE4
			TXIN7	RE7	RE5
			TXIN8	GE0	
			TXIN9	GE1	
			TXIN10	GE2	GE0
			TXIN11	GE3	GE1
			TXIN12	GE4	GE2
			TXIN13	GE5	GE3
			TXIN14	GE6	GE4

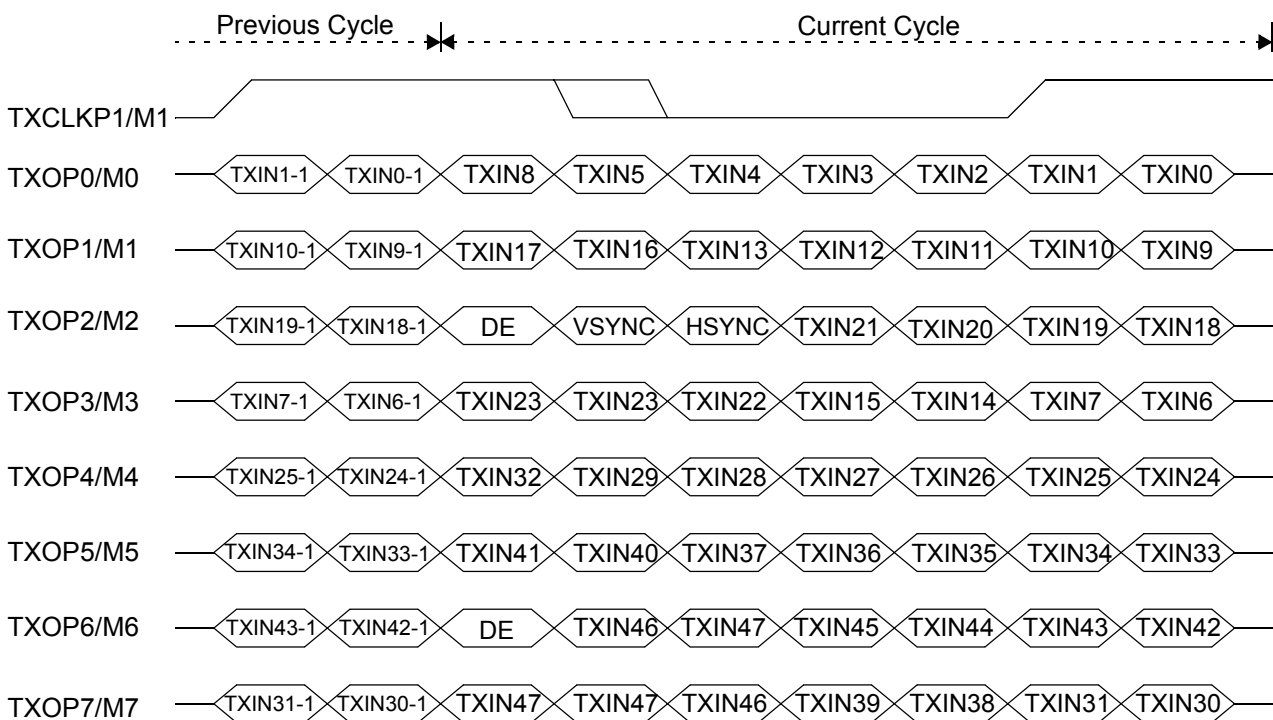
VGA - TFT Data Signals Color Bits			CS5830 Input Pin Names	TFT Panel Data Signals	
			TXIN15	GE7	GE5
			TXIN16	BE0	
			TXIN17	BE1	
			TXIN18	BE2	BE0
			TXIN19	BE3	BE1
			TXIN20	BE4	BE2
			TXIN21	BE5	BE3
			TXIN22	BE6	BE4
			TXIN23	BE7	BE5

## LVDS CLOCK/DATA CHANNEL TIMING

### With DC Balance



### Without DC Balance



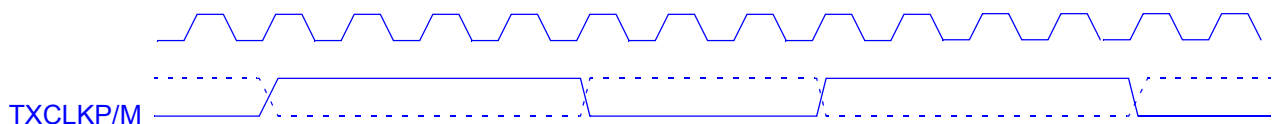
**DC Balance**

Running-Word-Disparity	Current-Word-Disparity	DCBAL	The-Sent-Word
+	+	1	Reversed
+	0/-	0	No-changed
-	+	0	No-changed
-	0/-	1	Reversed
0	+/-0/-	1	Reversed

**Note:** Current-Word-Disparity = ((1's #) - (0's #)) of Need-To-Be-Sent-Data; Running-Word-Disparity = ((1's #) - (0's #)) of All-Been-Sent-Data.

**Deskew**

In non-DC balanced mode (BAL=0), the CS5830's clock channel will send 1111000 pattern, like:



In DC balanced mode (BAL = 1), the CS5830's clock channel will send 1110000 or 1111000 pattern when DE = High, like:



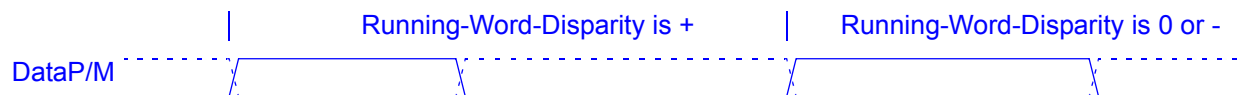
In DC balanced mode (BAL=1), the CS5830's clock channel will send 1100000 or 1111100 pattern when DE = Low, like:



In DC balanced mode (BAL=1), the CS5830's 2, 3, 6, 7 data channel will send 1110000 or 1111000 pattern when DE =Low, like:



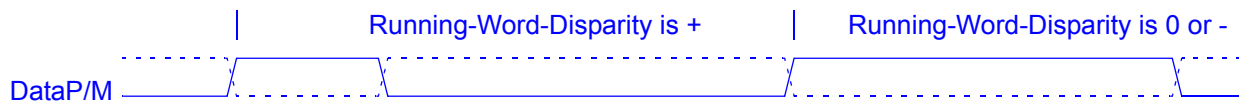
In DC balanced mode (BAL=1), the CS5830's 0,1, 4, 5 data channel will send 1110000 or 1111000 pattern in (DE = Low and CTRL = Low), like:



In DC balanced mode (BAL=1), the CS5830's 0, 1, 4, 5 data channel will send 1100000 or 1111100 pattern in

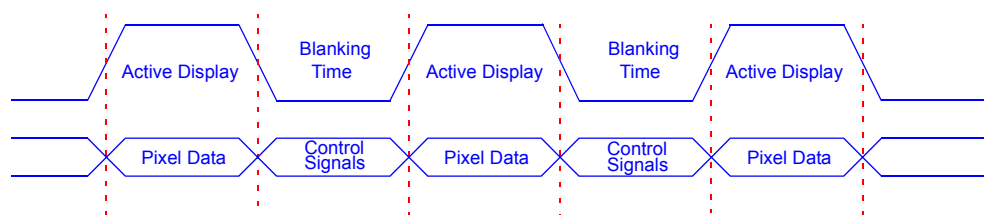


(DE=Low and CTRL = High), like:



### Configuration table

Pin Condition	Configuration
R_FB = Vdd R_FB = Vss	Rising edge data strobe. Falling edge data strobe.
R_FDE = Vdd R_FDE = Vss	Active data DE = high. Active data DE = low.
BAL = Vdd BAL = Vss	DC balanced enabled. DC balanced disabled.
DUAL = Vdd DUAL = Floating DUAL = Vss	Dual-In-Dual-Out Single-In-Dual-Out Single-In-Single-Out

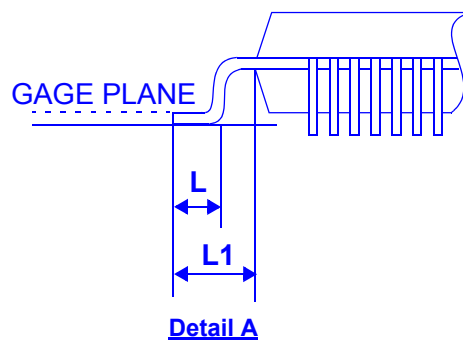
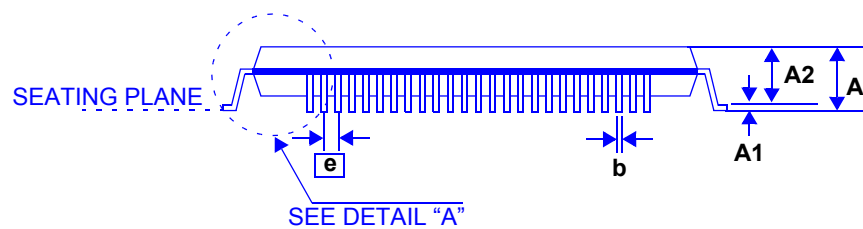
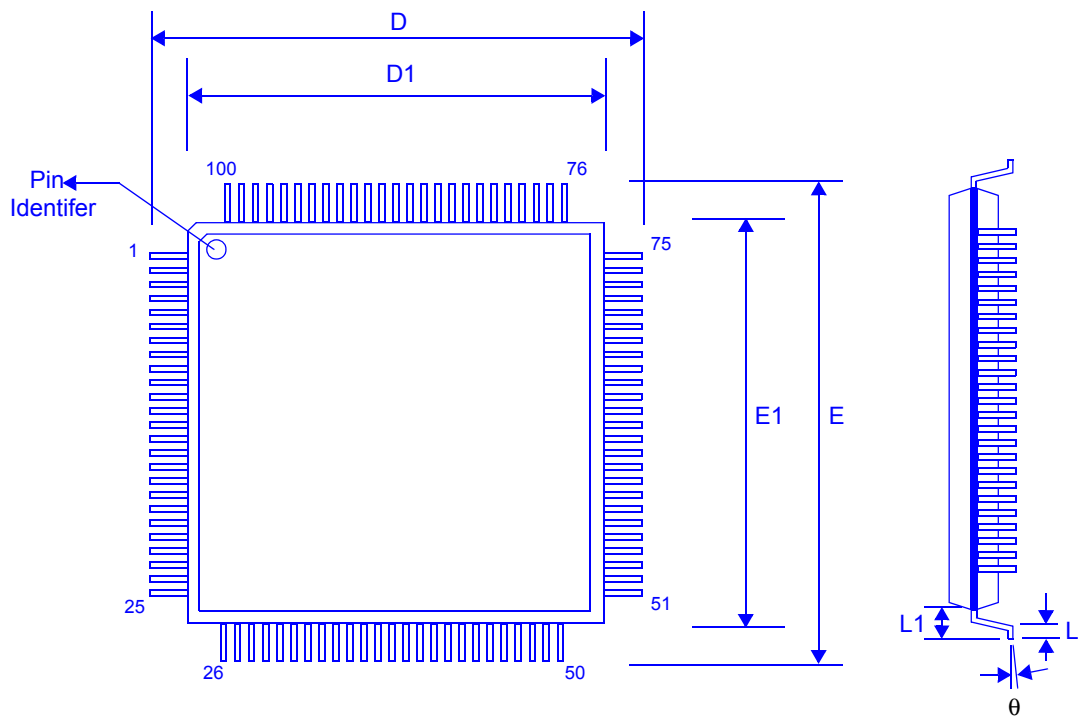


**Figure-8 Control Signals Transmitted During Blanking**

### Control Signals Transmitted During Blanking ( in DC Balanced Mode )

Control Signal	Signal Level	Channel	Pattern
DE	High Low	TXCLKOUT	1111000 or 1110000 1111100 or 1100000
HSYNC	High Low	TXOUT0	1100000 or 1111100 1110000 or 1111000
VSYNC	High Low	TXOUT1	1100000 or 1111100 1110000 or 1111000
CNTLF	High Low	TXOUT4	1100000 or 1111100 1110000 or 1111000
CNTLE	High Low	TXOUT5	1100000 or 1111100 1110000 or 1111000

**PACKAGE OUTLINE (100-pin LQFP)**



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

**Ordering Information**
**Part Number**

Prefix	Part Type	Package Type
CS	5830	G:LQFP