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N02M0818L2A

2Mb Ultra-Low Power Asynchronous Medical CMOS SRAM

256Kx8 bit

Overview

The N02M0818L2A is an integrated memory device intended for implanted life-support (Class 3) medical applications**.** This device comprises a 2 Mbit Static Random Access Memory organized as 262,144 words by 8 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology with reliability inhancements for medical users. The base design is the same as NanoAmp's N02M0818L1A, which is intended for non life-support (Class 1 and 2) medical applications. The device operates with two chip enable ($\overline{CE1}$ and CE2) controls and output enable ($\overline{OE}$) to allow for easy memory expansion. The N02M0818L2A is optimal for various applications where low-power is critical such as implanted pacemaker devices. The device can operate over a very wide temperature range of -20^{o}C to +60^{o}C and is available in die form as well as in JEDEC standard packages compatible with other standard 256Kb x 8 SRAMs

Features

- **Single Wide Power Supply Range**
  1.3 to 2.3 Volts
- **Very low standby current**
  200nA typical at 2.1V and 37 deg C
- **Very low operating current**
  1 mA at 2.0V and 1µs (Typical)
- **Very low Page Mode operating current**
  0.5mA at 1.0V and 1µs (Typical)
- **Simple memory control**
  Dual Chip Enables ($\overline{CE1}$ and CE2)
  Output Enable ($\overline{OE}$) for memory expansion
- **Low voltage data retention**
  Vcc = 1.0V
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**

Product Family

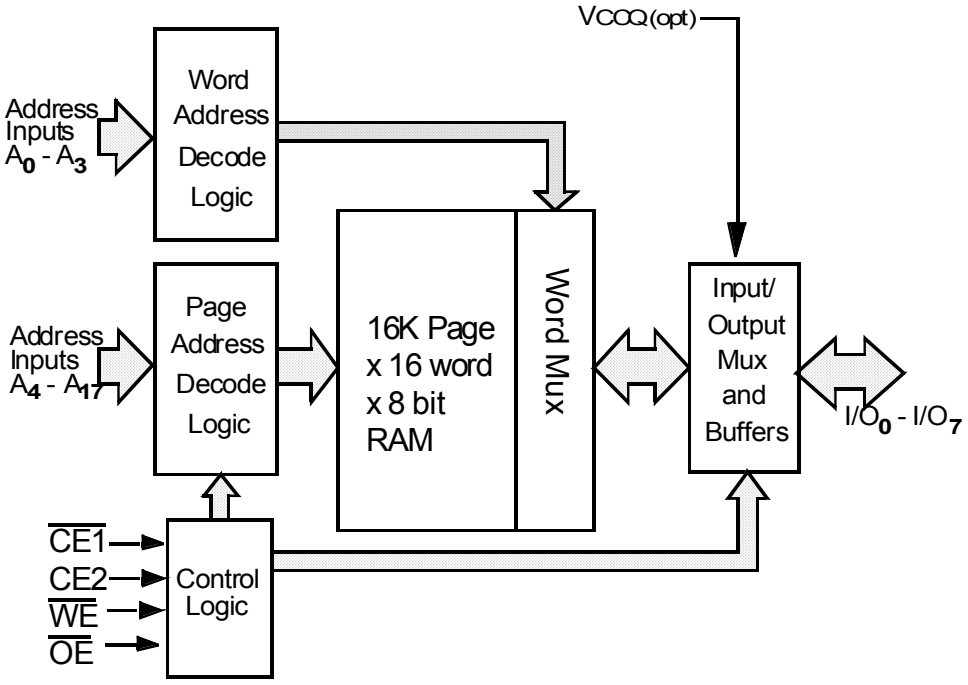
Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I_{SB})	Operating Current (Icc), Max
N02M0818L2AN	32 - STSOP I	-20^{o}C to +60^{o}C	1.3V - 2.3V	100ns @ 1.65V 500ns @ 1.3V	450nA @ 2.3V	2.5 mA @ 1MHz
N02M0818L2AD	Known Good Die					

Pin Configuration

Pin Descriptions

Pin Name	Pin Function
A_0-A_{17}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$, CE2	Chip Enable Input
$\overline{OE}$	Output Enable Input
I/O_0-I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	I/O_0 - I/O_7	MODE	POWER
H	X	X	X	High Z	Standby[1]	Standby
X	L	X	X	High Z	Standby[1]	Standby
L	H	L	X[2]	Data In	Write[2]	Active
L	H	H	L	Data Out	Read	Active
L	H	H	H	High Z	Active	Active

1. When the device is in standby mode, control inputs ($\overline{WE}$ and $\overline{OE}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
2. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 3.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-20 to +60	°C
Soldering Temperature and Time	T_{SOLDER}	240°C, 10sec(Lead only)	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Limits (Not all inclusive values tested)[1]

Item	Symbol	Test Conditions	Min.	Max	Unit
Core Supply Voltage	V_{CC}		1.3	2.3	V
Data Retention Voltage	V_{DR}	Chip Disabled (Note 3)	1.0		V
Input High Voltage	V_{IH}		$0.7V_{CCQ}$	V_{CCQ}+0.5	V
Input Low Voltage	V_{IL}		–0.5	$0.3V_{CCQ}$	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	V_{CCQ}–0.3		V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA		0.3	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		0.1	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled		0.1	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=2.3 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		2.5	mA
Read/Write Operating Supply Current @ 85 ns Cycle Time[2]	I_{CC2}	V_{CC}=2.3 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		13.0	mA
Standby Current[3]	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 37°C, V_{CC} = 2.3 V		450	nA
Data Retention Current[3]	I_{DR}	V_{CC} = 1.0V, V_{IN} = V_{CC} or 0 Chip Disabled, t_A= 85°C		1.0	µA

1. These limits are the expected operating conditions for this device. Only selected points within this range of conditions are specifically tested and guaranteed.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

3. The chip is Disabled when CE1# is high or CE2 is low or UB# and LB# are high. The chip is Enabled when CE1# is low and CE2 is high.

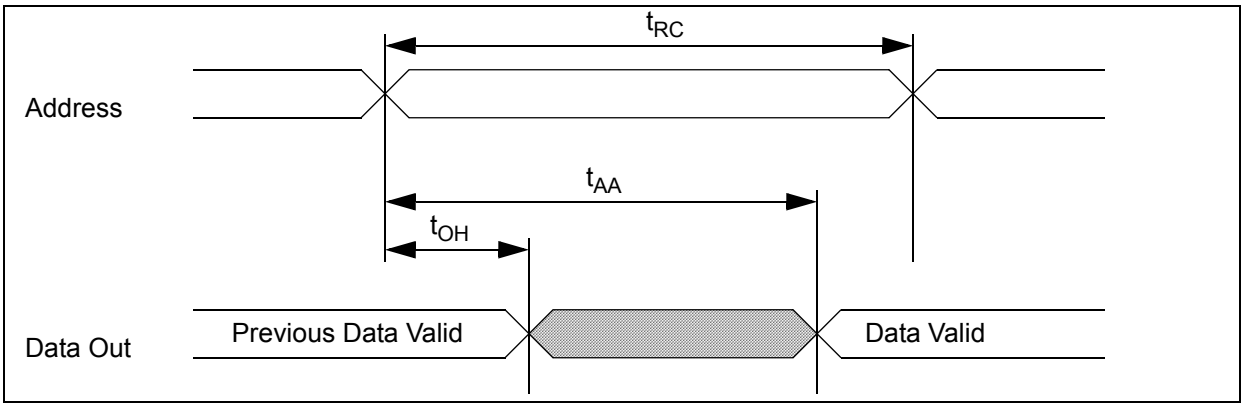
Recommended Timing Limits - Read Cycle (Not all inclusive values tested)

Item	Symbol	1.3 - 2.3 V		1.65 - 2.3 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	500		100		ns
Address Access Time	t_{AA}		500		100	ns
Chip Enable to Valid Output	t_{CO}		500		100	ns
Output Enable to Valid Output	t_{OE}		200		50	ns
Chip Enable to Low-Z output	t_{LZ}	100		20		ns
Output Enable to Low-Z Output	t_{OLZ}	50		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	150	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	150	0	30	ns
Output Hold from Address Change	t_{OH}	50		10		ns

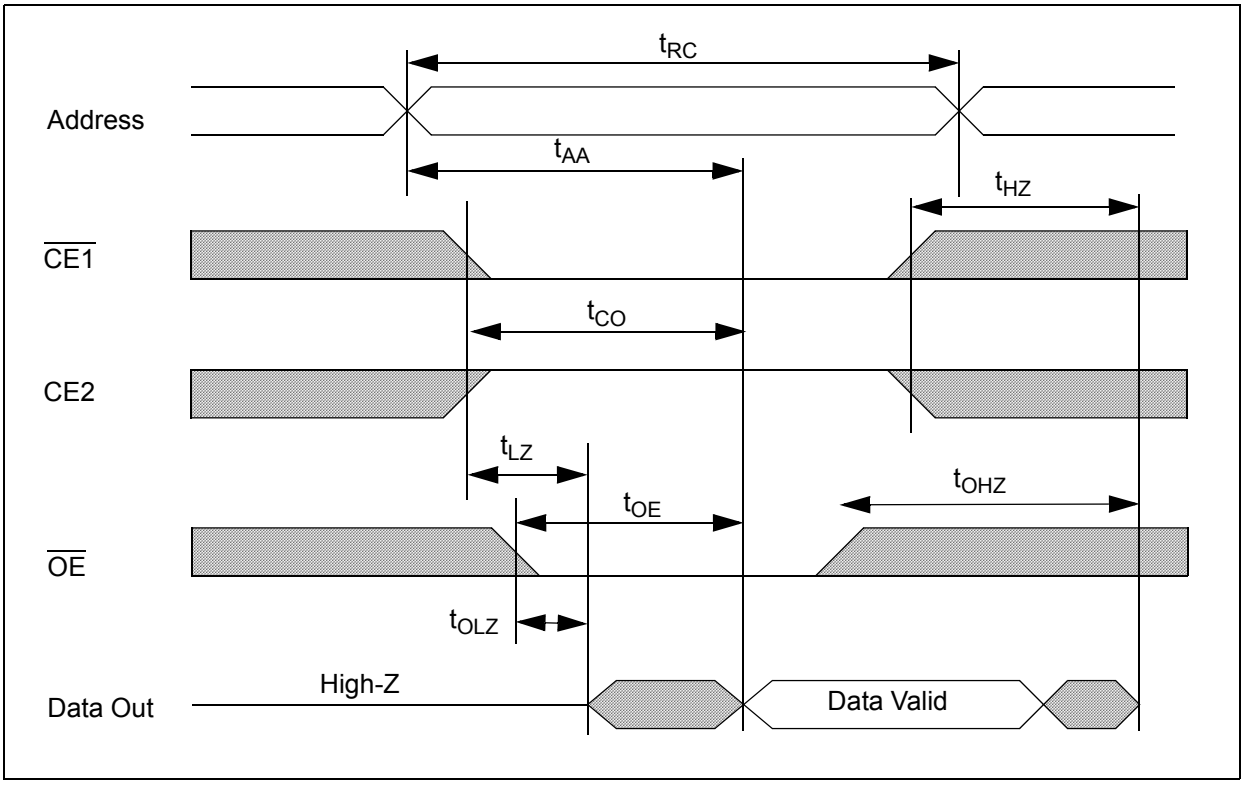
Recommended Timing Limits - Write Cycle (Not all inclusive values tested)

Item	Symbol	1.3 - 2.3 V		1.65 - 2.3 V		Units
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	500		85		ns
Chip Enable to End of Write	t_{CW}	400		50		ns
Address Valid to End of Write	t_{AW}	400		50		ns
Address Setup Time	t_{WP}	300		40		ns
Write Pulse Width	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		50		15	ns
Data to Write Time Overlap	t_{DW}	300		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	50		10		ns
Output Hold from Address Change	t_{OH}	0		0		ns

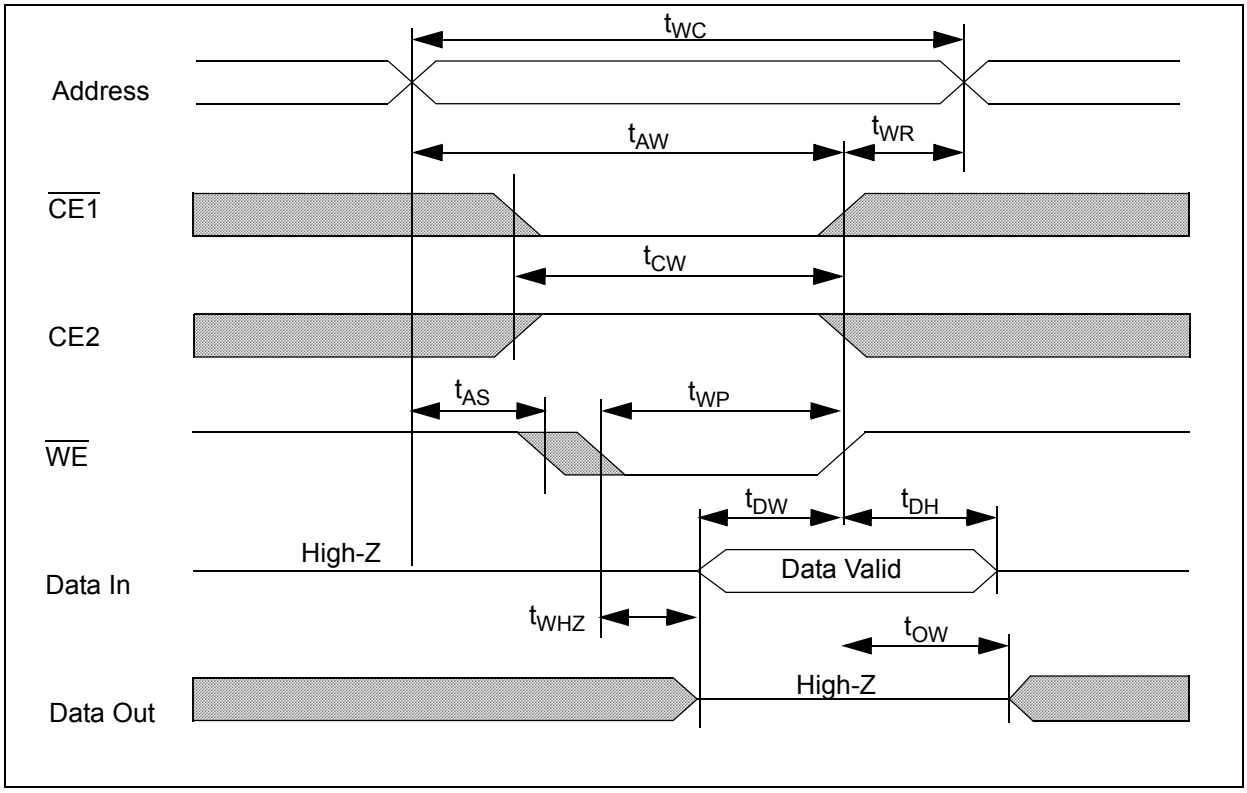
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



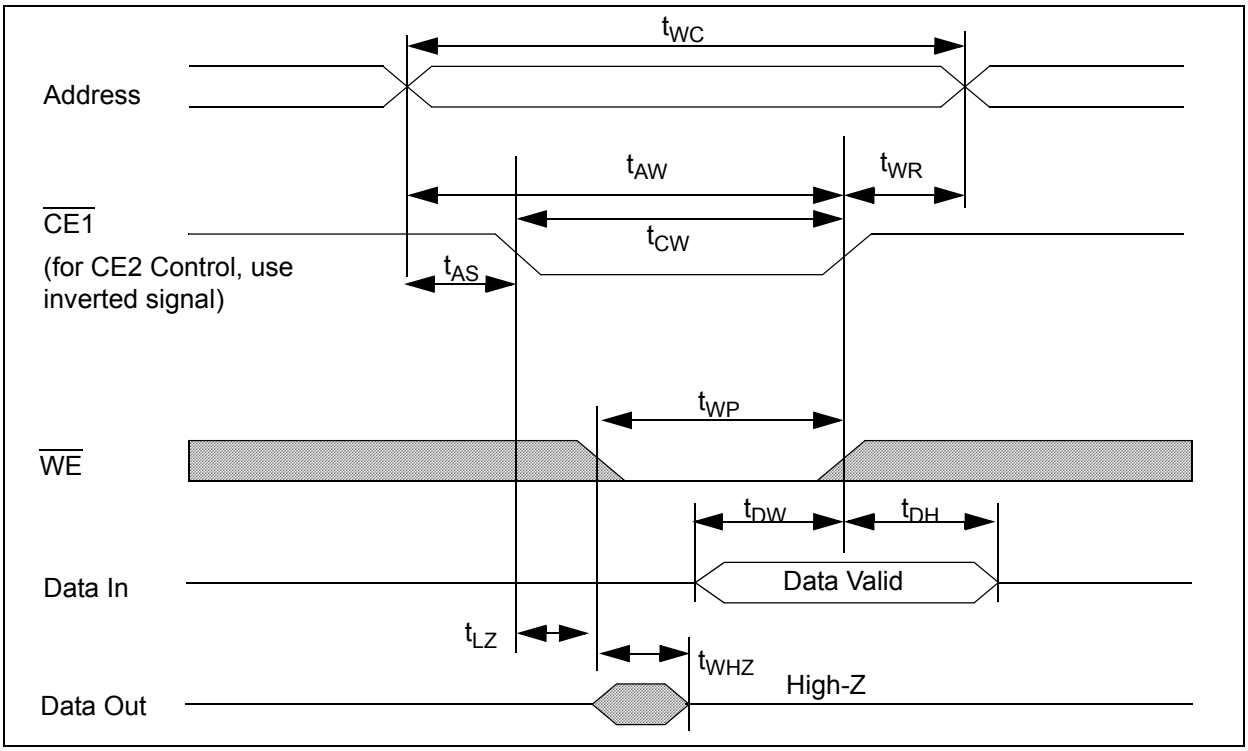
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



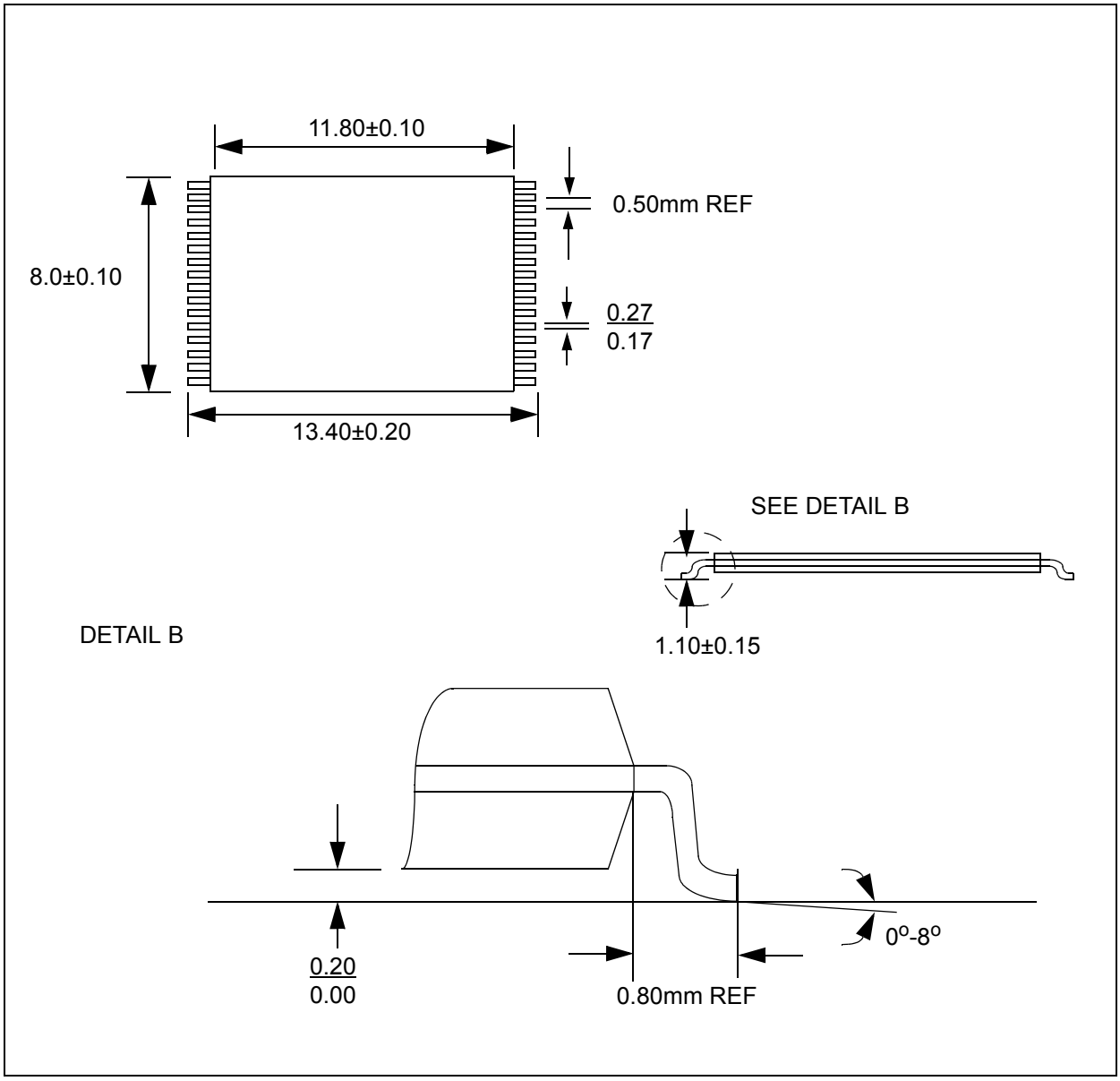
Timing Waveform of Write Cycle ($\overline{WE}$ control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)



32-Lead STSOP-I Package (N32)



Note:
1. All dimensions in millimeters
2. Package dimensions exclude molding flash

Ordering Information

N02M0818L2AX-XX X

- **Temperature**: 20°C to 60°C
- **Performance**: 100 = 100ns @ 1.65V
- **Package Type**: N = 32-pin STSOP I; D = Known Good Die

Revision History

Revision #	Date	Change Description
A	Dec 2002	Initial Release
B	January 2004	Updated with power characteristics
C	July 2004	General Update