

18Mb High Speed Synchronous Flow-Thru SRAMs with Fast bus Turn-around FTRAM™ Architecture

Features

- **High performance flow-thru operation**
- **Cycle times up to 133MHz**
Access times as fast as 6.5nS
- **Fully compatible with other bus latency-free SRAMs**
- **Fully synchronous operation**
- **Options for power supply**
3.3V +10% and -5% or
2.5V +/- 5%
- **Separate I/O power supply of 3.3V or 2.5V**
- **Individual byte write operation**
- **Three chip enable signals**
Simple depth expansion
- **ZZ mode for low power sleep mode**
- **Mode pin for setting interleave or linear burst mode of operation**
- **JTAG Boundary Scan (BGA only)**
- **JEDEC standard 100-pin TQFP, 165-ball FPBGA and 119-ball PBGA packages**

Functional Description

The N18N3625F1B, N18N3633F1B, N18N1825F1B and N18N1833F1B are 18Mb high performance synchronous SRAMs that are part of a family of devices for those demanding high performance. The FTRAM family of devices is designed to operate without the need of NOP or deselect clock cycles when transitioning from read to write cycles and thereby allowing the use of all available bandwidth. These high-speed devices are fully compatible with other no bus turn-around SRAMs such as NoBL™, ZBT™ and NtRAM™ devices.

The memory devices contain 18Mb of memory cells organized as 524,288 x 36 (N18N3625F1B, N18N3633F1B) and 1,048,576 x 18 (N18N1825F1B, N18N1833F1B). The devices operate in a synchronous manner with control signals, addresses and data inputs synchronized and captured at the rising edge of clock for ease of use. An asynchronous OE is available for disabling the outputs at any time. An asynchronous ZZ signal can be used to put the device into sleep mode with all data retained. The devices are fabricated using

NanoAmp's advanced CMOS process and high-speed/ultra low-power circuit technology. The N18N3625F1B, N18N3633F1B, N18N1825F1B and N18N1833F1B are ideal for networking and communication systems where high-density, high-performance memory elements are required. The architecture allows the data bus to be fully utilized when moving data into and out of the SRAM.

Flow-Thru Performance and Power

	SORT (MHz)			Unit
	100	117	133	
t _{CYCLE}	10.0	8.5	7.5	nS
t _{ACCESS}	8.5	7.5	6.5	nS
I _{CC}	175	190	210	mA
I _{SB}	70	70	70	mA

Options

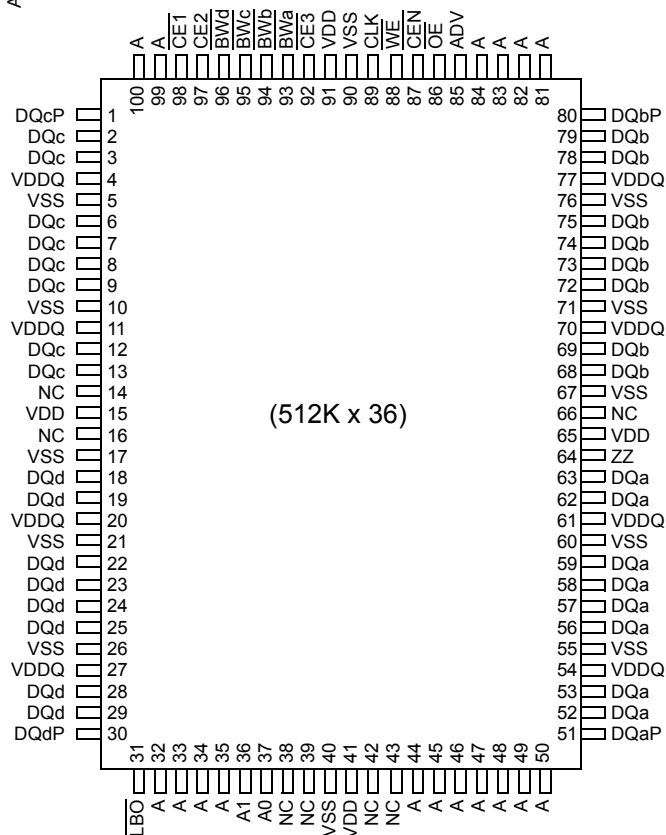
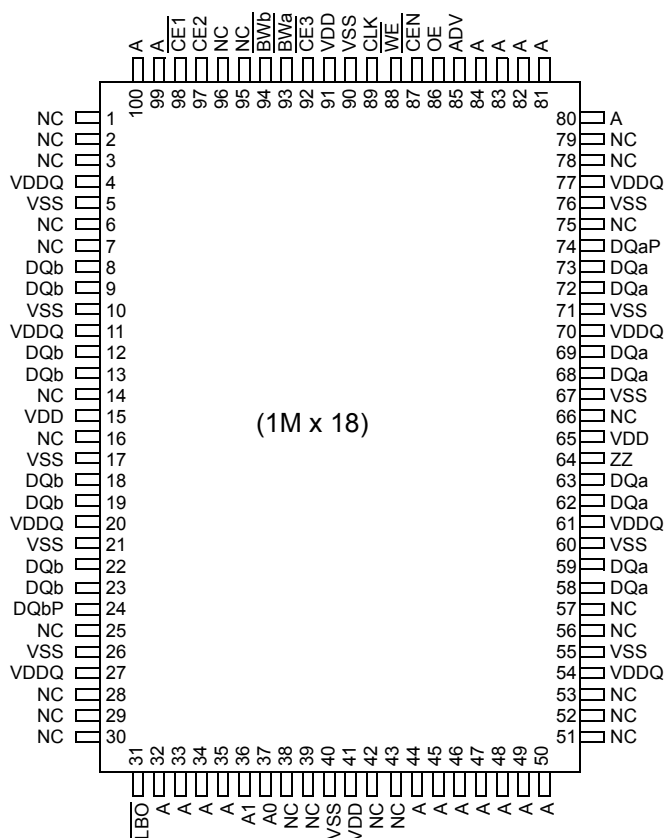
- **Organization**
512Kb x 36 N18N36
1Mb x 18 N18N18
- **Power supply**
3.3V w/ V_{DDQ} = 3.3/2.5V 33
2.5V w/ V_{DDQ} = 2.5V 25
- **Operating Mode**
Flow-Thru F1
- **Package**
100-pin TQFP Q
119-ball PBGA G
165-ball FPBGA F
- **Speed**
10MHz 10
117MHz 11
133MHz 13

Part number example:
N18N3625F1BQ-11C

FTRAM is a trademark of NanoAmp Solutions, Inc.
NoBL is a trademark of Cypress Semiconductor Corporation
ZBT is a trademark of Integrated Device Technology
NtRAM is a trademark of Samsung Electronics Corporation

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100-Pin TQFP Packages



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119-Ball PBGA Packages

1Mb x 18

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CE2	A	ADV	A	$\overline{\text{CE3}}$	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQaP	NC
E	NC	DQb	VSS	$\overline{\text{CE1}}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{\text{BWb}}$	A	VSS	NC	DQa
H	DQb	NC	VSS	$\overline{\text{WE}}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	$\overline{\text{BWa}}$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{\text{CKE}}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A1	VSS	DQa	NC
P	NC	DQbP	VSS	A0	VSS	NC	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

512Kb x 36

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CE2	A	ADV	A	$\overline{\text{CE3}}$	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQcP	VSS	NC	VSS	DQbP	DQb
E	DQc	DQc	VSS	$\overline{\text{CE1}}$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{\text{OE}}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{\text{BWc}}$	A	$\overline{\text{BWb}}$	DQb	DQb
H	DQc	DQc	VSS	$\overline{\text{WE}}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{\text{BWd}}$	NC	$\overline{\text{BWa}}$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{\text{CKE}}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A1	VSS	DQa	DQa
P	DQd	DQdP	VSS	A0	VSS	DQaP	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

7 x 17 Ball BGA with 1.27 mm Ball Pitch

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165-Ball FPBGA Packages

1M x 18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CE1}}$	$\overline{\text{BWb}}$	NC	$\overline{\text{CE3}}$	$\overline{\text{CKE}}$	ADV	A	A	A
B	NC	A	CE2	NC	$\overline{\text{BWa}}$	CLK	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQaP
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQbP	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC
R	$\overline{\text{LBO}}$	NC	A	A	TMS	A0	TCK	A	A	A	A

512K x 36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CE1}}$	$\overline{\text{BWc}}$	$\overline{\text{BWb}}$	$\overline{\text{CE3}}$	$\overline{\text{CKE}}$	ADV	A	A	NC
B	NC	A	CE2	$\overline{\text{BWd}}$	$\overline{\text{BWa}}$	CLK	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A	A	NC
C	DQcP	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQbP
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQdP	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQaP
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC
R	$\overline{\text{LBO}}$	NC	A	A	TMS	A0	TCK	A	A	A	A

11 x 15 Ball BGA with 1.0 mm Ball Pitch

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Pin Descriptions

Signal	Type	POWER
A0, A1	Synch Input	Address inputs sampled at the rising edge of CLK. Least significant address bits are used to set the internal burst counter (if used).
Ax	Synch Input	Address inputs 2 through 18/19, sampled at the rising edge of CLK.
$\overline{\text{LBO}}$	Synch Input	Linear burst order, active low, used for setting the address order of the burst counter. A low selects linear burst order while a high selects interleave burst order and if floating, this input will default to a high (interleave order) This should not be changed while operating the SRAM.
ADV	Synch Input	Advance/load, sampled at the rising edge of clock. When high, the internal burst counter is advanced for the next address and when low, a new address is loaded from the address pins.
$\overline{\text{BWA}}$ $\overline{\text{BWB}}$ $\overline{\text{BWC}}$ $\overline{\text{BWD}}$	Synch Input	Byte writes, active low, sampled at the rising edge of CLK if $\overline{\text{WE}}$ is low for a write cycle. $\overline{\text{BWA}}$ controls byte a (DQa) inputs, $\overline{\text{BWB}}$ controls byte b (DQb) inputs, $\overline{\text{BWC}}$ controls byte c (DQc) inputs and $\overline{\text{BWD}}$ controls byte d (DQd) inputs. For x18 devices, only $\overline{\text{BWA}}$ and $\overline{\text{BWB}}$ apply.
$\overline{\text{WE}}$	Synch Input	Write enable, active low, sampled at the rising edge of CLK. A low state initiates a write cycle.
CLK	Clock Input	Clock
CE1	Synch Input	Chip enable 1, active low, sampled on the rising edge of CLK. Used with CE2 and CE3 and to select the device.
CE2	Synch Input	Chip enable 2, active high, sampled on the rising edge of CLK. Used with CE1 and CE3 and to select the device.
CE3	Synch Input	Chip enable 3, active low, sampled on the rising edge of CLK. Used with CE2 and CE1 and to select the device.
$\overline{\text{CKE}}$	Synch Input	Clock enable, active low and while low, allows CLK to be recognized by the SRAM. While high, CKE inhibits CLK from driving SRAM cycles and extends cycles already in progress.
OE	Asynch Input	Output enable, asynchronous active low, tri-states the output buffers when high and enables the output buffers when low.
ZZ	Asynch Input	Sleep mode, asynchronous active high, puts the device in a low power sleep mode that retains all data while high.
DQa DQb DQc DQd	Synch Input/ Output	During a write cycle, the data lines are synchronous inputs that are sampled at the rising edge of CLK to specify data to be written to the memory array. During a read cycle, the data lines are driven out with data from the SRAM array. DQ(a, b, c, d) refer to the bytes a, b, c, d. For x18 devices, only DQa and DQb apply.
VDD	Power Supply	Supplies power to the device core.
VDDQ	I/O Power Supply	Supplies power to the I/O section of the device.
VSS	Ground supply	Ground
TMS	Input	Test Mode Select supplies input command to the TAP controller with TCK.
TDI	Input	Test Data Input supplies serial input to test registers.
TDO	Output	Test Data Output supplies serial data out from test registers.
TCK	Input	Test Clock controls TAP controller and serial data in and data out.
NC	-	No connect

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Functional Truth Table ^{1,7}

Operation	Address	$\overline{CE1}$	CE2	$\overline{CE3}$	ADV	\overline{WE}	\overline{BWx}^2	\overline{OE}	ZZ	\overline{CKE}^8	CLK ³	DQ ⁹	Notes
DESELECT	NA	H	X	X	L	X	X	X	L	L	L-H	High-Z	
DESELECT	NA	X	L	X	L	X	X	X	L	L	L-H	High-Z	
DESELECT	NA	X	X	H	L	X	X	X	L	L	L-H	High-Z	
Continue DESELECT	NA	X	X	X	H	X	X	X	L	L	L-H	High-Z	4
READ, begin burst	Ext	L	H	L	L	H	X	L	L	L	L-H	Data-out	
READ, continue burst	Int	X	X	X	H	X	X	L	L	L	L-H	Data-out	4,10
DUMMY READ, begin burst	Ext	L	H	L	L	H	X	H	L	L	L-H	High-Z	5
DUMMY READ, continue burst	Int	X	X	X	H	X	X	H	L	L	L-H	High-Z	4,5,10
WRITE, begin burst	Ext	L	H	L	L	L	L	X	L	L	L-H	Data-in	
WRITE, continue burst	Int	X	X	X	H	X	L	X	L	L	L-H	Data-in	4,10
WRITE ABORT, begin burst	Ext	L	H	L	L	L	H	X	L	L	L-H	High-Z	5
IGNORE CLOCK	Current	X	X	X	X	X	X	X	L	H	L-H	-	6,8
Deep Sleep	NA	X	X	X	X	X	X	X	H	X	X	High-Z	

Notes:

1. X = don't care; H = logic HIGH; L = logic LOW.
2. BWx = H means all BW signals are high; BWx = L means one or more BW signals are low.
3. L-H refers to the CLK edge transitioning from a low to a high state.
4. All continue burst cycles use the same control inputs. The type of cycle is chosen in the first cycle prior to the continue cycle.
5. Dummy read and write abort commands perform no external operation, they are NOP cycles.
6. If an ignore clock (\overline{CKE} high) cycle happens during a read, the DQ bus will remain active. If this happens during a write, the DQ bus will remain High-Z, no write occurs.
7. All inputs except \overline{OE} must meet set-up and hold times.
8. Wait states are inserted by setting \overline{CKE} high.
9. All outputs will remain in high-Z during power-up.
10. A 2-bit burst counter is included which is incremented for all continue burst cycles. The address wraps around every fourth burst cycle.

Write Truth Table ^{1,2}

Function	\overline{WE}	\overline{BWa}	\overline{BWb}	\overline{BWc}	\overline{Bwd}
READ	H	X	X	X	X
WRITE byte a ³	L	L	H	H	H
WRITE byte b ³	L	H	L	H	H
WRITE byte c ³	L	H	H	L	H
WRITE byte d ³	L	H	H	H	L
WRITE all byte	L	L	L	L	L
WRITE ABORT	L	H	H	H	H

Notes:

1. This represents the x36 device. For the x18 device, only \overline{BWa} and \overline{BWb} are used.
2. X = don't care; H = logic HIGH; L = logic LOW.
3. Multiple bytes may be exercised during a cycle.

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Burst Order Tables

Interleave	Starting digits		Starting digits		Starting digits		Starting digits	
$\overline{\text{LBO}} = \text{High}$	A1	A0	A1	A0	A1	A0	A1	A0
First address	0	0	0	1	1	0	1	1
Second address	0	1	0	0	1	1	1	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	1	0	0	1	0	0

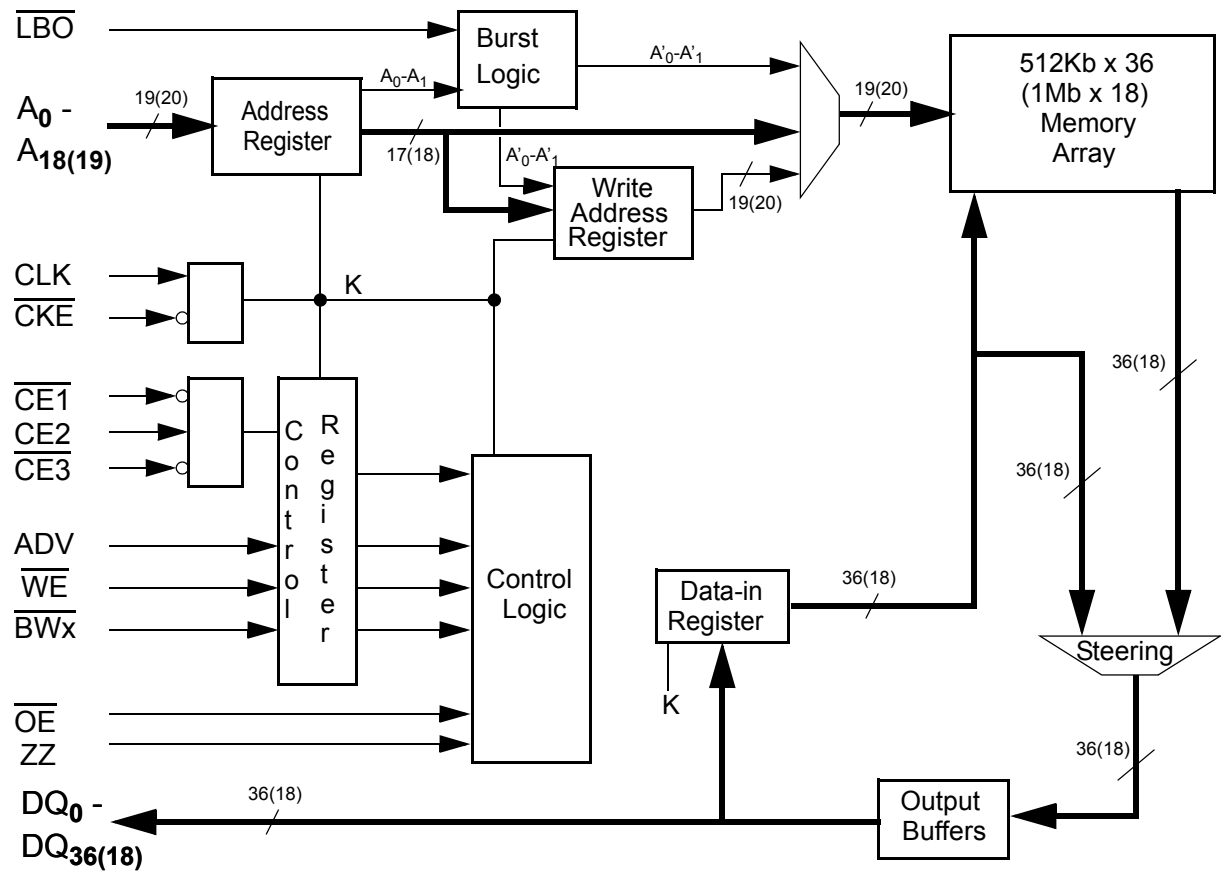
Linear	Starting digits		Starting digits		Starting digits		Starting digits	
$\overline{\text{LBO}} = \text{Low}$	A1	A0	A1	A0	A1	A0	A1	A0
First address	0	0	0	1	1	0	1	1
Second address	0	1	1	0	1	1	0	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	0	0	0	1	1	0

Note:

At the end of a burst of four, the burst counter wraps to the starting address and continues.

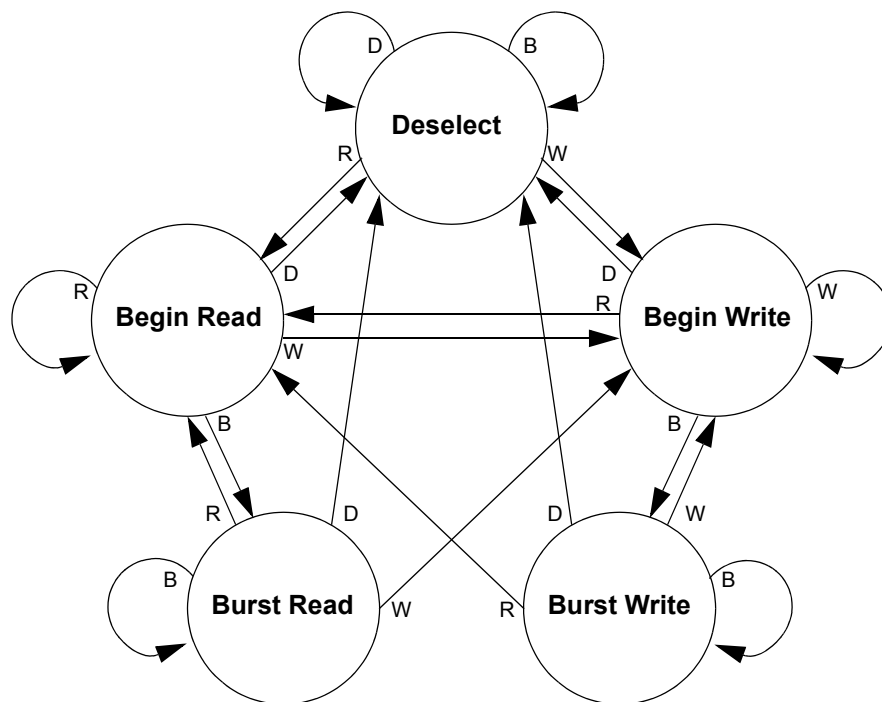
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Functional Block Diagram



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Read and Write State Diagram



Key:

State diagram shows current state and transitions to possible next states.

D = Deselect

R = Read

W = Write

B = Burst (read, write or deselect)

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Functional Operation

The N18N1825F1B, N18N1833F1B, N18N3625F1B and N18N3633F1B are developed for the high performance needs of the networking and communications markets. Devices are available for both pipeline and flow-through modes of operation depending on the particular system needs. All inputs except OE, LBO and ZZ are synchronized and registered by the rising edges of the clock (CLK). Three chip enables are available for depth expansion with CE1 and CE3 being active low and CE2 active high. For a cycle to start, all three must be active and any one inactive will deselect the device. Read operations are started with CKE, CE1, CE3 and ADV being asserted low at the rising edge of CLK along with WE and CE2 being asserted high. Write operations are started with CKE, CE1, CE3, ADV and WE being asserted low at the rising edge of CLK along with CE2 being asserted high. The byte write enable (BWx) inputs are used to determine which bytes (or all bytes) will be written to. The address inputs are latched and used as the location in memory to start a memory cycle. Clock enable input (CKE) allows operations to be stalled or suspended while CKE is inactive high. In this operation, all internal registers retain data from the previous operation. Output enable (OE), linear burst mode (LBO) and sleep mode (ZZ) are asynchronous signals that control other aspects of the device. OE is used to disable the output buffers at any time. LBO is either tied high for interleave burst order or low for linear burst order. ZZ is used to put the device in a low power sleep mode, while all data is retained in the SRAM memory array.

Burst Operation

The previous operations discussed were initiated with ADV being asserted low, thereby activating a cycle with a new external address being loaded and used for array operations. If ADV is asserted high at the rising edge of CLK, the internal burst counter is incremented and an internal address is used to access the SRAM array. The burst counter is a four bit counter and can be incremented in two orders, interleave and linear. The burst counter wraps around after four addresses and continues to operate as long as ADV is high and valid CLK cycles are performed.

Flow-Thru Operation

For a read cycle, all the necessary control signals must be setup at the rising edge of CLK as stated

above. The memory array is then accessed. During this first cycle, data is driven out of (or flows thru) the SRAM in the same cycle as the activation instead of waiting until the next rising edge of CLK (as in a pipeline device).

For a write cycle, all the necessary control signals must be setup at the rising edge of CLK as stated above. The BWx must be setup active low for whichever bytes will be written too at this first rising edge of CLK. The data to be written to the SRAM is not registered until the second rising edge of CLK. This is called a late write cycle as data is not necessary until the second cycle while address and write command information is required at the first cycle.

Flow-thru reads and writes can be performed in single access (ADV = L) cycles or burst (ADV = H) cycles.

Sleep Mode

Sleep mode is a low power mode that allows the device to continue to retain data in a power down mode. ZZ is asserted high to enter sleep mode and after two clock cycles, the operating current will be reduced to I_{SL} . Since ZZ is an asynchronous operation, sleep mode should not be started until all operations are completed. ZZ should be asserted low for normal operation.

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Absolute Maximum Ratings

Symbol	Description		Value	Unit
V_{DD}	Voltage on any V_{DD} pin wrt Ground	3.3V Device	-0.5 to 4.6	V
		2.5V Device	-0.5 to 3.6	
V_{IN}^1	Voltage on any input pin		-0.5 to $V_{DDQ} + 0.5V$	V
V_{IO}^1	Voltage on any DQ pin		-0.5 to $V_{DDQ} + 0.5V$	V
T_{BIAS}	Temperature under bias		-55 to 125	°C
T_{STOR}	Storage temperature		-65 to 150	°C
I_{OUT}	Current into output circuit		20	mA
ESD	Static Discharge Voltage		> 2100	V
I_{Latch}	Latch-Up Current		> 200	mA

.1) Minimum voltage must not exceed -2V for pulse widths of < 20ns.

Pin Capacitance¹

Item	Symbol	Conditions	Max	Unit	
Input Capacitance	C_{in}	$T_a = 25^\circ C$, $V_{DD} = Typ$, $f = 1MHz$	tbd	pF	
Clock Capacitance	C_{clk}		tbd	pF	
Input/Output Capacitance	$C_{i/o}$		tbd	pF	

1) Not 100% tested.

Thermal Resistance¹

Item	Conditions	Theta JA Junction to Ambient	Theta JC Junction to Case	Unit
100-pin TQFP	Still air, soldered on a 2 layer board	31	6	°C/W
119-ball PBGA	Still air, soldered on a 4 layer board	45	7	°C/W
165-ball FPBGA		46	3	

1) Not 100% tested.

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Operating Conditions and DC Characteristics

Over the operating range. All voltages referenced to ground (V_{SS}).

3.3V Device¹

Item1		Conditions	Min	Typ ⁴	Max	Unit
Supply Voltage	V_{DD}		3.135	3.3	3.63	V
I/O Supply Voltage	V_{DDQ}		2.375	2.5	V_{DD}	V
Input High Voltage	V_{IH}	w/ 3.3V V_{DDQ}	2.0		$V_{DD} + 0.3$	V
		w/ 2.5V V_{DDQ}	1.7		$V_{DD} + 0.3$	
Input Low Voltage	V_{IL}	w/ 3.3V V_{DDQ}	-0.3		0.8	V
		w/ 2.5V V_{DDQ}	-0.3		0.7	
Output High Voltage ⁵	V_{OH}	w/ 3.3V V_{DDQ} , $I_{OH} = -4.0mA$	2.4			V
		w/ 2.5V V_{DDQ} , $I_{OH} = -1.0mA$	2.0			
Output Low Voltage ⁵	V_{OL}	w/ 3.3V V_{DDQ} , $I_{OL} = 8.0mA$			0.4	V
		w/ 2.5V V_{DDQ} , $I_{OL} = 1.0mA$			0.4	
Operating Current ^{2, 3}	I_{DD}	Device selected; All inputs < V_{IL} or > V_{IH} ; Frequency = $1/T_{cyc}$ (MIN); Outputs open	- 10		175	mA
			- 11		190	
			- 13		210	
Deselect Current - Standby (CMOS) ³	I_{SB1}	Device deselected; All inputs static and < 0.3V or > $V_{DDQ}-0.3$, Frequency = 0	All		70	mA
Device Current - Standby (TTL) ³	I_{SB2}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = 0	All		80	mA
Deselect Current - Clock running (CMOS) ³	I_{SB3}	Device deselected; All inputs < 0.3V or > $V_{DDQ}-0.3$; Frequency = $1/T_{cyc}$	- 10		95	mA
			- 11		100	
			- 13		105	
Deselect Current - Clock running (TTL) ³	I_{SB4}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = $1/T_{cyc}$	- 10		100	mA
			- 11		110	
			- 13		120	

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2.5V Device¹

Item		Conditions	Min	Typ ⁴	Max	Unit
Supply Voltage	V_{DD}		2.375	2.5	2.625	V
I/O Supply Voltage	V_{DDQ}		2.375	2.5	2.625	V
Input High Voltage	V_{IH}		1.7		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		-0.3		0.7	V
Output High Voltage ⁵	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.0			V
Output Low Voltage ⁵	V_{OL}	$I_{OL} = 1.0\text{mA}$			0.4	V
Operating Current ^{2,3}	I_{DD}	Device selected; All inputs < V_{IL} or > V_{IH} ; Frequency = $1/T_{cyc}$ (MIN); Outputs open	- 10		175	mA
			- 11		190	
			- 13		210	
Deselect Current - Standby (CMOS) ³	I_{SB1}	Device deselected; All inputs static and < 0.3V or > $V_{DDQ}-0.3$, Frequency = 0	All		70	mA
Device Current - Standby (TTL) ³	I_{SB2}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = 0	All		80	mA
Deselect Current - Clock running (CMOS) ³	I_{SB3}	Device deselected; All inputs < 0.3V or > $V_{DDQ}-0.3$; Frequency = $1/T_{cyc}$	- 10		95	mA
			- 11		100	
			- 13		105	
Deselect Current - Clock running (TTL) ³	I_{SB4}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = $1/T_{cyc}$	- 10		100	mA
			- 11		110	
			- 13		120	

1) Currents are specified for $V_{DD} = V_{DD} \text{ max}$.

2) Does not include output currents.

3) Device selected refers to a device in the active mode. Device deselected refers to a device as defined in the truth table.

4) Typical values measured at $V_{DD} \text{ TYP}$ and 25°C.

5) Output load B used.

Leakage Currents (both 3.3V and 2.5V devices)

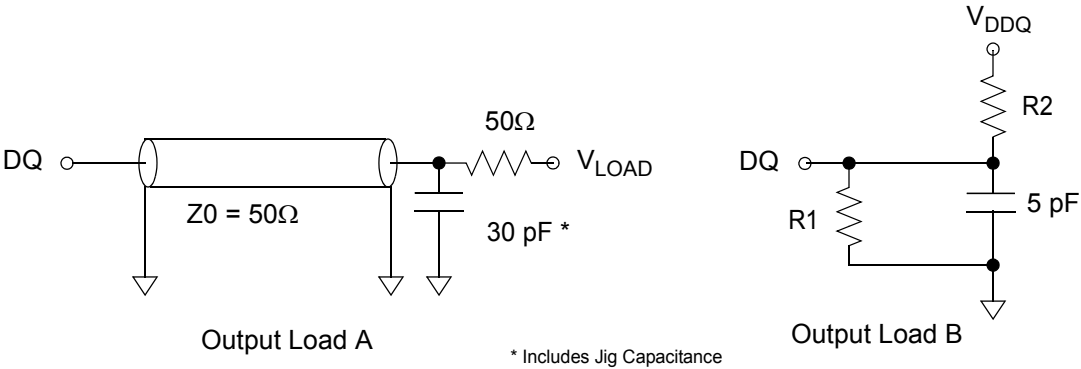
Item	Symbol	Conditions	Min	Max	Units	Notes
Input Leakage Current	I_{LI} ¹	$0V < V_{IN} < V_{DD}$	-5.0	5.0	μA	1
Input Leakage Current of LBO and ZZ pins			-30.0	30.0		
Output Leakage Current	I_{LO}	Outputs disabled $0V < V_{IN} < V_{DDQ}$	-5.0	5.0	μA	

1. LBO and ZZ inputs: $I_{LI} = \pm 30\mu\text{A}$ due to internal resistors for floating conditions.

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AC Test Conditions

Item	Value
Input Pulse Level	0V to Vcc
Input Rise and Fall Time	1.0V/nS (10% to 90%)
Input Timing Reference Level	V _{DD} /2
Output Timing Reference Level	V _{DDQ} /2
Output Load	See diagram below



AC Output Load

Component	Value		Unit
	3.3V VDDQ	2.5V VDDQ	
VLOAD	1.5	1.25	V
R1	351	1538	Ω
R2	317	1667	Ω

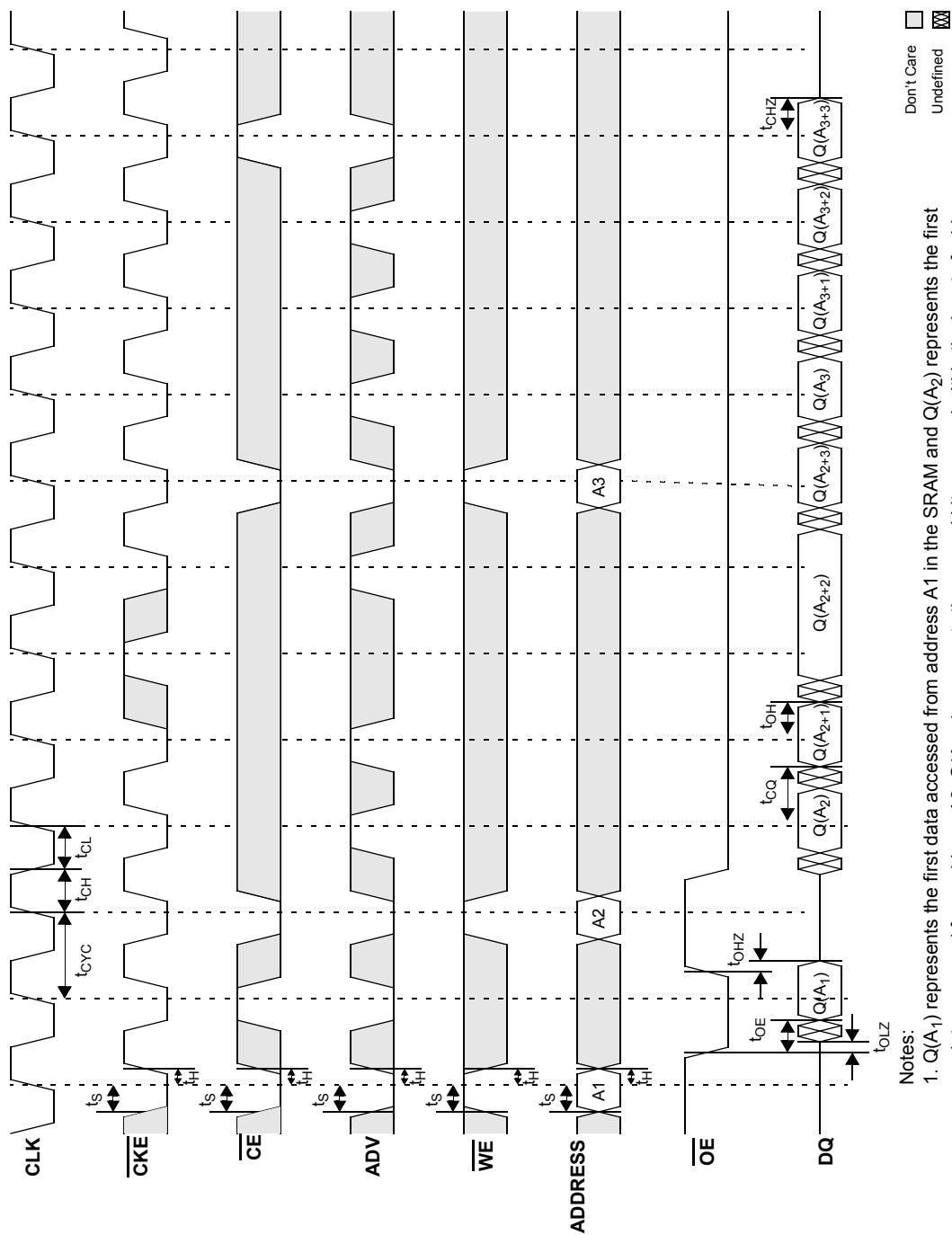
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AC Timing Characteristics

Parameter	Symbol	-13		-11		-10		Unit
		Min	Max	Min	Max	Min	Max	
CLOCK TIMINGS								
Clock Cycle Time	t _{CYC}	7.5		8.5		10.0		nS
Clock High Pulse Width	t _{CH}	2.1		2.3		2.5		nS
Clock Low Pulse Width	t _{CL}	2.1		2.3		2.5		nS
Clock Frequency	F _{MAX}		133		117		100	MHz
OUTPUT TIMINGS								
Clock high to output valid	t _{CQ}		6.5		7.5		8.5	nS
Output hold from clock high	t _{OH}	2.0		2.0		2.0		nS
Clock to output in low-Z ¹	t _{CLZ}	2.0		2.0		2.0		nS
Clock to output in high-Z ¹	t _{CHZ}		4.0		4.0		5.0	nS
OE low to output valid	t _{toE}		3.2		3.4		3.8	nS
OE low to output in low-Z ¹	t _{OLZ}	0		0		0		nS
OE high to output in high-Z ¹	t _{OHZ}		4.0		4.0		5.0	nS
SETUP AND HOLD TIMES								
Setup Time	t _S	1.5		1.5		1.5		nS
Hold Time	t _H	0.5		0.5		0.5		nS

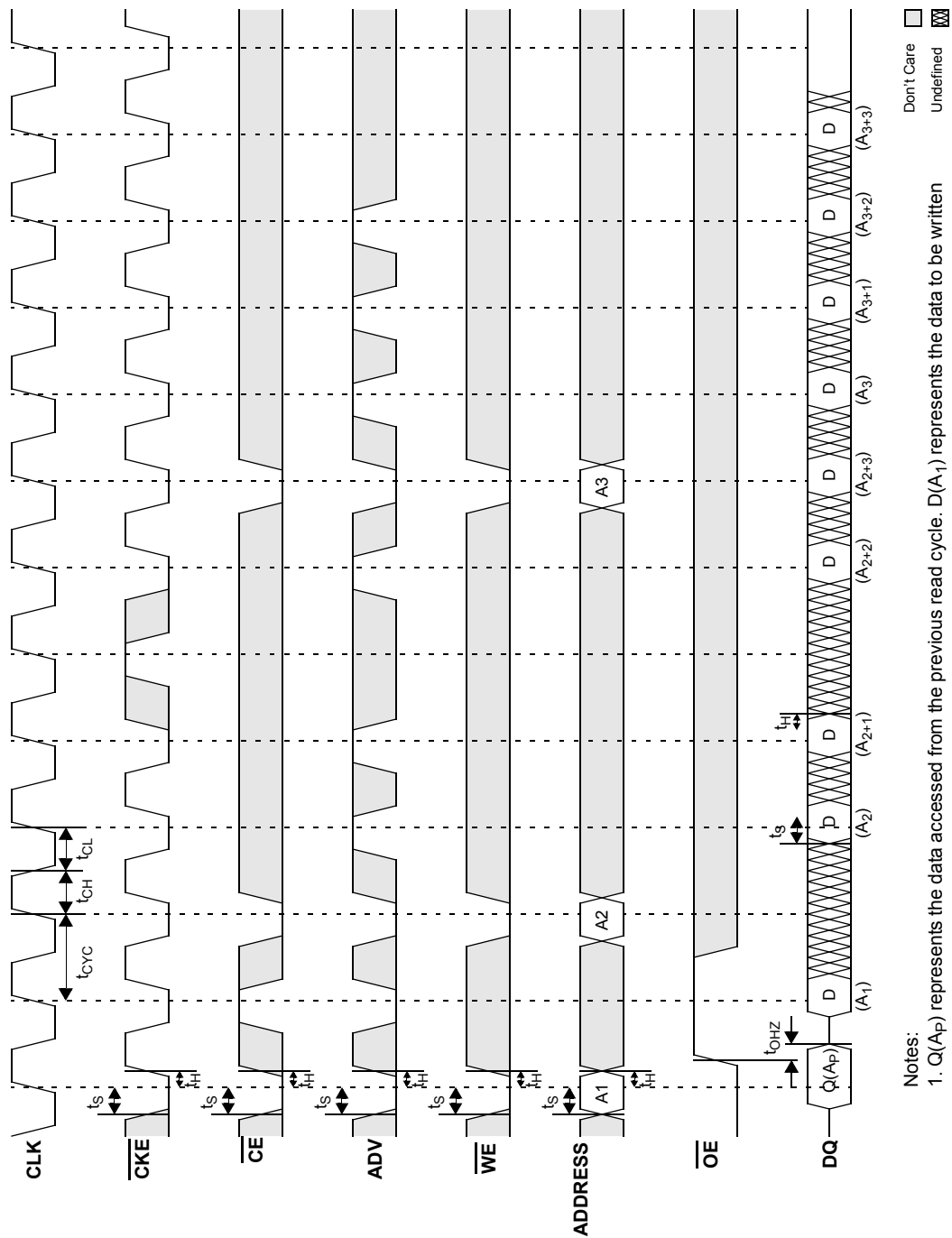
1) t_{CLZ} , t_{CHZ} , t_{OLZ} , t_{OHZ} are specified with output load B.

Timing Waveforms for READ Cycles



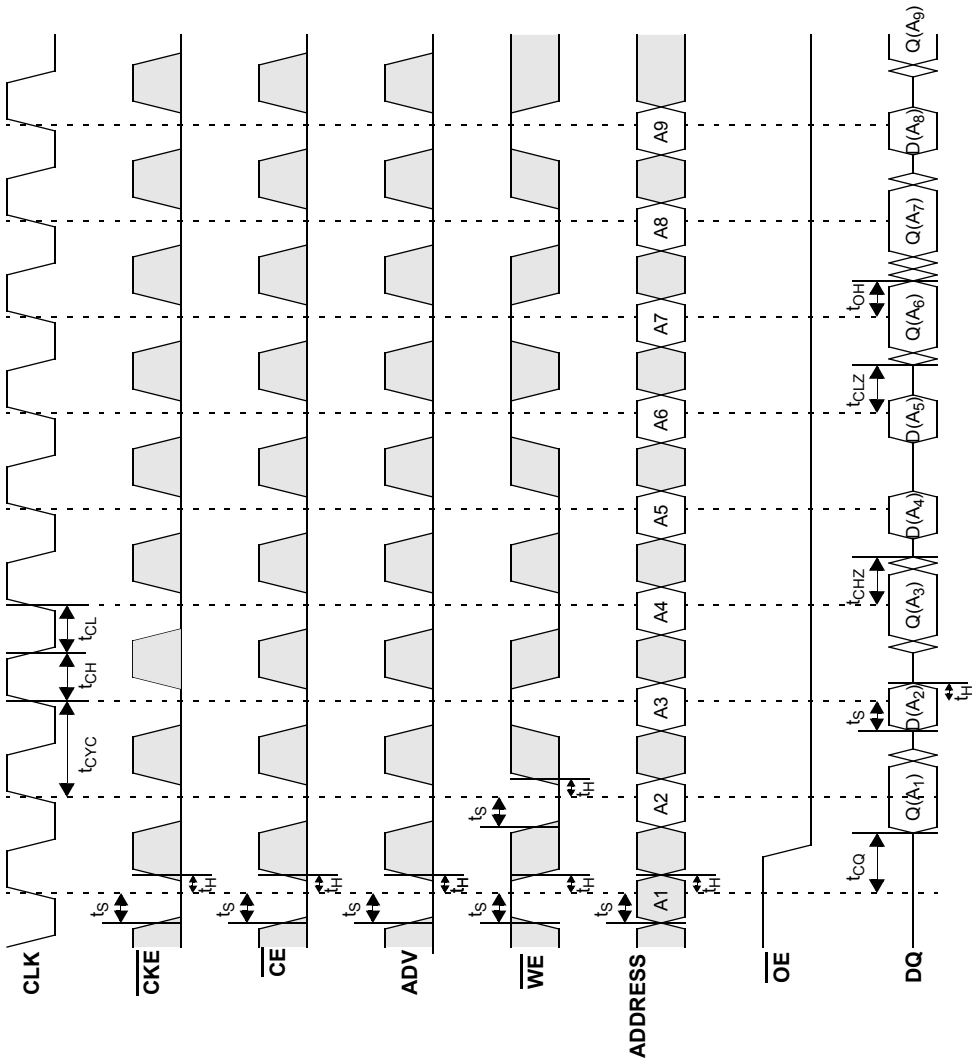
- Notes:
1. Q(A₁) represents the first data accessed from address A1 in the SRAM and Q(A₂) represents the first data accessed from address A2. Q(A₂₊₁) represents the second bit accessed within the burst of address A2.
 2. CE = L means CE1 = L and CE2 = H. CE = H means CE1 = H or CE2 = L or CE3 = H.

Timing Waveforms for WRITE Cycles



- Notes:
1. $Q(A_p)$ represents the data accessed from the previous read cycle. $D(A_1)$ represents the data to be written to address A1 in the SRAM and $D(A_2)$ represents the data to be written to address A2. $D(A_{2+1})$ represents the second bit to be written to address A2+1 during the burst.
 2. CE = L means CE1 = L and CE2 = H. CE = H means CE1 = H or CE2 = L or CE3 = H.

Timing Waveforms for Combined READ/WRITE Cycles



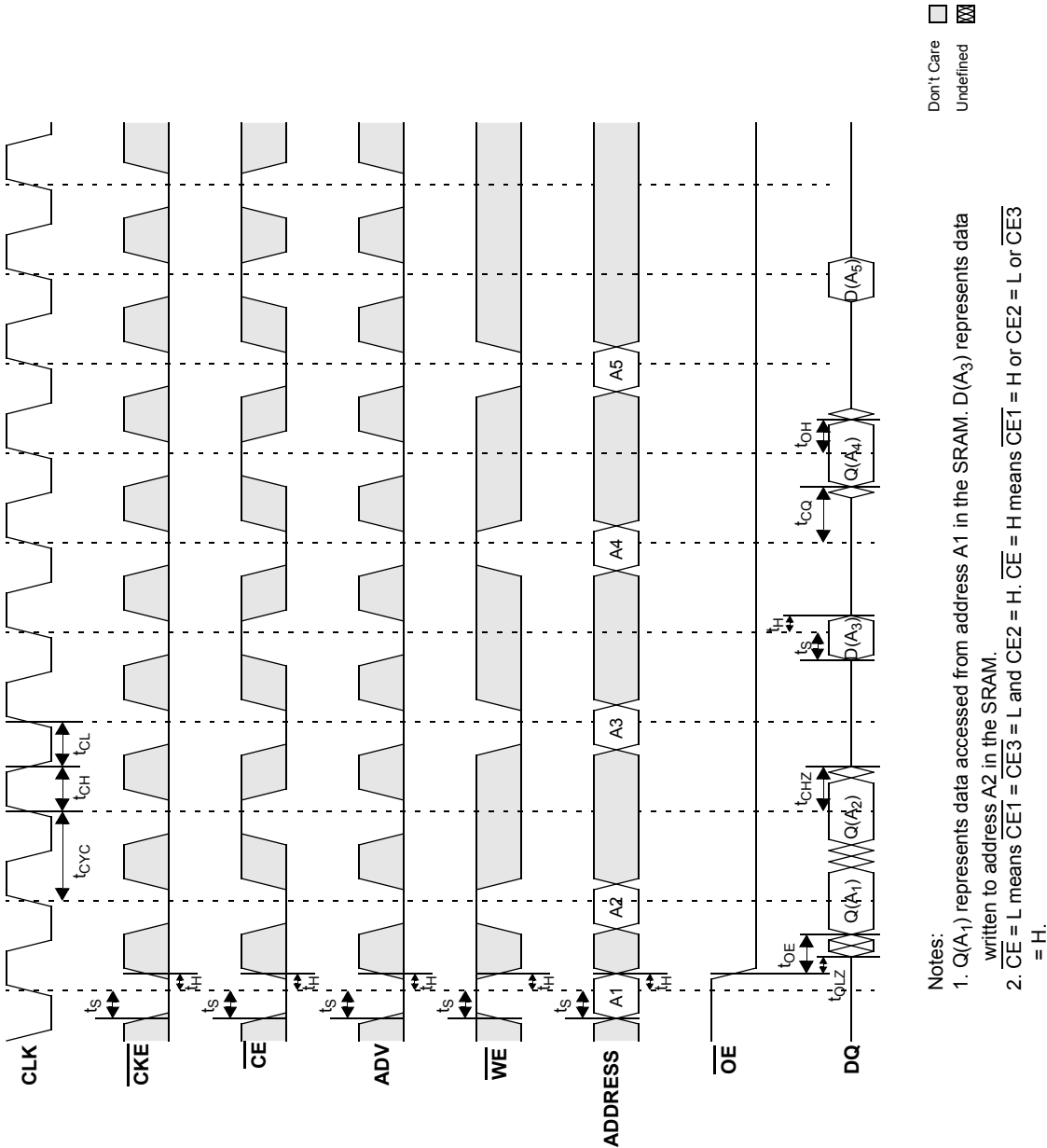
Don't Care
Undefined

- Notes:
1. Q(A₁) represents the data accessed from address A1 in the SRAM. D(A₂) represents data written to address A2 in the SRAM.

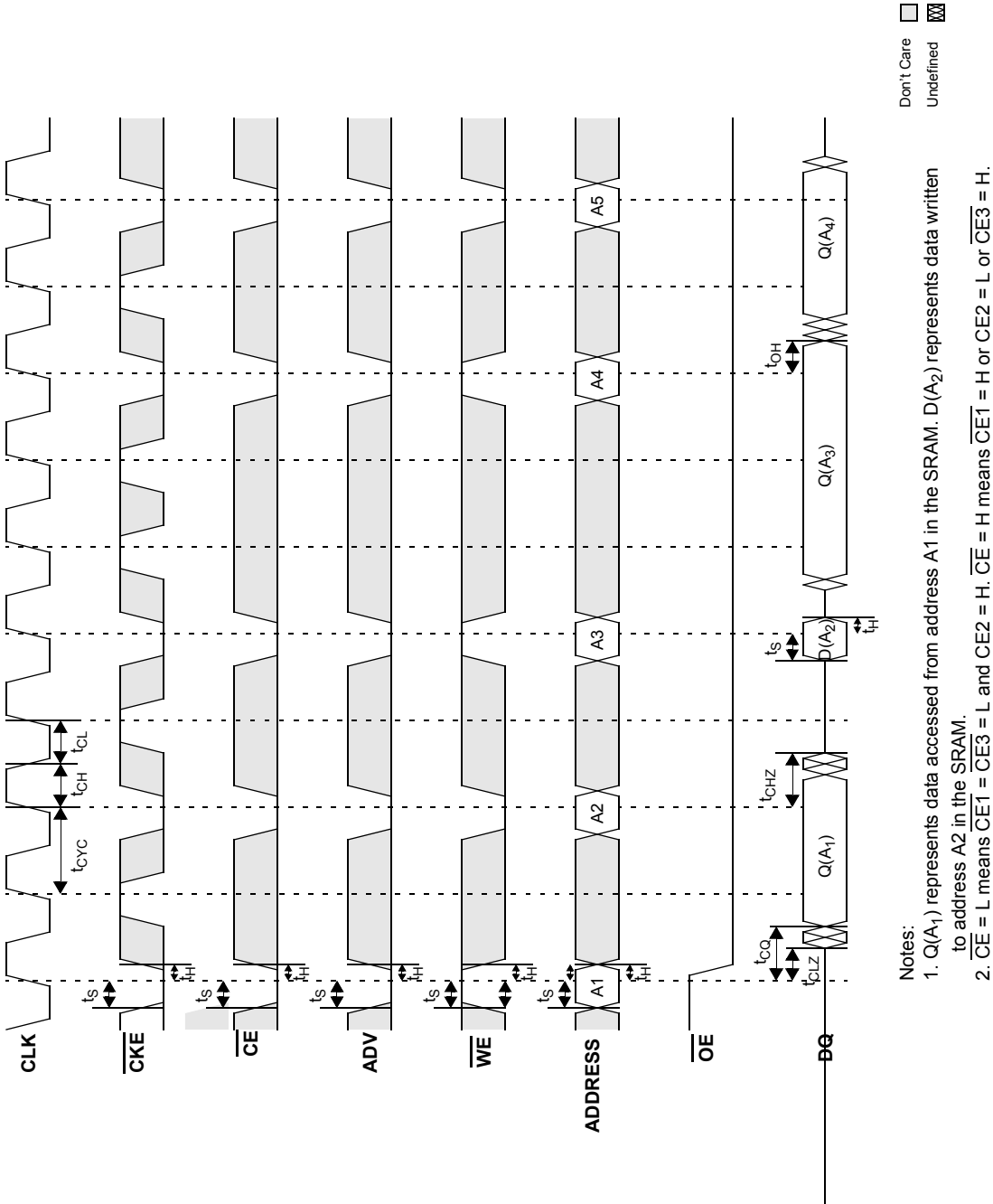
2. CE = L means CE1 = L and CE2 = H. CE = H means CE1 = H or CE2 = L or CE3 = H.

3. \overline{WE} = L means \overline{WE} and all \overline{BWx} are L.

Timing Waveforms for $\overline{\text{CE}}$ Operation

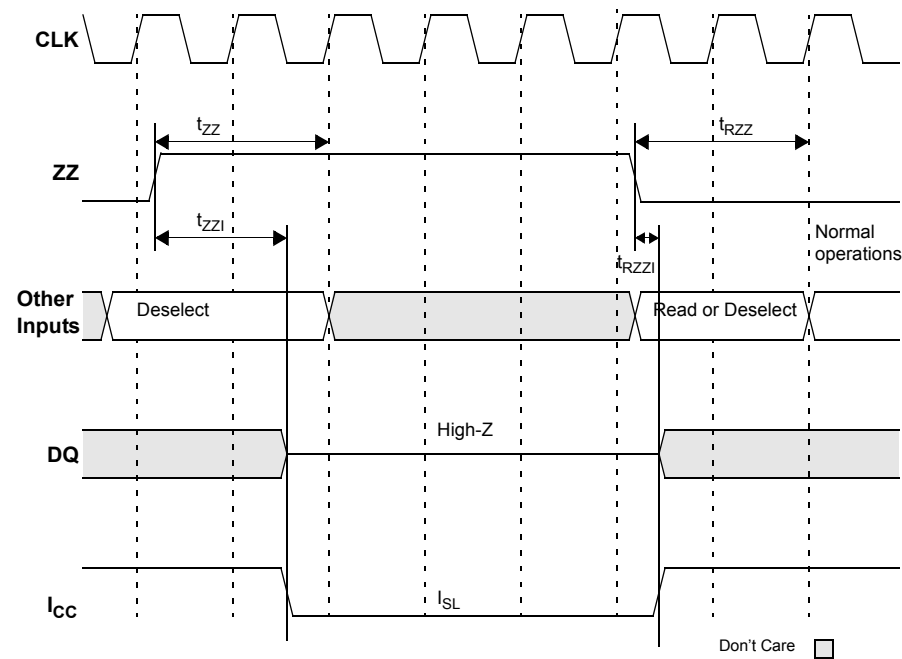


Timing Waveforms for $\overline{\text{CKE}}$ Operation



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Timing Waveforms Sleep Mode



Sleep Mode Characteristics

Item	Symbol	Conditions	Min	Max	Units	Notes
ZZ active to input ignored	t _{ZZ}	ZZ > V _{IH}		2	cycles	
ZZ inactive to input sampled	t _{RZZ}		2		cycles	
ZZ active to sleep current	t _{ZZI}			2	cycles	
ZZ inactive to exit sleep current	t _{RZZI}		2		cycles	
Sleep mode power supply current	I _{SL}			60	mA	

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JTAG Serial Boundary Scan

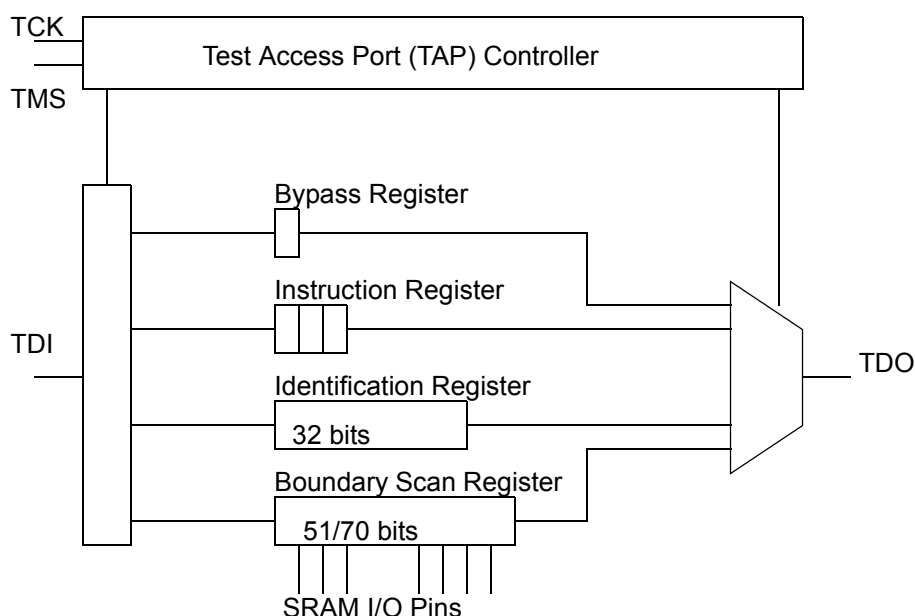
The N18N1825F1B, N18N1833F1B, N18N3625F1B and N18N3633F1B all incorporate JTAG serial boundary scan capability in the BGA packages only. This test function utilizes the test Access Port (TAP) to and operates consistent with IEEE Standard 1149.1-1900, but is not fully compliant since a subset of functions are omitted. The exclusion of these TAP controller functions does not conflict with other 1149.1 compliant devices. This test function allows connectivity scan testing during board level debug. This JTAG port operates using standard 2.5V I/O levels.

Disabling the JTAG Feature

There are no issues with using this SRAM and not using the JTAG feature. For normal operation with the TAP controller disabled, TCK must be tied low and TDI and TMS should be left floating or tied to Vdd. TDO should be left unconnected.

Performing a TAP Reset

Upon power-up, the TAP controller will be in a reset state and it will not interfere with the operation of the SRAM. A reset can be entered by holding TMS at a high level for five consecutive rising edges of TCK.



JTAG Block Diagram

TAP Pin Description

Signal	Name	Type	Description
TCK	Test Clock	Input clock	Clock for all TAP events. All inputs are captured on the rising edge of TCK. All outputs are driven with the falling edge of TCK.
TMS	Test Mode Select	Input	Input for commands to the TAP controller. Sampled on the rising edge of TCK.
TDI	Test Data-In	Input	Input for serial registers sampled on rising edge of TCK.
TDO	Test Data-Out	Output	Output of serial registers that changes on the falling edge of TCK.

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TAP Registers

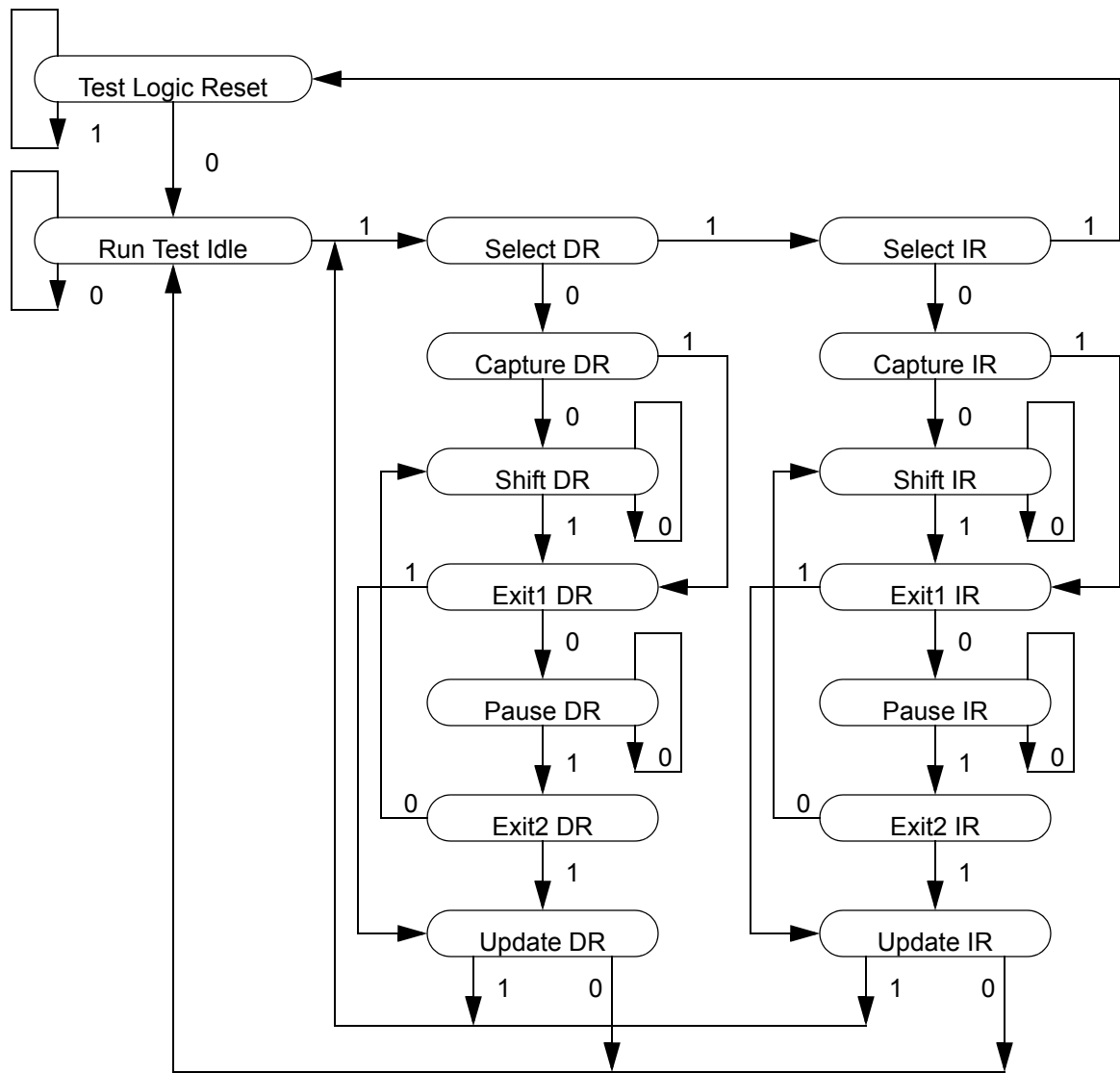
Name	Length	Description
Instruction	3	Holds instruction for the TAP controller. Loaded when placed between TDI and TDO and automatically loaded with IDCODE at power-up and after a reset.
Boundary Scan	51 for x18 70 for x36	Loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state.
Identification Code	32	The ID register is loaded with a vendor-specific code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. Defined in the ID Register Definition table.
Bypass	1	Register allows serial test data to be shifted through the SRAM with minimal delay.

TAP Controller Instructions

Code	Instruction	Description	Notes
000	EXTEST	Captures I/O ring contents and places boundary scan register between TDI and TDO. Places SRAM outputs in High-Z.	
001	IDCODE	Loads ID register and places it between TDI and TDO.	
010	SAMPLE-Z	Captures I/O ring contents and places boundary scan register between TDI and TDO. Places SRAM outputs in High-Z.	
011	Reserved	Reserved for future, do not use.	
100	SAMPLE/ PRELOAD	Captures I/O ring contents and places boundary scan register between TDI and TDO. Does not implement the preload function.	
101	Reserved	Reserved for future, do not use.	
110	Reserved	Reserved for future, do not use.	
111	BYPASS	Places the bypass register between TDI and TDO.	

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TAP Controller State Diagram



Identification Register Description

	Die Revision	Device ID	Device Type	Width & Density	JEDEC ID Code
Bit #s	31... 28	27... 24	23... 18	17... 12	11... 1
512K x 36	0100	1011	001001	100101	000001101001
1M x 18	0100	1011	001001	010101	000001101001

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TAP DC Operating Conditions
3.3V VDDQ

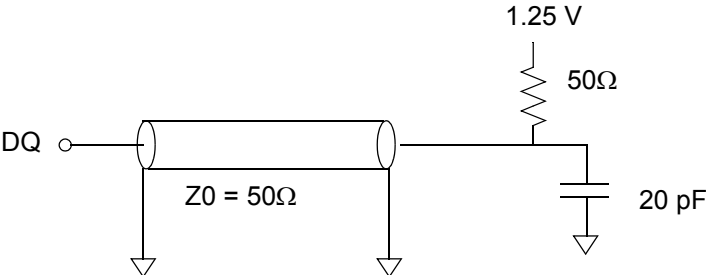
Parameter	Symbol	Min	Max	Unit	Notes
Input High Level	V _{IHT}	2.0	V _{DD} + 0.3	V	
Input Low Level	V _{ILT}	-0.5	0.7	V	
Output High Level	V _{OHT1}	2.4		V	I _{OHT1} = -4.0mA
	V _{OHT2}	2.9		V	I _{OHT2} = -100uA
Output Low Level	O _{ILT1}		0.4	V	I _{OLT1} = 8.0mA
	O _{ILT2}		0.2	V	I _{OLT2} = 100uA
Input Leakage Current	I _{LIT}	-5	5	uA	

2.5V VDDQ

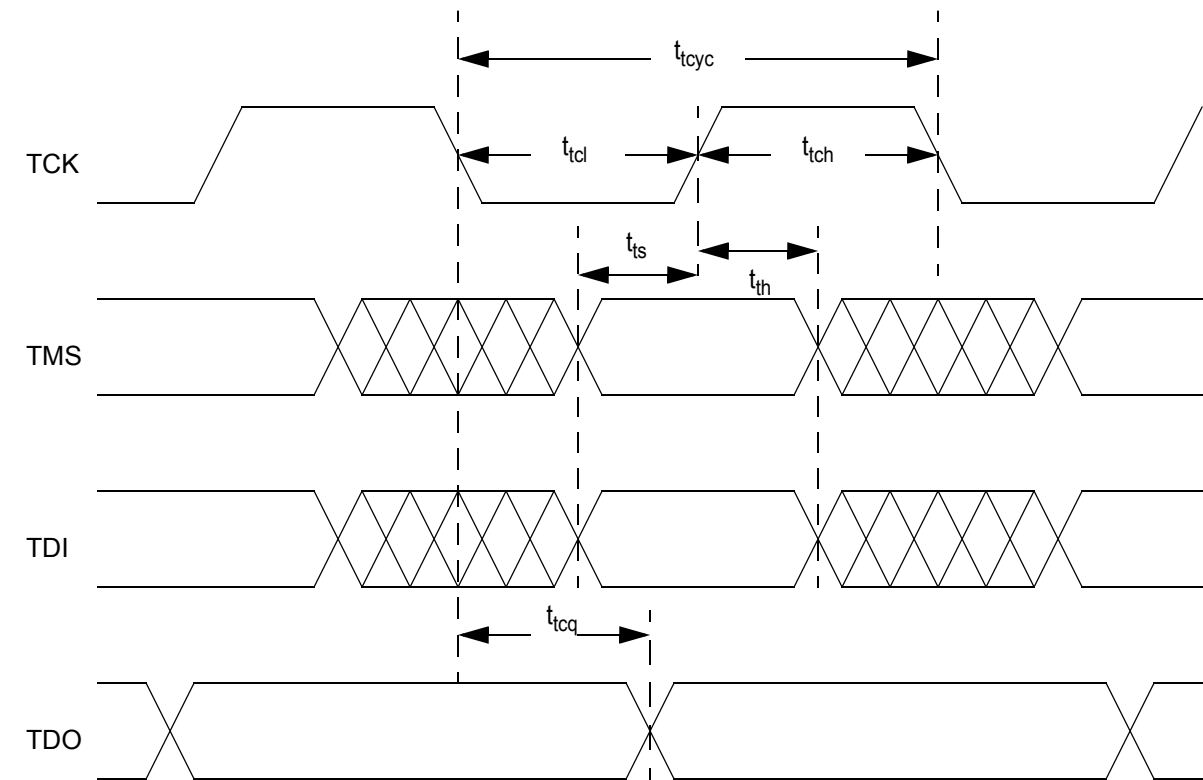
Parameter	Symbol	Min	Max	Unit	Notes
Input High Level	V _{IHT}	1.7	V _{DD} + 0.3	V	
Input Low Level	V _{ILT}	-0.3	0.7	V	
Output High Level	V _{OHT1}	1.7		V	I _{OHT1} = -1.0mA
	V _{OHT2}	2.1		V	I _{OHT2} = -100uA
Output Low Level	O _{ILT1}	-	0.4	V	I _{OLT1} = 1.0mA
	O _{ILT2}	-	0.2	V	I _{OLT2} = 100uA
Input Leakage Current	I _{LIT}	-5	5	uA	

TAP AC Test Conditions

Parameter	Conditions
Input High Level	2.5 V
Input Low Level	0.0 V
Input Slew Rate	1 nS
Input and Output Reference Level	1.25 V



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TAP AC Timing Characteristics

Parameter	Symbol	Min	Max	Units
TCK Cycle Time	t_{tcyc}	100	-	nS
TCK High Pulse Width	t_{tch}	40	-	nS
TCK Low Pulse Width	t_{tcl}	40	-	nS
TMS / TDI Setup Time	t_{ts}	10	-	nS
TMS / TDI Hold Time	t_{th}	10	-	nS
TCK Low to Output Valid	t_{tcq}	-	20	nS

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Boundary Scan Order (119 PBGA)

512Kx36

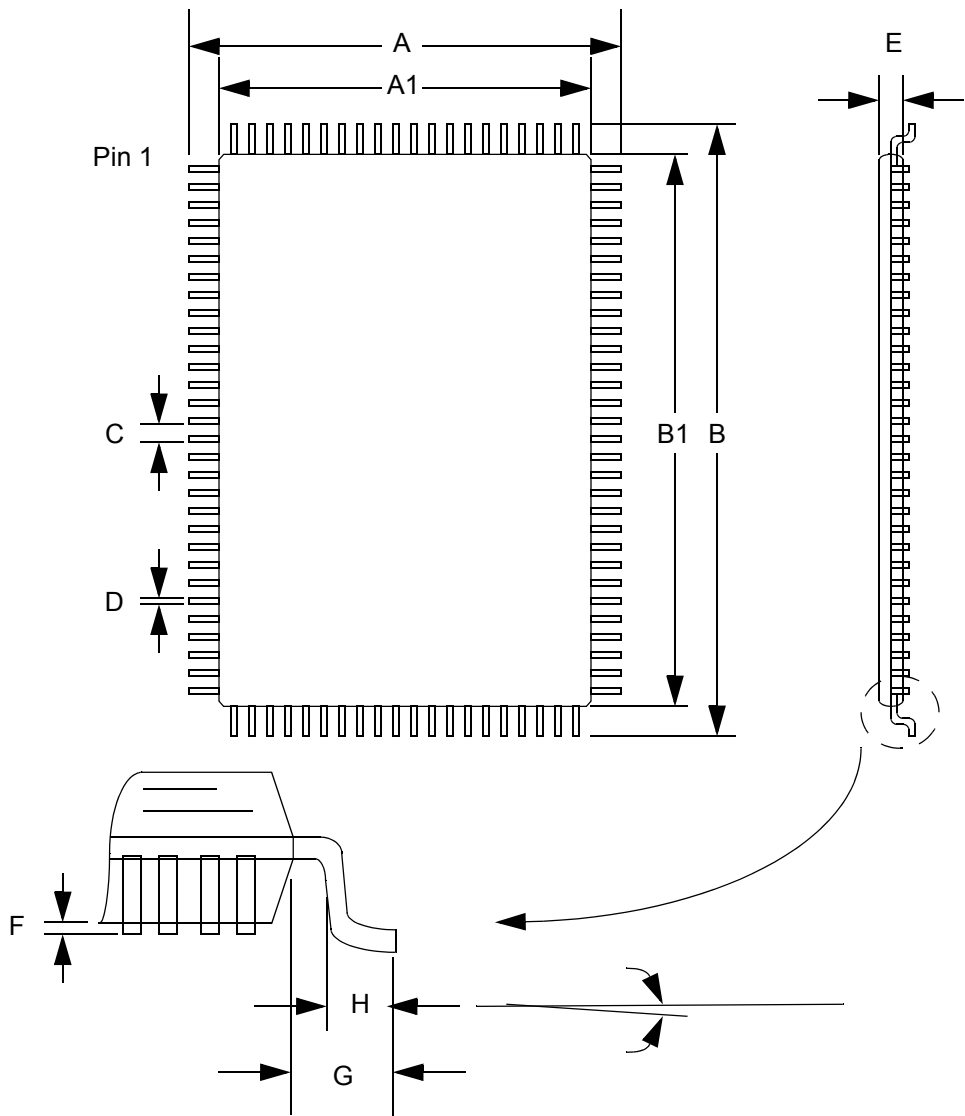
Bit #	Name	Bump ID	Bit #	Name	Bump ID
1	tbd	tbd	36	tbd	tbd
2	tbd	tbd	37	tbd	tbd
3	tbd	tbd	38	tbd	tbd
4	tbd	tbd	39	tbd	tbd
5	tbd	tbd	40	tbd	tbd
6	tbd	tbd	41	tbd	tbd
7	tbd	tbd	42	tbd	tbd
8	tbd	tbd	43	tbd	tbd
9	tbd	tbd	44	tbd	tbd
10	tbd	tbd	45	tbd	tbd
11	tbd	tbd	46	tbd	tbd
12	tbd	tbd	47	tbd	tbd
13	tbd	tbd	48	tbd	tbd
14	tbd	tbd	49	tbd	tbd
15	tbd	tbd	50	tbd	tbd
16	tbd	tbd	51	tbd	tbd
17	tbd	tbd	52	tbd	tbd
18	tbd	tbd	53	tbd	tbd
19	tbd	tbd	54	tbd	tbd
20	tbd	tbd	55	tbd	tbd
21	tbd	tbd	56	tbd	tbd
22	tbd	tbd	57	tbd	tbd
23	tbd	tbd	58	tbd	tbd
24	tbd	tbd	59	tbd	tbd
25	tbd	tbd	60	tbd	tbd
26	tbd	tbd	61	tbd	tbd
27	tbd	tbd	62	tbd	tbd
28	tbd	tbd	63	tbd	tbd
29	tbd	tbd	64	tbd	tbd
30	tbd	tbd	65	tbd	tbd
31	tbd	tbd	66	tbd	tbd
32	tbd	tbd	67	tbd	tbd
33	tbd	tbd	68	tbd	tbd
34	tbd	tbd	69	tbd	tbd
35	tbd	tbd	70	tbd	tbd

1M x18

Bit #	Name	Bump ID	Bit #	Name	Bump ID
1	tbd	tbd	27	tbd	tbd
2	tbd	tbd	28	tbd	tbd
3	tbd	tbd	29	tbd	tbd
4	tbd	tbd	30	tbd	tbd
5	tbd	tbd	31	tbd	tbd
6	tbd	tbd	32	tbd	tbd
7	tbd	tbd	33	tbd	tbd
8	tbd	tbd	34	tbd	tbd
9	tbd	tbd	35	tbd	tbd
10	tbd	tbd	36	tbd	tbd
11	tbd	tbd	37	tbd	tbd
12	tbd	tbd	38	tbd	tbd
13	tbd	tbd	39	tbd	tbd
14	tbd	tbd	40	tbd	tbd
15	tbd	tbd	41	tbd	tbd
16	tbd	tbd	42	tbd	tbd
17	tbd	tbd	43	tbd	tbd
18	tbd	tbd	44	tbd	tbd
19	tbd	tbd	45	tbd	tbd
20	tbd	tbd	46	tbd	tbd
21	tbd	tbd	47	tbd	tbd
22	tbd	tbd	48	tbd	tbd
23	tbd	tbd	49	tbd	tbd
24	tbd	tbd	50	tbd	tbd
25	tbd	tbd	51	tbd	tbd
26	tbd	tbd			

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100-Pin TQFP Package Dimensions

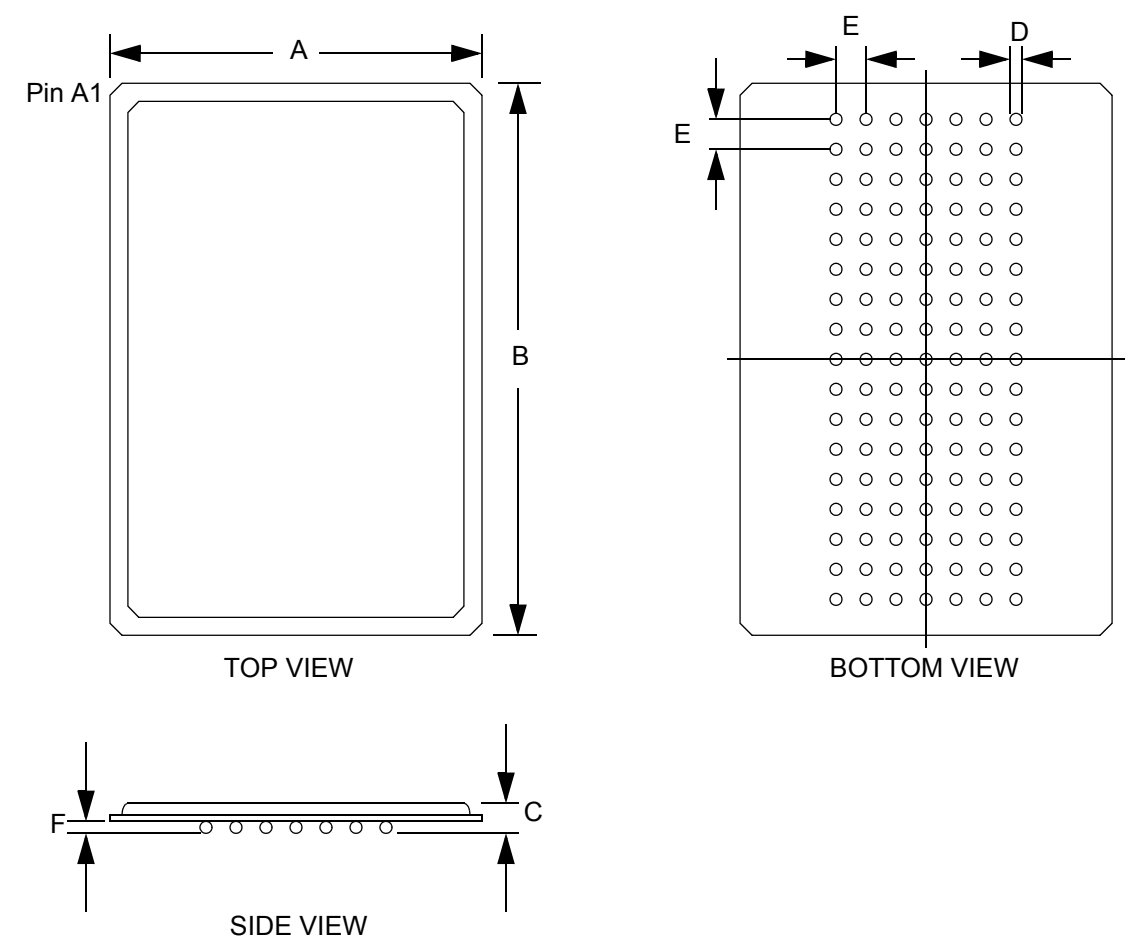


All dimensions in mm

Symbol	Description	Min	Nom	Max	Notes
A	Overall Width	15.80	16.00	16.20	
A1	Width	13.90	14.00	14.10	
B	Overall Length	21.80	22.00	22.20	
B1	Length	19.90	20.00	20.10	
C	Pin Pitch		0.65		
D	Lead Width	0.22	0.30	0.38	
E	Package Height	1.35	1.40	1.45	
F	Standoff	0.05		0.15	
G	Lead Extension		1.00		
H	Lead Bend Length	0.45	0.60	0.75	

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119-Ball BGA Package Dimensions

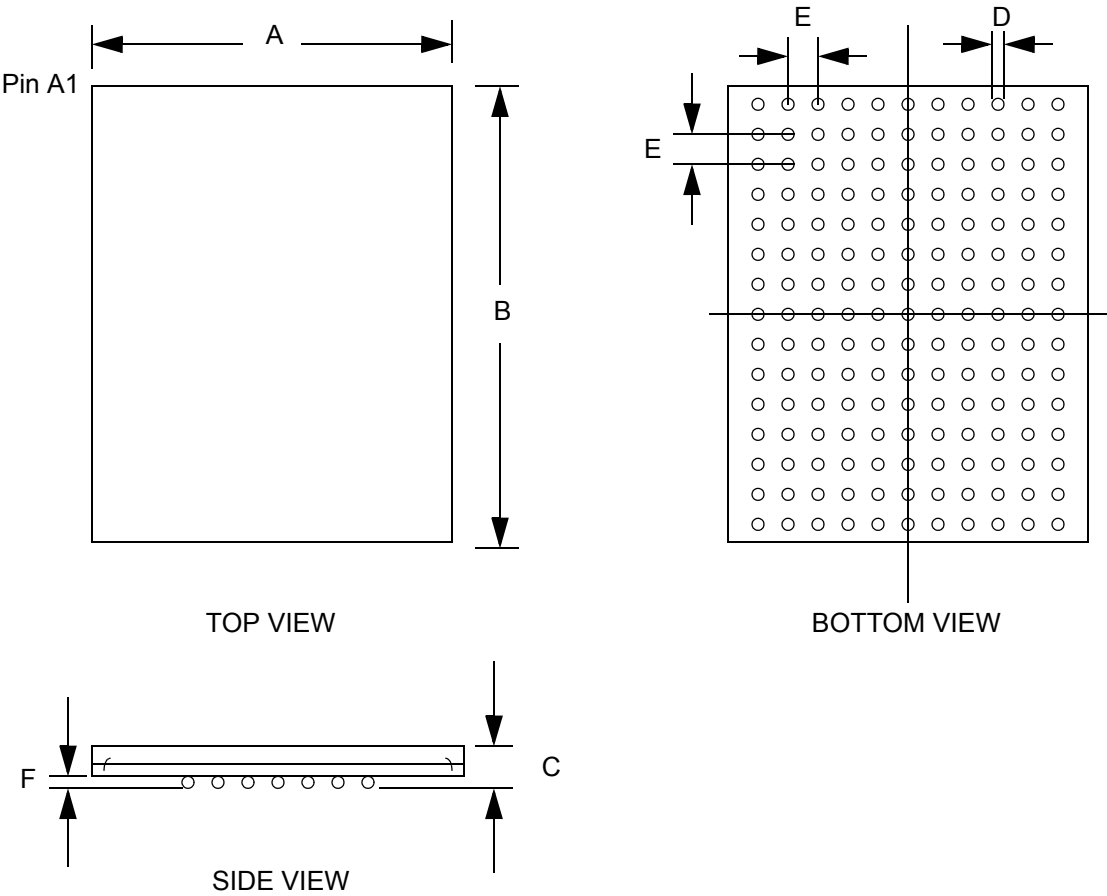


All Dimensions in mm

Symbol	Description	Min	Nom	Max
A	Package Width	13.80	14.00	14.20
B	Package Length	21.80	22.00	22.20
C	Package Height			2.40
D	Ball Width	0.70	0.75	0.80
E	Ball Pitch		1.27	
F	Ball Height	0.60	0.65	0.70

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165-Ball BGA Package Dimen-



All Dimensions in mm

Symbol	Description	Min	Nom	Max
A	Package Width	12.90	13.00	13.10
B	Package Length	14.90	15.00	15.10
C	Package Height			1.20
D	Ball Width	0.40	0.45	0.50
E	Ball Pitch		1.00	
F	Ball Height	0.25		0.40

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Ordering Information

N18NxyyF1Bz- ##C

Valid Part Number	I/O		Vcc		Package		Performance Options
	xx	I/O	yy	Vcc	z	Package	##
N18N1833F1BQ-	18	x18	33	3.3V	Q	100-TQFP	10, 11, 13
N18N3633F1BQ-	36	x36	33	3.3V			
N18N1825F1BQ-	18	x18	25	2.5V			
N18N3625F1BQ-	36	x36	25	2.5V			
N18N1833F1BF-	18	x18	33	3.3V	F	165-FPBGA	
N18N3633F1BF-	36	x36	33	3.3V			
N18N1825F1BF-	18	x18	25	2.5V			
N18N3625F1BF-	36	x36	25	2.5V			
N18N1833F1BG-	18	x18	33	3.3V	G	119-BGA	
N18N3633F1BG-	36	x36	33	3.3V			
N18N1825F1BG-	18	x18	25	2.5V			
N18N3625F1BG-	36	x36	25	2.5V			

Revision History

Revision #	Date	Change Description
A	June 2003	Initial Release