

36Mb High Speed Synchronous SRAMs with Fast Bus Turn-around™ FTRAM™ Architecture

Features

- **High performance synchronous operation**
- **Cycle times up to 300MHz**
Access times as fast as 2.3nS
- **Full 100% bus utilization**
- **Fully compatible with other no bus turn-around SRAMs**
- **Single device supports power supply of 3.3V or 2.5V**
- **Separate I/O power supply of 3.3V or 2.5V**
- **User selectable pipeline and flow-thru operating modes for BGA devices**
- **Individual byte write operation**
- **Three chip enables**
Simple depth expansion
- **ZZ mode for low power sleep mode**
- **Mode pin for setting interleave or linear burst mode of operation**
- **JTAG Boundary Scan (BGA only)**
- **JEDEC standard packages: 100-pin TQFP, 165-ball FPBGA, 119-ball PBGA and 209-ball PBGA (x72)**

Functional Description

These 36Mb high performance synchronous SRAMs form a family of device options for those demanding high performance. The FTRAM™ family of devices is designed to operate without the need of NOP or deselect clock cycles when transitioning from read to write cycles and thereby allowing the use of all available bandwidth. The high speed devices are fully compatible with other no bus turn-around SRAMs such as NoBL™, ZBT™ and NtRAM™ devices.

The memory devices contain 36Mb of memory cells organized as 2,097,152 x 18 (N36N18), 1,048,576 x 36 (N36N36) and 524,288 x 72 (N36N72). The devices operate in a synchronous manner with control signals, addresses and data inputs synchronized and captured at the rising edge of clock for ease of use. An asynchronous OE is available for disabling the outputs at any time. An asynchronous ZZ signal can be used to put the device into sleep mode with all data

retained. User configurable operation in pipeline or flow-thru modes is allowed through control of the \overline{FT} input for BGA devices. Either pipeline or flow-thru devices are available in TQFP packages. The devices are fabricated using NanoAmp's advanced CMOS process and high-speed/ultra low-power circuit technology.

This 36Mb family is ideal for networking and communication systems where high-density, high-performance memory elements are required. The architecture allows the data bus to be fully utilized when moving data into and out of the SRAM.

Performance and Power examples for P1 and PF devices

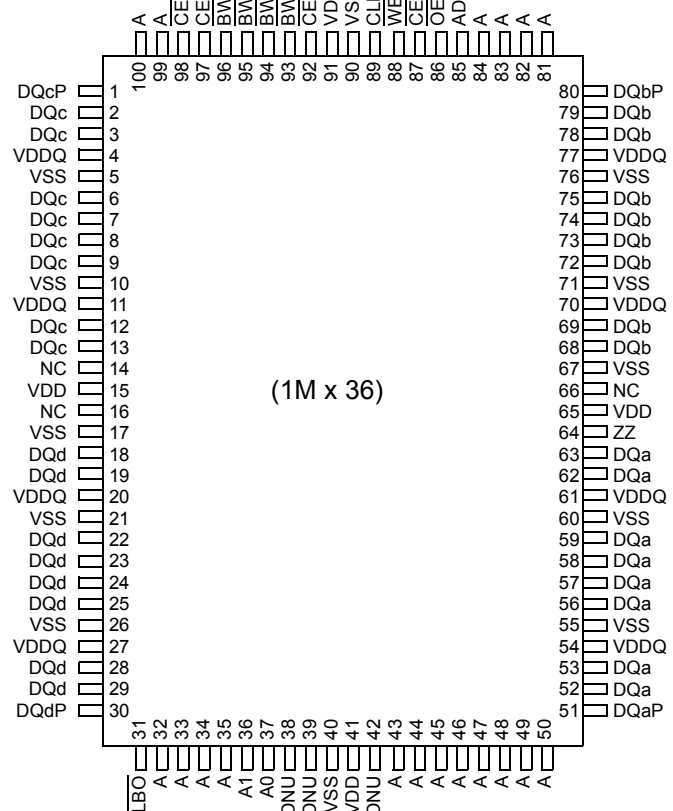
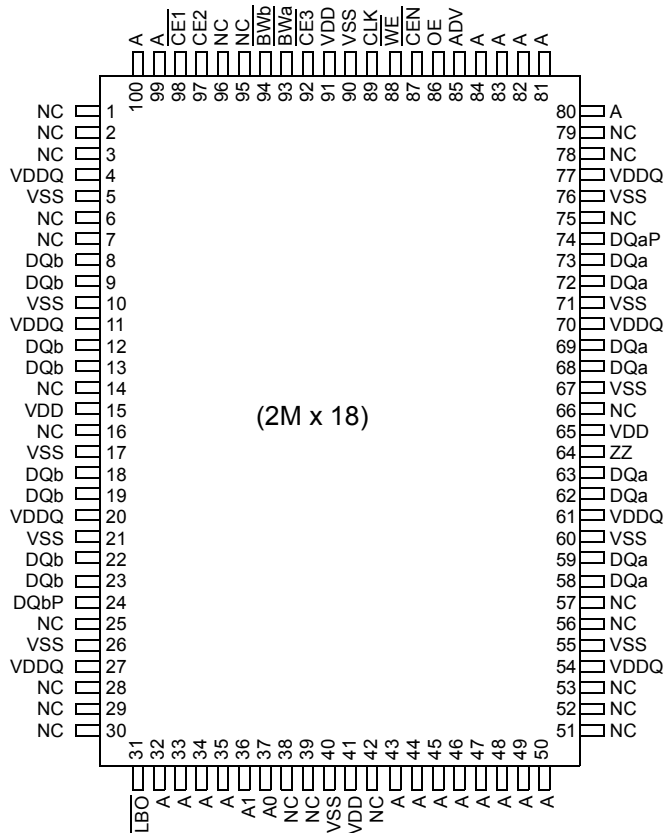
	SORT							Unit
	-13	-15	-16	-20	-22	-25	-30	
In Pipeline Mode								
t _{CYCLE}	7.5	6.7	6.0	5.0	4.4	4.0	3.3	nS
t _{ACCESS}	4.0	3.8	3.5	3.0	2.8	2.7	2.3	nS
I _{CC}	200	220	250	300	310	320	tbd	mA
I _{SB}	20	20	20	20	20	20	20	mA
In Flow-Thru Mode								
t _{CYCLE}	15.0	10.0	10.0	8.5	7.5	6.7		nS
t _{ACCESS}	11.0	10.0	8.5	7.0	6.5	6.0		nS
I _{CC}	110	120	130	150	200	220		mA
I _{SB}	20	20	20	20	20	20		mA

Options

• Organization		
2Mb x 18		N36N183W
1Mb x 36		N36N363W
512Kb x 72		N36N723W
• Operating Mode		
P1 (only for TQFP)		Pipeline
F1 (only for TQFP)		Flow-Thru
PF (for all BGA)		Pipeline or Flow-Thru
• Package		
100-pin TQFP		Q
119-ball PBGA		G
165-ball FPBGA		F
209-ball PBGA		X

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NoBL is a trademark of Cypress Semiconductor Corporation
ZBT is a trademark of Integrated Device Technology
NtRAM is a trademark of Samsung Electronics Corporation

100-Pin TQFP Packages



119-Ball PBGA Packages

2M x 18

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CE2	A	ADV	A	$\overline{\text{CE3}}$	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	VSS	NC	VSS	DQaP	NC
E	NC	DQb	VSS	$\overline{\text{CE1}}$	VSS	NC	DQa
F	VDDQ	NC	VSS	$\overline{\text{OE}}$	VSS	DQa	VDDQ
G	NC	DQb	$\overline{\text{BWb}}$	A	VSS	NC	DQa
H	DQb	NC	VSS	$\overline{\text{WE}}$	VSS	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	VSS	CLK	VSS	NC	DQa
L	DQb	NC	VSS	NC	$\overline{\text{BWa}}$	DQa	NC
M	VDDQ	DQb	VSS	$\overline{\text{CKE}}$	VSS	NC	VDDQ
N	DQb	NC	VSS	A1	VSS	DQa	NC
P	NC	DQbP	VSS	A0	VSS	NC	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	$\overline{\text{FT}}$	A	NC
T	NC	A	A	A	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

1M x 36

	1	2	3	4	5	6	7
A	VDDQ	A	A	A	A	A	VDDQ
B	NC	CE2	A	ADV	A	$\overline{\text{CE3}}$	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQcP	VSS	NC	VSS	DQbP	DQb
E	DQc	DQc	VSS	$\overline{\text{CE1}}$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{\text{OE}}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{\text{BWc}}$	A	$\overline{\text{BWb}}$	DQb	DQb
H	DQc	DQc	VSS	$\overline{\text{WE}}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{\text{BWd}}$	NC	$\overline{\text{BWa}}$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{\text{CKE}}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A1	VSS	DQa	DQa
P	DQd	DQdP	VSS	A0	VSS	DQaP	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	$\overline{\text{FT}}$	A	NC
T	NC	NC	A	A	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

7 x 17 Ball BGA with 1.27 mm Ball Pitch

165-Ball FPBGA Packages

2M x 18

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	CE1	BWb	NC	CE3	CKE	ADV	A	A	A
B	NC	A	CE2	NC	BW _a	CLK	WE	OE	A	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQaP
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	FT	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQbP	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC
R	LBO	A	A	A	TMS	A0	TCK	A	A	A	A

1M x 36

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	CE1	BW _c	BW _b	CE3	CKE	ADV	A	A	NC
B	NC	A	CE2	BW _d	BW _a	CLK	WE	OE	A	A	NC
C	DQcP	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQbP
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	FT	VDD	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQdP	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQaP
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC
R	LBO	A	A	A	TMS	A0	TCK	A	A	A	A

11 x 15 Ball BGA with 1.0 mm Ball Pitch

209-Pin BGA Package

512Kb x 72

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	CE2	A	ADV	A	CE3	A	DQb	DQb
B	DQg	DQg	\overline{BWc}	\overline{BWg}	NC	\overline{WE}	A	\overline{BWb}	\overline{BWf}	DQb	DQb
C	DQg	DQg	\overline{BWh}	\overline{BWd}	NC	$\overline{CE1}$	NC	\overline{BWe}	\overline{BWa}	DQb	DQb
D	DQg	DQg	VSS	NC	NC	\overline{OE}	NC	NC	VSS	DQb	DQb
E	DQgP	DQcP	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQfP	DQbP
F	DQc	DQc	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQf	DQf
G	DQc	DQc	VDDQ	VDDQ	VDD	NC	VDD	VDDQ	VDDQ	DQf	DQf
H	DQc	DQc	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQf	DQf
J	DQc	DQc	VDDQ	VDDQ	VDD	NC	VDD	VDDQ	VDDQ	DQf	DQf
K	NC	NC	CLK	NC	VSS	\overline{CKE}	VSS	NC	NC	NC	NC
L	DQh	DQh	VDDQ	VDDQ	VDD	\overline{FT}	VDD	VDDQ	VDDQ	DQa	DQa
M	DQh	DQh	VSS	VSS	VSS	NC	VSS	VSS	VSS	DQa	DQa
N	DQh	DQh	VDDQ	VDDQ	VDD	NC	VDD	VDDQ	VDDQ	DQa	DQa
P	DQh	DQh	VSS	VSS	VSS	ZZ	VSS	VSS	VSS	DQa	DQa
R	DQdP	DQhP	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQaP	DQeP
T	DQd	DQd	VSS	NC	NC	\overline{LBO}	NC	NC	VSS	DQe	DQe
U	DQd	DQd	NC	A	NC	A	A	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Pin Descriptions

Signal	Type	POWER
A0, A1	Synch Input	Address inputs sampled at the rising edge of CLK. Least significant address bits are used to set the internal burst counter (if used).
Ax	Synch Input	Address inputs 2 through 18/19/20, sampled at the rising edge of CLK.
LBO	Synch Input	Linear burst order, active low, used for setting the address order of the burst counter. A low selects linear burst order while a high selects interleave burst order and if floating, this input will default to a high (interleave order) This should not be changed while operating the SRAM.
ADV	Synch Input	Advance/load, sampled at the rising edge of clock. When high, the internal burst counter is advanced for the next address and when low, a new address is loaded from the address pins.
BWx	Synch Input	Byte write, active low, sampled at the rising edge of CLK if \overline{WE} is low for a write cycle. BW(a-b) used for x18, BW(a-d) used for x36 and BW(a-h) used for x72.
\overline{WE}	Synch Input	Write enable, active low, sampled at the rising edge of CLK. A low state initiates a write cycle.
CLK	Clock Input	Clock
$\overline{CE1}$	Synch Input	Chip enable 1, active low, sampled on the rising edge of CLK. Used with $\overline{CE2}$ and $\overline{CE3}$ and to select the device.
$\overline{CE2}$	Synch Input	Chip enable 2, active high, sampled on the rising edge of CLK. Used with $\overline{CE1}$ and $\overline{CE3}$ and to select the device.
$\overline{CE3}$	Synch Input	Chip enable 3, active low, sampled on the rising edge of CLK. Used with $\overline{CE2}$ and $\overline{CE1}$ and to select the device.
\overline{CKE}	Synch Input	Clock enable, active low and while low, allows CLK to be recognized by the SRAM. While high, \overline{CKE} inhibits CLK from driving SRAM cycles and extends cycles already in progress.
\overline{OE}	Asynch Input	Output enable, asynchronous active low, tri-states the output buffers when high and enables the output buffers when low.
ZZ	Asynch Input	Sleep mode, asynchronous active high, puts the device in a low power sleep mode that retains all data while high. Defaults to an inactive low state.
\overline{FT}	DC Input (BGA only)	Flow-thru mode, active low. Floated or connected high for pipeline mode.
DQx	Synch Input/ Output	During a write cycle, the DQs are synchronous inputs that are sampled at the rising edge of CLK to specify data to be written to the memory array. During a read cycle, the DQs are driven out with data from the SRAM array. DQ(a-b) apply for x18, DQ(a-d) apply for x36 and DQ(a-h) apply for x72.
VDD	Power Supply	Supplies power to the device core.
VDDQ	I/O Power Supply	Supplies power to the I/O section of the device.
VSS	Ground supply	Ground
TMS	Input (BGA)	Test Mode Select supplies input command to the TAP controller with TCK.
TDI	Input (BGA)	Test Data Input supplies serial input to test registers.
TDO	Output (BGA)	Test Data Output supplies serial data out from test registers.
TCK	Input (BGA)	Test Clock controls TAP controller and serial data in and data out.

Functional Truth Table¹

Operation	Address	$\overline{\text{CE1}}$	CE2	$\overline{\text{CE3}}$	ADV	$\overline{\text{WE}}$	$\overline{\text{BWx}}^2$	$\overline{\text{OE}}$	ZZ	$\overline{\text{CKE}}^3$	CLK ⁴	DQ ⁵
DESELECT	NA	H	X	X	L	X	X	X	L	L	L-H	High-Z
DESELECT	NA	X	L	X	L	X	X	X	L	L	L-H	High-Z
DESELECT	NA	X	X	H	L	X	X	X	L	L	L-H	High-Z
Continue DESELECT ⁶	NA	X	X	X	H	X	X	X	L	L	L-H	High-Z
READ, begin burst	Ext	L	H	L	L	H	X	L	L	L	L-H	Data-out
READ, continue burst ^{6,7}	Int	X	X	X	H	X	X	L	L	L	L-H	Data-out
DUMMY READ, begin burst ⁸	Ext	L	H	L	L	H	X	H	L	L	L-H	High-Z
DUMMY READ, continue burst ^{7,8}	Int	X	X	X	H	X	X	H	L	L	L-H	High-Z
WRITE, begin burst	Ext	L	H	L	L	L	L	X	L	L	L-H	Data-in
WRITE, continue burst ⁶	Int	X	X	X	H	X	L	X	L	L	L-H	Data-in
WRITE ABORT, begin burst ⁸	Ext	L	H	L	L	L	H	X	L	L	L-H	High-Z
IGNORE CLOCK ⁹	Current	X	X	X	X	X	X	X	L	H	L-H	-
Deep Sleep	NA	X	X	X	X	X	X	X	H	X	X	High-Z

1. X = don't care; H = logic HIGH; L = logic LOW.
All inputs except OE and ZZ must meet set-up and hold times.
2. BWx = H means all BW signals are high; BWx = L means one or more BW signals are low.
3. Wait states are inserted by setting $\overline{\text{CKE}}$ high.
4. L-H refers to the CLK edge transitioning from a low to a high state.
5. All outputs will remain in high-Z during power-up.
6. All continue burst cycles use the same control inputs. The type of cycle is chosen in the first cycle prior to the continue cycle.
7. A 2-bit burst counter is included which is incremented for all continue burst cycles. The address wraps around every fourth burst cycle.
8. Dummy read and write abort commands perform no external operation, they are NOP cycles.
9. If an ignore clock ($\overline{\text{CKE}}$ high) cycle happens during a read, the DQ bus will remain active. If this happens during a write, the DQ bus will remain High-Z, no write occurs.

Burst Order Tables

Interleave	Starting digits		Starting digits		Starting digits		Starting digits	
$\overline{\text{LBO}} = \text{High}$	A1	A0	A1	A0	A1	A0	A1	A0
First address	0	0	0	1	1	0	1	1
Second address	0	1	0	0	1	1	1	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	1	0	0	1	0	0

Linear	Starting digits		Starting digits		Starting digits		Starting digits	
$\overline{\text{LBO}} = \text{Low}$	A1	A0	A1	A0	A1	A0	A1	A0
First address	0	0	0	1	1	0	1	1
Second address	0	1	1	0	1	1	0	0
Third address	1	0	1	1	0	0	0	1
Fourth address	1	1	0	0	0	1	1	0

Note:

At the end of a burst of four, the burst counter wraps to the starting address and continues.

Flow-Thru/Pipeline and Burst Order Mode Controls

Mode Pin	Description	State	Function
\overline{FT}^1	Operating mode for output registers	L	Flow-thru
		H	Pipeline
\overline{LBO}	Burst order	L	Linear
		H	Interleave

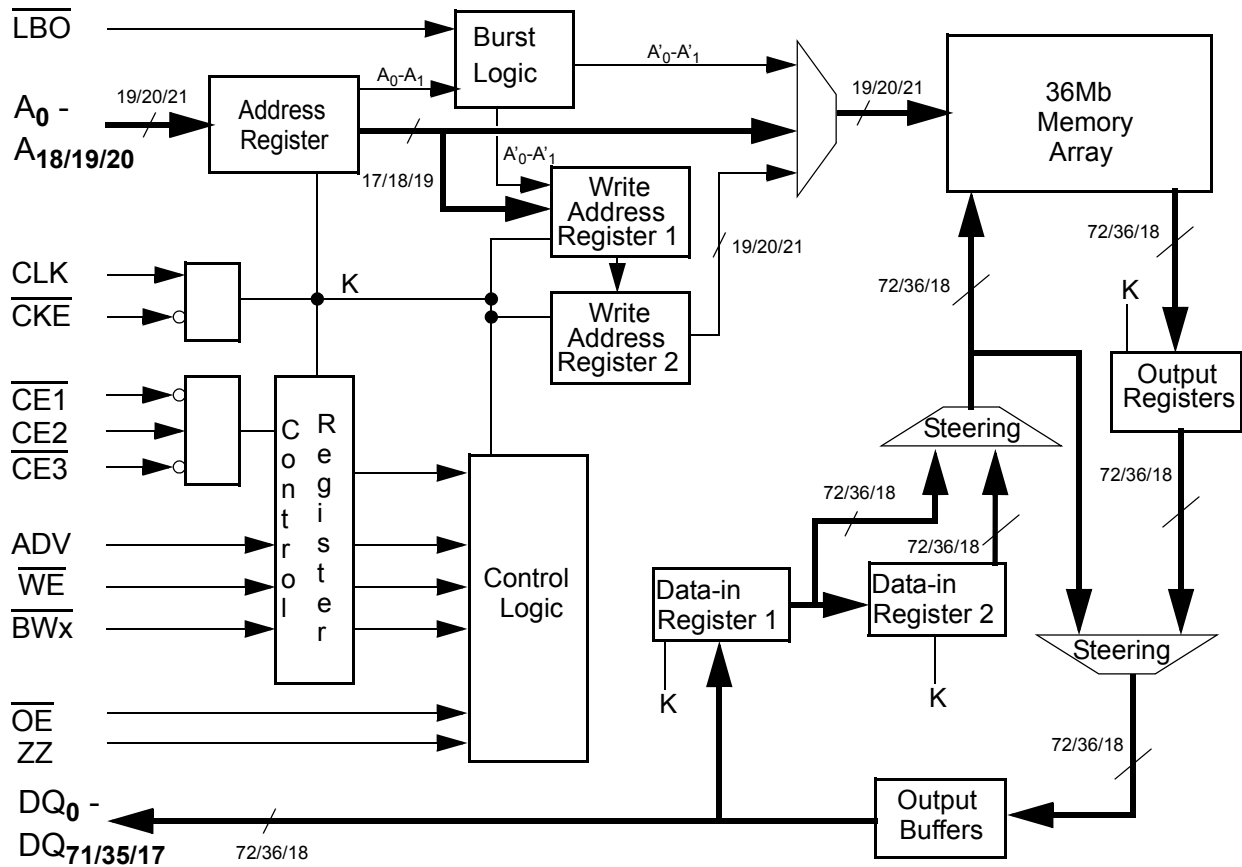
1. If unconnected, the \overline{FT} input will default "high" and the device will operate in the pipeline mode. Applicable to BGA only.

WRITE TRUTH TABLE^{1 2}

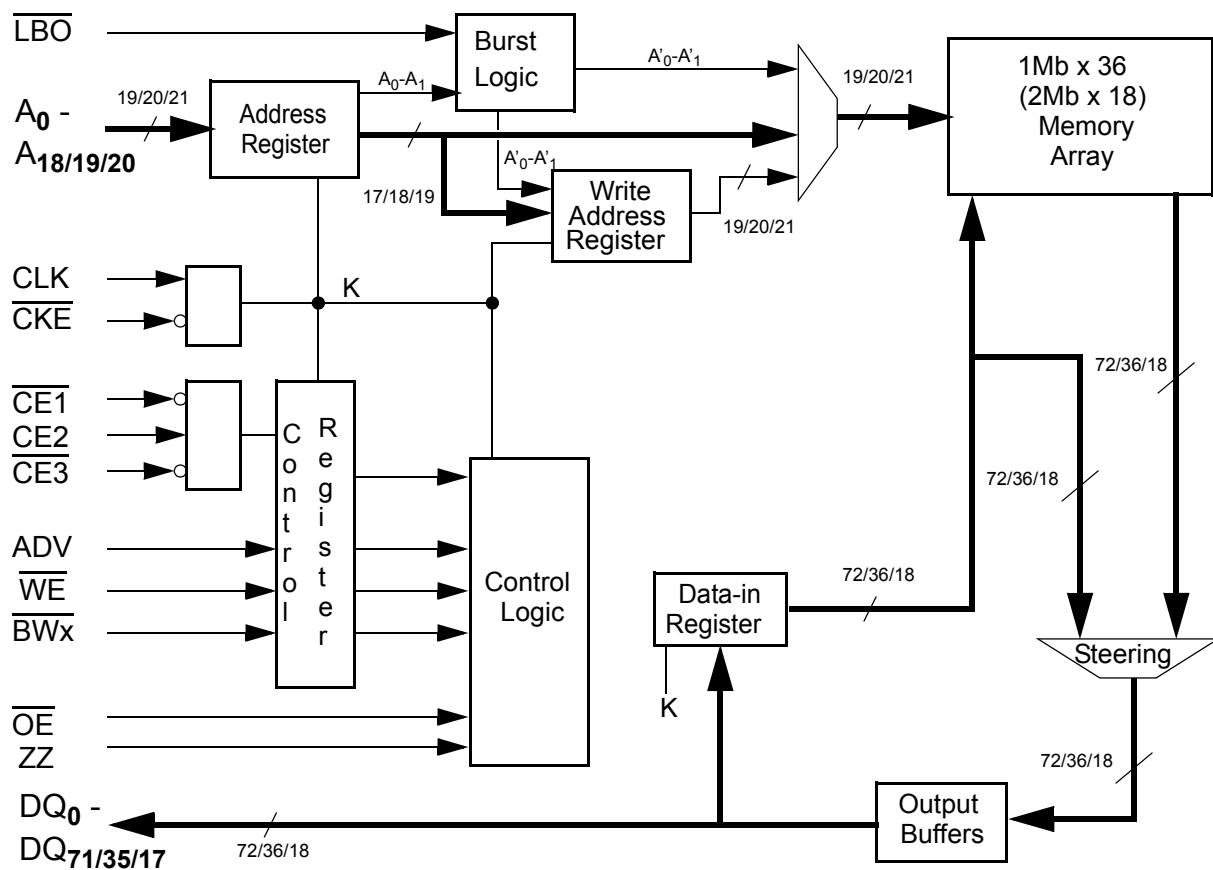
Function	\overline{WE}	\overline{BWA}	\overline{BWB}	\overline{BWC}	\overline{BWD}	\overline{BWE}	\overline{BWF}	\overline{BWG}	\overline{BWH}	x72	x36	x18
READ	H	X	X	X	X	X	X	X	X			
WRITE byte a	L	L	H	H	H	H	H	H	H			
WRITE byte b	L	H	L	H	H	H	H	H	H			
WRITE byte c	L	H	H	L	H	H	H	H	H			
WRITE byte d	L	H	H	H	L	H	H	H	H			
WRITE byte e	L	H	H	H	H	L	H	H	H			
WRITE byte f	L	H	H	H	H	H	L	H	H			
WRITE byte g	L	H	H	H	H	H	H	L	H			
WRITE byte h	L	H	H	H	H	H	H	H	L			
WRITE all byte	L	L	L	L	L	L	L	L	L			
WRITE abort/NOP	L	H	H	H	H	H	H	H	H			
x72												
x36												
x18												

1. \overline{BWA} and \overline{BWB} are used for the x18 device, \overline{BWA} , \overline{BWB} , \overline{BWC} and \overline{BWD} are used for the x36 device and \overline{BWA} through \overline{BWH} are used for the x72 device.
2. X = don't care; H = logic HIGH; L = logic LOW.

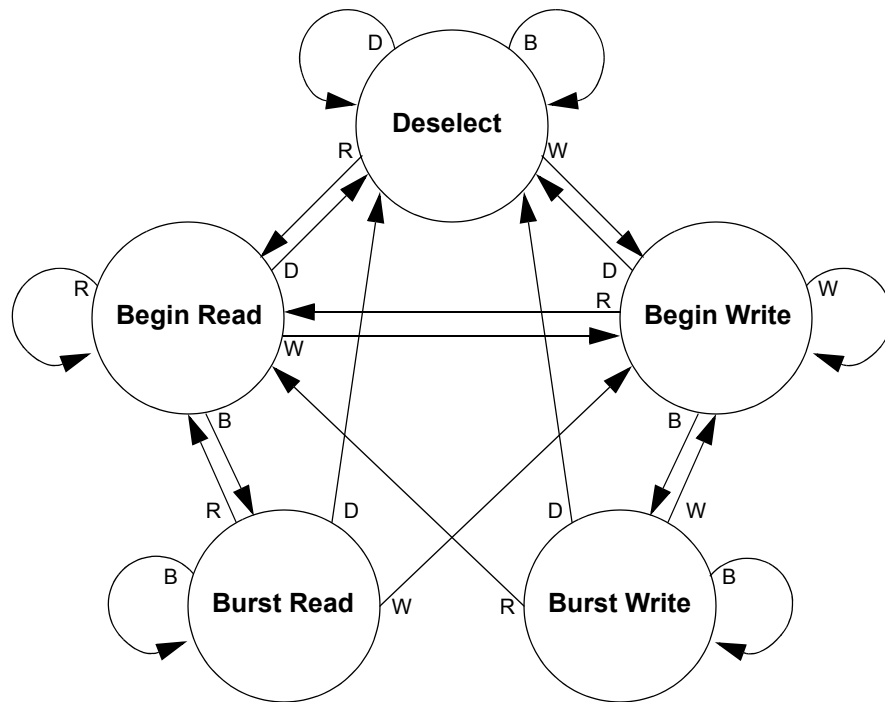
Pipeline Functional Block Diagram



Flow-Thru Functional Block Diagram



Read and Write State Diagram



Key:

State diagram shows current state and transitions to possible next states.

D = Deselect

R = Read

W = Write

B = Burst (read, write or deselect)

Functional Operation

The N36N18, N36N36 and N36N72 family of devices is developed for the high performance needs of the networking and communications markets. Devices are available with a user configurable choice of either pipeline or flow-thru modes of operation depending on the particular system needs. All inputs except OE, LBO and ZZ are synchronized and registered by the rising edges of the clock (CLK). Three chip enables are available for depth expansion with CE1 and CE3 being active low and CE2 active high. For a cycle to start, all three must be active and any one inactive will deselect the device. Read operations are started with CKE, CE1, CE3 and ADV being asserted low at the rising edge of CLK along with WE and CE2 being asserted high. Write operations are started with CKE, CE1, CE3, ADV and WE being asserted low at the rising edge of CLK along with CE2 being asserted high. The byte write enable (BWx) inputs are used to determine which bytes (or all bytes) will be written to. The address inputs are latched and used as the location in memory to start a memory cycle. Clock enable input (CKE) allows operations to be stalled or suspended while CKE is inactive high. In this operation, all internal registers retain data from the previous operation. Output enable (OE), linear burst mode (LBO) and sleep mode (ZZ) are asynchronous signals that control other aspects of the device. OE is used to disable the output buffers at any time. LBO is either tied high for interleave burst order or low for linear burst order. ZZ is used to put the device in a low power sleep mode, while all data is retained in the SRAM memory array.

Burst Operation

The previous operations discussed were initiated with ADV being asserted low, thereby activating a cycle with a new external address being loaded and used for array operations. If ADV is asserted high at the rising edge of CLK, the internal burst counter is incremented and an internal address is used to access the SRAM array. The burst counter is a four bit counter and can be incremented in two orders, interleave and linear. The burst counter wraps around after four addresses and continues to operate as long as ADV is high and valid CLK cycles are performed.

Pipeline Operation

For a read cycle, all the necessary control signals must be setup at the rising edge of CLK as stated

above. The memory array is then accessed. During this first cycle, data propagates through to the output registers. At the next rising edge of CLK, data moves through the output registers and out of the SRAM on the DQ pins. This pipeline operation reads data out on the clock edge following the initial rising edge.

For a write cycle, all the necessary control signals must be setup at the rising edge of CLK as stated above. The BWx must be setup active low for whichever bytes will be written too at this first rising edge of CLK. The data to be written to the SRAM is not registered until the third rising edge of CLK. This is called a late-late write (or double late write) cycle as data is not necessary until the third cycle while address and write command information is required at the first cycle.

Pipeline reads and writes can be performed in single access (ADV = L) cycles or burst (ADV = H) cycles.

Flow Thru Operation

The flow thru device is very similar in operations to the pipeline device. The fundamental difference is that the latency of data (read and write) is one cycle shorter than pipeline mode.

For a flow thru read operation, initiating the cycle is identical to the pipeline operation. The difference is in that fact that the data propagates out of the SRAM sooner. Data is driven out of (or flows through) the SRAM in the same cycle as the activation instead of waiting until the next rising edge of CLK.

For a flow thru write operation, again initiation of the cycle is identical. The difference here is the fact that the input data is required to be registered at the second rising edge of CLK instead of the third. This is called a late write cycle as data is not necessary until the cycle after address and write command information.

Flow thru reads and writes can be performed in single access (ADV = L) cycles or burst (ADV = H) cycles.

Sleep Mode

Sleep mode is a low power mode that allows the device to continue to retain data in a power down mode. ZZ is asserted high to enter sleep mode and after two clock cycles, the operating current will be reduced to I_{SL} . Since ZZ is an asynchronous operation, sleep mode should not be started until all operations are completed. ZZ should be asserted low for normal operation. The input will default to a low if left floating.

Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Voltage on any V_{DD} pin wrt Ground	-0.5 to 4.6	V
V_{DDQ}	Voltage on any V_{DDQ} pin	-0.5 to V_{DD}	V
V_{IN}^1	Voltage on any input pin	-0.5 to V_{DD}	V
$V_{I/O}^1$	Voltage on any DQ pin	-0.5 to V_{DDQ}	V
PD	Package power dissipation	1.5	W
T_{BIAS}	Temperature under bias	-55 to 125	°C
T_{STOR}	Storage temperature	-60 to 150	°C
I_{OUT}	Current into output circuit	20	mA

1. Minimum voltage must not exceed -2V for pulse widths of < 20% t_{CYC}

Pin Capacitance

Item	Symbol	Conditions	Typ	Max	Unit	
Control Pins	C_i	$T_a = 25^\circ\text{C}$, $V_{DD} = \text{Typ}$, $f = 1\text{MHz}$	4	5	pF	
Address Pins	C_a		4	5	pF	
Output Pins	C_o		5	7	pF	

Thermal Resistance

Item	Conditions	Theta JA Junction to Ambient	Theta JC Junction to Case	Unit
100-pin TQFP	Still air, soldered on a 2 layer board	tbd	tbd	°C/W
119-ball PBGA	Still air, soldered on a 4 layer board	tbd	tbd	°C/W
165-ball FPBGA		tbd	tbd	

Operating Conditions and DC CharacteristicsOver the operating range. All voltages referenced to ground (V_{SS}).**Power Supply and Input/Output Levels**

Item	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage ¹	V_{DD1}		3.0	3.3	3.6	V
	V_{DD2}		2.3	2.5	2.7	
I/O Supply Voltage	V_{DDQ1}		3.0	3.3	3.6	V
	V_{DDQ2}		2.375	2.5	2.7	
Input High Voltage	V_{IH}	Operating with V_{DD1}	2.0		$V_{DD}+0.3$	V
		Operating with V_{DD2}	1.7		$V_{DD}+0.3$	
Input Low Voltage	V_{IL}	Operating with V_{DD1}	-0.3		0.8	V
		Operating with V_{DD2}	-0.3		0.7	
Output High Voltage	V_{OH}	Operating w/ V_{DDQ1} , $I_{OH} = -4.0\text{mA}$	2.4		-	V
		Operating w/ V_{DDQ2} , $I_{OH} = -1.0\text{mA}$	2.0		-	
Output Low Voltage	V_{OL}	$I_{OL} = 8.0\text{mA}$	-		0.4	V
Input Leakage Current	I_{LI}	$0V < V_{IN} < V_{DD}$	-1.0		1.0	μA
Input Leakage Current of $\overline{\text{LBO}}$, ZZ and $\overline{\text{FT}}$ inputs ²			-30.0		30.0	
Output Leakage Current	I_{LO}	Outputs disabled $0V < V_{IN} < V_{DDQ}$	-1.0		1.0	μA

1. For operation using V_{DD1} , either V_{DDQ1} or V_{DDQ2} can be used. For operation using V_{DD2} , V_{DDQ2} must be used.2. $\overline{\text{LBO}}$, ZZ and $\overline{\text{LBO}}$ inputs $I_{LI} = \pm 30\mu\text{A}$ due to internal resistors for floating conditions.

VDD Operating Currents - Pipeline Device¹

Over the operating range.

Current	Symbol	Conditions	Sort	Typ	Max	Unit
Operating Current ²	I_{DD}	Device selected; All inputs < V_{IL} or > V_{IH} ; Frequency < $1/T_{cyc}$ (MIN); Outputs open	- 13		200	mA
			- 15		220	
			- 16		250	
			- 20		300	
			- 22		310	
			- 25		320	
			- 30		TBD	
Deselect Current - Standby (CMOS)	I_{SB1}	Device deselected; All inputs static and < 0.2V or > $V_{DD}-0.2$, Frequency = 0	All		20	mA
Deselect Current - Standby (TTL)	I_{SB2}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = 0	All		50	mA
Deselect Current - Clock running (CMOS)	I_{SB3}	Device deselected; All inputs < 0.2V or > $V_{DD}-0.2$; Frequency < $1/T_{cyc}$ (MIN)	- 13		50	mA
			- 15		60	
			- 16		65	
			- 20		75	
			- 22		80	
			- 25		85	
			- 30		95	
Deselect Current - Clock running (TTL)	I_{SB4}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = $1/T_{cyc}$	- 13		60	mA
			- 15		70	
			- 16		75	
			- 20		85	
			- 22		90	
			- 25		95	
			- 30		105	
Sleep Mode Current	I_{SL}	$ZZ > V_{IH}$	All		20	mA

1. Currents are specified for $V_{DD} = V_{DD} \text{ max.}$

2. Does not include output currents.

VDD Operating Currents - Flow Thru Device¹

Over the operating range.

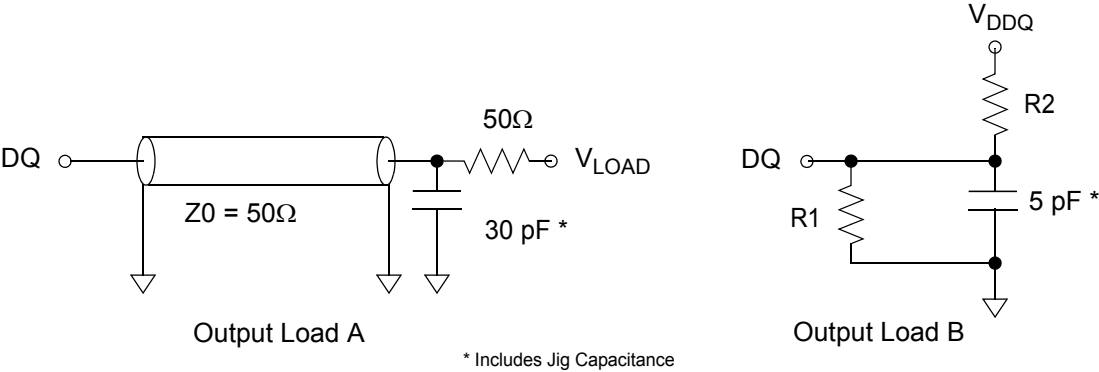
Current	Symbol	Conditions	Sort	Typ	Max	Unit
Operating Current ²	I_{DD}	Device selected; All inputs < V_{IL} or > V_{IH} ; Frequency < $1/T_{cyc}$ (MIN); Outputs open	- 13		110	mA
			- 15		120	
			- 16		130	
			- 20		250	
			- 22		200	
			- 25		220	
Deselect Current - Standby (CMOS)	I_{SB1}	Device deselected; All inputs static and < 0.2V or > $V_{DD}-0.2$, Frequency = 0	All		20	mA
Deselect Current - Standby (TTL)	I_{SB2}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = 0	All		50	mA
Deselect Current - Clock running (CMOS)	I_{SB3}	Device deselected; All inputs < 0.2V or > $V_{DD}-0.2$; Frequency < $1/T_{cyc}$ (MIN)	- 13		50	mA
			- 15		50	
			- 16		50	
			- 20		60	
			- 22		65	
			- 25		70	
Deselect Current - Clock running (TTL)	I_{SB4}	Device deselected; All inputs static and < V_{IL} or > V_{IH} , Frequency = $1/T_{cyc}$	- 13		60	mA
			- 15		60	
			- 16		60	
			- 20		70	
			- 22		75	
			- 25		80	
Sleep Mode Current	I_{SL}	$ZZ > V_{IH}$	All		20	mA

1. Currents are specified for $V_{DD} = V_{DD} \text{ max}$.

2. Does not include output currents.

AC Test Conditions

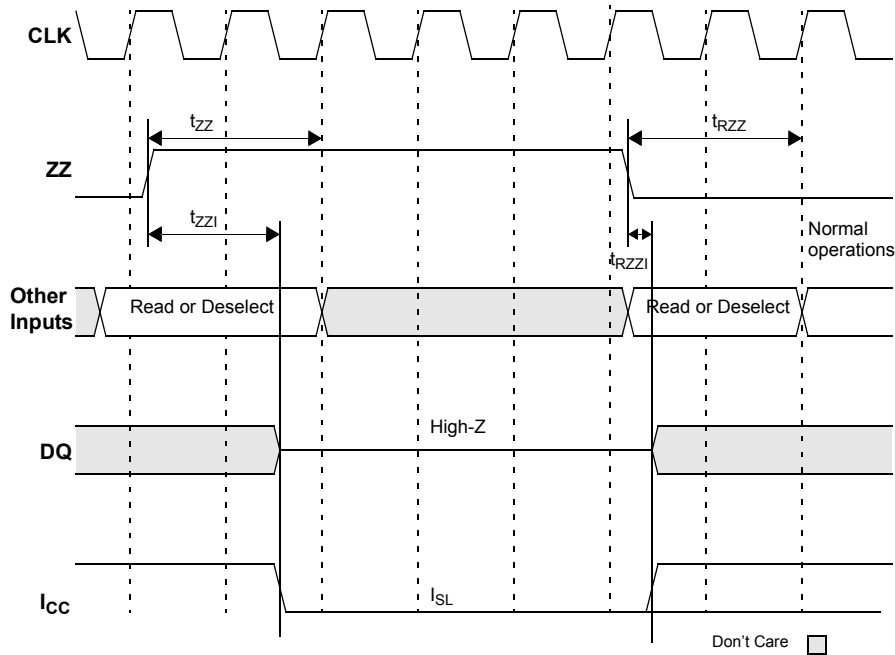
Item	Value
Input Pulse Level	0V to 2.5V
Input Rise and Fall Time	1.0V/nS
Input Timing Reference Level	V _{DD} /2
Output Timing Reference Level	V _{DDQ} /2
Output Load	See diagram below



AC Output Load

Component	Value		Unit
	3.3V I/O	2.5V I/O	
VLOAD	1.5	1.25	V
R1	351	1538	Ω
R2	317	1667	Ω
VDDQ	3.3	2.5	V

Timing Waveforms Sleep Mode



Sleep Mode Characteristics

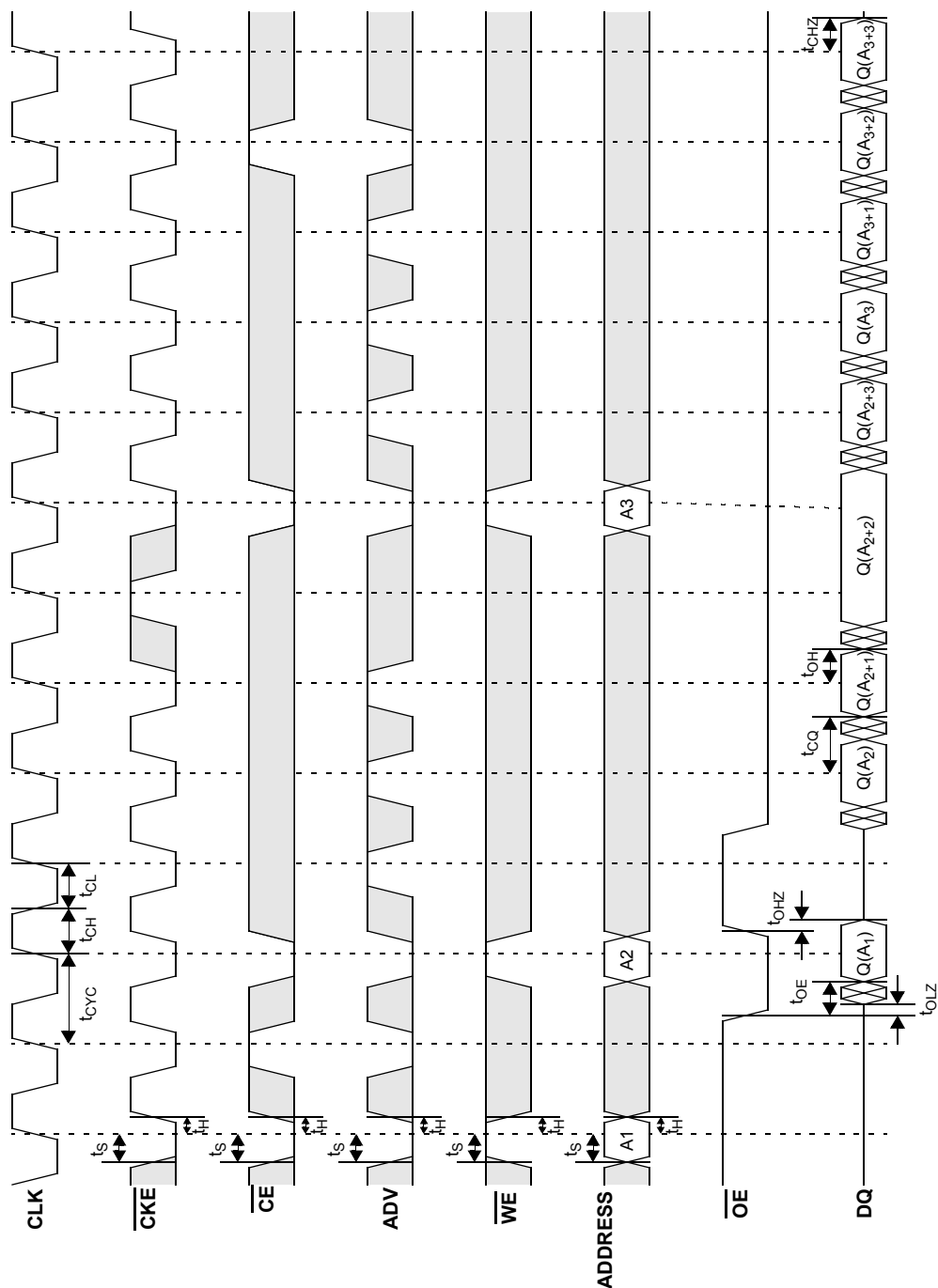
Item	Symbol	Conditions	Min	Max	Units	Notes
ZZ active to input ignored	t _{ZZ}	ZZ > V _{IH}	0	2	cycles	
ZZ inactive to input sampled	t _{RZZ}		0	2	cycles	
ZZ active to sleep current	t _{ZZI}			2	cycles	
ZZ inactive to exit sleep current	t _{RZZI}		0		nS	
Sleep mode power supply current	I _{SL}			10	mA	

AC Timing Characteristics - Pipeline Device

Parameter		-30		-25		-22		-20		-16		-15		-13		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CLOCK TIMINGS																
Clock Cycle Time	t _{CYC}	3.3		4.0		4.4		5.0		6.0		6.7		7.5		nS
Clock High Pulse Width	t _{CH}	1.5		1.5		1.5		1.5		1.5		1.7		2.0		nS
Clock Low Pulse Width	t _{CL}	1.5		1.5		1.5		1.5		1.5		1.7		2.0		nS
Clock Frequency	F _{MAX}		300		250	225			200		167		150		133	MHz
OUTPUT TIMINGS																
Clock high to output valid	t _{CQ}		2.3		2.7		2.8		3.0		3.5		3.8		4.0	nS
Output hold from clock high	t _{OH}	1.5		1.5		1.5		1.5		1.5		1.5		1.5		nS
Clock to output in low-Z ¹	t _{CLZ}	1.5		1.5		1.5		1.5		1.5		1.5		1.5		nS
Clock to output in high-Z ¹	t _{CHZ}		2.3		2.3		2.3		3.0		3.0		3.0		3.0	nS
OE low to output valid	t _{IOE}		2.3		2.7		2.8		3.0		3.5		3.8		4.0	nS
OE low to output in low-Z ¹	t _{OLZ}	0		0		0		0		0		0		0		nS
OE high to output in high-Z ¹	t _{OHZ}		2.3		2.3		2.3		3.0		3.0		3.0		3.5	nS
SETUP AND HOLD TIMES																
Setup Time	t _S	1.5		1.5			1.5	1.5		1.5		1.5		1.5		nS
Hold Time	t _H	0.5		0.5			0.5	0.5		0.5		0.5		0.5		nS

1. t_{CLZ} , t_{CHZ} , t_{OLZ} , t_{OHZ} are specified with output load B.

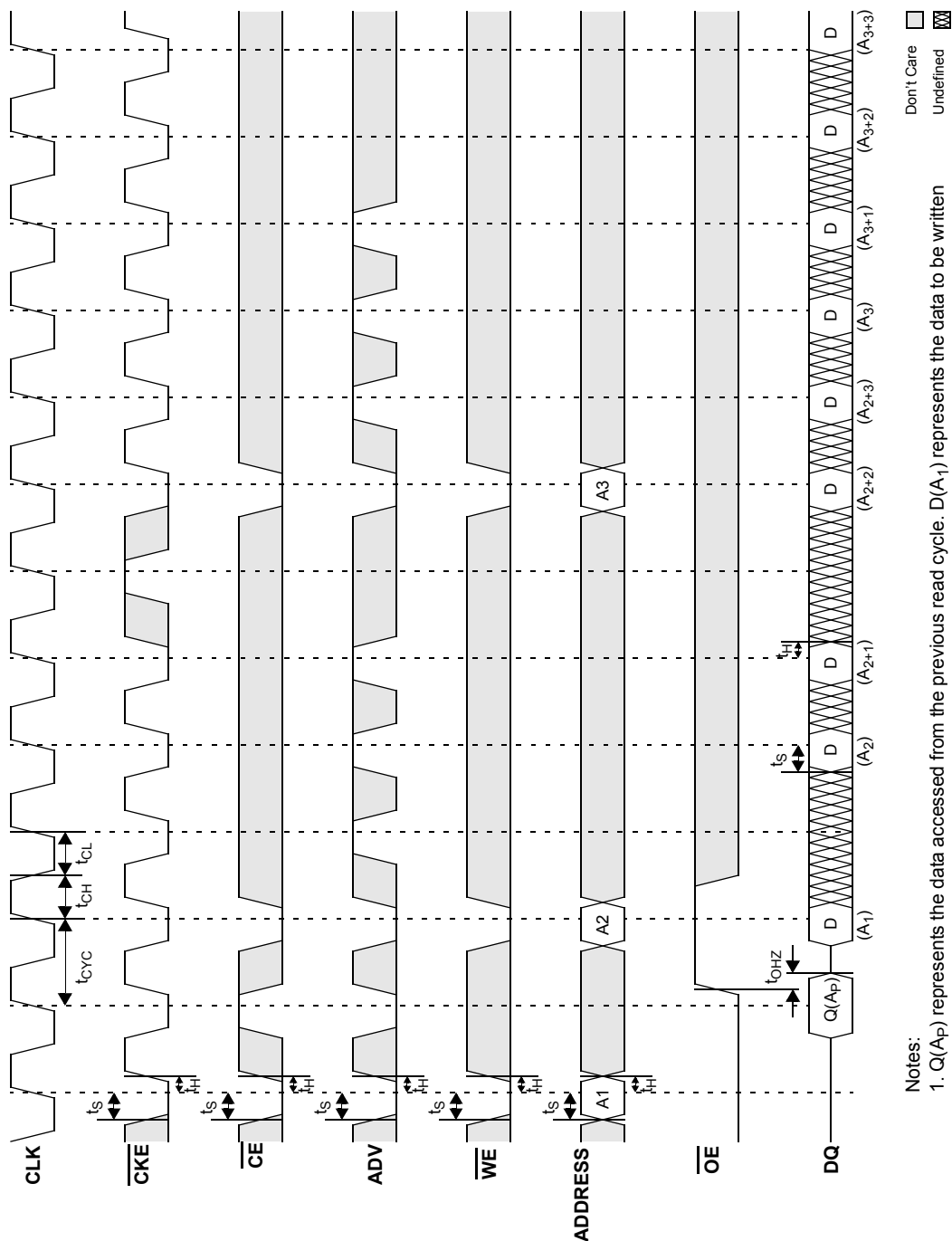
Timing Waveforms for READ Cycles - Pipeline Device



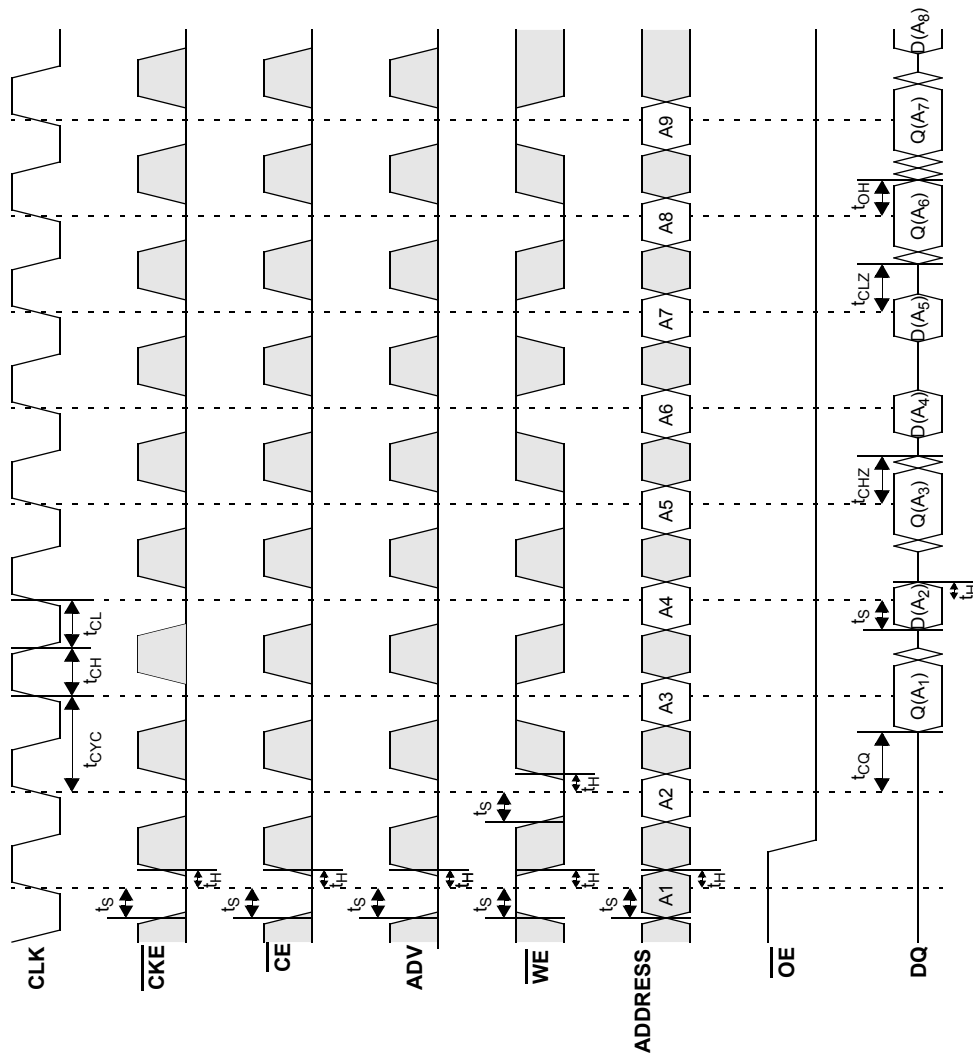
Notes:

1. Q(A₁) represents the first data accessed from address A1 in the SRAM and Q(A₂) represents the first data accessed from address A2. Q(A₂₊₁) represents the second bit accessed within the burst of address A2.
2. CE = L means CE1 = L and CE2 = H. CE = H means CE1 = H or CE2 = L or CE3 = H.

Timing Waveforms for WRITE Cycles - Pipeline Device



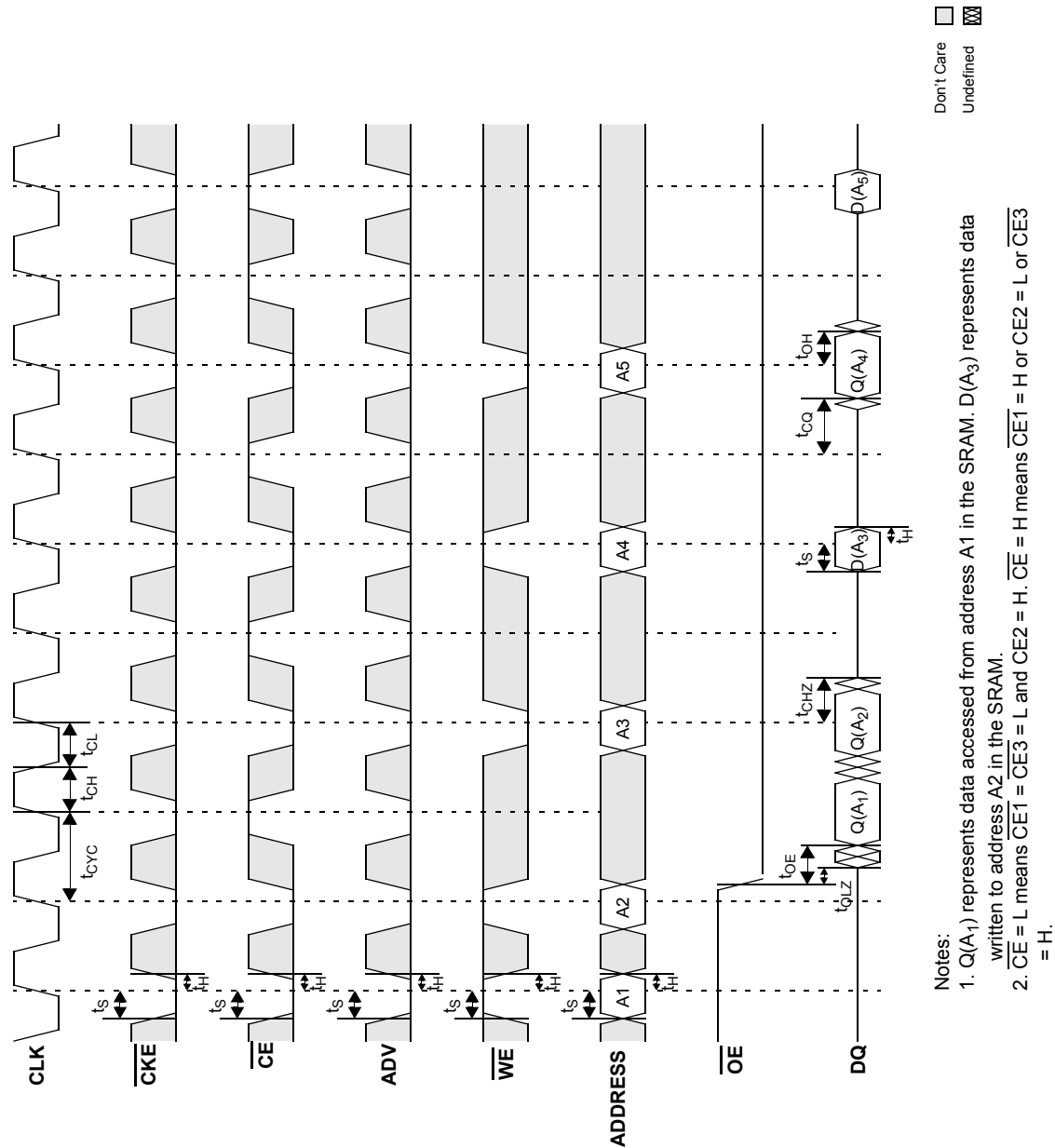
Timing Waveforms for Combined READ/WRITE Cycles - Pipeline Device



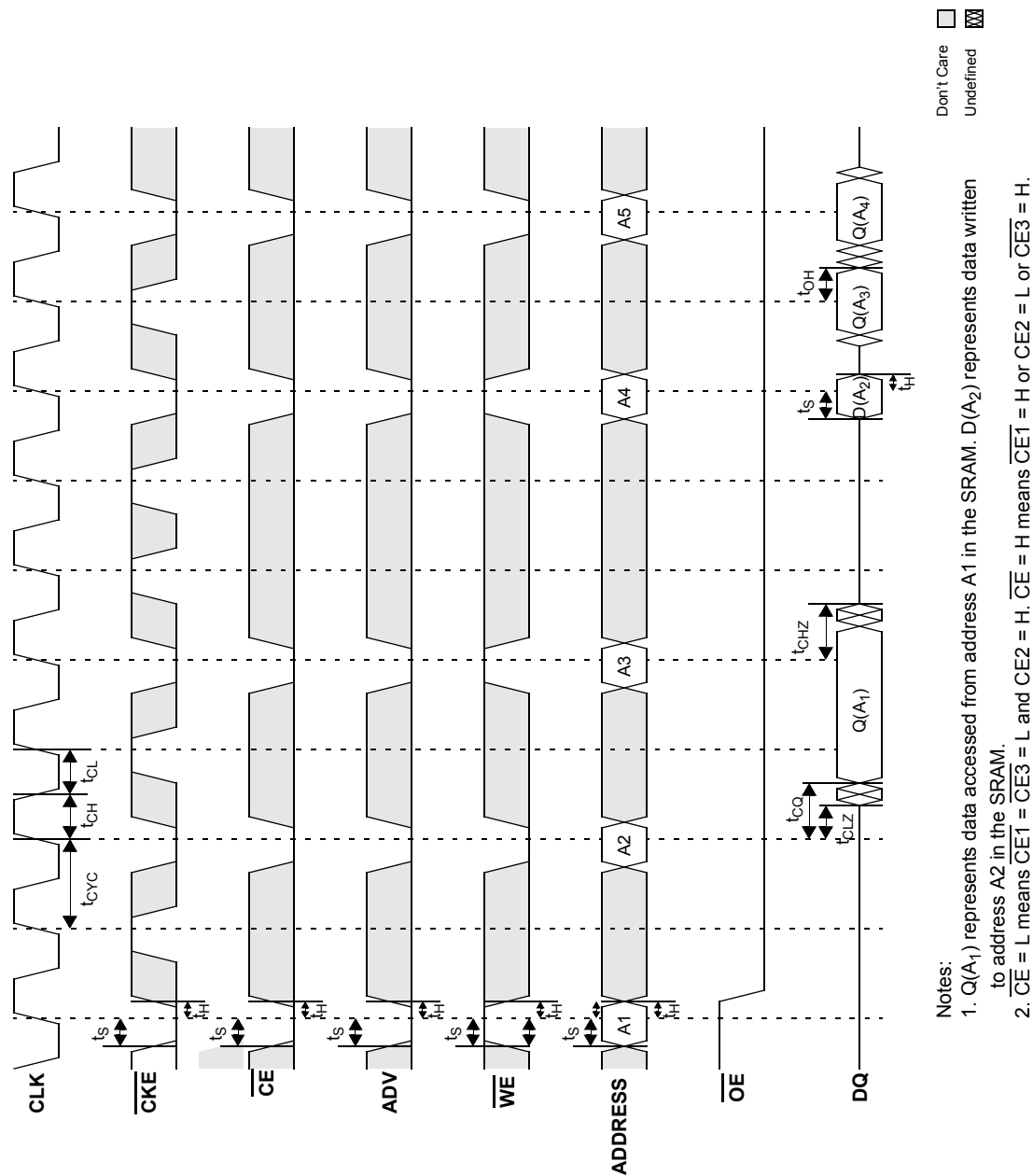
Don't Care
Undefined

- Notes:
1. $Q(A_1)$ represents the data accessed from address A1 in the SRAM. $D(A_2)$ represents data written to address A2 in the SRAM.
 2. $CE = L$ means $CE1 = L$ and $CE2 = H$. $CE = H$ means $CE1 = H$ or $CE2 = L$ or $CE3 = H$.
 3. $\overline{WE} = L$ means \overline{WE} and all \overline{BWx} are L.

Timing Waveforms for $\overline{\text{CE}}$ Operation - Pipeline Device



Timing Waveforms for $\overline{\text{CKE}}$ Operation - Pipeline Device

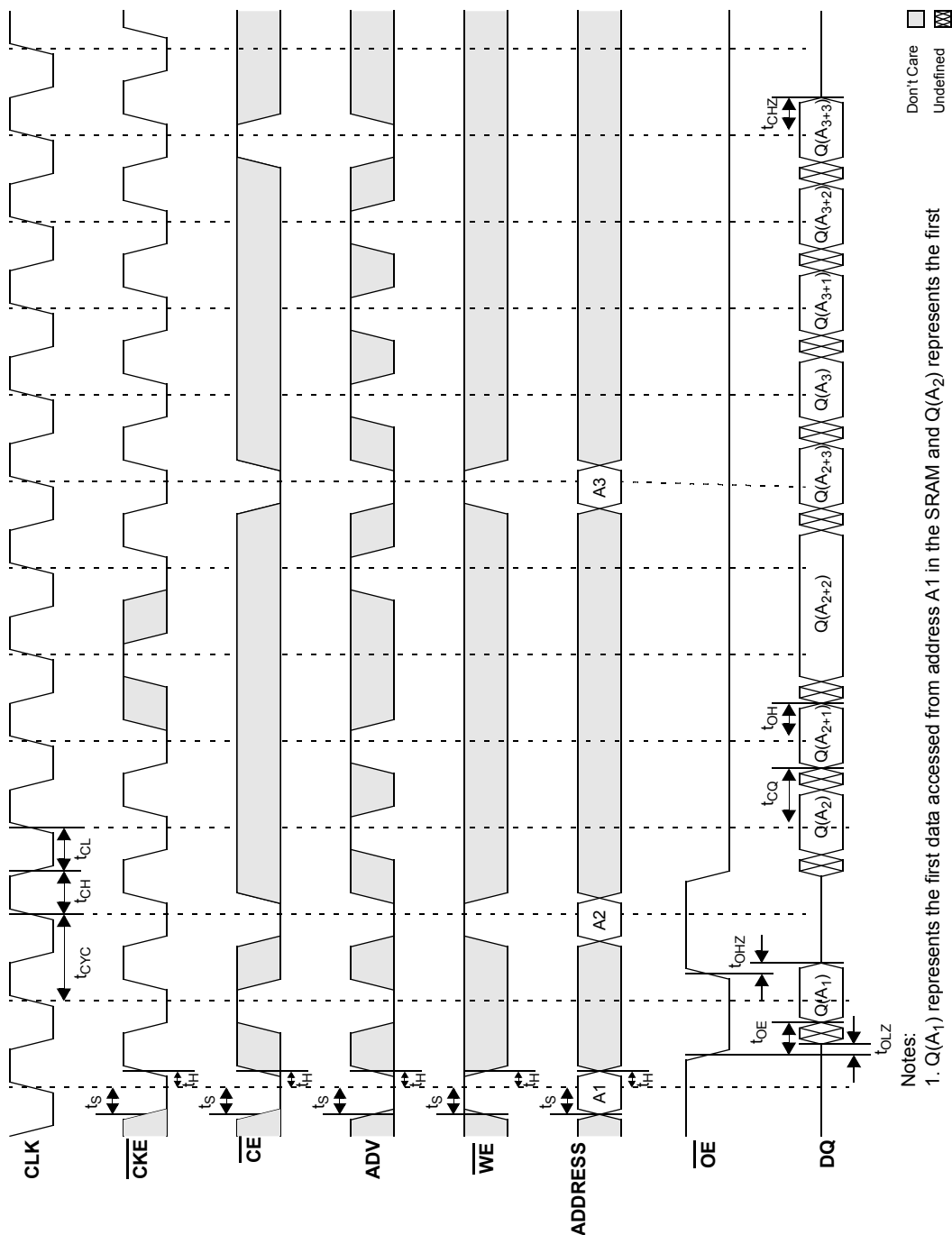


AC Timing Characteristics - Flow Thru Device

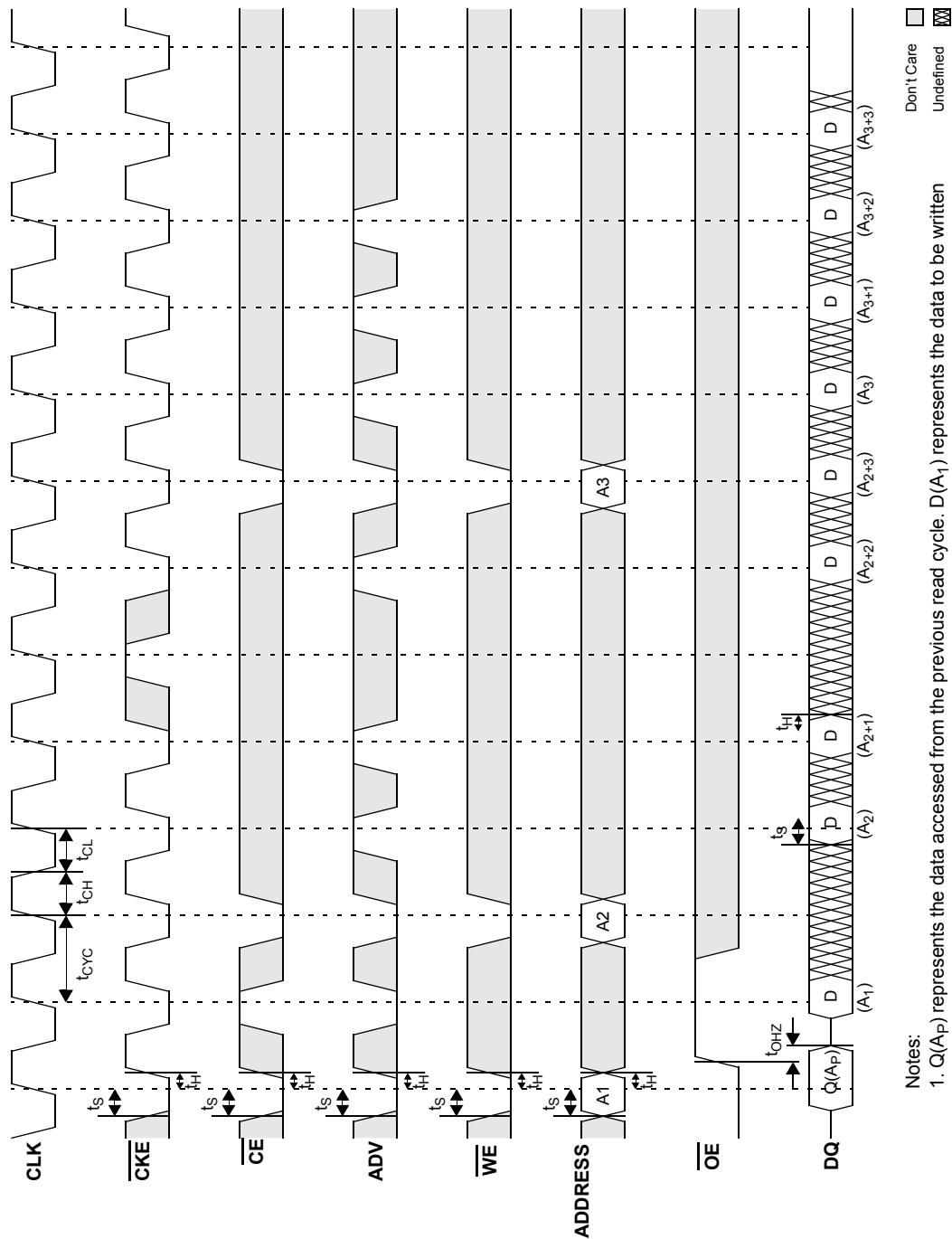
Parameter	Symbol	-25		-22		-20		-16		-15		-13		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CLOCK TIMINGS														
Clock Cycle Time	t _{CYC}	6.7		7.5		8.5		10		10		15		nS
Clock High Pulse Width	t _{CH}	2.5		2.5		3.0		3.0		3.0		3.0		nS
Clock Low Pulse Width	t _{CL}	2.5		2.5		3.0		3.0		3.0		3.0		nS
Clock Frequency	F _{MAX}		150		133		117		100		100		83	MHz
OUTPUT TIMINGS														
Clock high to output valid	t _{CQ}		6.0		6.5		7.0		8.5		10		11	nS
Output hold from clock high	t _{OH}	1.5		1.5		1.5		1.5		1.5		1.5		nS
Clock to output in low-Z ¹	t _{CLZ}	2.5		2.5		2.5		2.5		2.5		2.5		nS
Clock to output in high-Z ¹	t _{CHZ}		5.0		5.0		5.0		5.0		5.0		5.0	nS
OE low to output valid	t _{toE}		3.0		3.0		3.5		3.5		3.5		3.5	nS
OE low to output in low-Z ¹	t _{OLZ}	0		0		0		0		0		0		nS
OE high to output in high-Z ¹	t _{OHZ}		4.0		4.0		4.0		4.0		4.0		4.0	nS
SETUP AND HOLD TIMES														
Setup Time	t _S	1.5		1.5		1.5		1.5		1.5		1.5		nS
Hold Time	t _H	0.5		0.5		0.5		0.5		0.5		0.5		nS

1. t_{CLZ} , t_{CHZ} , t_{OLZ} , t_{OHZ} are specified with output load B.

Timing Waveforms for READ Cycles - Flow Thru Device







Timing Waveforms for WRITE Cycles - Flow Thru Device





The diagram shows the timing relationships for the 64K16020. The signals are: CLK (clock), CKE (clock enable), CE (chip enable), ADV (address valid), WE (write enable), ADDRESS (address), OE (output enable), and DQ (data bus). The internal data path is shown with flip-flops (Q) and buffers (D). The timing parameters are defined as follows:

- t_{CYC} : Clock cycle time
- t_{CH} : Clock high pulse width
- t_{CL} : Clock low pulse width
- t_s : Setup time
- t_H : Hold time
- t_{CQ} : Clock-to-output delay
- t_{CHZ} : Clock high-to-output delay
- t_{CHZ} : Clock high-to-output delay
- t_{CLZ} : Clock low-to-output delay
- t_{OH} : Output high delay
- t_{OL} : Output low delay
- t_u : Output delay

Don't Care		
Undefined		

Notes:

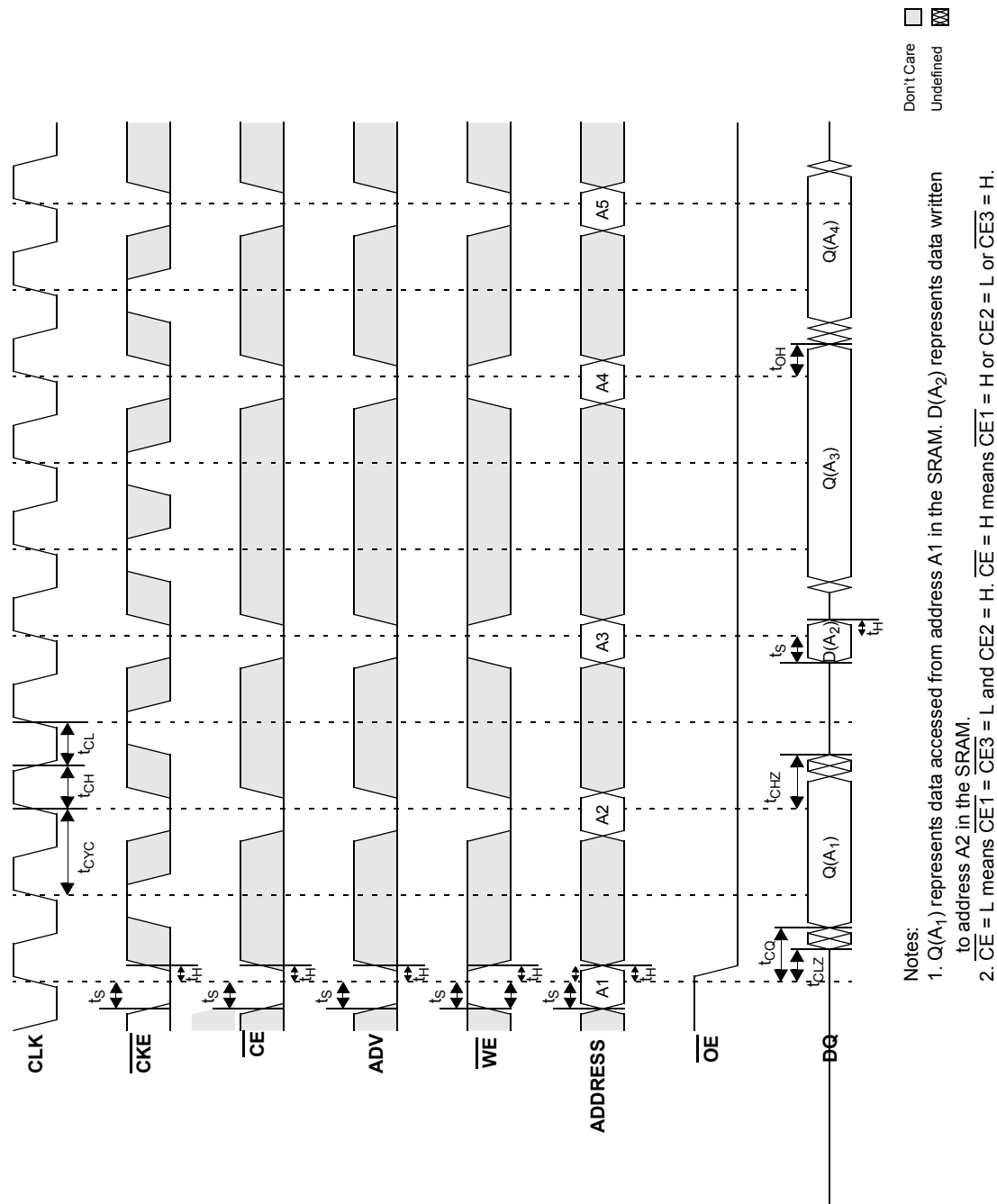
1. $Q(A_1)$ represents the data accessed from address A_1 in the SRAM. $D(A_2)$ represents data written to address A_2 in the SRAM.
2. $CE = L$ means $CE1 = CE3 = L$ and $CE2 = H$. $CE = H$ means $CE1 = H$ or $CE2 = L$ or $CE3 = H$.
3. $\overline{WE} = L$ means \overline{WE} and all \overline{BWx} are L .

Don't Care		
Undefined		

Notes:

1. $Q(A_1)$ represents data accessed from address A_1 in the SRAM. $D(A_3)$ represents data written to address A_2 in the SRAM.
2. $\overline{CE}1 = L$ means $\overline{CE}1 = \overline{CE}3 = L$ and $\overline{CE}2 = H$. $\overline{CE} = H$ means $\overline{CE}1 = H$ or $\overline{CE}2 = L$ or $\overline{CE}3 = H$.

Timing Waveforms for $\overline{\text{CKE}}$ Operation - Flow Thru Device



JTAG Serial Boundary Scan

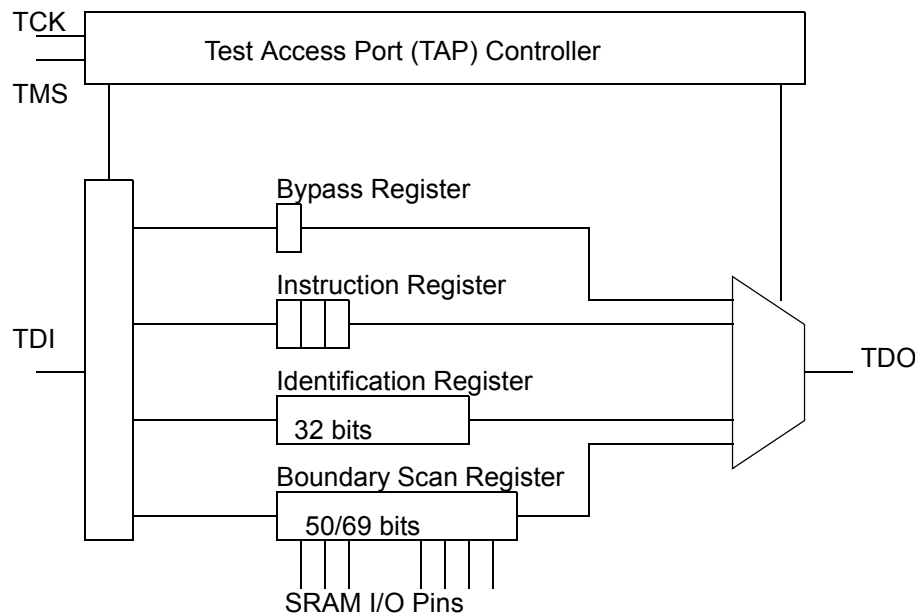
The family of SRAM devices all incorporate JTAG serial boundary scan capability in the BGA package only. This test function utilizes the test Access Port (TAP) to and operates consistent with IEEE Standard 1149.1-1900, but is not fully compliant since a subset of functions are omitted. The exclusion of these e TAP controller functions does not conflict with other 1149.1 compliant devices. This test function allows connectivity scan testing during board level debug. This JTAG port operates using standard 2.5V I/O levels.

Disabling the JTAG Feature

There are no issues with using this SRAM and not using the JTAG feature. For normal operation with the TAP controller disable, TCK, TDI and TMS should be left floating or tied to Vdd. TDO should be left unconnected.

Performing a TAP Reset

Upon power-up, the TAP controller will be in a reset state and it will not interfere with the operation of the SRAM. A reset can be entered by holding TMS at a high level for five consecutive rising edges of TCK.



JTAG Block Diagram

TAP Pin Description

Signal	Name	Type	Description
TCK	Test Clock	Input clock	Clock for all TAP events. All inputs are captured on the rising edge of TCK. All outputs are driven with the falling edge of TCK.
TMS	Test Mode Select	Input	Input for commands to theTAP controller. Sam- pled on the rising edge of TCK
TDI	Test Data-In	Input	Input for serial registers sampled on rising edge of TCK.
TDO	Test Data-Out	Output	Output of serial registers that changes on the fall- ing edge of TCK.

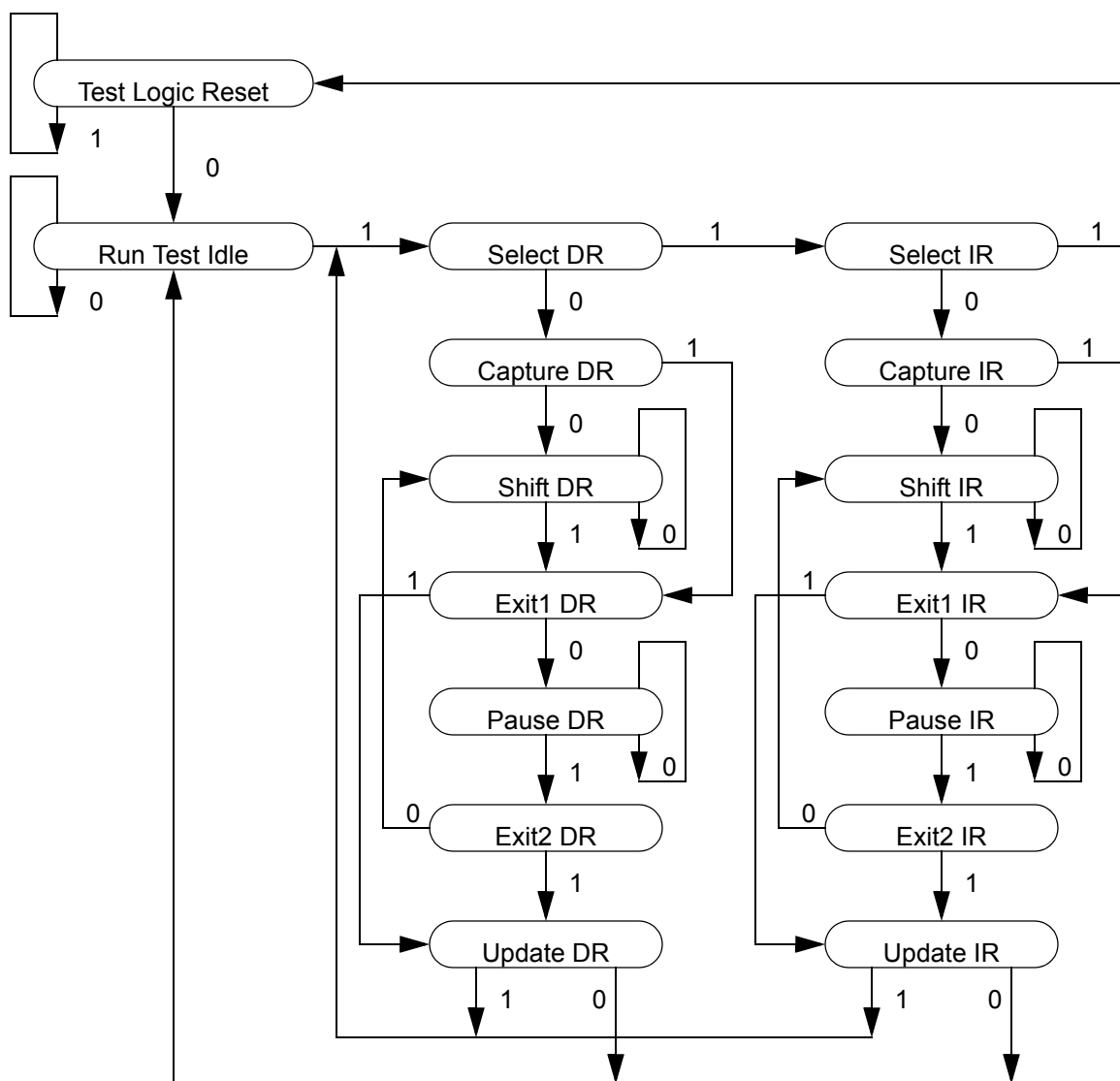
TAP Registers

Name	Length	Description
Instruction	3	Holds instruction for the TAP controller. Loaded when placed between TDI and TDO and automatically loaded with IDCODE at power-up and after a reset.
Boundary Scan	50 for x18 69 for x36	Loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state.
Identification Code	32	The ID register is loaded with a vendor-specific code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. Defined in the ID Register Definition table.
Bypass	1	Register allows serial test data to be shifted through the SRAM with minimal delay.

TAP Controller Instructions

Code	Instruction	Description	Notes
000	EXTEST	Captures I/O ring contents and places boundary scan register between TDI and TDO. Places SRAM outputs in High-Z.	
001	IDCODE	Loads ID register and places it between TDI and TDO.	
010	SAMPLE-Z	Captures I/O ring contents and places boundary scan register between TDI and TDO. Places SRAM outputs in High-Z.	
011	Reserved	Reserved for future, do not use.	
100	SAMPLE/ PRELOAD	Captures I/O ring contents and places boundary scan register between TDI and TDO. Does not implement the preload function.	
101	Reserved	Reserved for future, do not use.	
110	Reserved	Reserved for future, do not use.	
111	BYPASS	Places the bypass register between TDI and TDO.	

TAP Controller State Diagram



Identification Register Description

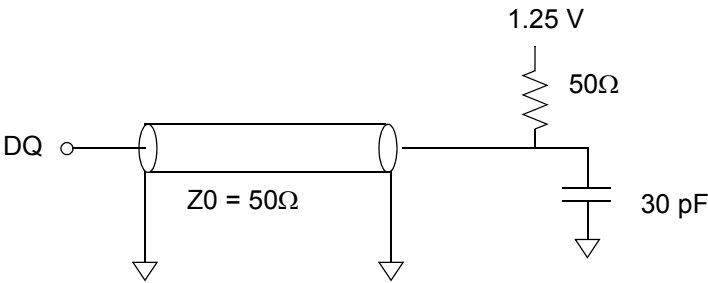
Device	Die Rev 31... 28	Device Config Id 27... 18	Not Used 17... 12	JEDEC ID Code 11... 1	Presence Register 0
512Kb x 72	0000	00111 00101	XXXXXX	00111100010	1
1Mb x 36	0000	01000 00100	XXXXXX	00111100010	1
2Mb x18	0000	01001 00011	XXXXXX	00111100010	1

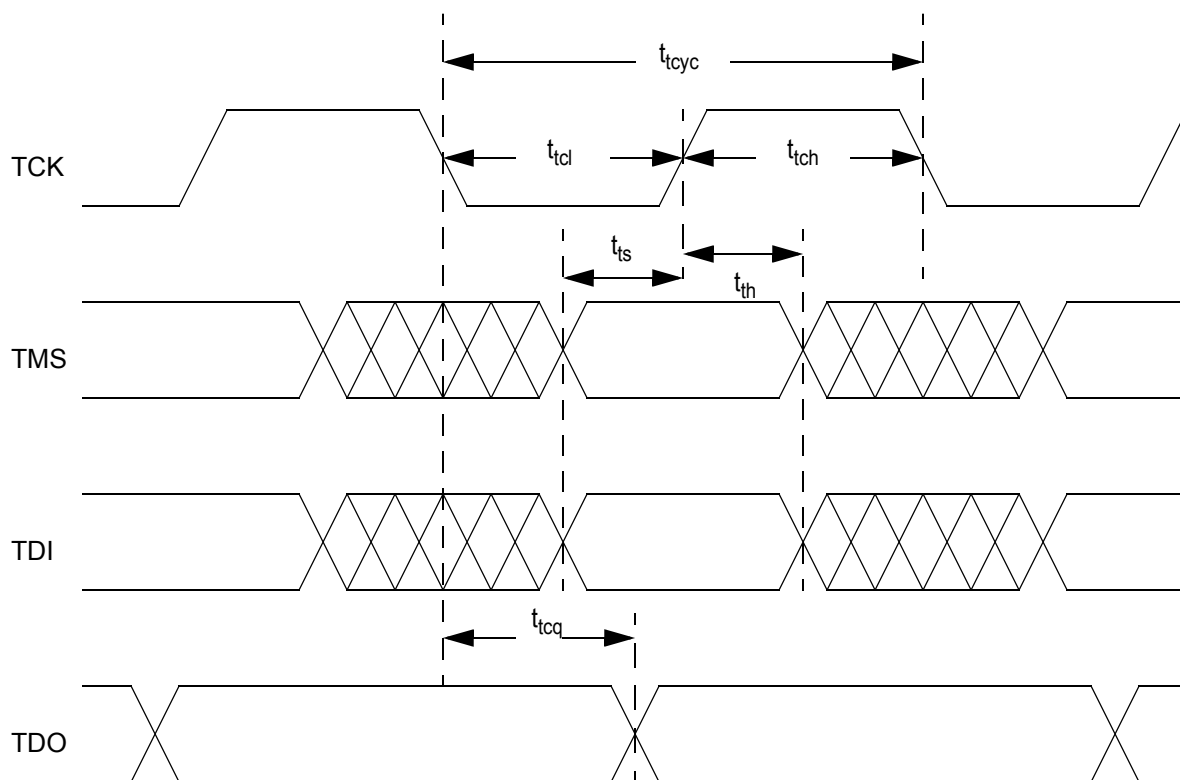
TAP DC Operating Conditions

Parameter	Symbol	Min	Max	Unit	Notes
Input High Level	V_{IHT}	1.7	$V_{DD} + 0.3$	V	
Input Low Level	V_{ILT}	-0.3	0.7	V	
Output High Level	V_{OHT}	2.0	-	V	
Output Low Level	O_{ILT}	-	0.4	V	
Input Leakage Current	I_{LIT}	tbd	tbd		
Output Leakage Current	I_{LOT}	tbd	tbd		

TAP AC Test Conditions

Parameter	Conditions
Input High Level	2.3 V
Input Low Level	0.2 V
Input Slew Rate	1 V / nS
Input and Output Reference Level	1.25 V

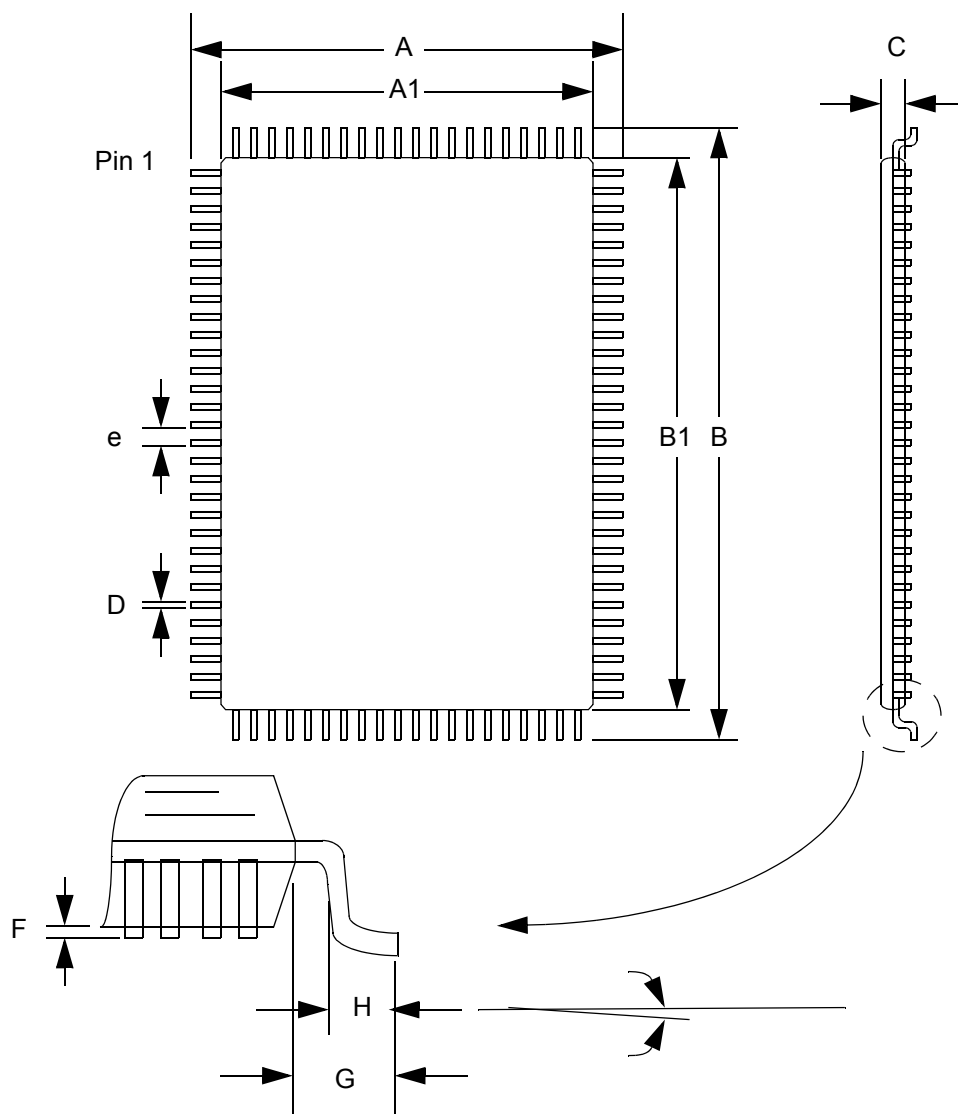




TAP AC Timing Characteristics

Parameter	Symbol	Min	Max	Units
TCK Cycle Time	t_{tcyc}	100	-	nS
TCK High Pulse Width	t_{tch}	40	-	nS
TCK Low Pulse Width	t_{tcl}	40	-	nS
TMS / TDI Setup Time	t_{ts}	10	-	nS
TMS / TDI Hold Time	t_{th}	10	-	nS
TCK Low to Output Valid	t_{tcq}	-	20	nS

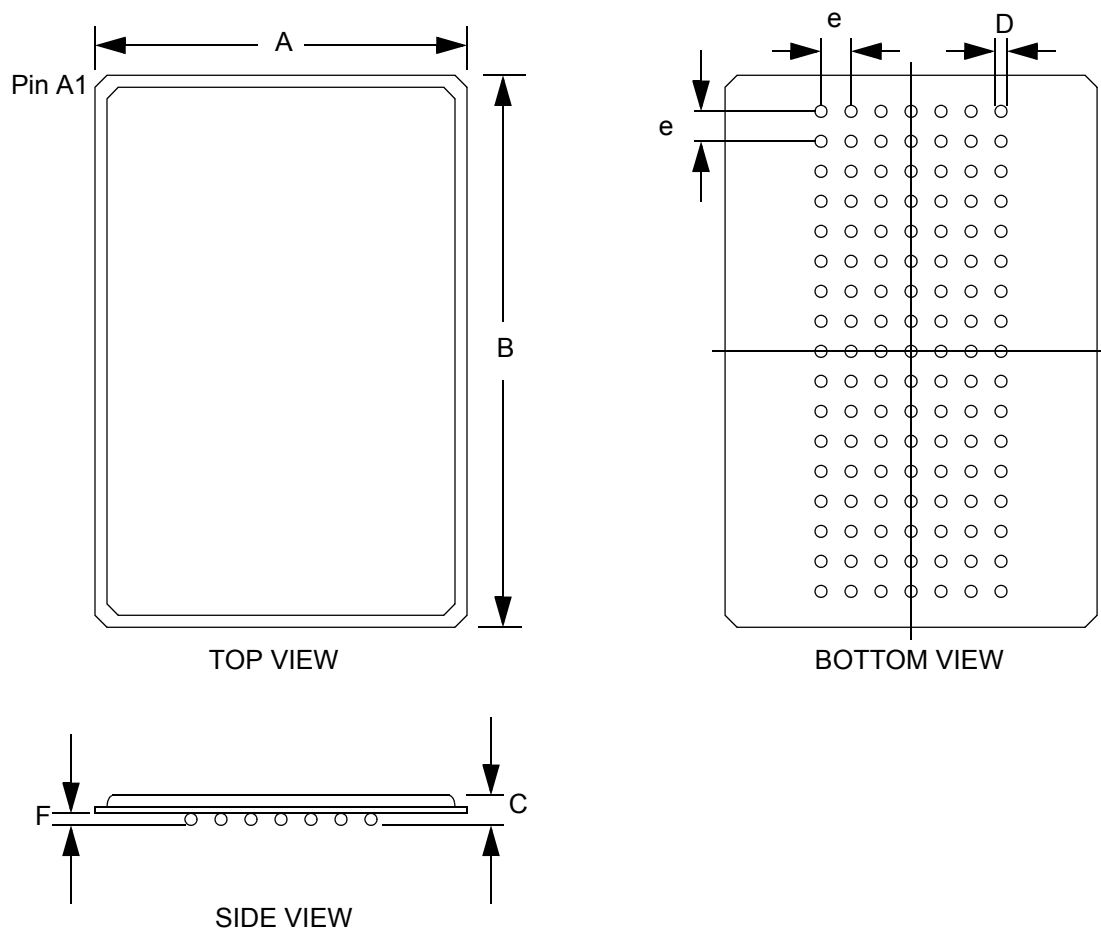
100-Pin LQFP Package Dimensions



All dimensions in mm

Symbol	Description	Min	Nom	Max	Notes
A	Overall Width		16.00		BSC
A1	Width (Package)		14.00		BSC
B	Overall Length	21.95	22.00	22.20	BSC
B1	Length (Package)	20.00			BSC
C	Package Height			1.60	
D	Lead Width	0.22	0.30	0.38	
E	Lead Pitch		0.65		BSC
F	Standoff	0.05		0.15	
G	Lead Extension		1.00		
H	Lead Bend Length	0.45	0.60	0.75	

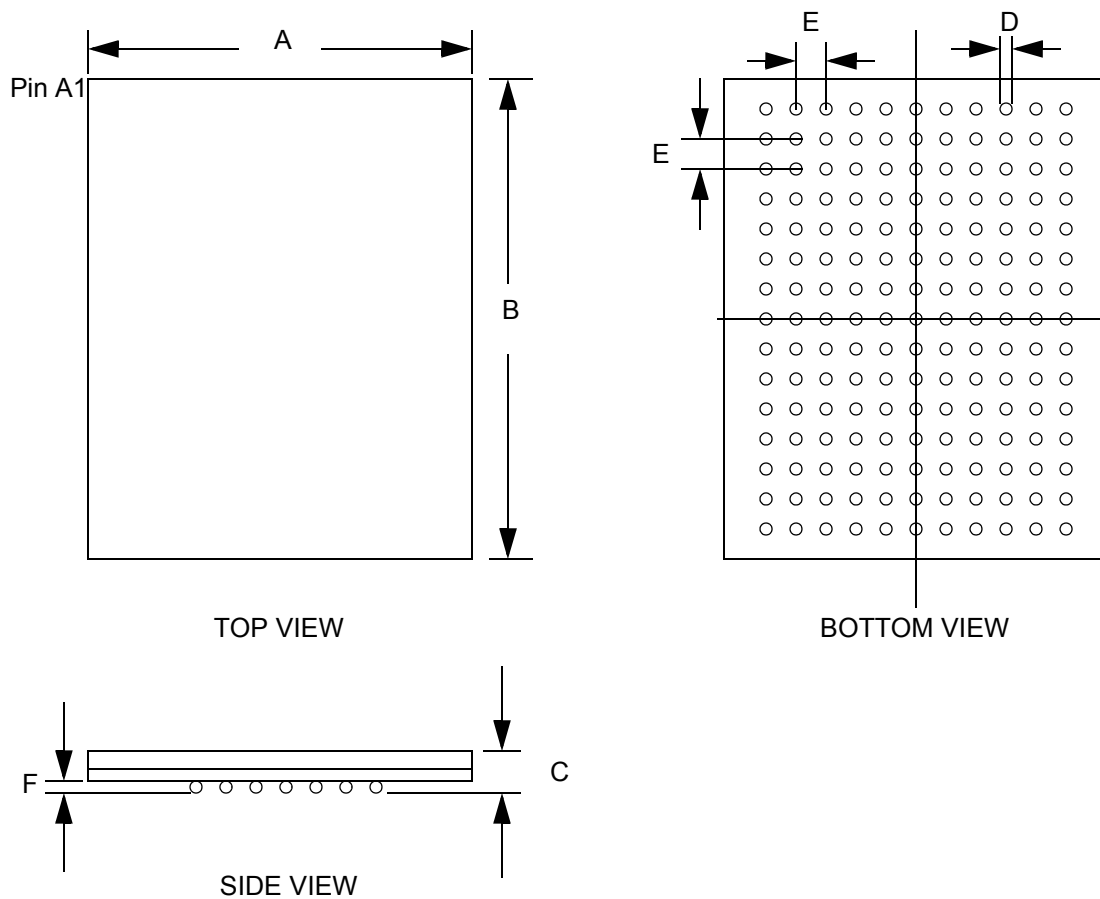
119-Pin BGA Package Dimensions



All Dimensions in mm

Symbol	Description	Min	Nom	Max
A	Package Width	13.80	14.00	14.20
B	Package Length	21.80	22.00	22.20
C	Package Height	1.93	2.06	2.19
D	Ball Diameter		0.75	
e	Ball Pitch		1.27	
F	Ball Height	0.50	0.60	0.70

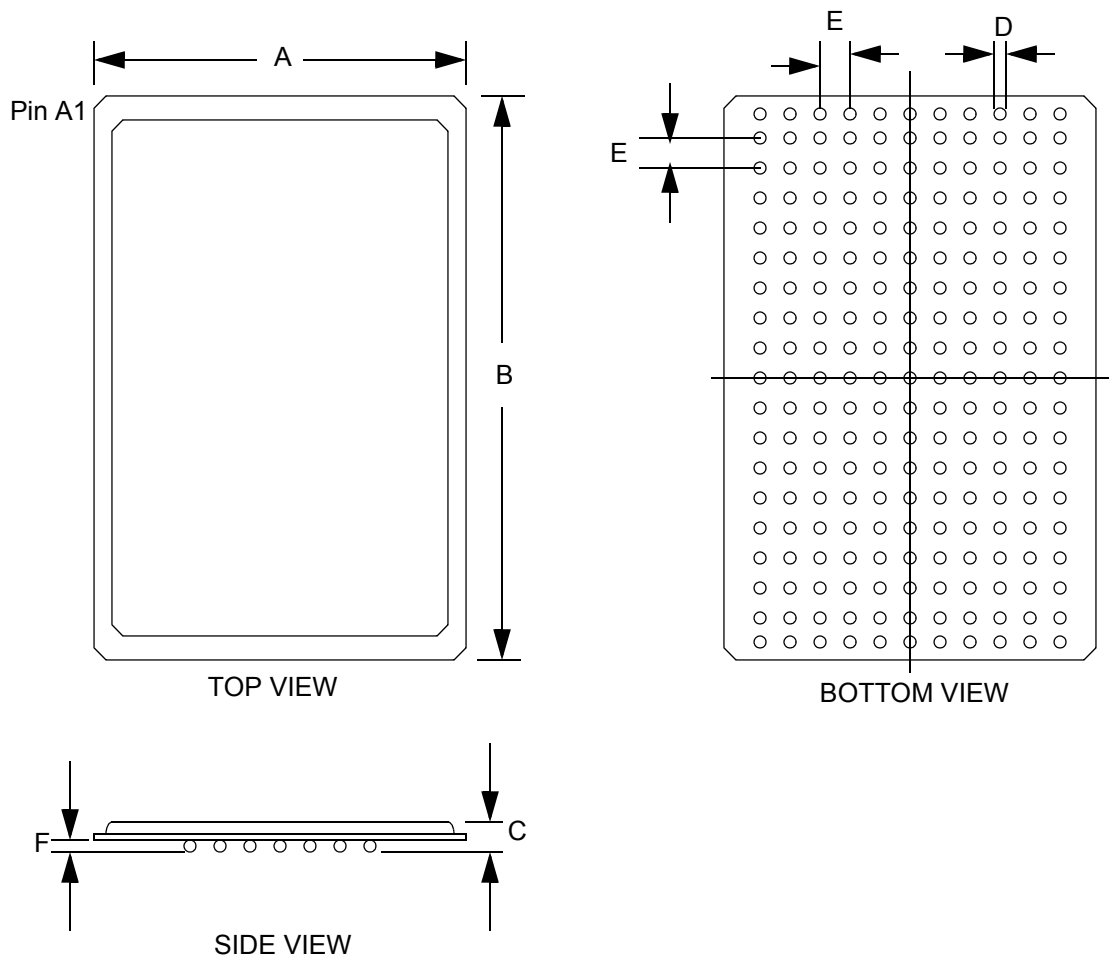
165-Ball FPBGA Package Dimensions



All Dimensions in mm

Symbol	Description	Min	Nom	Max
A	Package Width	14.90	15.00	15.10
B	Package Length	16.90	17.00	17.10
C	Package Height			1.20
D	Ball Width	0.40	0.45	0.50
E	Ball Pitch		1.00	
F	Ball Height	0.30	0.35	0.40

209-Ball PBGA Package Dimensions



All Dimensions in mm

Symbol	Description	Min	Nom	Max
A	Package Width	13.80	14.00	14.20
B	Package Length	21.80	22.00	22.20
C	Package Height			2.20
D	Ball Width	0.50	0.60	0.70
E	Ball Pitch		1.00	
F	Ball Height	0.40	0.50	0.60

Ordering Information

N36Nxx3WyyAz- ##C

Valid Part Number	I/O		Operating Mode		Package		Performance Options
	xx	I/O	yy	Mode	Z	Package	##
N36N183WP1AQ-	18	x18	P1	Pipeline	Q	100-TQFP	13, 15, 16, 20, 22, 25, 30
N36N363WP1AQ-	36	x36					
N36N183WF1AQ-	18	x18	F1	Flow-thru			67, 10, 11, 13, 15
N36N363WF1AQ-	36	x36					
N36N183WPFAG-	18	x18	PF	Pipeline or Flow-Thru	G	119-BGA	13, 15, 16, 20, 22, 25, 30
N36N363WPFAG-	36	x36					
N36N183WPF AF-	18	x18			F	165-FPBGA	
N36N363WPF AF-	36	x36					13, 15, 16, 20, 22, 25
N36N723WPFAX-	72	x72			X	209-PBGA	

Revision History

Revision #	Date	Change Description
A	October 2002	Initial 36Mb Combined Device Release
B	May 2003	Updated part number and ordering information