

## SWITCHING

## N-CHANNEL POWER MOS FET

### DESCRIPTION

The 2SK3943 is N-channel MOS Field Effect Transistor designed for high current switching applications.

### ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3943-ZP	TO-263 (MP-25ZP)

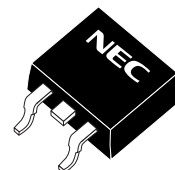
### FEATURES

- Super low on-state resistance

$R_{DS(on)1} = 3.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 41 \text{ A)}$

- Low  $C_{iss}$ :  $C_{iss} = 5800 \text{ pF TYP.}$

(TO-263)



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	40	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 82$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 328$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	104	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	185	mJ
Repetitive Avalanche Current <sup>Note3</sup>	$I_{AR}$	43	A
Repetitive Avalanche Energy <sup>Note3</sup>	$E_{AR}$	185	mJ

**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 20 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$ ,  $L = 100 \mu\text{H}$

**3.**  $T_{ch(peak)} \leq 150^\circ\text{C}$ ,  $R_G = 25 \Omega$

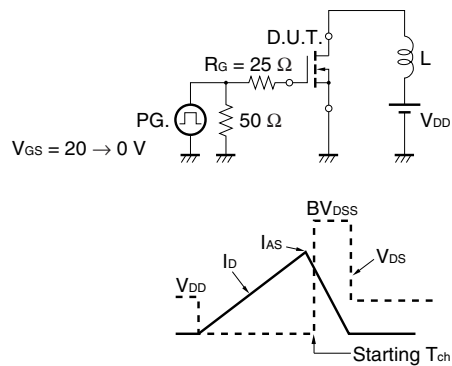
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# ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

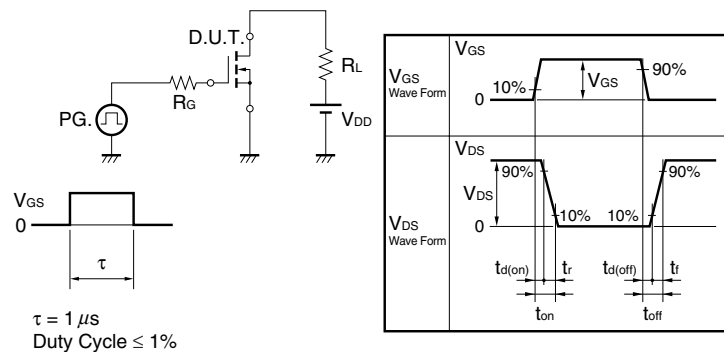
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1.0	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.0	2.5	3.0	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 41 A	21	43		S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 41 A		2.9	3.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 5.5 V, I <sub>D</sub> = 41 A		3.8	5.6	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		5800		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		860		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		510		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 41 A		29		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		10		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		69		ns
Fall Time	t <sub>f</sub>			12		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 32 V		93		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		28		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 82 A		28		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)1</sub>	I <sub>F</sub> = 60 A, V <sub>GS</sub> = 0 V		0.88	1.2	V
	V <sub>F(S-D)2</sub>	I <sub>F</sub> = 82 A, V <sub>GS</sub> = 0 V		0.92	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 82 A, V <sub>GS</sub> = 0 V		40		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		49		nC

**Note** Pulsed

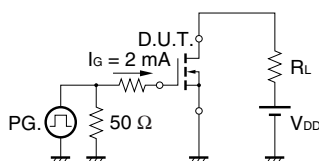
## TEST CIRCUIT 1 AVALANCHE CAPABILITY



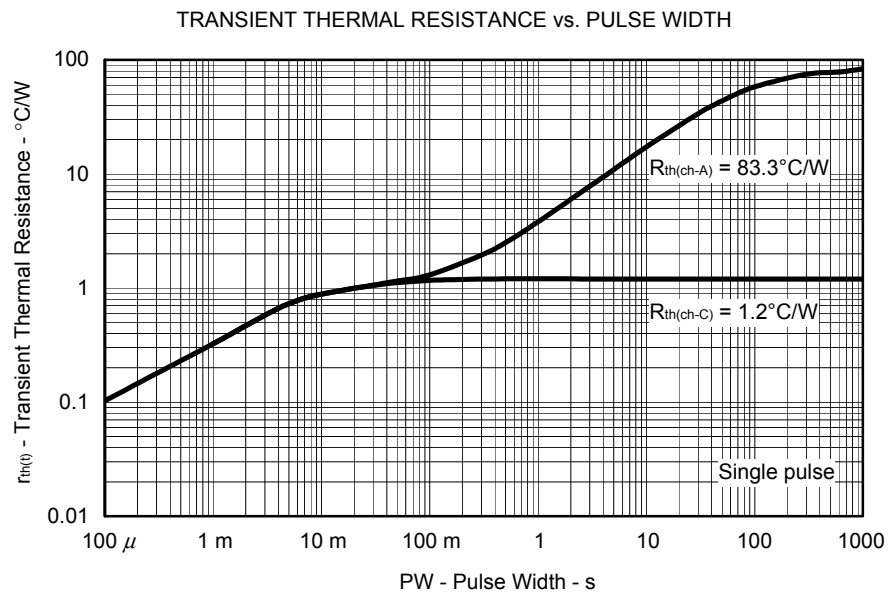
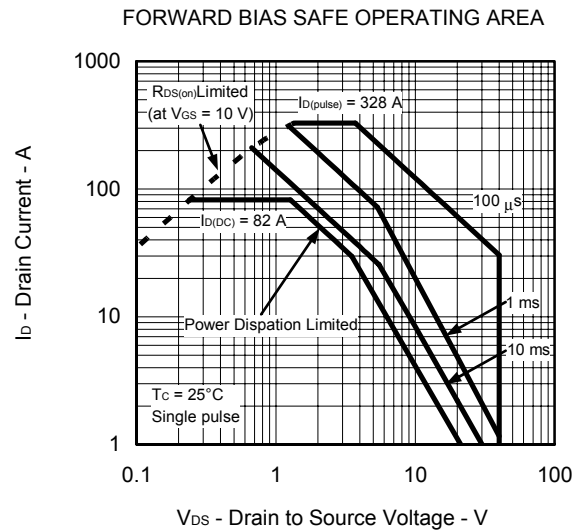
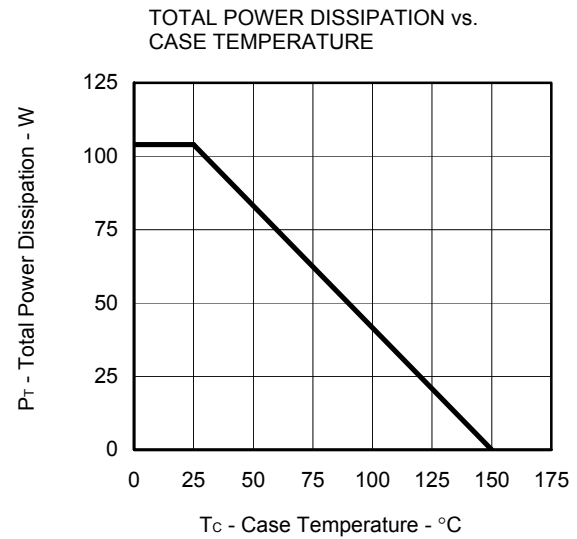
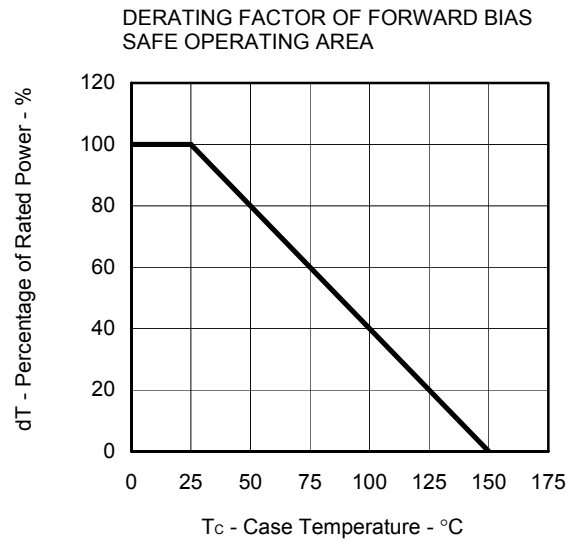
## TEST CIRCUIT 2 SWITCHING TIME



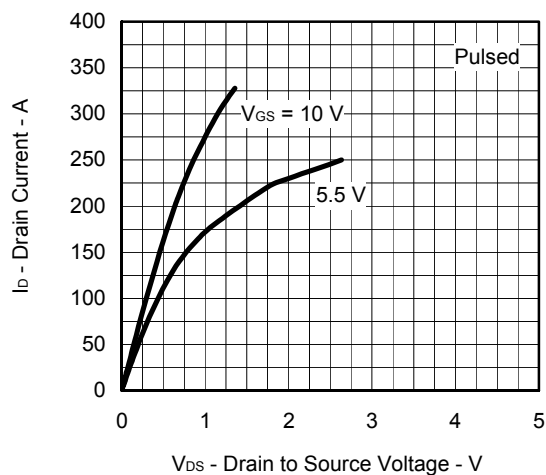
## TEST CIRCUIT 3 GATE CHARGE



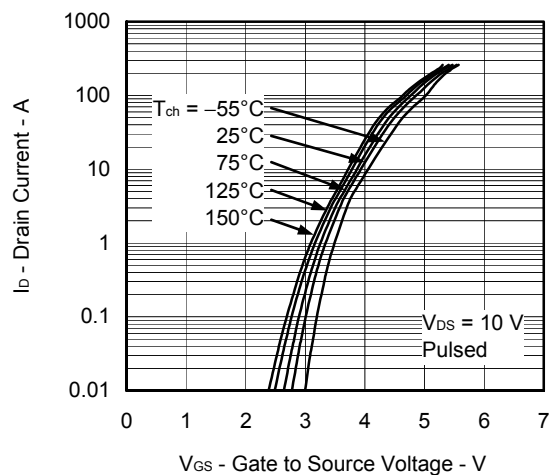
TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



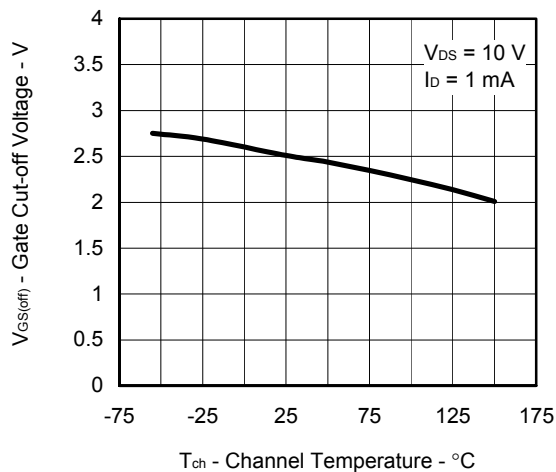
DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE



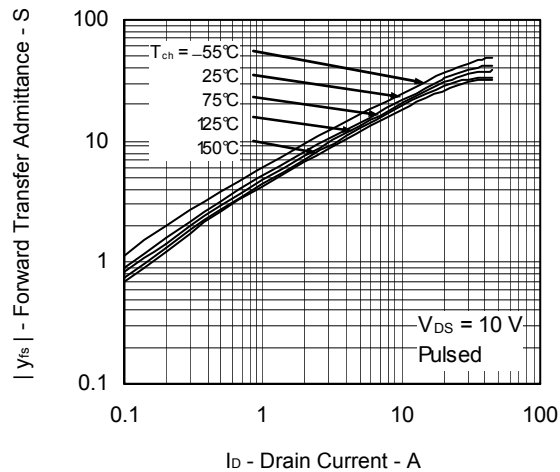
FORWARD TRANSFER CHARACTERISTICS



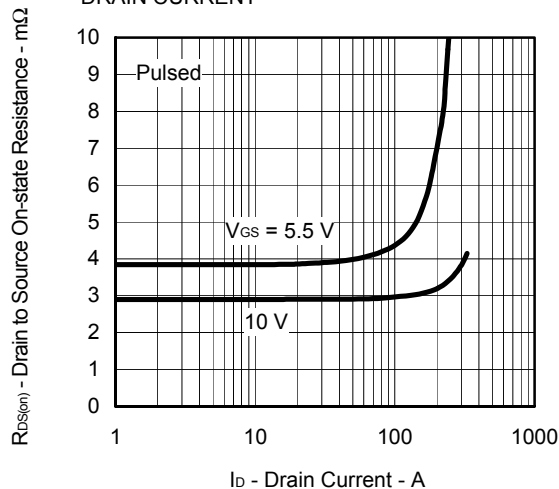
GATE CUT-OFF VOLTAGE vs.  
CHANNEL TEMPERATURE



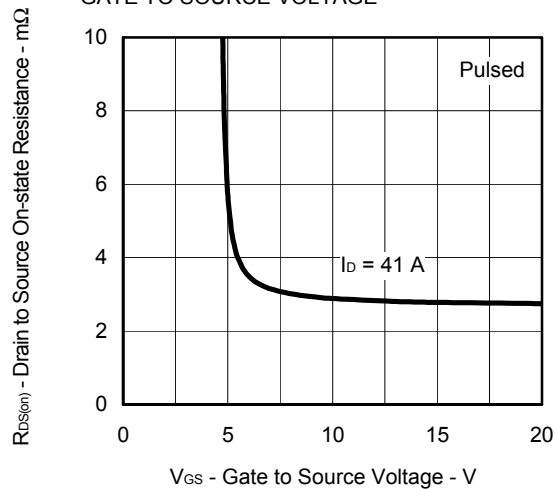
FORWARD TRANSFER ADMITTANCE vs.  
DRAIN CURRENT



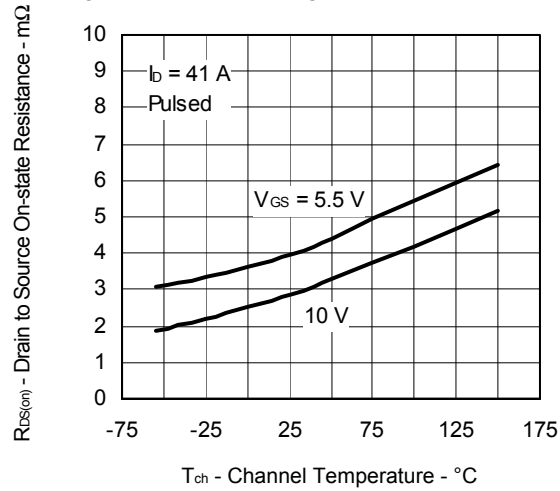
DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
DRAIN CURRENT



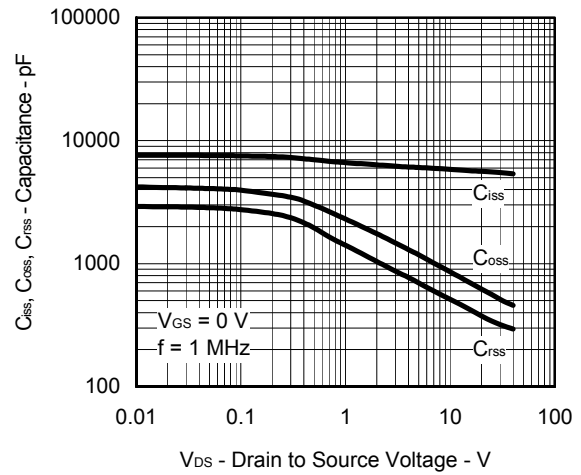
DRAIN TO SOURCE ON-STATE RESISTANCE vs.  
GATE TO SOURCE VOLTAGE



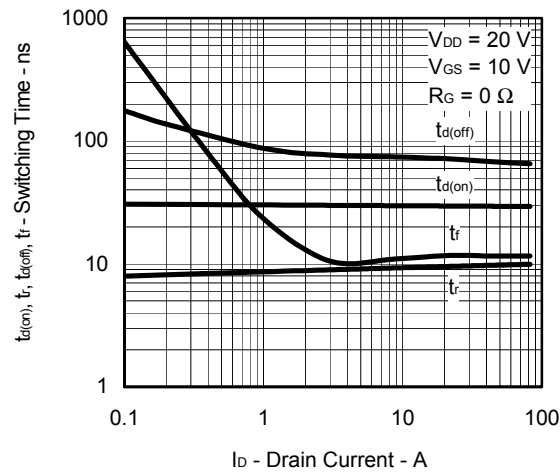
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



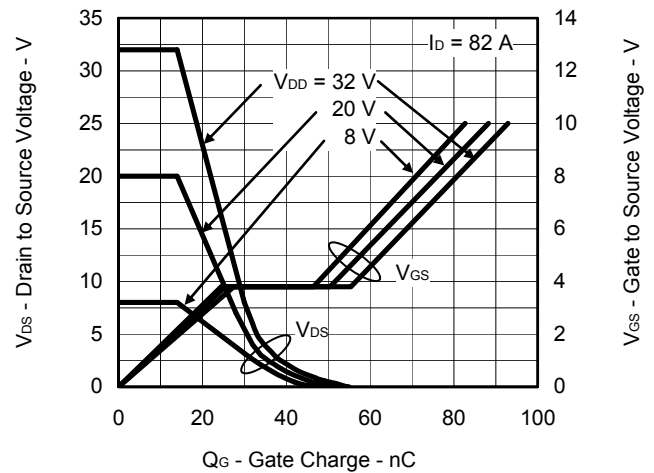
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



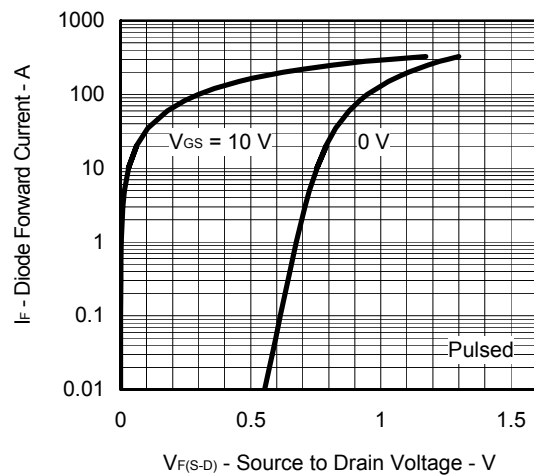
SWITCHING CHARACTERISTICS



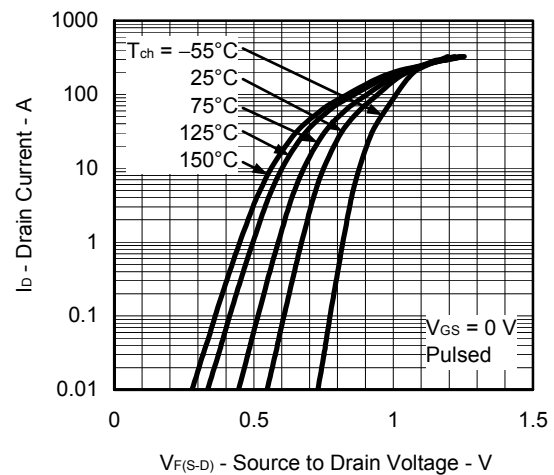
DYNAMIC INPUT/OUTPUT CHARACTERISTICS

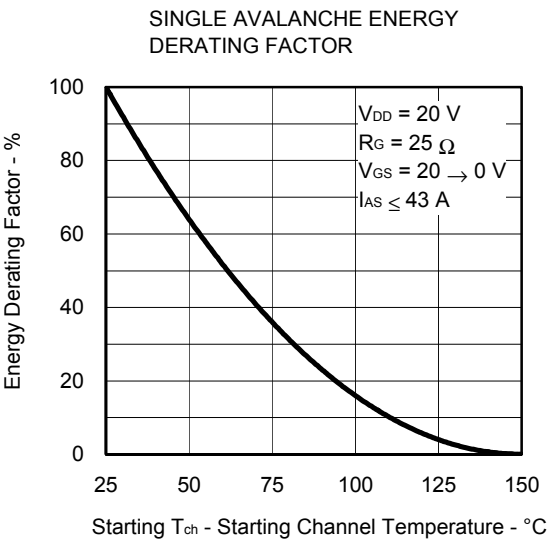
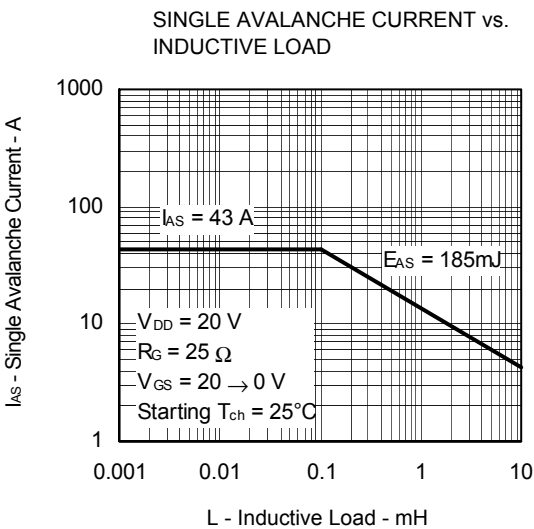
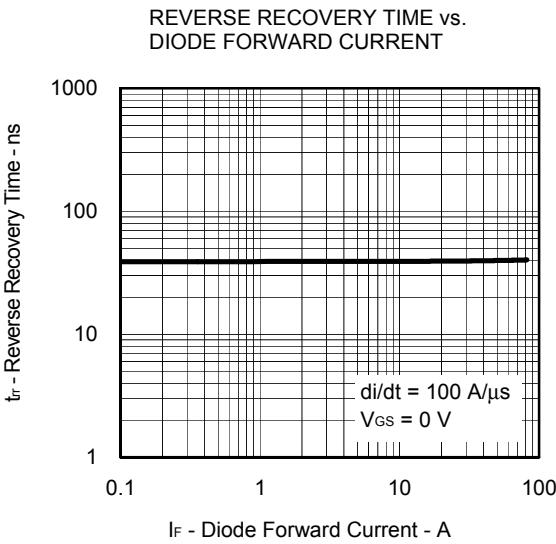


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



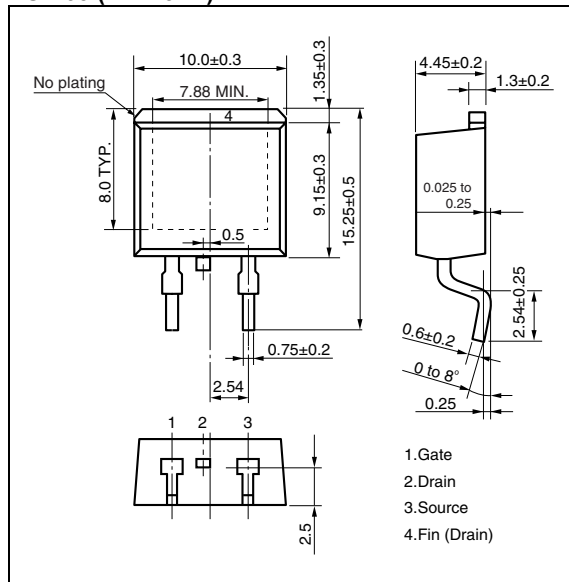
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



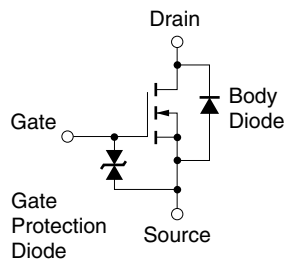


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.  
When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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