

MOS INTEGRATED CIRCUIT MC-454AC724

4 M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE UNBUFFERED TYPE

Description

The MC-454AC724 is a 4,194,304 words by 72 bits synchronous dynamic RAM module on which 18 pieces of 16 M SDRAM : μ PD4516821 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 4,194,304 words by 72 bits organization (ECC type)
- Clock frequency and Clock access time

Family	/CAS latency	Clock frequency (MAX.)	Clock access time (MAX.)	Power consumption (MAX.)	
				Active	Standby
MC-454AD644-A10	CL = 3	100 MHz	8 ns	5,119 mW	129.6 mW (CMOS level input)
	CL = 2	67 MHz	9 ns		
MC-454AD644-A67	CL = 3	67 MHz	9 ns	4,536 mW	
	CL = 2		9 ns		
MC-454AD644-A12	CL = 3	83 MHz	9 ns	4,471 mW	
	CL = 2	54 MHz	12 ns		

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Dual internal banks controlled by BA0 (Bank Select)
- ★ Programmable burst-length : 1, 2, 4, 8 and Full Page
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- Single +3.3 V ± 0.3 V power supply
- LVTTTL compatible
- 2,048 refresh cycles / 32 ms
- Burst termination by Burst Stop command and Precharge command
- All I/Os have $10\Omega \pm 10\%$ of series resistor
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Unbuffered type
- Serial PD

The information in this document is subject to change without notice.

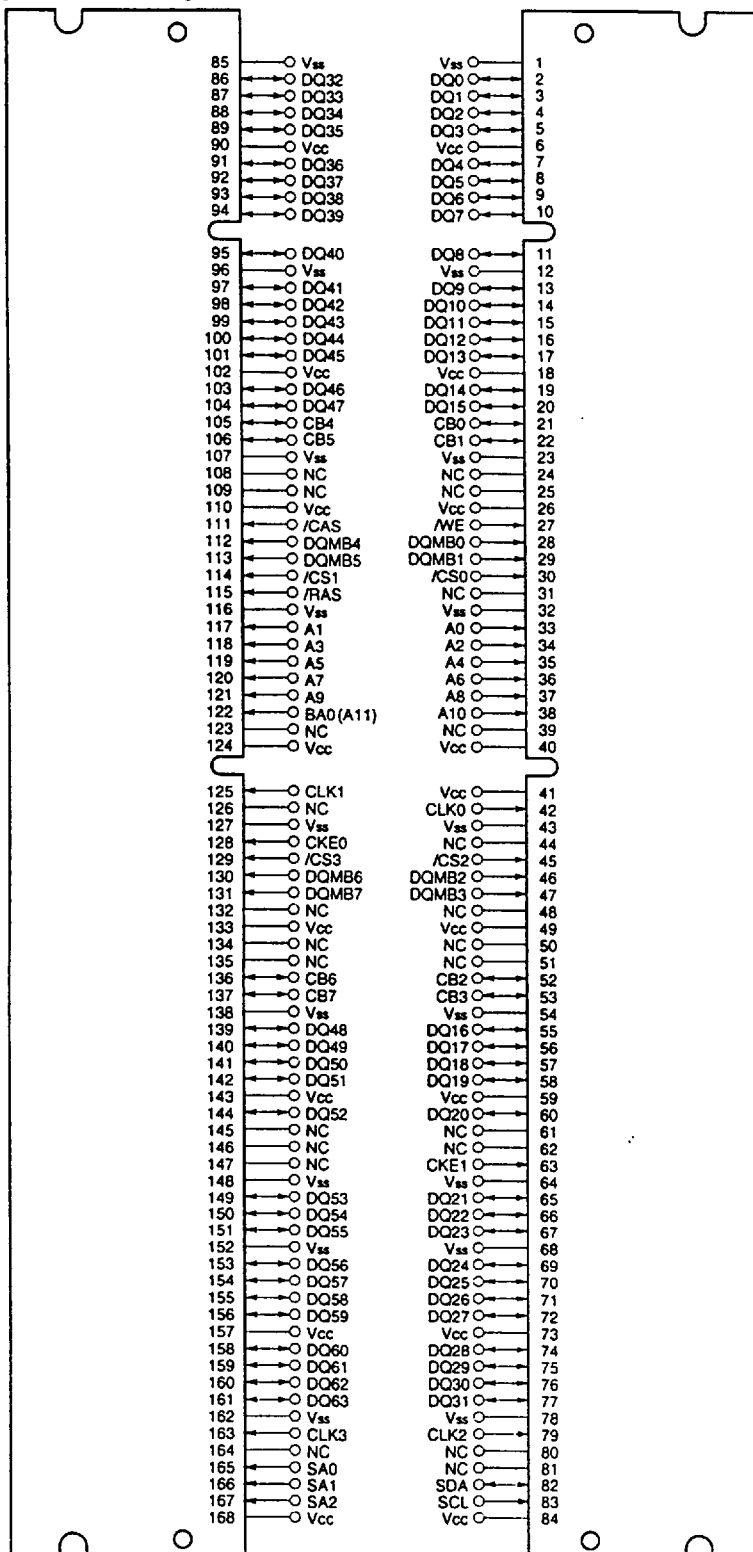
Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-454AC724F-A10	100 MHz	168-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated 29.21 mm (1.15 inch) height	18 pieces of μ PD4516821G5 (400 mil TSOP (II)) [Double side]
MC-454AC724F-A67	67 MHz		18 pieces of μ PD4516821G5-PC (400 mil TSOP (II)) SDRAM Lite [Double side]
MC-454AC724F-A12	83 MHz		18 pieces of μ PD4516821G5 (400 mil TSOP (II)) [Double side]

Pin Configuration

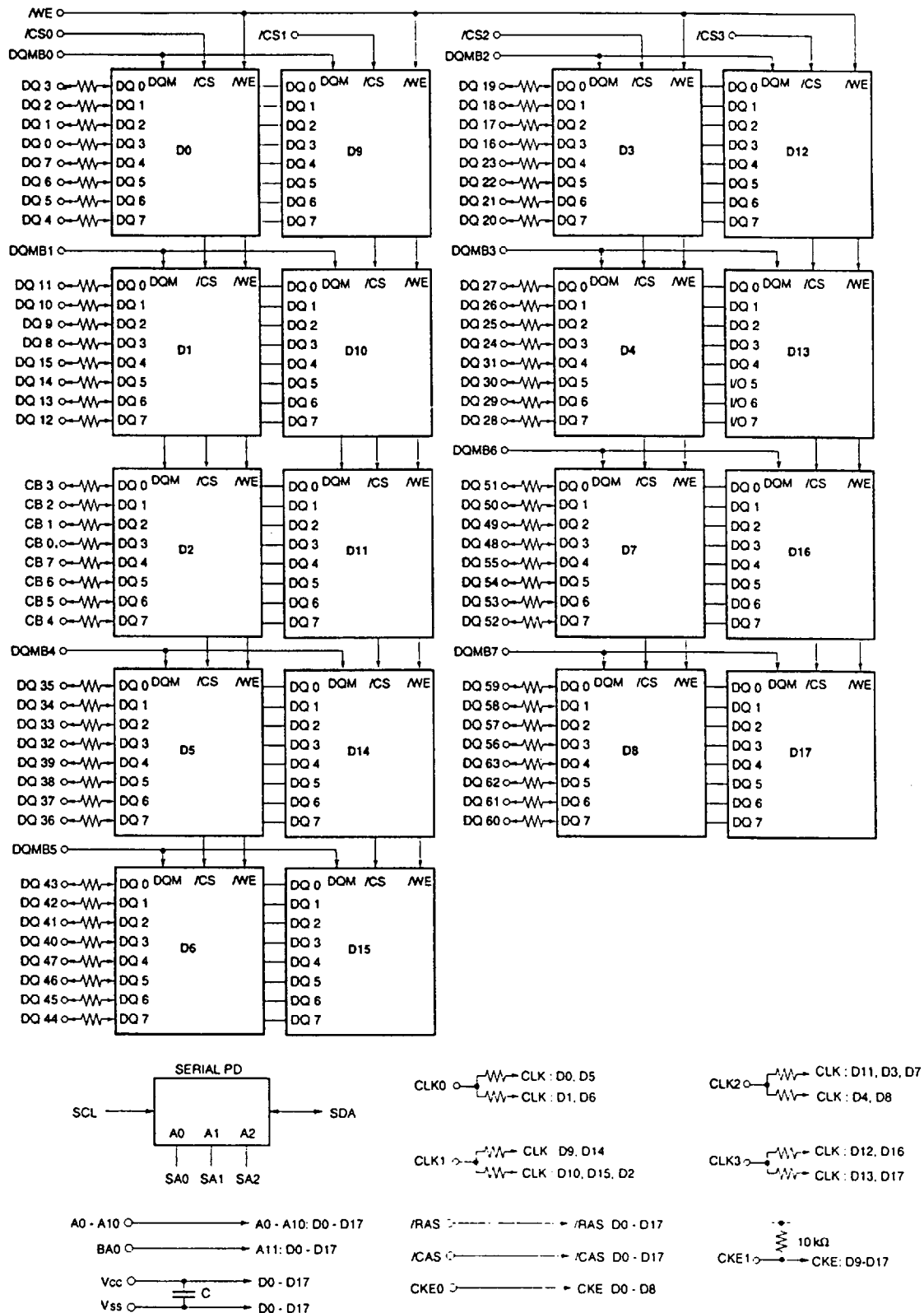
168-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plated)

[MC-454AC724F]



- A0 - A10 : Address Inputs
- [Row : A0 - A10, Column : A0 - A8]
- BA0 (A11) : SDRAM Bank Select
- DQ0 - DQ63, CB0 - CB7 : Data Inputs/Outputs
- CLK0 - CLK3 : Clock Input
- CKE0, CKE1 : Clock Enable Input
- /CS0 - /CS3 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SA0 - SA2 : Address Input for EEPROM
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- V_{cc} : Power Supply
- V_{ss} : Ground
- NC : No Connection

Block Diagram



Remarks 1. The value of all resistors is 10 Ω except CKE1.

2. D0 - D17 : μPD4516821 (1M word x 8 words x 2 banks)

Electrical Specifications (Preliminary)

- All voltages are referenced to Vss (GND).
- After power up, wait more than 100 μ s and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	Vcc		- 1.0 to +4.6	V
Voltage on input pin relative to GND	V _I		- 1.0 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		18	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		- 55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		4.6	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A10, BA0(A11), /RAS, /CAS, /WE			90	pF
	C _{I2}	CLK0, CLK1			36	
	C _{I3}	CLK2, CLK3			40	
	C _{I4}	CKE0, CKE1			50	
	C _{I5}	/CS0 - /CS3			40	
	C _{I6}	DQMB0 - DQMB7			25	
Data input/output capacitance	C _{I/O}	DQ0 - DQ63, CB0 - CB7			15	pF

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DC Characteristics (Recommended Operating Conditions unless otherwise noted)

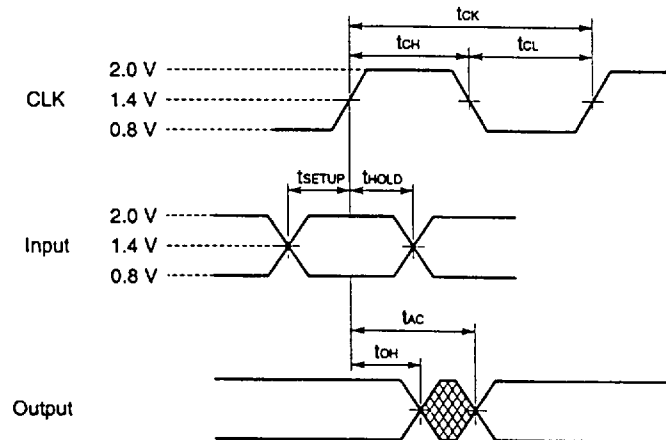
Parameter	Symbol	Test condition				MIN.	MAX.	Unit	Notes
Operating Current	I _{CC1}	Burst Length = 1 t _{RC} ≥ t _{RC(MIN.)} I _O = 0 mA	/CAS latency = 2	-A10			972	mA	
				-A67			990		
				-A12			972		
			/CAS latency = 3	-A10			1,017		
				-A67			1,035		
				-A12			1,017		
Precharge standby current in power down mode	I _{CC2P}	C _{KE} ≤ V _{IL(MAX.)} , t _{CK} = 15 ns					54	mA	
	I _{CC2PS}	C _{KE} ≤ V _{IL(MAX.)} , t _{CK} = ∞					36		
Precharge standby current in non power down mode	I _{CC2N}	C _{KE} ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.					450	mA	
	I _{CC2NS}	C _{KE} ≥ V _{IH(MIN.)} , t _{CK} = ∞ Input signals are stable.					108		
Active standby current in power down mode	I _{CC3P}	C _{KE} ≤ V _{IL(MAX.)} , t _{CK} = 15 ns					54	mA	
	I _{CC3PS}	C _{KE} ≤ V _{IL(MAX.)} , t _{CK} = ∞					36		
Active standby current in non power down mode	I _{CC3N}	C _{KE} ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.	-A10			504	mA		
			-A67			540			
			-A12			504			
	I _{CC3NS}	C _{KE} ≥ V _{IH(MIN.)} , t _{CK} = ∞ Input signals are stable.							180
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} I _O = 0 mA	/CAS latency = 2	-A10			1,152	mA	2
				-A67			1,170		
				-A12			972		
			/CAS latency = 3	-A10			1,422		
				-A67			1,260		
				-A12			1,242		
Refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	-A10			1,062	mA	3	
			-A67			1,080			
			-A12			1,062			
Self refresh current	I _{CC6}	C _{KE} ≤ 0.2 V					36	mA	
Input leakage current	I _{IL}	V _I = 0 to 3.6 V, All other pins not under test = 0 V				-90	+90	μA	
Input leakage current (C _{KE1})						-500	+500		
Output leakage current	I _{OL}	DO _{UT} is disabled, V _O = 0 to 3.6 V				-10	+10	μA	
High level output voltage	V _{OH}	I _O = -2.0 mA				2.4		V	
Low level output voltage	V _{OL}	I _O = +2.0 mA					0.4	V	

- Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.
3. I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN)}.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

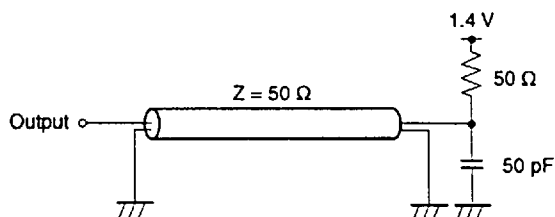
- AC measurements assume $t_r = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL} .
- If t_r is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN)}$ and $V_{IL(MAX)}$.
- An access time is measured at 1.4 V.



★ Synchronous Characteristics

Parameter		Symbol	-A10		-A67		-A12		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t _{CK3}	10		15		12		ns	
	/CAS latency = 2	t _{CK2}	15		15		18		ns	
Access time from CLK	/CAS latency = 3	t _{AC3}		8		9		9	ns	1
	/CAS latency = 2	t _{AC2}		9		9		12	ns	1
CLK high level width		t _{CH}	3.5		4		4		ns	
CLK low level width		t _{CL}	3.5		4		4		ns	
Data-out hold time		t _{OH}	4		3		4		ns	1
Data-out low-impedance time		t _{LZ}	0		0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t _{HZ3}	3	8	3	8	3	8	ns	
	/CAS latency = 2	t _{HZ2}	3	9	3	8	3	11	ns	
Data-in setup time		t _{DS}	2.5		3		3		ns	
Data-in hold time		t _{DH}	1		1.5		1.5		ns	
Address setup time		t _{AS}	2.5		3		3		ns	
Address hold time		t _{AH}	1		1.5		1.5		ns	
CKE setup time		t _{CKS}	2.5		3		3		ns	
CKE hold time		t _{CKH}	1		1.5		1.5		ns	
CKE setup time (Power down exit)		t _{CKSP}	2.5		3		3		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t _{CMS}	2.5		3		3		ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t _{CMH}	1		1.5		1.5		ns	

Note 1. Output load



★ Asynchronous Characteristics

Parameter	Symbol	-A10		-A67		-A12		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period	t _{RC}	100		105		102		ns	
ACT to PRE command period	t _{RAS}	60	120,000	75	120,000	72	120,000	ns	
PRE to ACT command period	t _{RP}	30		30		30		ns	
Delay time ACT to READ/WRITE command	t _{ACD}	30		30		30		ns	
ACT(0) to ACT(1) command period	t _{ARD}	20		30		24		ns	
Data-in to PRE command period	t _{DPL}	10		15		12		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t _{DAL3}	2CLK+ 30		2CLK+ 30		2CLK+ 30	ns	
	/CAS latency = 2	t _{DAL2}	1CLK+ 30		1CLK+ 30		1CLK+ 30	ns	
Mode register set cycle time	t _{RSC}	20		20		20		ns	
Transition time	t _{tr}	1	30	1	30	1	30	ns	
Refresh time	t _{REF}		32		32		32	ms	1

Note 1. 2,048 rows

★ Serial PD

(1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows		0BH	0	0	0	0	1	0	1	1	11 rows
4	Number of columns		09H	0	0	0	0	1	0	0	1	9 columns
5	Number of banks		02H	0	0	0	0	0	0	1	0	2 banks
6	Data width		48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTL
9	CL = 3 Cycle time	(-A10)	A0H	1	0	1	0	0	0	0	0	10 ns
		(-A67)	F0H	1	1	1	1	0	0	0	0	15 ns
		(-A12)	C0H	1	1	0	0	0	0	0	0	12 ns
10	CL =3 Access time	(-A10)	80H	1	0	0	0	0	0	0	0	8 ns
		(-A67)	90H	1	0	0	1	0	0	0	0	9 ns
		(-A12)	90H	1	0	0	1	0	0	0	0	9 ns
11	DIMM configuration type		02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate/type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		08H	0	0	0	0	1	0	0	0	x8
14	Error checking SDRAM width		08H	0	0	0	0	1	0	0	0	x8
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM		02H	0	0	0	0	0	0	1	0	2 banks
18	/CAS latency supported		06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes		00H	0	0	0	0	0	0	0	0	
22	SDRAM device attributes : General		0EH	0	0	0	0	1	1	1	0	
23	CL = 2 Cycle time	(-A10)	F0H	1	1	1	1	0	0	0	0	15 ns
		(-A67)	F0H	1	1	1	1	0	0	0	0	15 ns
		(-A12)	30H	0	0	1	1	0	0	0	0	18 ns
24	CL = 2 Access time	(-A10)	90H	1	0	0	1	0	0	0	0	9 ns
		(-A67)	90H	1	0	0	1	0	0	0	0	9 ns
		(-A12)	C0H	1	1	0	0	0	0	0	0	12 ns
25-26			00H	0	0	0	0	0	0	0	0	
27	t _{RP} (MIN.)	(-A10)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A67)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A12)	1EH	0	0	0	1	1	1	1	0	30 ns
28	t _{RD} (MIN.)	(-A10)	14H	0	0	0	1	0	1	0	0	20 ns
		(-A67)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A12)	18H	0	0	0	1	1	0	0	0	24 ns
29	t _{RC} (MIN.)	(-A10)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A67)	1EH	0	0	0	1	1	1	1	0	30 ns
		(-A12)	1EH	0	0	0	1	1	1	1	0	30 ns
30	t _{AS} (MIN.)	(-A10)	3CH	0	0	1	1	1	1	0	0	60 ns
		(-A67)	4BH	0	1	0	0	1	0	1	1	75 ns
		(-A12)	48H	0	1	0	0	1	0	0	0	72 ns
31	Module bank density		04H	0	0	0	0	0	1	0	0	16M bytes

(2/2)

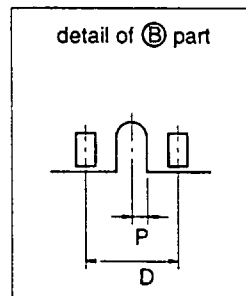
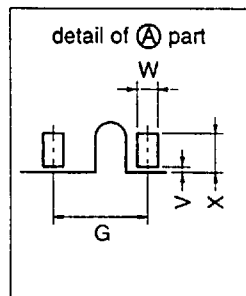
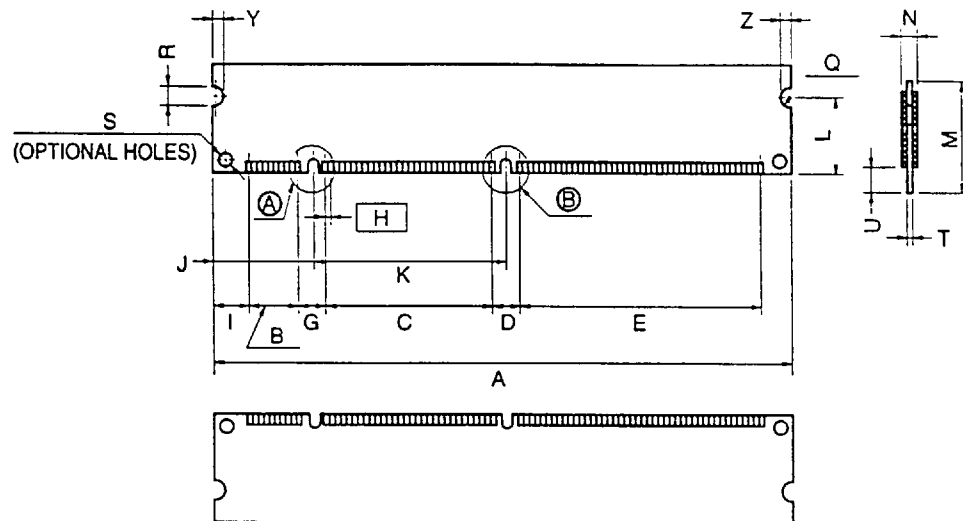
Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32-61		00H	0	0	0	0	0	0	0	0	
62	SPD revision	01H	0	0	0	0	0	0	0	1	1
63	Checksum for bytes 0 - 62	(-A10) 56H	0	1	0	1	0	1	1	0	
		(-A67) CFH	1	1	0	0	1	1	1	1	
		(-A12) 06H	0	0	0	0	0	1	1	0	
64-71	Manufacture's JEDEC ID code										
72	Manufacturing location										
73-90	Manufacture's P/N										
91-92	Revision code										
93-94	Manufacturing date										
95-98	Assembly serial number										
99-126	Mfg specific										
126	Intel specification frequency	66H	0	1	1	0	0	1	1	0	66 MHz
127	Intel specification /CAS latency support	06H	0	0	0	0	0	1	1	0	2, 3

Timing Chart

Please refer to NEC Synchronous DRAM Data sheet.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.250±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	24.495	0.964
K	42.18	1.661
L	17.78	0.700
M	29.21	1.150
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	0.157 ^{+0.005} _{-0.004}
S	φ3.0	φ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 ^{+0.003} _{-0.002}
X	2.54 MIN.	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.