

120-/128-OUTPUT TFT-LCD GATE DRIVER

The μ PD16650 is a TFT-LCD gate driver. Provided with a level shift circuit at the logic input, this chip can output a high gate scan voltage for a CMOS-level input. The μ PD16650 has an output change-over function for switching from the 120-output mode to the 128-output mode, and vice versa, thereby supporting the VGA, SVGA, and XGA panels. Its output enable function ($\overline{\text{OE}}$) enables installing the driver on either side.

FEATURES

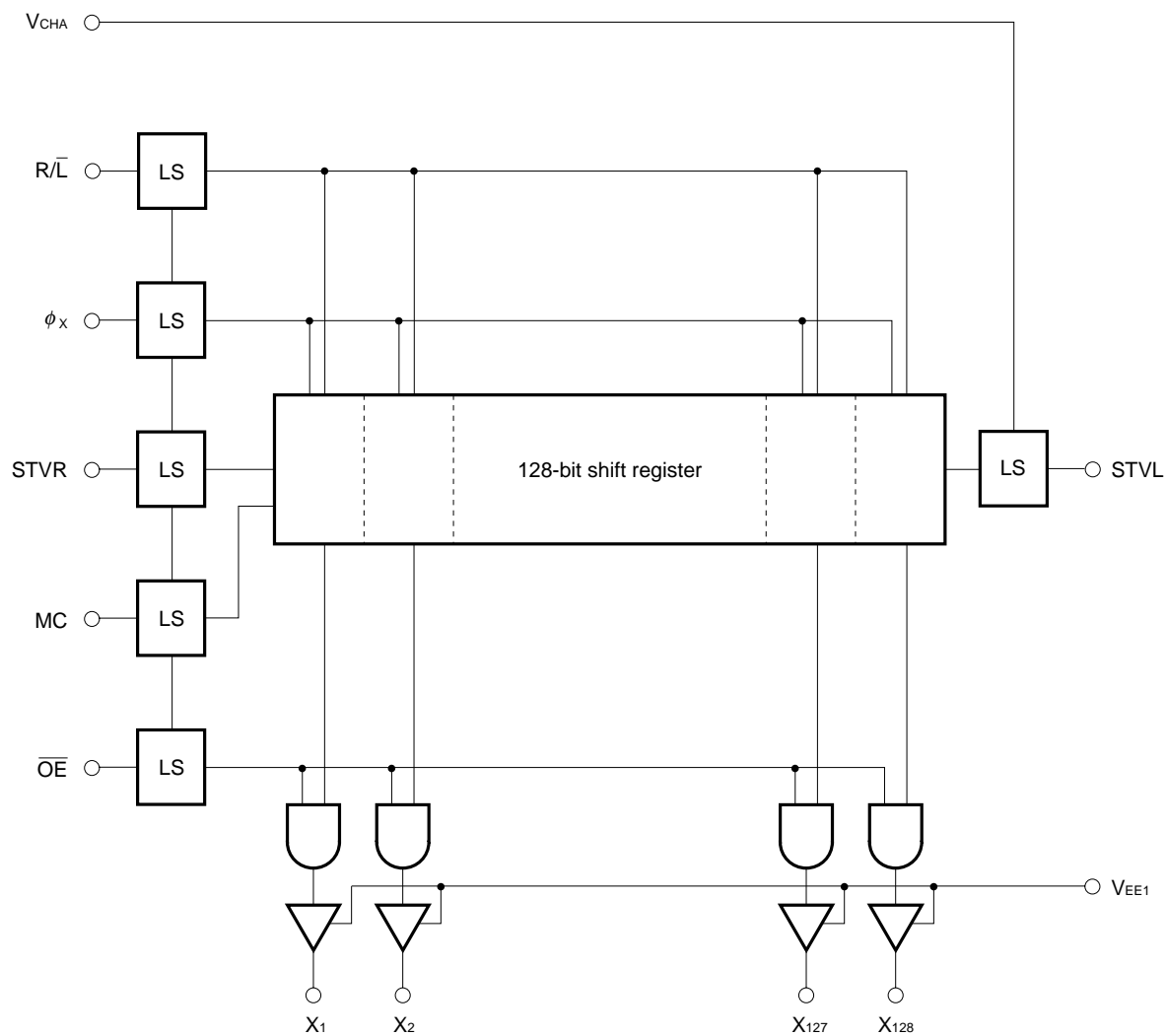
- Output with high dielectric strength (on/off range: $V_{\text{DD}} - V_{\text{EE1}} = 40 V_{\text{MAX.}}$)
- Built-in shift direction change-over function
- Shiftable negative supply voltage (V_{EE1}) level (shift range: $|V_{\text{EE1}} - V_{\text{EE2}}| = 10 \text{ V}$)
- Two acceptable CMOS input levels (3.3 and 5 V)
- Output enable function
- MC-selectable output count (MC = high: 120-output mode)
(MC = low : 128-output mode)
- Slim TCP

ORDERING INFORMATION

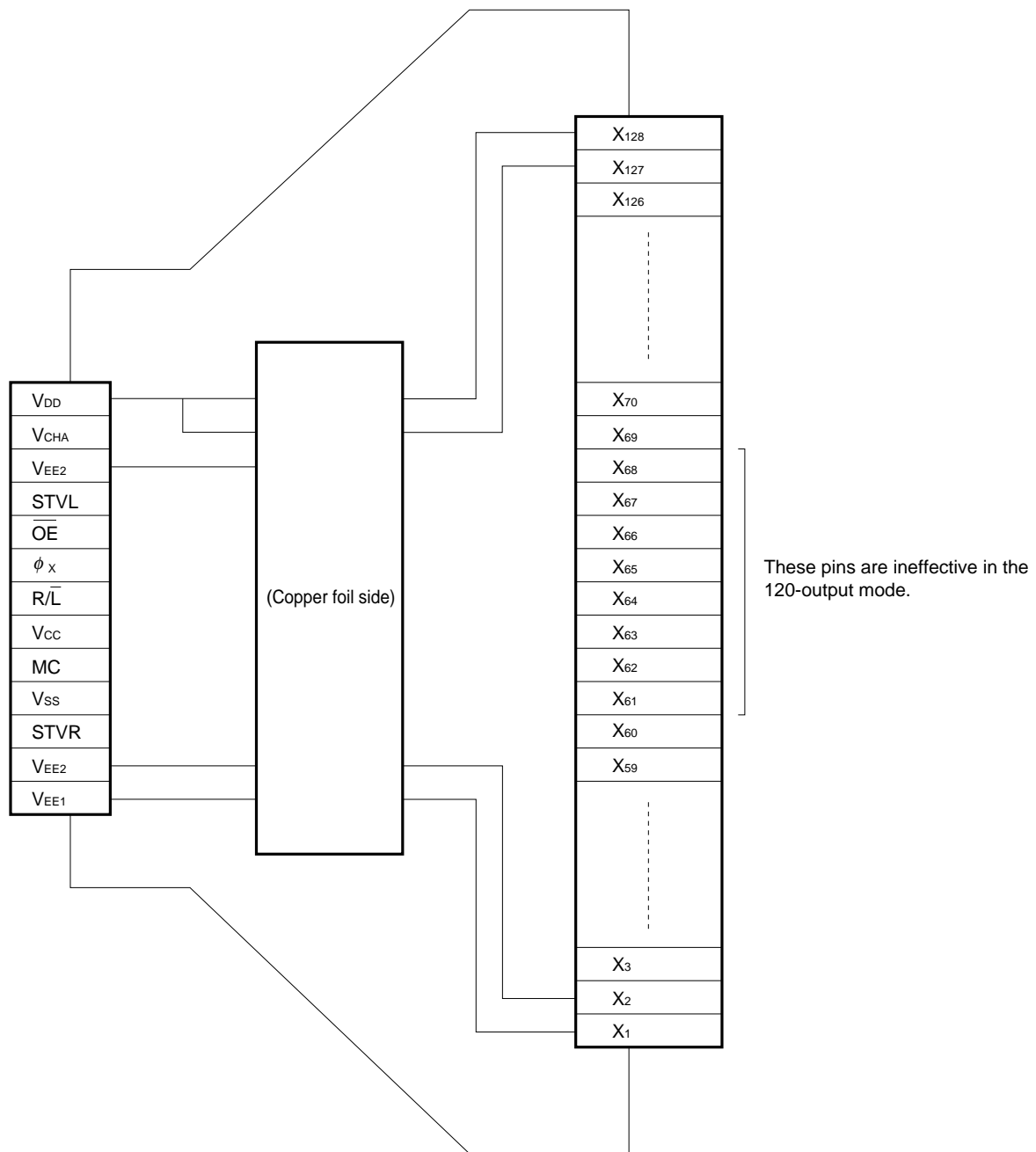
Part number	Package
μ PD16650N-xxx	TCP (TAB package)
μ PD16650N-xxx	Standard TCP (OL pitch = 220 μm)

Remark When ordering, the customer can specify the external form of the TCP. Call one of our sales representatives for more information.

BLOCK DIAGRAM



Remark LS (level shifter): Interfaces the 5 V CMOS level with the V_{DD} - V_{EE2} level.

PIN CONNECTION DIAGRAM (μ PD16650N-xxx)

Caution The V_{CHA} pin should be connected to the V_{DD} or V_{EE2} pin on the TCP. (This method eliminates the necessity to provide the V_{CHA} input pin on the TCP, resulting in a reduction in the number of required input pins.)

PIN DESCRIPTION

Pin symbol	Pin name	Description of function
X_1 to X_{128}	Driver output	Output scan signals to drive the TFT-LCD gate electrodes. The output changes when the shift clock ϕ_x rises. The amplitude of the driver output is $V_{DD} - V_{EE1}$. See the timing charts shown later for details of how to switch between the 120-output mode and 128-output mode.
MC	Output count change-over input	Receives a signal that changes the number of outputs. For the 120-output mode, this pin must be supplied with a high level (V_{CC}). For the 128-output mode, it must be supplied with a low level (V_{SS} or V_{EE2}).
V_{CHA}	Logic voltage change-over input	Must be supplied with the V_{EE2} level when the logic supply voltage is 3.3 V, and with the V_{DD} level when the logic supply voltage is 5.0 V.
STVR STVL	Start pulse input/output	Receives an input to the internal shift register. The input data is loaded on the shift register at the positive-going edge of the shift clock ϕ_x . The scan signals are output from X_1 to X_{128} . The input/output level is the CMOS level. Outputs a start pulse to the next stage if a cascade connection is used. In the 120-output mode, the start pulse is output at the negative-going edge of the 120th shift clock ϕ_x pulse, and cleared at the negative-going edge of the 121st pulse. In the 128-output mode, the start pulse is output at the negative-going edge of the 128th shift clock ϕ_x pulse, and cleared at the negative-going edge of the 129th pulse.
R/\bar{L}	Shift direction change-over input	$R/L = \text{high (for shift right)}: STVR \rightarrow X_1 \rightarrow X_{128} \rightarrow STVL$ $R/L = \text{low (for shift left)} : STVL \rightarrow X_{128} \rightarrow X_1 \rightarrow STVR$
ϕ_x	Shift clock input	Receives a shift clock pulse for the internal shift register. A shift occurs at the positive-going edge of the shift clock pulse.
\overline{OE}	Output enable input	When this pin is at a high level, the driver output is fixed at a low level. The shift register is not cleared, however. The internal logic circuit operates even when the pin is at a high level. The signal supplied to this pin is not synchronized with the clock.
V_{DD}	Driver positive supply voltage	Receives the supply voltage for both the logic circuit and driver.
V_{CC}	Reference voltage	$5 \pm 0.5 \text{ V} / 3.3 \pm 0.3 \text{ V}$ Reference voltage for the LS1 and LS2 level shifters.
V_{SS}	Ground	Must be connected to the system ground.
V_{EE1}	Driver negative supply voltage	V_{EE1} (for the driver)
V_{EE2}	Driver negative supply voltage	V_{EE2} (for the logic circuit)

CAUTIONS FOR USE

1) Power-on sequence

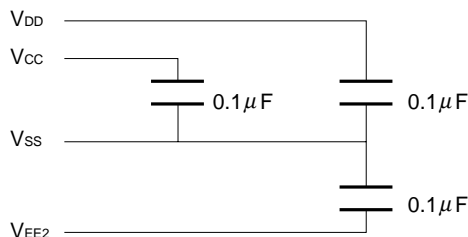
To prevent latch-up disruption, the power must be switched on in the order:

$V_{CC} \rightarrow V_{EE1} \rightarrow V_{EE2} \rightarrow V_{DD} \rightarrow \text{Logic input}$

When switching off, reverse the order. This order must be observed also during transition.

2) Insertion of bypass capacitors

The internal logic circuit operates at a high voltage. To make V_{IH} and V_{IL} immune to noise, use capacitors of $0.1 \mu\text{F}$ or so between supply voltages as shown below.



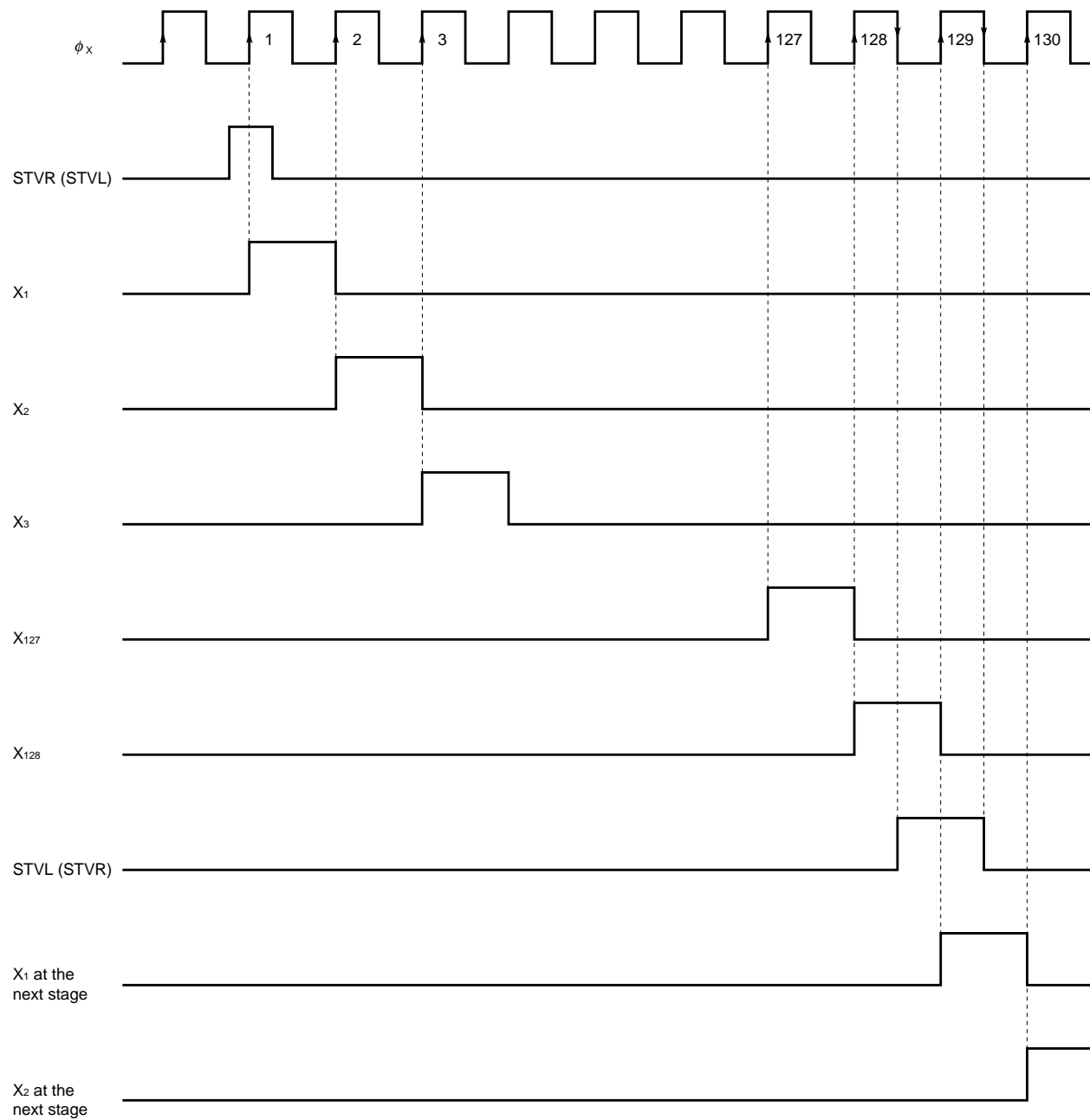
3) Negative voltage level shift

If it is necessary to shift the level of a negative supply voltage, shift the V_{EE1} (driver supply voltage) level. The shift should be limited to within: $V_{EE2} \leq V_{EE1} \leq V_{EE2} + 10 \text{ V}$

Note that shifting the V_{EE1} level results in the ON-state output resistance and output fall time ratings being changed.

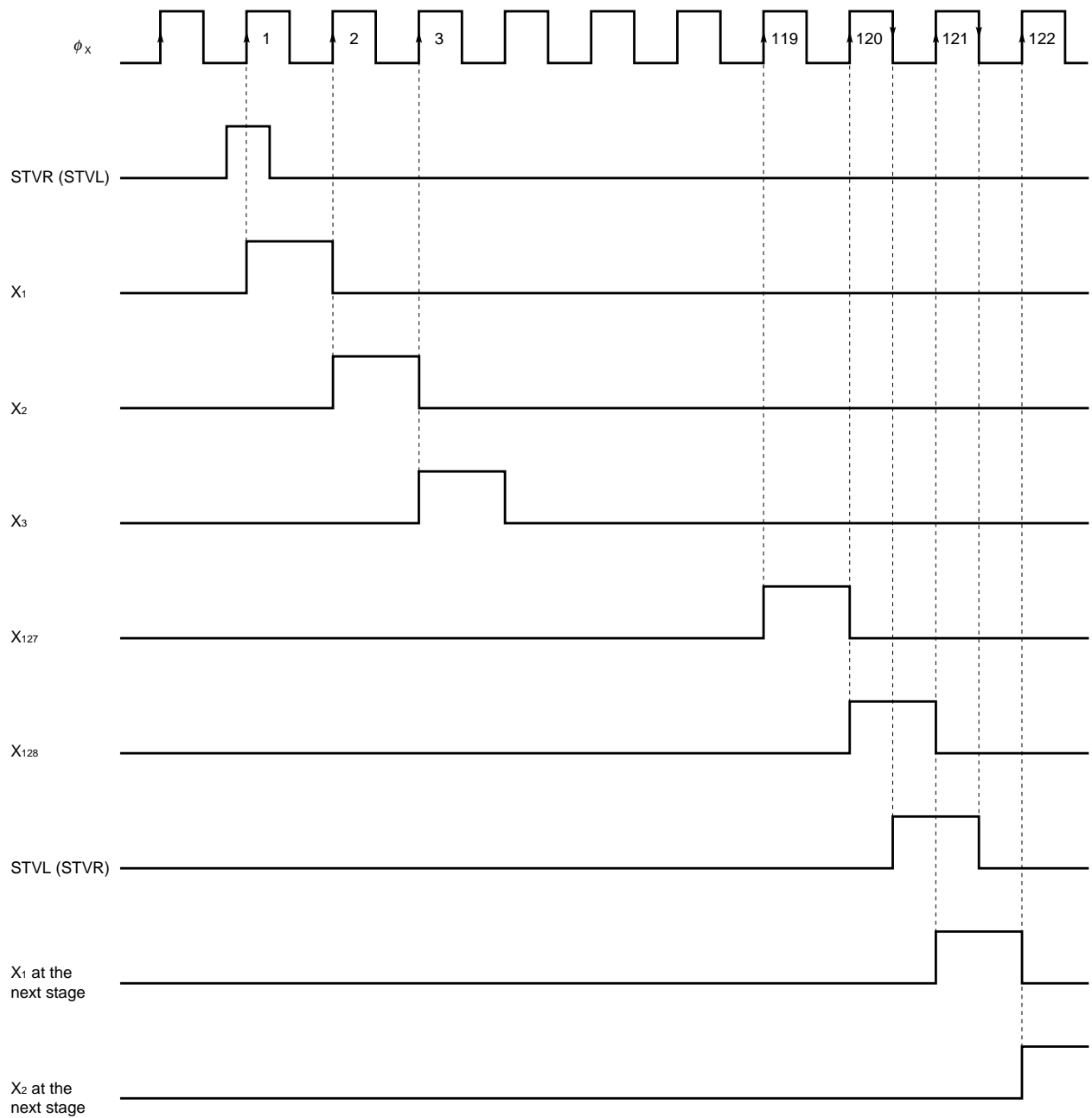
4) Handling the V_{EE1} and V_{EE2} driver negative supply voltage pins

For applications in which a negative supply voltage level is not shifted, connect the V_{EE1} pin (driver supply voltage) to the V_{EE2} pin (logic supply voltage) outside the TCP. Fix all unused input pins to the V_{EE2} level.

TIMING CHART (MC = V_{SS}, 128-OUTPUT MODE, AND R/ \bar{L} = V_{CC})

Caution Do not change all outputs simultaneously, because such a sequence may result in malfunction.

TIMING CHART (MC = V_{CC}, 120-OUTPUT MODE, AND R/ \bar{L} = V_{CC})



Cautions 1. Do not change all outputs simultaneously, because such a sequence may result in malfunction.

2. The output sequence in the 120-output mode is as follows:

STVR (STVL) → X₁ → X₂ ... X₆₀ → X₆₉ ... X₁₂₇ → X₁₂₈ → STVL (STVR)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Rated value	Unit
Supply voltage	V_{DD}		-0.5 to +28	V
Supply voltage	V_{CC}		-0.5 to +7	V
Supply voltage	$V_{DD}-V_{EE1}$ $V_{DD}-V_{EE2}$		-0.5 to +42	V
Supply voltage	V_{EE1} , V_{EE2}		-22 to +0.5	V
Input voltage	V_I		$V_{EE2} - 0.5$ to $V_{DD2} + 0.5$	V
Input current	I_I		± 10	mA
Output current	I_O		± 10	mA
Operating temperature range	T_A		-20 to +85	$^{\circ}\text{C}$
Storage temperature range	$T_{stg.}$		-55 to +125	$^{\circ}\text{C}$

RECOMMENDED OPERATING RANGES ($T_A = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		16		25	V
Supply voltage	V_{EE1}		V_{EE2}		$V_{EE2} + 10$	V
Supply voltage	V_{EE2}		-20		0	V
Supply voltage	$V_{DD}-V_{EE1}$ $V_{DD}-V_{EE2}$		20		40	V
Supply voltage	V_{CC}	For the 3.3 V logic input	3.0	3.3	3.6	V
Supply voltage	V_{CC}	For the 5.0 V logic input	4.5	5.0	5.5	V

Remark When shifting the level of V_{EE1} (driver supply voltage), satisfy the condition:

$$V_{EE2} \leq V_{EE1} \leq V_{EE2} + 10\text{ V}$$

Note that shifting the V_{EE1} level results in the ON-state output resistance and output fall time ratings being changed.

ELECTRICAL CHARACTERISTICS

($T_A = -20\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$, $V_{DD} = 20\text{ V}$, $V_{EE1} = V_{EE2} = -20\text{ V}$, $V_{CC} = 3.3 \pm 0.3\text{ V}$ or $5.0 \pm 0.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	Other than V_{CHA}	$0.7V_{CC}$		V_{CC}	V
Input low voltage	V_{IL}	Other than V_{CHA}	V_{EE2}		$0.3V_{CC}$	V
Output high voltage	V_{OH}	STVR(STVL), $I_{OH} = -40\text{ }\mu\text{A}$	$V_{CC} - 0.4$		V_{CC}	V
Output low voltage	V_{OL}	STVR(STVL), $I_{OL} = 40\text{ }\mu\text{A}$	V_{SS}		$V_{SS} + 0.4$	V
Output high current	I_{XOH}	X_n , $V_X = V_{DD} - 1\text{ V}$			-1.5	mA
Output low current	I_{XOL}	X_n , $V_X = V_{EE1} + 1\text{ V}$	1.5			mA
ON-state output resistance	R_{ON1}	$V_X = V_{EE1} + 1\text{ V}$ or $V_{DD} - 1\text{ V}$			660	Ω
Input leakage current	I_{IL}	$V_I = 0\text{ V}$, 5.0 V , or 3.3 V			± 1.0	μA
Dynamic drain current	I_{DD}	V_{DD} , $f\phi_X = 31.5\text{ kHz}$		0.5	1.0	mA
	I_{EE}	$V_{EE1/2}$, $f\phi_X = 31.5\text{ kHz}$		-0.5	-1.0	mA
	I_{CC}	V_{CC} , $f\phi_X = 31.5\text{ kHz}$		50	100	μA

SWITCHING CHARACTERISTICS(T_A = -20 °C to +70 °C, V_{DD} = 20 V, V_{EE1} = V_{EE2} = -20 V, V_{SS} = 0 V, V_{CC} = 3.3 ±0.3 V or 5.0 ±0.5 V)

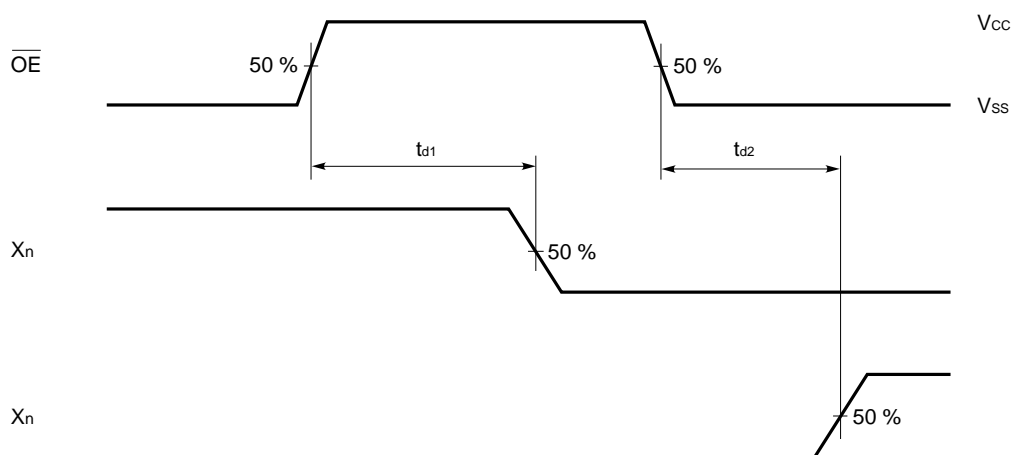
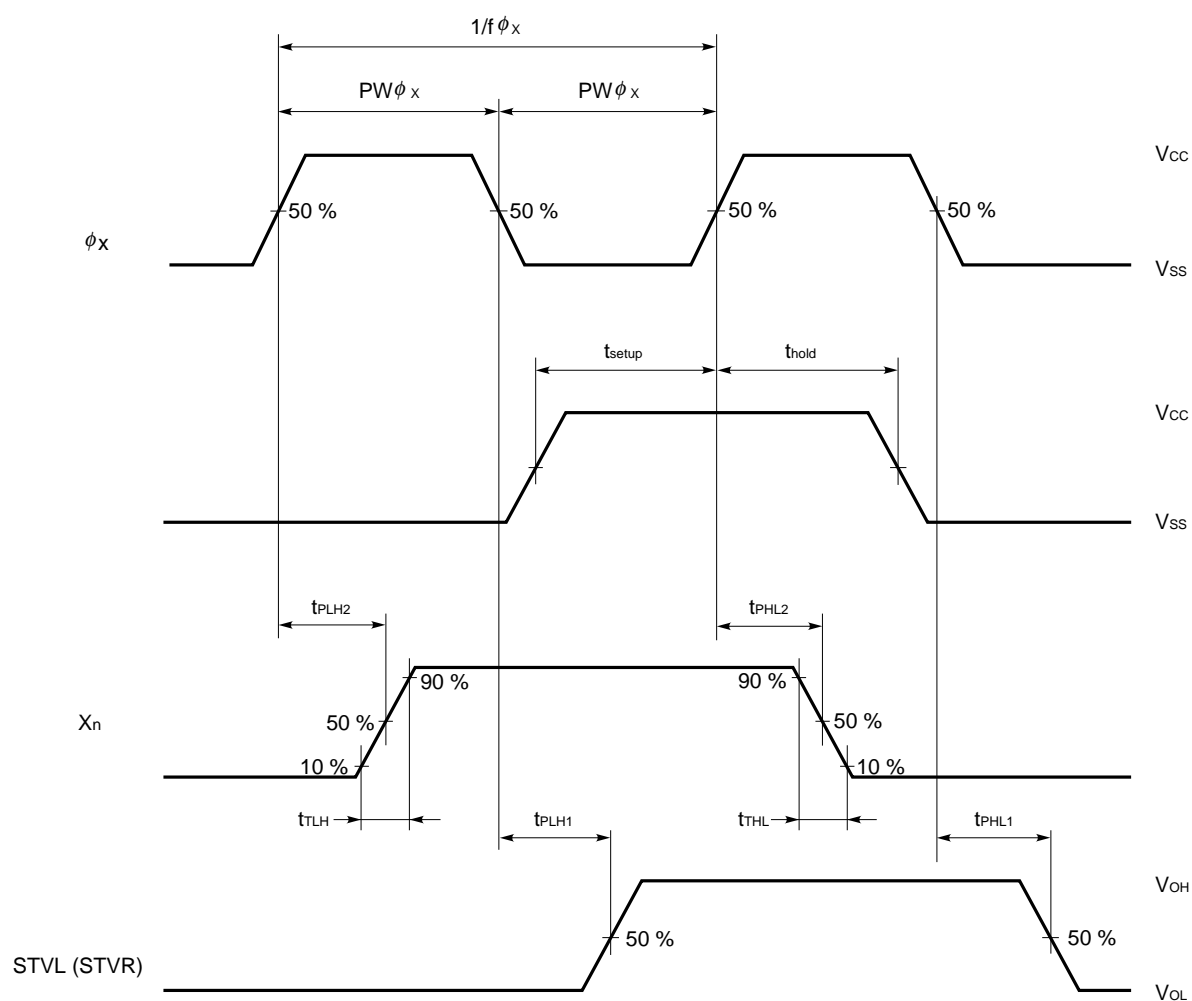
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
STVR and STVL output delay	t _{PHL1}	C _L = 20 pF			600	ns
	t _{PLH1}	CLK → STVR(STVL)			600	ns
Driver output delay	t _{PHL2}	C _L = 220 pF			700	ns
	t _{PLH2}	CLK → X _n			700	ns
	t _{d1}	C _L = 220 pF, \overline{OE} : L → H			700	ns
	t _{d2}	C _L = 220 pF, \overline{OE} : H → L			700	ns
Output rise time	t _{THL}	C _L = 220 pF			300	ns
Output fall time	t _{TLH}	C _L = 220 pF			300	ns
Input capacitance	C _i	T _A = 25 °C			15	pF
Maximum clock frequency	f ϕ _x	For cascade connection	100			kHz

TIMING REQUIREMENTS(T_A = -20 °C to +70 °C, V_{DD} = 20 V, V_{EE1} = V_{EE2} = -20 V, V_{SS} = 0 V, V_{CC} = 3.3 ±0.3 V or 5.0 ±0.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse high width	PW ϕ _x (H)	Duty = 50 %	500			ns
Clock pulse low width	PW ϕ _x (L)	Duty = 50 %	500			ns
Data setup time	t _{setup}	STVR(STVL) ↑ → CLK ↑	100			ns
Data hold time	t _{hold}	CLK ↑ → STVR(STVL) ↓	100			ns

Remark The logic input rise time (t_r) and fall time (t_f) must be within 20 ns (between 10 % and 90 % of the peak amplitude of the input).

SWITCHING CHARACTERISTIC WAVEFORM (R/L = HIGH)



RECOMMENDED MOUNTING CONDITIONS

When mounting this product, please make sure that the following recommended conditions are satisfied.

For packaging methods and conditions other than those recommended below, please contact NEC sales personnel.

μPD16650N-xxx

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C; heating for 2 to 3 seconds; pressure 100 g (per solder)
	ACF (Sheet-shape bonding agent)	Temporary bonding 70 to 100 °C; pressure 3 to 8 kg/cm ² ; time 3 to 5 secs. Real bonding 165 to 180 °C; pressure 25 to 45 kg/cm ² ; time 30 to 40 secs. (when using the anisotropic conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.

Reference

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)

Quality Grades to NEC's Semiconductor Devices (IEI-1209)

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The quality grade of NEC devices in "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.