NEC

MOS INTEGRATED CIRCUIT

μPD178076,178078,178096,178098

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD178076, 178078, 178096, and 178098 are 8-bit single-chip CMOS microcontrollers containing hardware for digital tuning systems.

These microcontrollers employ a 78K/0 series architecture CPU and allow easy access to internal memories at high speed and easy control of peripheral hardware units. The high-speed 78K/0 series instructions are ideal for system control.

As peripheral hardware, a prescaler, PLL frequency synthesizer, and frequency counter for digital tuning systems are provided, as well as many I/O ports, timers, A/D converter, serial interface, and a power-ON clear circuit. In addition, the μPD178076 and 178078 have an asynchronous serial interface (UART) mode, and the μPD178096 and 178098 have an IEBus™ controller.

Moreover, a flash memory model, the μPD178F098, that operates in the same supply voltage range as the mask ROM models, and various development tools are also under development.

For the detailed functional description, refer to the following User's Manuals:

μPD178078, 178098 Subseries User's Manual : U12790E
78K/0 Series User's Manual - Instruction : U12326E

FEATURES

● High-capacity ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory		
		Internal high-speed RAM	Internal buffer RAM	Internal extension RAM
μPD178076, 178096	48K bytes	1024 bytes	32 bytes	1024 bytes
μPD178078, 178098	60K bytes			2048 bytes

● Instruction cycle:
0.32 μs (with crystal resonator of f_X = 6.3 MHz)

● Many internal hardware units
General-purpose I/O ports, A/D converter, serial interface (UART mode: μPD178076 and 178078 only), IEBus controller (μPD178096 and 178098 only), timers, frequency counter, power-ON clear circuit

● Hardware for PLL frequency synthesizer
dual modulus prescaler, programmable divider, phase comparator, charge pump

● Vectored interrupt sources
- μPD178076, 178078: 22
- μPD178096, 178098: 21

● Supply voltage
:V_{DD} = 4.5 to 5.5 V (during PLL and CPU operations)
:V_{DD} = 3.5 to 5.5 V (during CPU operation)

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The mark ★ shows major revised points.

APPLICATION FIELD

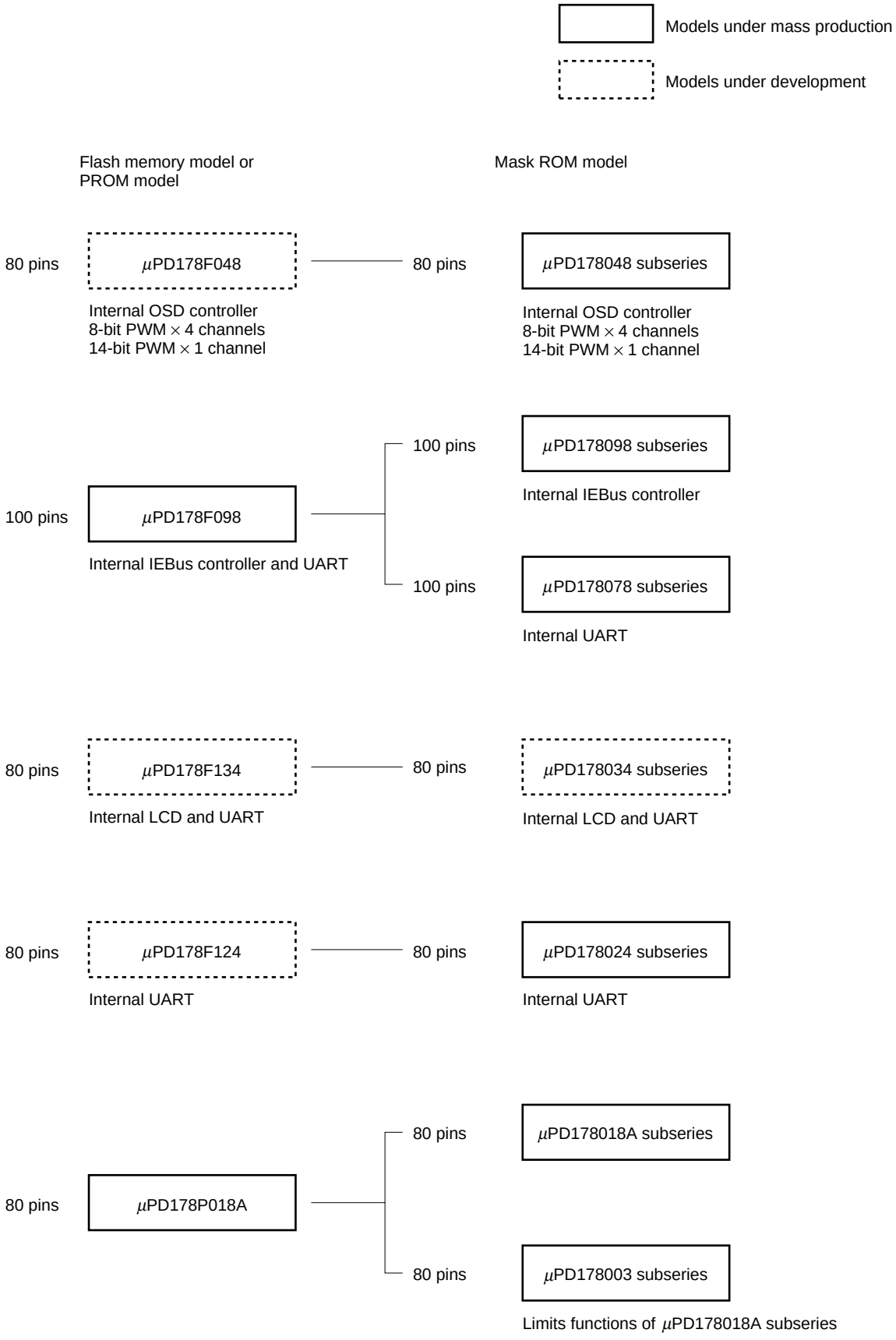
Car stereos

ORDERING INFORMATION

Part Number	Package
μPD178076GF-×××-3BA	100-pin plastic QFP (14 × 20)
μPD178078GF-×××-3BA	100-pin plastic QFP (14 × 20)
μPD178096GF-×××-3BA	100-pin plastic QFP (14 × 20)
μPD178098GF-×××-3BA	100-pin plastic QFP (14 × 20)

Remark ××× indicates ROM code suffix, which is E×× when the I^2C bus is used.

★ DEVELOPMENT OF 8-BIT DTS SERIES



FUNCTIONAL OUTLINE

(1/2)

Item		μPD178076	μPD178078	μPD178096	μPD178098
Internal memory	ROM	48K bytes	60K bytes	48K bytes	60K bytes
	High-speed RAM	1024 bytes			
	Buffer RAM	32 bytes			
	Extension RAM	1024 bytes	2048 bytes	1024 bytes	2048 bytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		• 0.32 μs/0.64 μs/1.27 μs/2.54 μs/5.08 μs (with crystal resonator of f_X = 6.3 MHz) • 0.44 μs/0.89 μs/1.78 μs/3.56 μs/7.11 μs (with crystal resonator of f_X = 4.5 MHz)**Note 1**			
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test Boolean operation) • BCD adjustment, etc.			
I/O port		Total : 80 pins • CMOS input : 8 pins • CMOS I/O : 64 pins • N-ch open-drain output : 8 pins			
A/D converter		8-bit resolution × 8 channels			
Serial interface		• 3-wire/SBI/2-wire/I^2C bus**Note 2** mode selectable: 1 channel • 3-wire mode: 1 channel • 3-wire mode (with automatic transmit/receive function of up to 32 bytes): 1 channel • UART mode: 1 channel		• 3-wire/SBI/2-wire/I^2C bus**Note 2** mode selectable: 1 channel • 3-wire mode: 1 channel • 3-wire mode (with automatic transmit/receive function of up to 32 bytes): 1 channel	
IEBus controller		Not provided		Provided	
Timer		• Basic timer (timer carry FF (10 Hz)) : 1 channel • 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watchdog timer : 1 channel			
Buzzer output		BEEP0 pin: 1 kHz, 1.5 kHz, 3 kHz, 4 kHz			
		BUZ pin: 0.77 kHz, 1.54 kHz, 3.08 kHz, 6.15 kHz (with crystal resonator of f_X = 6.3 MHz)			

Notes 1. When using the IEBus controller of the μPD178096 or 178098, the 4.5-MHz crystal resonator cannot be used. Use the 6.3-MHz crystal resonator.

2. When the I^2C bus mode is used (including when the mode is implemented in software without using the peripheral hardware), consult NEC when ordering a mask.

(2/2)

Item		μPD178076	μPD178078	μPD178096	μPD178098
Vectored interrupt source	Maskable	Internal : 13 External: 8		Internal : 12 External: 8	
	Non-maskable	Internal: 1			
	Software	1			
PLL frequency synthesizer	Division mode	2 types • Direct division mode (VCOL pin) • Pulse swallow mode (VCOL and VCOH pins)			
	Reference frequency	Seven types selectable in software (1, 3, 9, 10, 12.5, 25, 50 kHz)			
	Charge pump	Error out output: 2 pins			
	Phase comparator	Unlock detectable in software			
Frequency counter		Frequency measurement • AMIFC pin: For 450-kHz counting • FMIFC pin: For 450-kHz/10.7-MHz counting			
Standby function		• HALT mode • STOP mode			
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Reset by power-ON clear circuit • Detection of less than 4.5 V[Note] (Reset does not occur, however.) • Detection of less than 3.5 V[Note] (during CPU operation) • Detection of less than 2.3 V[Note] (in STOP mode)			
Supply voltage		• V_{DD} = 4.5 to 5.5 V (during CPU, PLL operation) • V_{DD} = 3.5 to 5.5 V (during CPU operation)			
Package		• 100-pin plastic QFP (14 × 20)			

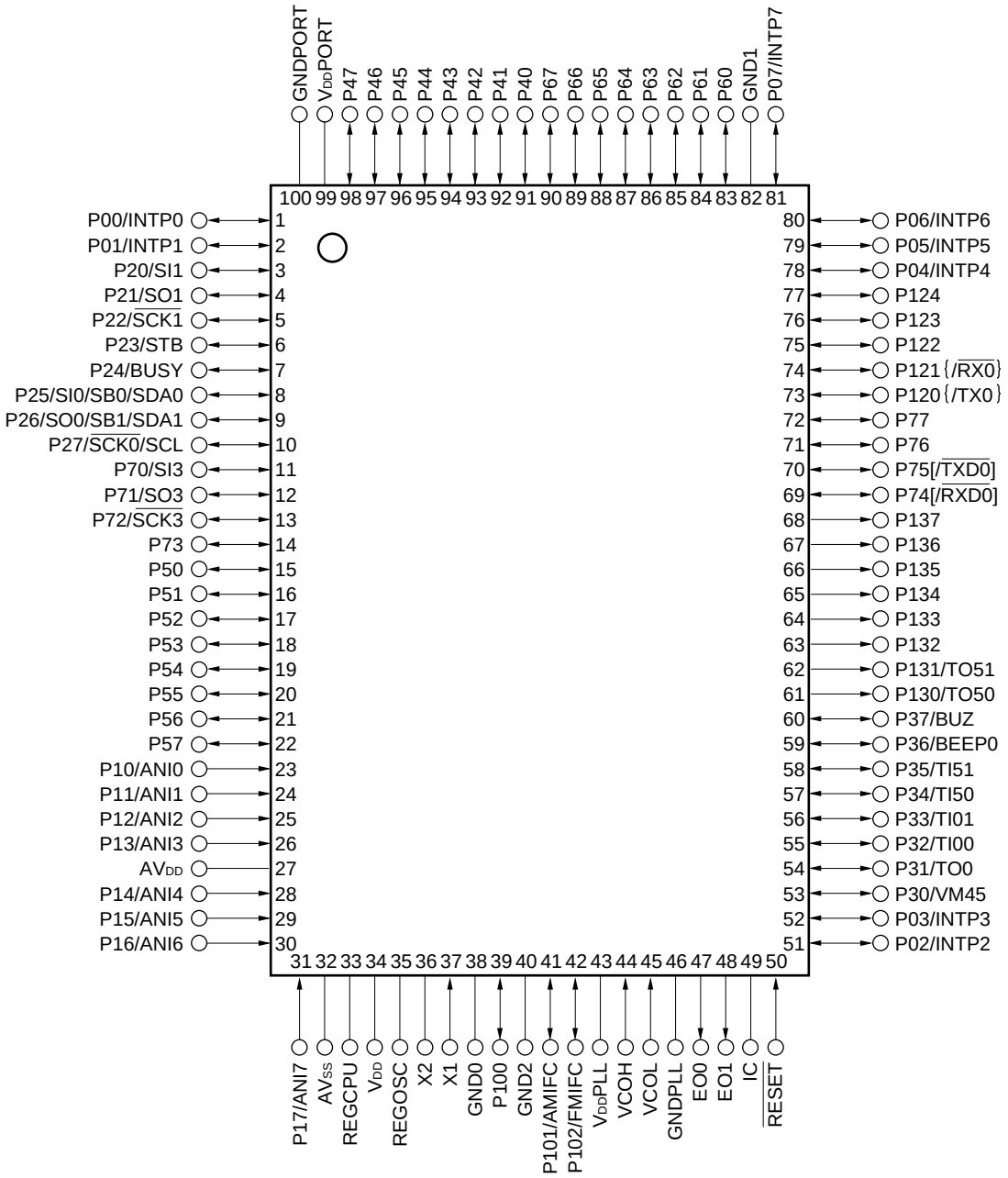
Note These voltages are the maximum values. In practice, the chip may be reset at voltages lower than these.

PIN CONFIGURATION (Top View)

• 100-pin plastic QFP (14 × 20)

μPD178076GF-×××-3BA, 178078GF-×××-3BA

μPD178096GF-×××-3BA, 178098GF-×××-3BA



Cautions 1. Directly connect the IC (Internally Connect) pin to GND0, GND1, or GND2.

2. Keep the voltage at AV_{DD}, V_{DD}PORT, and V_{DD}PLL pins same as that at the V_{DD} pin.

3. Keep the voltage at AV_{SS}, GNDPORT, and GNDPLL pins same as that at GND0, GND1, or GND2.

4. Connect each of the REGOSC and REGCPU pins to GND via a 0.1-μF capacitor.

Remark [ ]: μPD178076 and 178078 only

{ }: μPD178096 and 178098 only

Pin Name

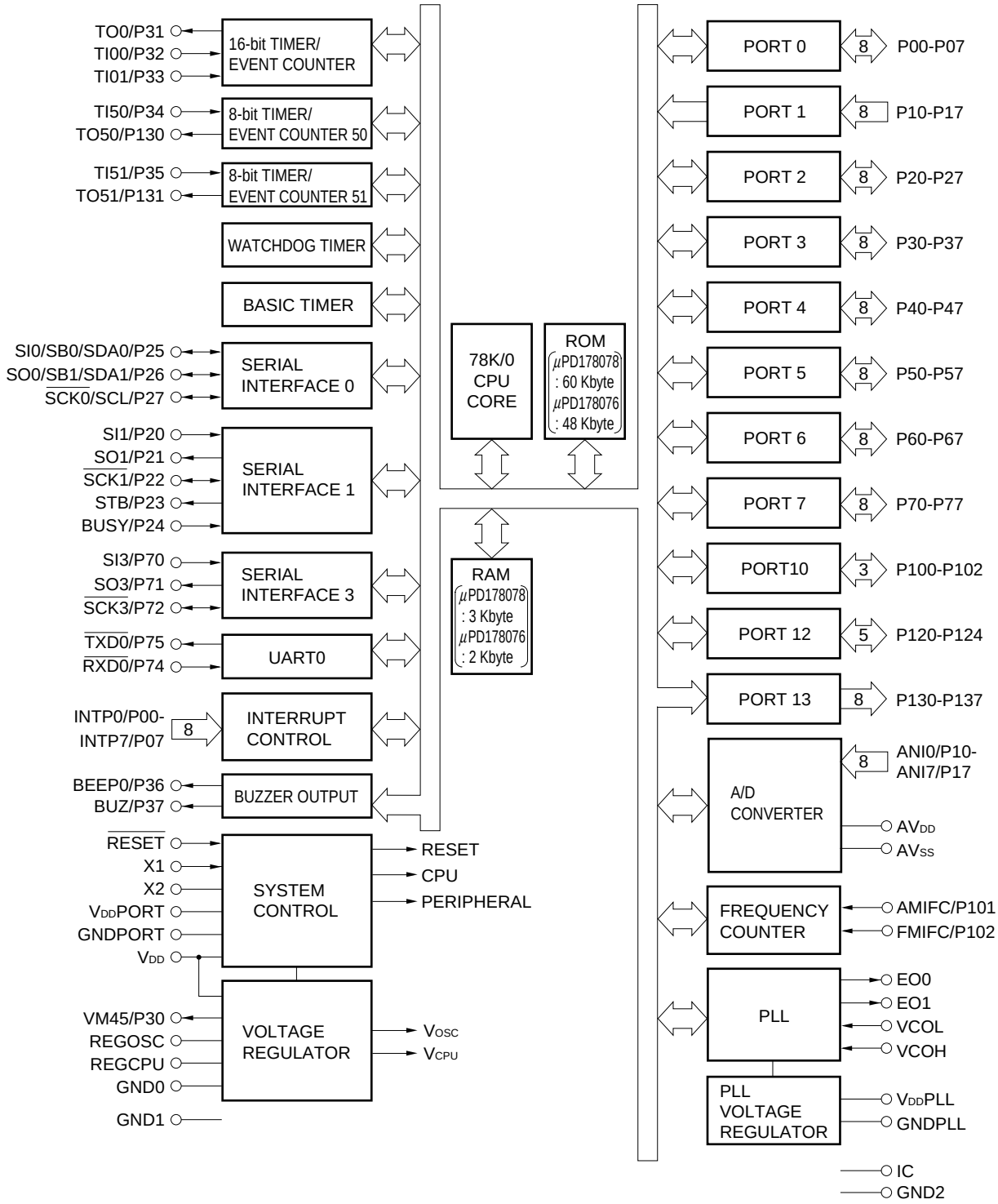
AMIFC	: AM intermediate frequency counter input	P130-P137	: Port 13
ANI0-ANI7	: A/D converter input	REGCPU	: Regulator for CPU power supply
AV_{DD}	: A/D converter power supply	REGOSC	: Regulator for oscillation circuit
AV_{SS}	: A/D converter ground	$\overline{RESET}$	: Reset input
BUSY	: Busy output	$\overline{RXD0}$ **Note 1**	: UART0 serial data input
BEEP0, BUZ	: Buzzer output	$\overline{RX0}$ **Note 2**	: IEBus serial data input
EO0, EO1	: Error out output	SB0, SB1	: Serial data bus input/output
FMIFC	: FM intermediate frequency counter input	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK3}$	: Serial clock input/output
		SCL	: Serial clock input/output
GNDPLL	: PLL ground	SDA0, SDA1	: Serial data input/output
GND0-GND2	: Ground	SI0, SI1, SI3	: Serial data input
IC	: Internally connected	SO0, SO1, SO3	: Serial data output
INTP0-INTP7	: Interrupt input	STB	: Strobe output
P00-P07	: Port 0	TI00, TI01	: 16-bit timer capture trigger input
P10-P17	: Port 1	TI50, TI51	: 8-bit timer clock input
P20-P27	: Port 2	TO0	: 16-bit timer output
P30-P37	: Port 3	TO50, TO51	: 8-bit timer output
P40-P47	: Port 4	$\overline{TXD0}$ **Note 1**	: UART0 serial data output
P50-P57	: Port 5	$\overline{TX0}$ **Note 2**	: IEBus serial data output
P60-P67	: Port 6	VCOL, VCOH	: Local oscillation input
P70-P77	: Port 7	V_{DD}PORT	: Port power supply
P100-P102	: Port 10	V_{DD}PLL	: PLL power supply
P120-P124	: Port 12	V_{DD}	: Power supply
		VM45	: V_{DD} = 4.5 V monitor output
		X1, X2	: Crystal resonator

Notes 1. μPD178076 and 178078 only

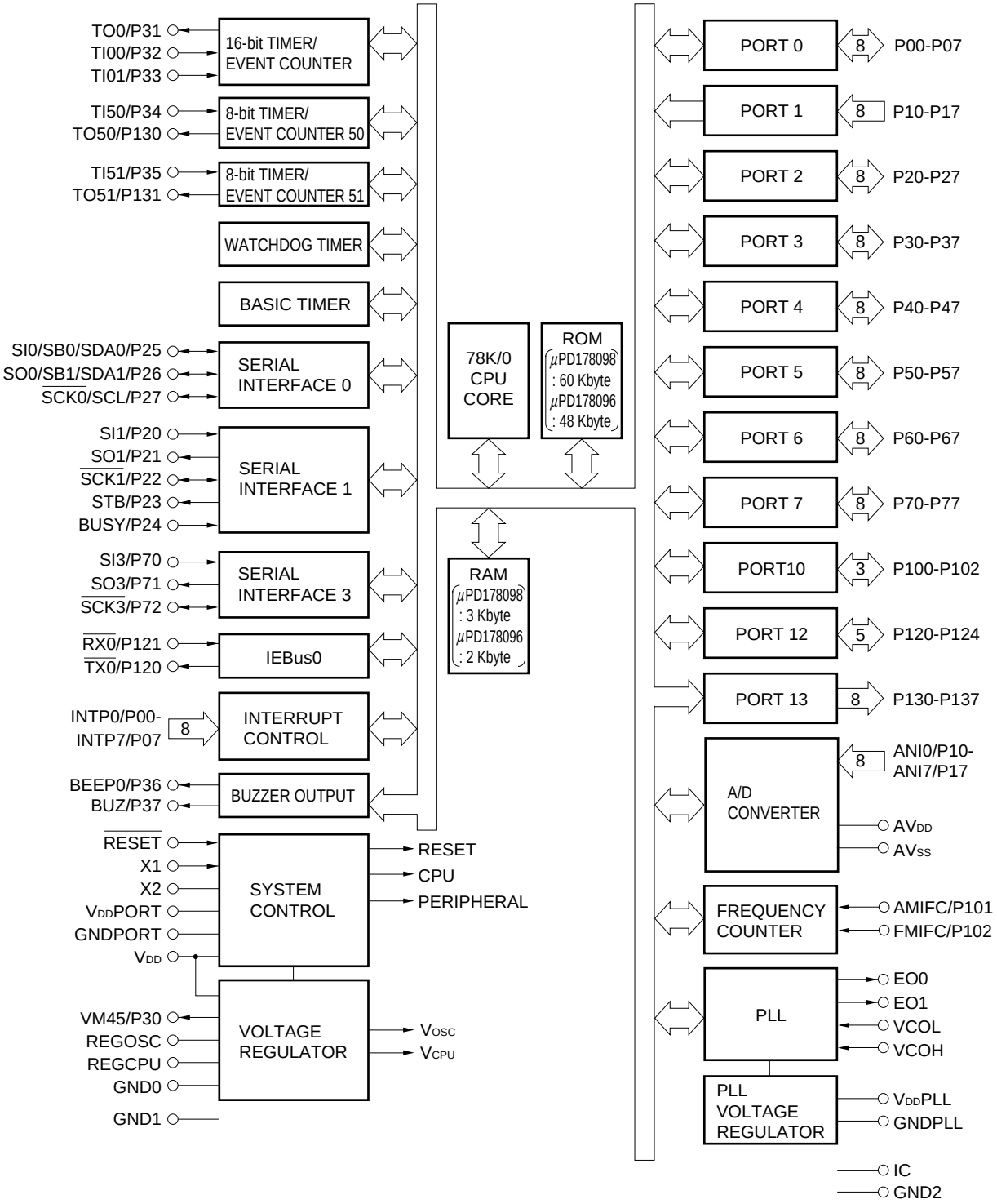
2. μPD178096 and 178098 only

BLOCK DIAGRAM

(1) μPD178076, 178078



(2) μPD178096, 178098



CONTENTS

1. PIN FUNCTION LIST

1.1 Port Pins (1/2)

Pin Name	I/O	Function	At Reset	Shared by:
P00-P07	I/O	Port 0. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	INTP0-INTP7
P10-P17	Input	Port 1. 8-bit input port.	Input	ANI0-ANI7
P20	I/O	Port 2. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	SI1
P21				SO1
P22				$\overline{\text{SCK1}}$
P23				STB
P24				BUSY
P25				SI0/SB0/SDA0
P26				SO0/SB1/SDA1
P27				$\overline{\text{SCK0}}$/SCL
P30	I/O	Port 3. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	VM45
P31				TO0
P32				TI00
P33				TI01
P34				TI50
P35				TI51
P36				BEEP0
P37				BUZ
P40-47	I/O	Port 4. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	–
P50-P57	I/O	Port 5. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	–
P60-P67	I/O	Port 6. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	–
P70	I/O	Port 7. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	SI3
P71				SO3
P72				$\overline{\text{SCK3}}$
P73				–
P74				$\overline{\text{RXD0}}$ **Note 1**
P75				$\overline{\text{TXD0}}$ **Note 1**
P76, P77				–

1.1 Port Pins (2/2)

Pin Name	I/O	Function	At Reset	Shared by:
P100	I/O	Port 10.	Input	–
P101		3-bit I/O port.		AMIFC
P102		Can be set in input or output mode in 1-bit units.		FMIFC
P120	I/O	Port 12.	Input	$\overline{TX0}$ Note 2
P121		5-bit I/O port.		$\overline{RX0}$ Note 2
P122-P124		Can be set in input or output mode in 1-bit units.		–
P130	Output	Port 13.	Low-level output	TO50
P131		8-bit output port.		TO51
P132-P137		N-ch open-drain output port (15 V withstand)		–

Notes 1. μPD178076 and 178078 only.

2. μPD178096 and 178098 only.

1.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Function		At Reset	Shared by:
INTP0-INTP7	Input	External maskable interrupt input whose valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.		Input	P00-P07
SI0	Input	Serial data input to serial interface.		Input	P25/SB0/SDA0
SI1					P20
SI3					P70
SO0	Output	Serial data output from serial interface.		Input	P26/SB1/SDA1
SO1					P21
SO3					P71
SB0	I/O	Serial data input/output to/from serial interface.	N-ch open drain I/O	Input	P25/SI0/SDA0
SB1					P26/SO0/SDA1
SDA0					P25/SI0/SB0
SDA1					P26/SO0/SB1
$\overline{SCK0}$	I/O	Serial clock input/output to/from serial interface.		Input	P27/SCL
$\overline{SCK1}$					P22
$\overline{SCK3}$					P72
SCL			N-ch open drain I/O		P27/$\overline{SCK0}$
STB	Output	Strobe output for serial interface automatic transmission/ reception.		Input	P23
BUSY	Input	Busy input for serial interface automatic transmission/ reception.		Input	P24
VW45	Output	V_{DD} = 4.5 V monitor output		Input	P30
TI00	Input	External count clock input to 16-bit timer 0.		Input	P32
TI01					P33
TI50	Input	External count clock input to 8-bit timer 50.		Input	P34
TI51		External count clock input to 8-bit timer 51.			P35

1.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Function	At Reset	Shared by:
TO0	Output	16-bit timer 0 output.	Input	P31
TO50		8-bit timer 50 output.	Low-level output	P130
TO51		8-bit timer 51 output.		P131
BEEP0	Output	Buzzer output.	Input	P36
BUZ				P37
ANI0-ANI7	Input	Analog input to A/D converter.	Input	P10-P17
EO0, EO1	Output	Error out output from charge pump of PLL frequency synthesizer.	–	–
VCOL	Input	Inputs local oscillation frequency of PLL (in HF and MF modes).	–	–
VCOH	Input	Inputs local oscillation frequency of PLL (in VHF mode).	–	–
AMIFC	Input	Input to AM intermediate frequency counter.	Input	P101
FMIFC	Input	Input to FM intermediate frequency or AM intermediate frequency counter.	Input	P102
$\overline{\text{RXD0}}$	Input	Serial data input to asynchronous serial interface (UART0). μPD178076 and 178078 only.	Input	P74
$\overline{\text{TXD0}}$	Output	Serial data output from asynchronous serial interface (UART0). μPD178076 and 178078 only.	Input	P75
$\overline{\text{TX0}}$	Output	IEBus controller data output. μPD178096 and 178098 only.	Input	P120
$\overline{\text{RX0}}$	Input	IEBus controller data input. μPD178096 and 178098 only.	Input	P121
$\overline{\text{RESET}}$	Input	System reset input.	–	–
X1	Input	Connection of crystal resonator for system clock oscillation.	–	–
X2	–		–	–
REGOSC	–	Regulator for oscillation circuit. Connect this pin to GND via 0.1-μF capacitor.	–	–
REGCPU	–	Regulator for CPU power supply. Connect this pin to GND via 0.1-μF capacitor.	–	–
V_{DD}	–	Positive power supply.	–	–
GND0-GND2	–	Ground.	–	–
V_{DD}PORT	–	Port power supply.	–	–
GNDPORT	–	Port ground.	–	–
AV_{DD}	–	A/D converter positive power supply. Keep voltage at this pin same as that at V_{DD}.	–	–
AV_{SS}	–	A/D converter ground. Keep voltage at this pin same as that at GND0 through GND2.	–	–
V_{DD}PLL**Note**	–	PLL positive power supply.	–	–
GNDPLL**Note**	–	PLL ground.	–	–
IC	–	Internally connected. Directly connect this pin to GND0, GND1, or GND2.	–	–

Note Connect a capacitor of about 1000 pF between the V_{DD}PLL and GNDPLL pins.

1.3 I/O Circuits of Pins and Recommended Connections of Unused Pins

Table 1-1 shows the types of the I/O circuits of the respective pins and the recommended connections of the pins when they are not used.

For the configuration of the I/O circuit of each pin, refer to Figure 1-1.

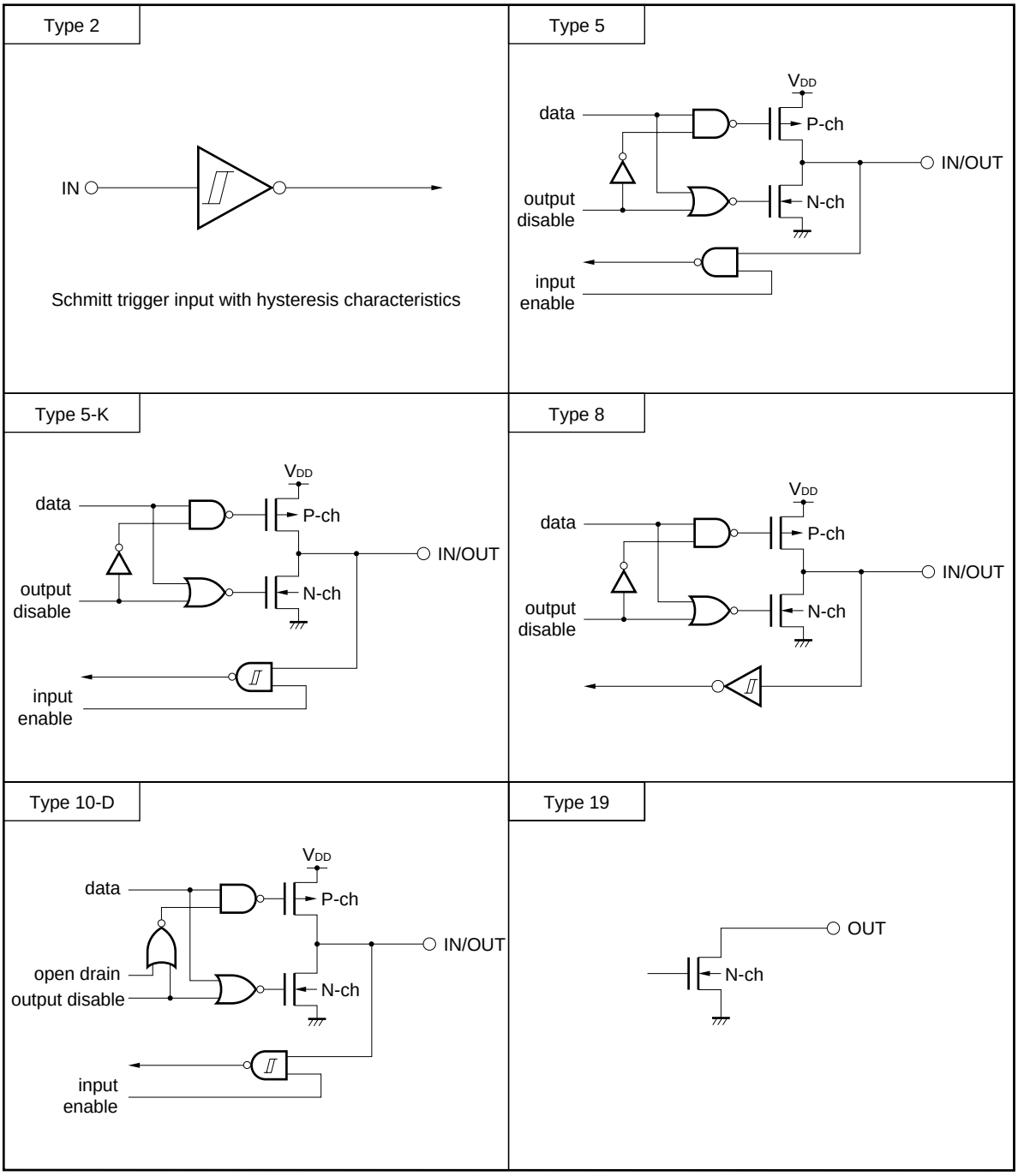
Table 1-1. I/O Circuit Type of Each Pin (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P00/INTP0-P07/INTP7	8	I/O	Input: Individually connect them to V_{DD}, V_{DD}PORT, GND0 to GND2, or GNDPORT via resistor. Output: Leave open.
P10/ANI0-P17/ANI7	25	Input	Connect them to V_{DD}, V_{DD}PORT, GND0 to GND2, or GNDPORT.
P20/SI1	5-K	I/O	Input: Individually connect them to V_{DD}, V_{DD}PORT, GND0 to GND2, or GNDPORT via resistor. Output: Leave open.
P21/SO1	5		
P22/$\overline{SCK1}$	5-K		
P23/STB	5		
P24/BUSY	5-K		
P25/SI0/SB0/SDA0	10-D		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/VM45	5		
P31/TO0			
P32/TI00	5-K		
P33/TI01			
P34/TI50			
P35/TI51			
P36/BEEP0	5		
P37/BUZ			
P40-P47			
P50-P57			
P60-P67			
P70/SI3	5-K		
P71/SO3	5		
P72/$\overline{SCK3}$	5-K		
P73	5		
P74/$\overline{RXD0}$	5-K		
P75/$\overline{TXD0}$	5		
P76, P77			
P100			
P101/AMIFC			
P102/FMIFC			
P120/$\overline{TX0}$			
P121/$\overline{RX0}$	5-K		
P122-P124	5		

Table 1-1. I/O Circuit Type of Each Pin (2/2)

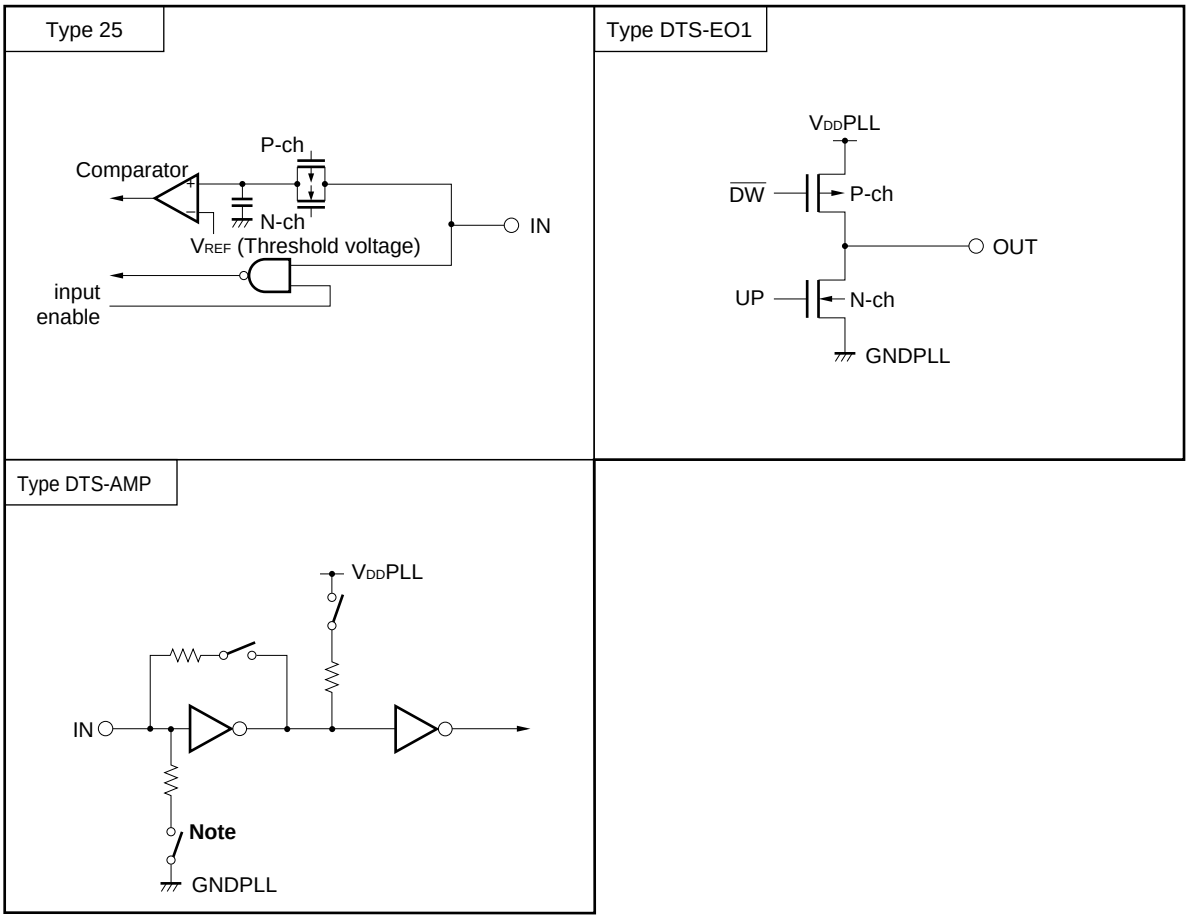
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P130/TO50	19	Output	Open these pins.
P131/TO51			
P132-P137			
EO0	DTS-EO1		
EO1			
VCOL, VCOH	DTS-AMP2	Input	Disable PLL in software and select pull-down.
REGOSC, REGCPU	–	–	Connect these pins to GND0, GND1, or GND2 via 0.1-μF capacitor.
$\overline{\text{RESET}}$	2	Input	–
AV_{DD}	–	–	Connect this pin to V_{DD} or V_{DD}PORT.
AV_{SS}			Directly connect these pins to GND0 to GND2, or GNDPORT.
IC			

Figure 1-1. I/O Circuits of Respective Pins (1/2)



Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT.

Figure 1-1. I/O Circuits of Respective Pins (2/2)



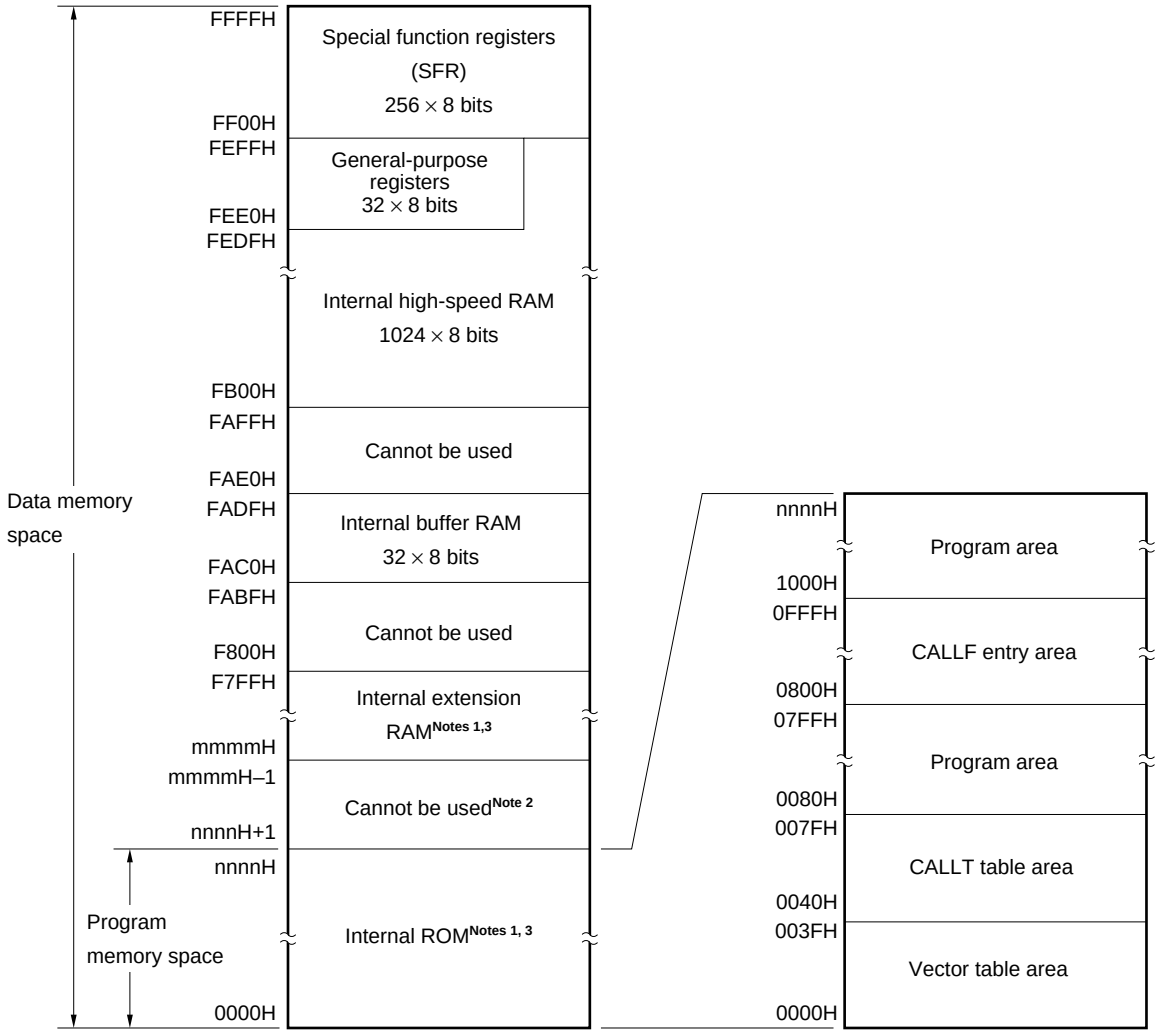
Note This switch is selectable in software only for the VCOL and VCOH pins.

Remark V_{DD} and GND are the positive power supply and ground pins for all port pins. Take V_{DD} and GND as V_{DD}PORT and GNDPORT.

2. MEMORY SPACE

Figure 2-1 shows the memory map of the μPD178076, 178078, 178096, and 178098.

Figure 2-1. Memory Map



Notes 1. The internal ROM and internal extension RAM capacities differ depending on the model (refer to the table below).

Target Model Name	Internal ROM End Address nnnnH	Internal Extension RAM First Address mmmmH
μPD178076, 178096	BFFFH	F400H
μPD178078, 178098	EFFFH	F000H

2. The μPD178078 and 178098 do not have this unusable area.

Note 3. The initial values of the memory size select register (IMS) and internal extension RAM size select register (IXS) are CFH and 0CH, respectively. The following values must be set to the registers of each model.

Part Number	IMS	IXS
μPD178076, 178096	CCH	0AH
μPD178078, 178098	CFH	08H

2.1 Memory Size Select Register (IMS)

This register is used to select the capacity of the internal memory.

Set CCH to this register of the μPD178076 and 178096. Set CFH to the IMS of the μPD178078 and 178098.

Use an 8-bit memory manipulation instruction to set the IMS.

This register is set to CFH at reset.

Figure 2-2. Format of Memory Size Select Register (IMS)

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
1	1	0	1024 bytes
Others			Setting prohibited

RAM3	RAM2	RAM1	RAM0	Selects internal ROM capacity
1	1	0	0	48K bytes
1	1	1	1	60K bytes
Others				Setting prohibited

2.2 Internal Extension RAM Size Select Register (IXS)

This register is used to select the capacity of the internal extension RAM.

Set 0AH of this register of the μPD178076 and 178096. Set 08H of the IXS of the μPD178078 and 178098.

Use an 8-bit memory manipulation instruction to set the IXS.

This register is set to 0CH at reset.

Figure 2-3. Format of Internal Extension RAM Size Select Register (IXS)

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selects internal extension RAM capacity
0	1	0	0	0	2048 bytes
0	1	0	1	0	1024 bytes
Others					Setting prohibited

3. FEATURES OF PERIPHERAL HARDWARE FUNCTIONS

3.1 Ports

The following three types of ports are available:

• CMOS input (port 1)	: 8 pins
• CMOS I/O (ports 0, 2 through 7, 10, and 12)	: 64 pins
• N-ch open-drain output (port 13)	: 8 pins
Total	: 80 pins

Table 3-1. Port Functions

Name	Pin Name	Function
Port 0	P00-P07	I/O port. Can be set in input or output mode in 1-bit units.
Port 1	P10-P17	Input-only port.
Port 2	P20-P27	I/O port. Can be set in input or output mode in 1-bit units.
Port 3	P30-P37	I/O port. Can be set in input or output mode in 1-bit units.
Port 4	P40-P47	I/O port. Can be set in input or output mode in 1-bit units.
Port 5	P50-P57	I/O port. Can be set in input or output mode in 1-bit units.
Port 6	P60-P67	I/O port. Can be set in input or output mode in 1-bit units.
Port 7	P70-P77	I/O port. Can be set in input or output mode in 1-bit units.
Port 10	P100-P102	I/O port. Can be set in input or output mode in 1-bit units.
Port 12	P120-P124	I/O port. Can be set in input or output mode in 1-bit units.
Port 13	P130-P137	N-ch open-drain output port.

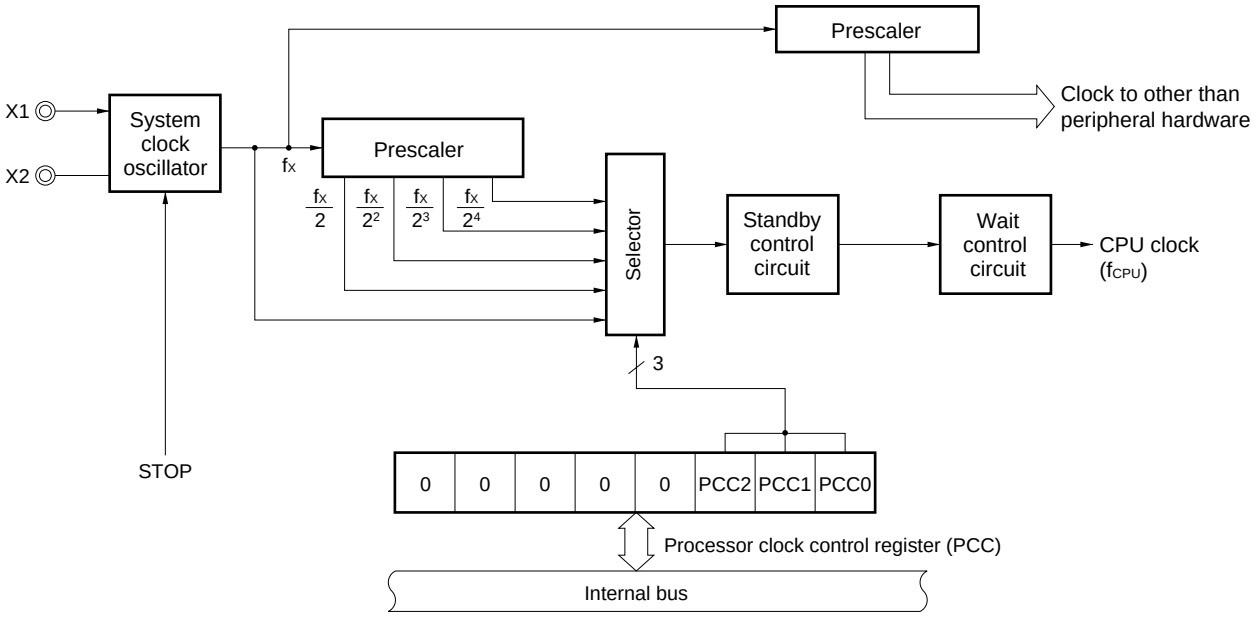
3.2 Clock Generation Circuit

The instruction execution time can be changed as follows:

- 0.32 μs/0.64 μs/1.27 μs/2.54 μs/5.08 μs (system clock: 6.3-MHz crystal resonator)
- 0.44 μs/0.89 μs/1.78 μs/3.56 μs/7.11 μs (system clock: 4.5-MHz crystal resonator)**Note**

Note When using the IEBus controller of the μPD178096 and 178098, the 4.5-MHz crystal resonator cannot be used. Use the 6.3-MHz crystal resonator.

Figure 3-1. Block Diagram of Clock Generation Circuit

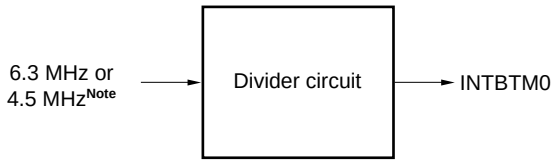


3.3 Timers

Five timer channels are provided.

- Basic timer : 1 channel
- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watchdog timer : 1 channel

Figure 3-2. Block Diagram of Basic Timer



Note When using the IEBus controller of the μPD178096 and 178098, the 4.5-MHz crystal resonator cannot be used. Use the 6.3-MHz crystal resonator.

Figure 3-3. Block Diagram of 16-Bit Timer/Event Counter

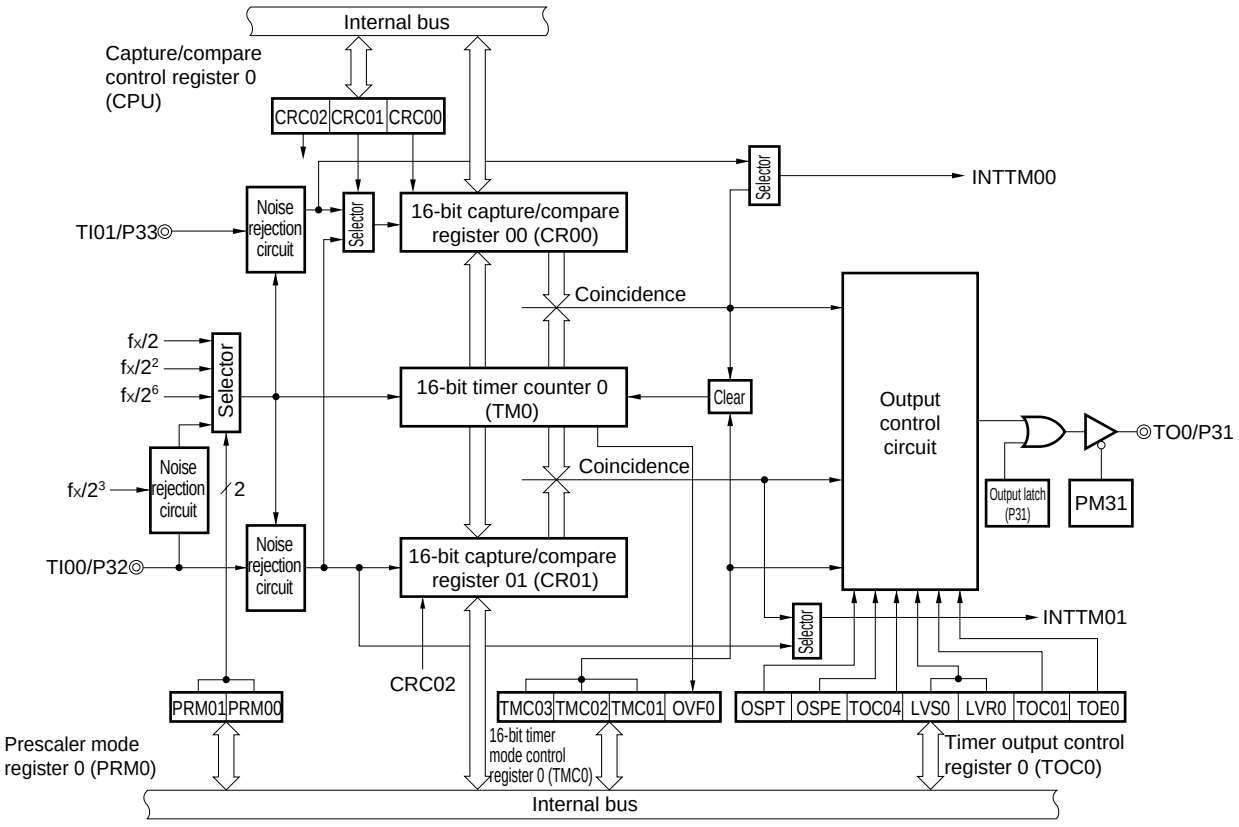


Figure 3-4. Block Diagram of 8-Bit Timer/Event Counter 50

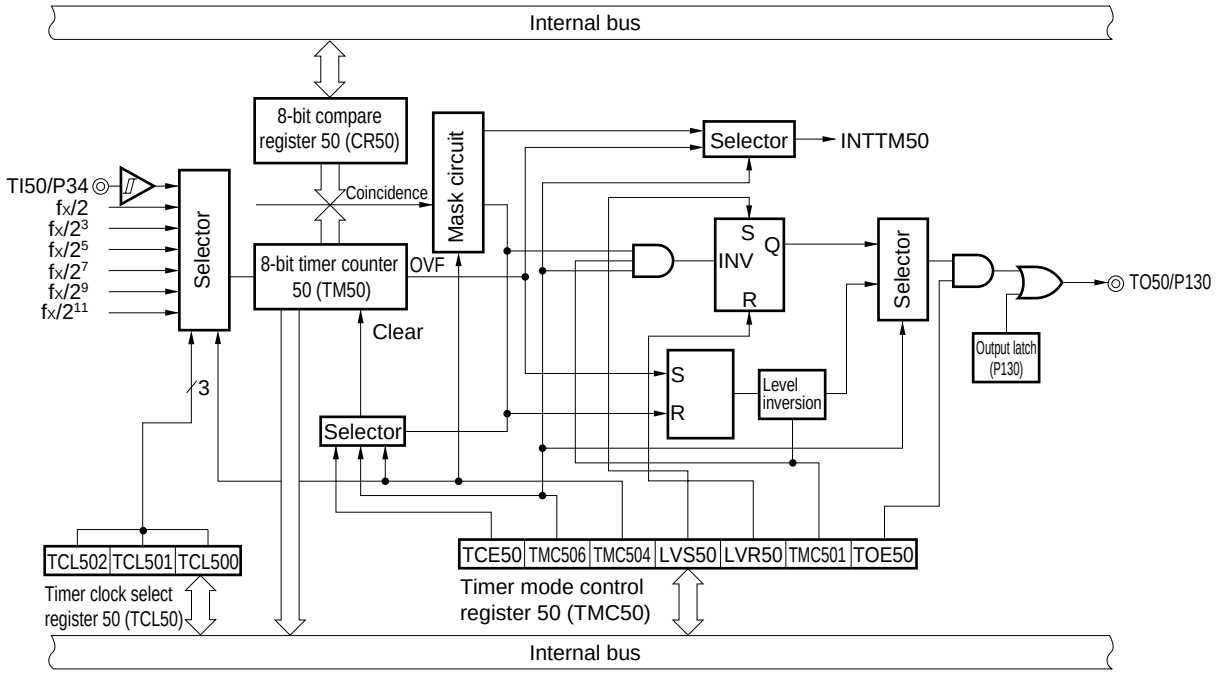


Figure 3-5. Block Diagram of 8-Bit Timer/Event Counter 51

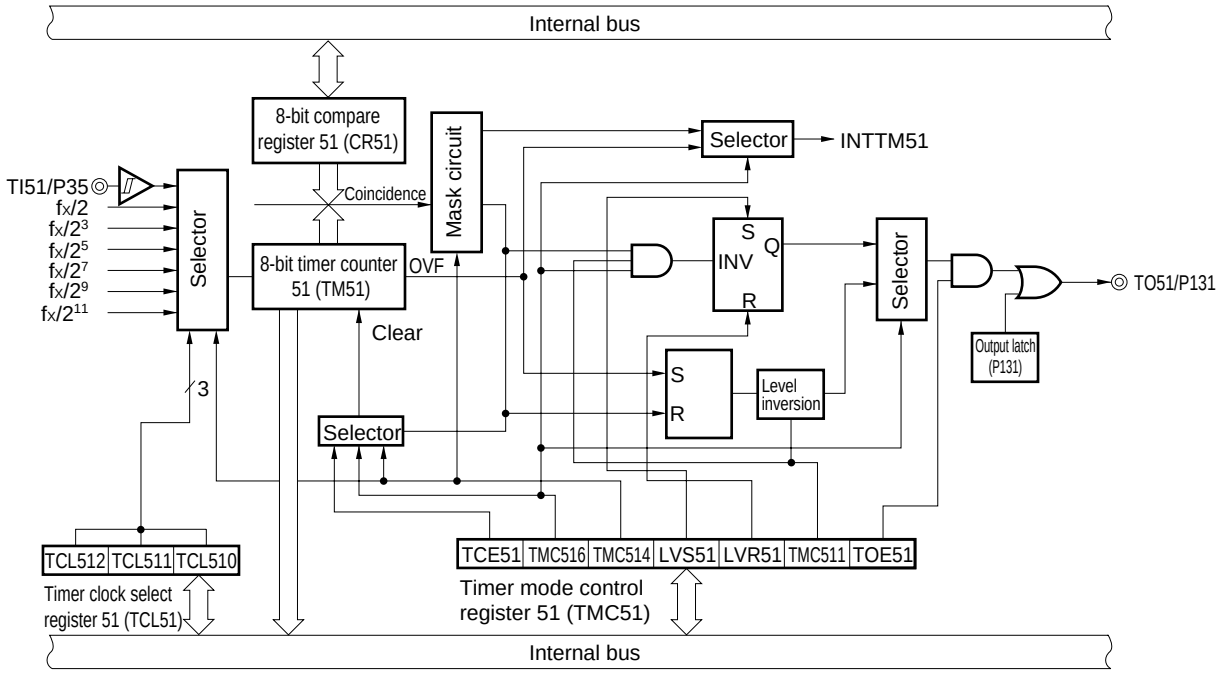
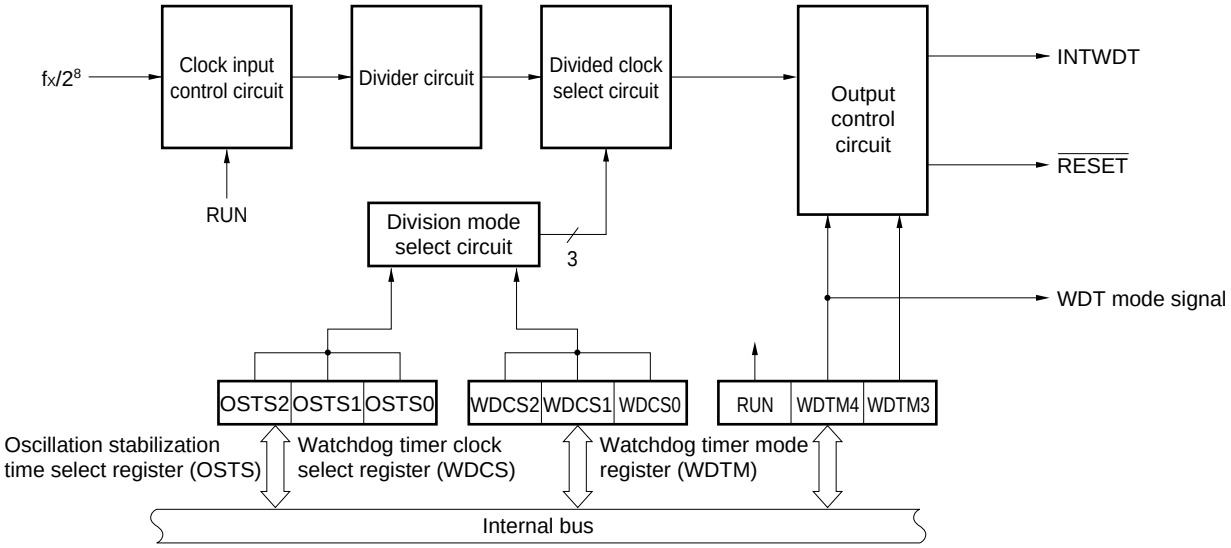


Figure 3-6. Block Diagram of Watchdog Timer



3.4 Buzzer Output Control Circuit

Two types of buzzer output control circuits are provided.

- BEEP0 ... 1 kHz/1.5 kHz/3 kHz/4 kHz
- BUZ ... 0.77 kHz/1.54 kHz/3.08 kHz/6.15 kHz (system clock: 6.3-MHz crystal resonator)

Figure 3-7. Block Diagram of Buzzer Output Control Circuit (BEEP0)

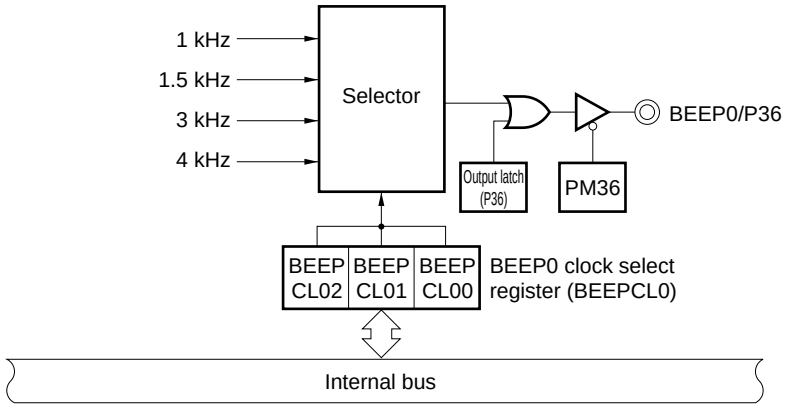
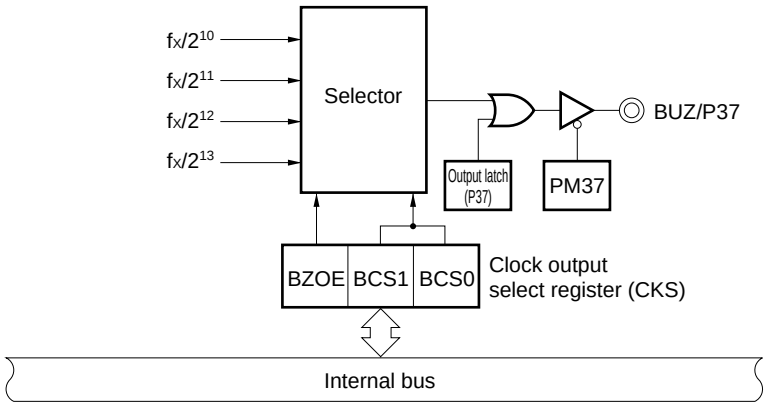


Figure 3-8. Block Diagram of Buzzer Output Control Circuit (BUZ)

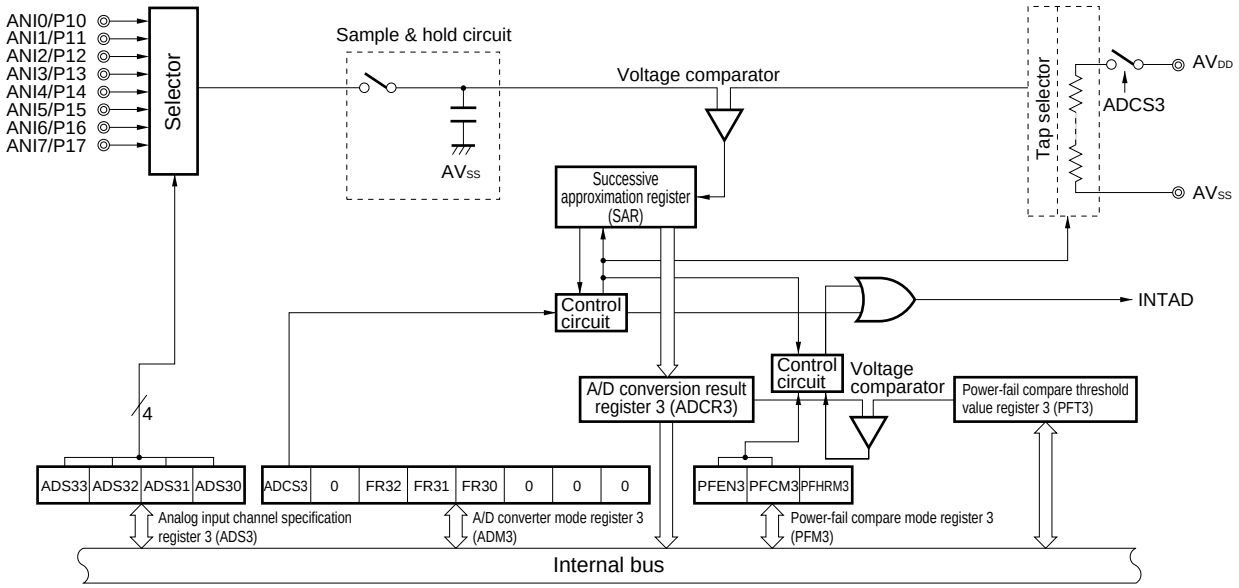


Remark fX: System clock frequency

3.5 A/D Converter

An A/D converter with a resolution of 8 bits × 8 channels is provided.

Figure 3-9. Block Diagram of A/D Converter



3.6 Serial Interface

The μPD178076 and 178078 have four serial interface channels, and the μPD178096 and 178098 have three channels.

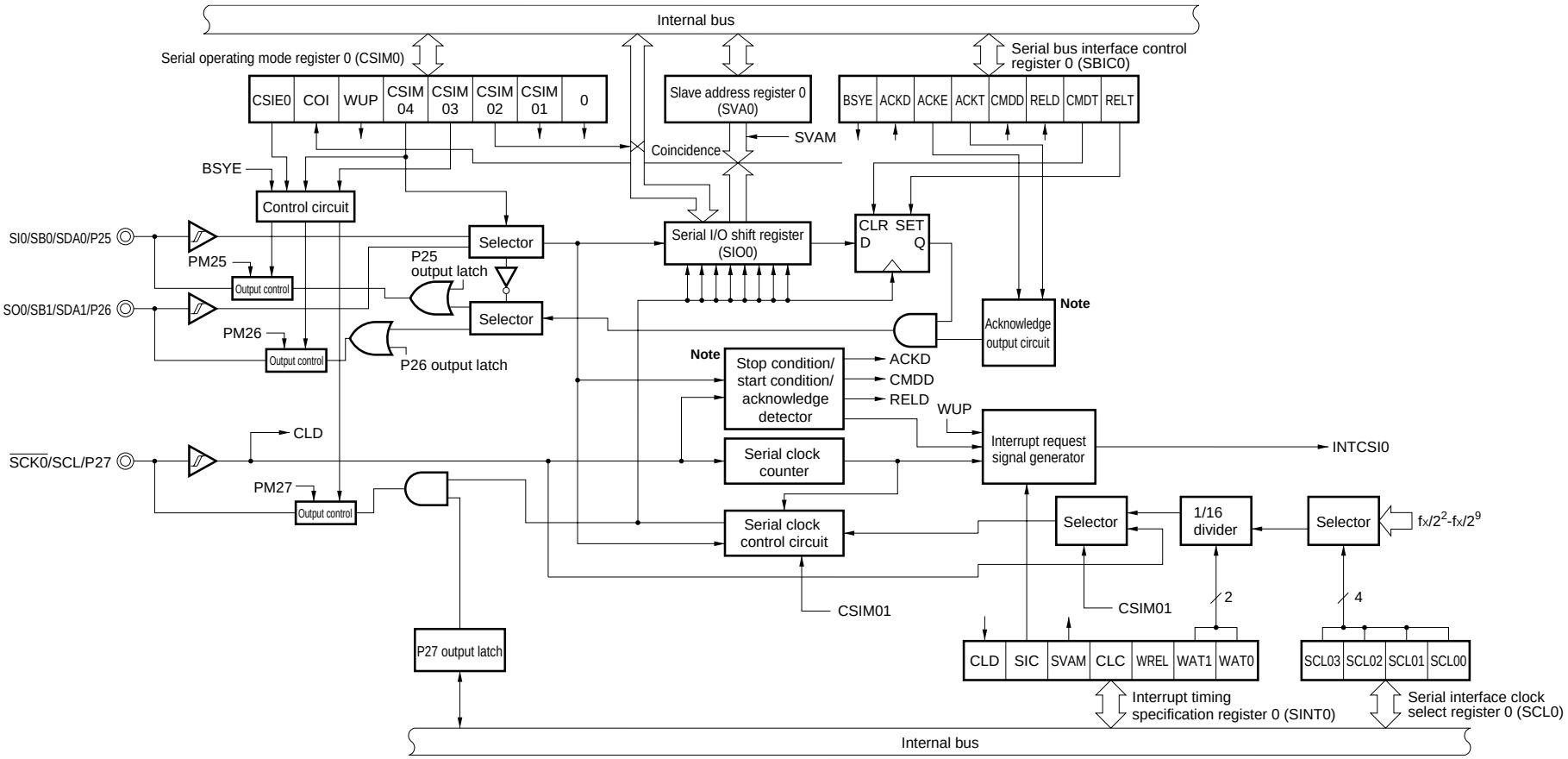
- Serial interface 0
- Serial interface 1
- Serial interface 3
- Serial interface UART0: μPD178076 and 178078 only

Table 3-2. Types and Functions of Serial Interfaces

Function	Serial interface 0	Serial interface 1	Serial interface 3	UART0[Note]
3-wire serial I/O mode	○ (MSB/LSB first selectable)	○ (MSB/LSB first selectable)	○ (MSB first)	–
3-wire serial I/O mode with automatic transmit/receive function	–	○ (MSB/LSB first selectable)	–	–
SBI (serial bus interface) mode	○ (MSB first)	–	–	–
2-wire serial I/O mode	○ (MSB first)	–	–	–
I^2C bus mode	○ (MSB first)	–	–	–
UART (asynchronous serial interface) mode	–	–	–	○ (Dedicated baud rate generator)

Note μPD178076 and 178078 only.

Figure 3-10. Block Diagram of Serial Interface 0



Note Example in I²C bus mode operation.

Remark Output Control performs selection between CMOS output and N-ch open drain output.

Figure 3-11. Block Diagram of Serial Interface 1

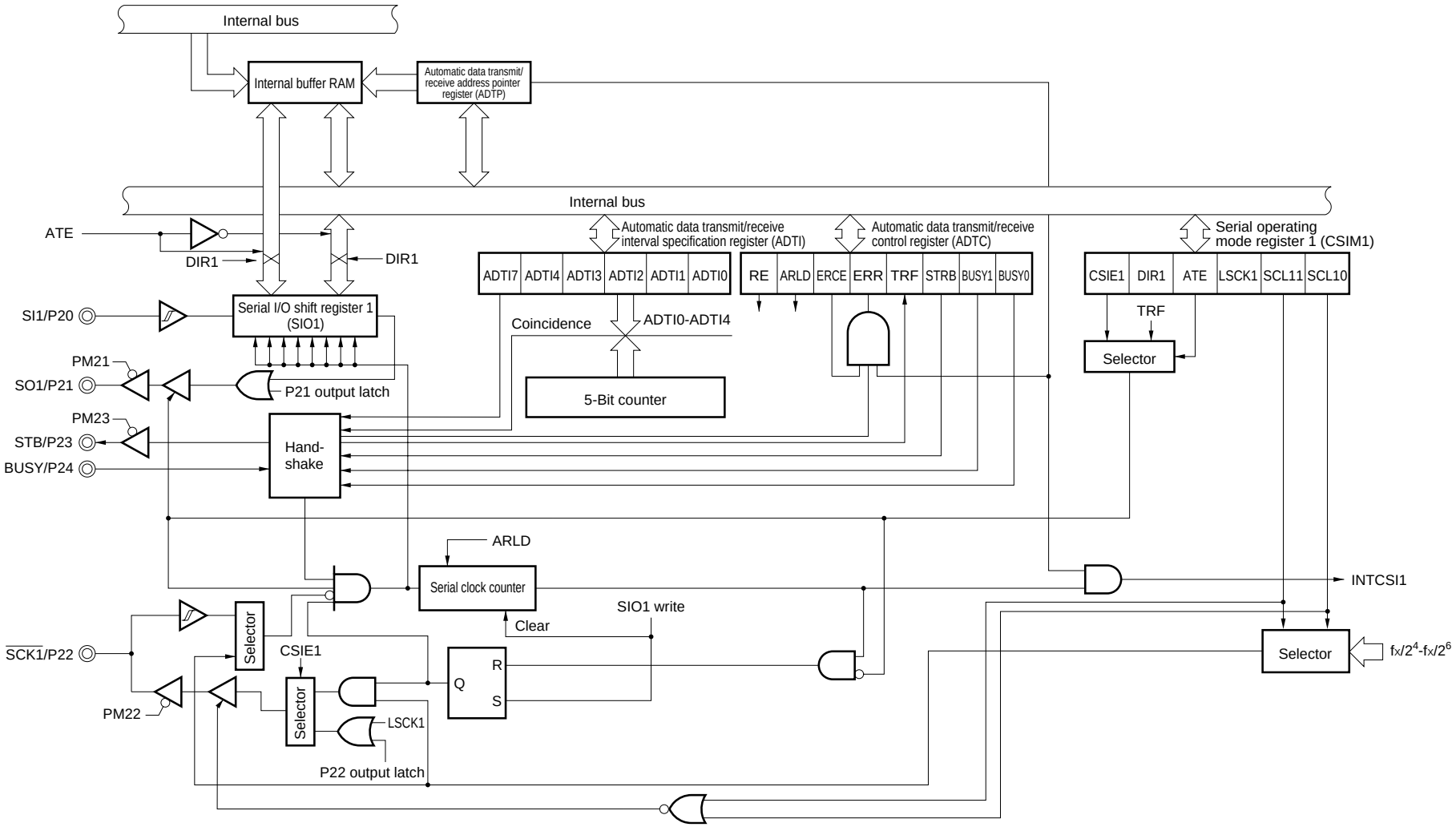
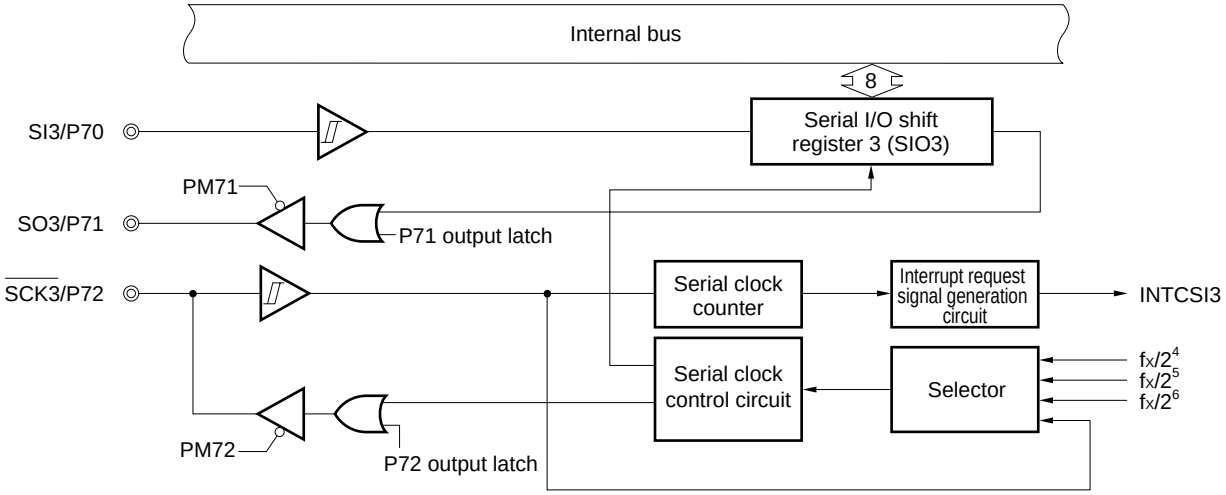
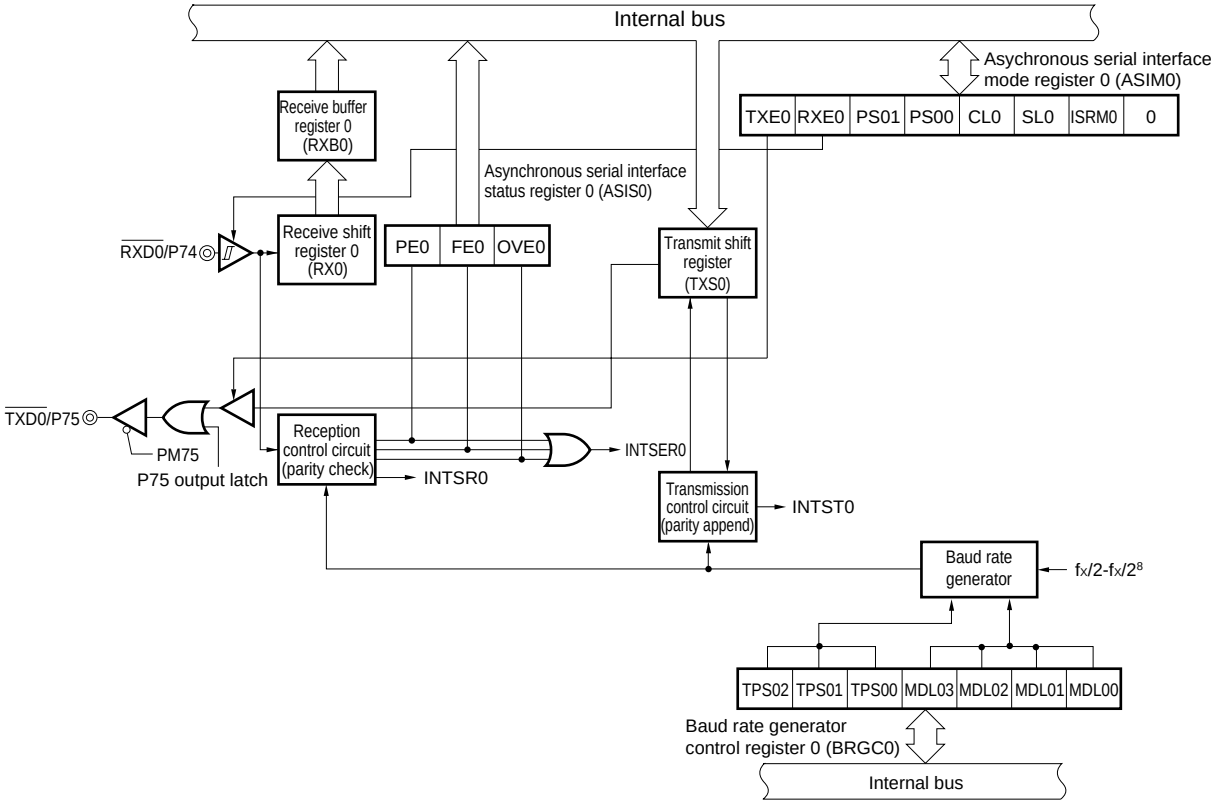


Figure 3-12. Block Diagram of Serial Interface 3



★ **Figure 3-13. Block Diagram of Serial Interface UART0 (μPD178076 and 178078 only)**



3.7 IEBus Controller (μPD178096 and 178098 only)

The μPD178096 and 178098 have an IEBus controller. The functions of this IEBus controller are limited as compared with the existing IEBus interface functions of the μPD78098 subseries.

Table 3-3 compares the interfaces of the μPD78098 subseries and μPD178098 subseries.

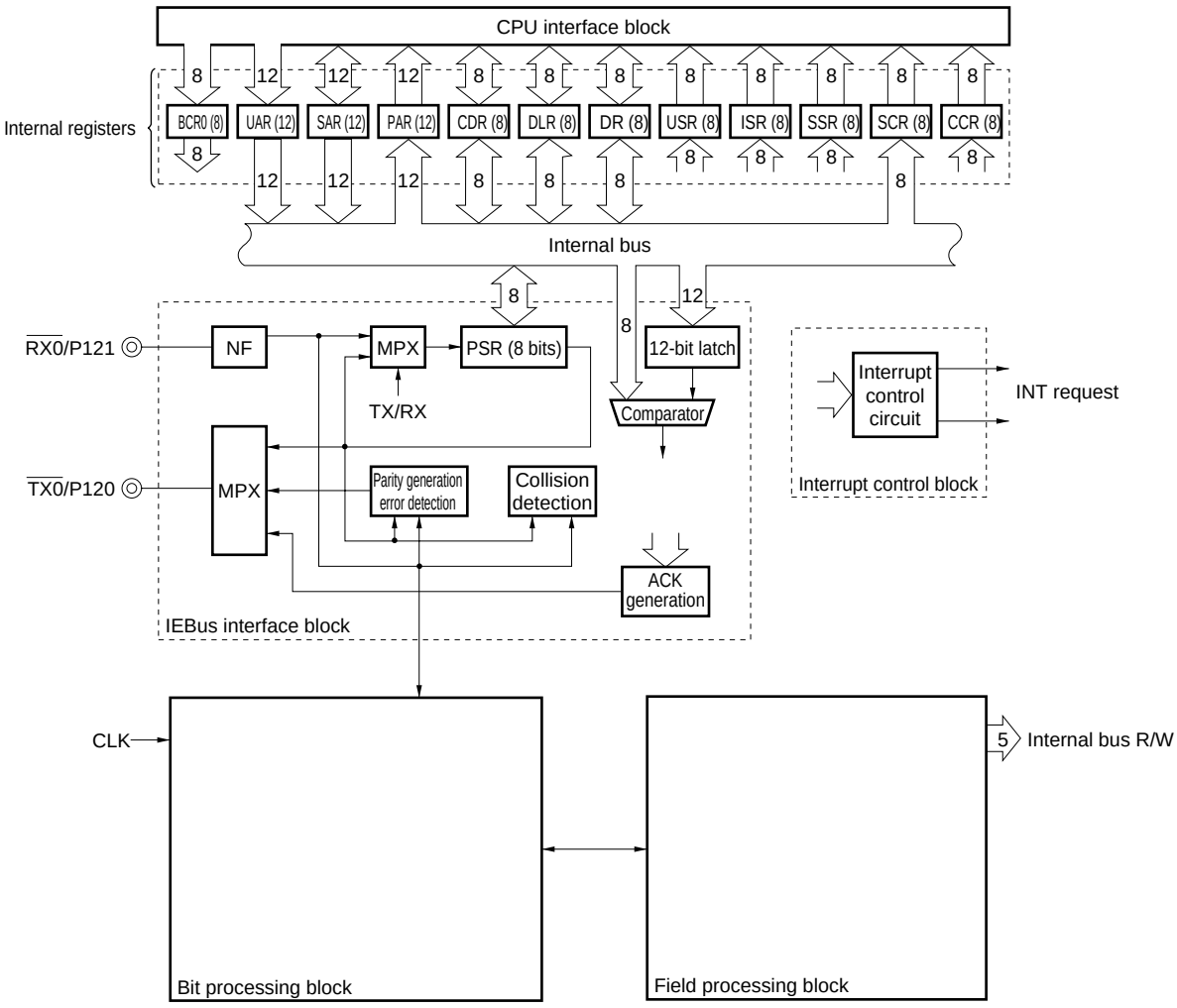
Table 3-3. Comparison of IEBus Interface (between μPD78098 Subseries and μPD178098 Subseries)

Item	μPD78098 Subseries IEBus	μPD178098 Subseries IEBus
Communication mode	Modes 0, 1, and 2	Fixed to mode 1
Internal system clock	f_X = 6.0 (6.29) MHz	f_X = 6.3 MHz[Note]
Internal buffer size	Transmit buffer: 33 bytes (FIFO) Receive buffer: 40 bytes (FIFO) Up to 4 frames can be received.	Transmit buffer: 1 byte Receive buffer: 1 byte
CPU processing	Communication start processing (data setting) Setting and management of each communication status Writing data to transmit buffer Reading data from receive buffer	Communication start processing (data setting) Setting and management of each communication status Writing data per 1 byte Reading data per 1 byte Management of transmission such as slave status Management of multiple frames, re-master request processing
Hardware processing	Bit processing (modulation/demodulation, error detection) Field processing (generation/management) Arbitration result detection Parity processing (generation/error detection) Automatic answering of ACK/NACK Automatic data re-transmission processing Automatic re-master processing Transmission processing such as automatic slave status Multiple frame reception processing	Bit processing (modulation/demodulation, error detection) Field processing (generation/management) Arbitration result detection Parity processing (generation/error detection) Automatic answering of ACK/NACK Automatic data re-transmission processing

Note The IEBus controller of the μPD178098 subseries operates at f_X = 6.3 MHz, and not at f_X = 4.5 MHz.

Remark f_X: System clock frequency

Figure 3-14. Block Diagram of IEBus Controller (μPD178096 and 178098 only)



The IEBus mainly consists of the following six internal blocks:

- CPU interface block
- Interrupt control block
- Internal registers
- Bit processing block
- Field processing block
- IEBus interface block

<CPU interface block>
This block interfaces between the CPU (78K/0) and IEBus.

<Interrupt control block>
This block passes interrupt request signals from the IEBus to the CPU.

<Internal registers>
These are control registers that are used to control the IEBus and settings of each field.

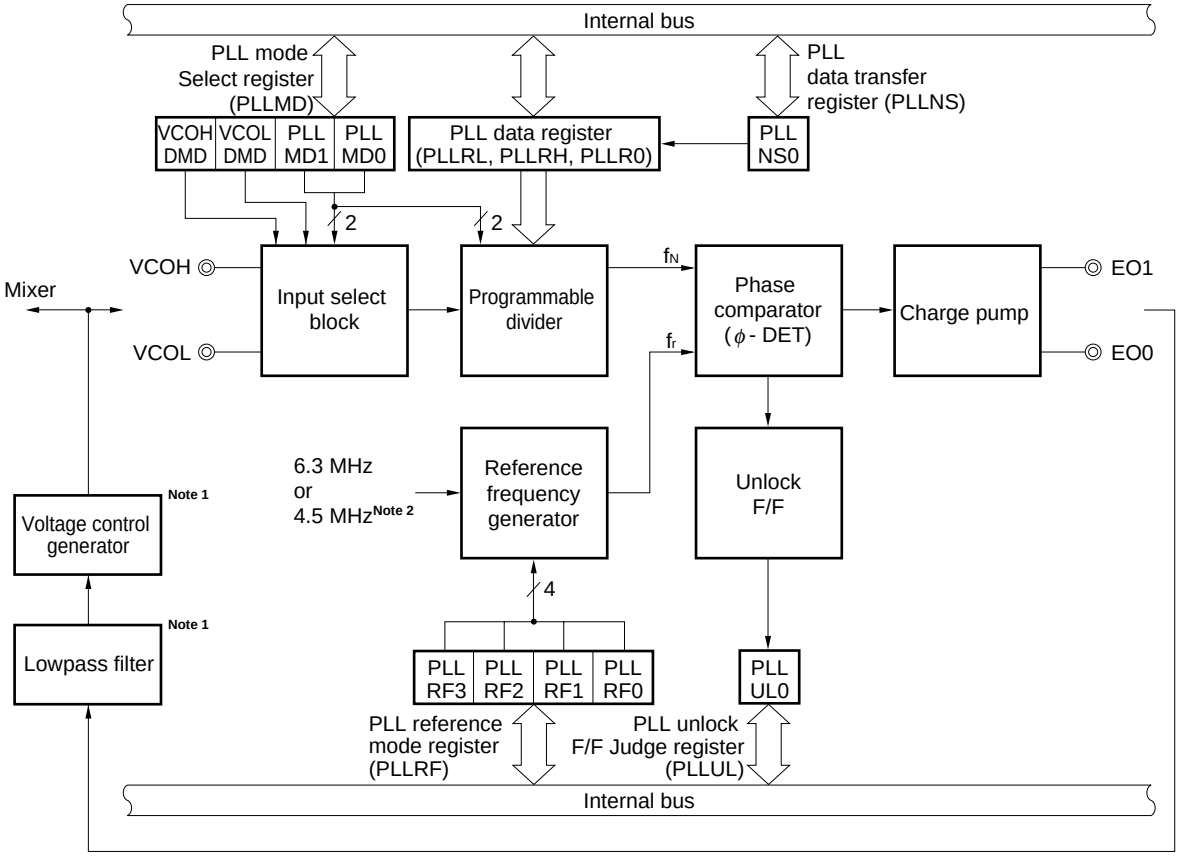
<Bit processing block>
This block generates and disassembles bit timing, and mainly consists of a bit sequence ROM, 8-bit preset timer, and decision unit.

<Field processing block>
This block generates each field in a communication frame and mainly consists of a field sequence ROM, 4-bit down counter, and decision unit.

<IEBus interface block>
This is the interface block for an external driver/receiver, and mainly consists of a noise filter, shift register, collision detector, parity detector, parity generation circuit, and ACK/NACK generation circuit.

3.8 PLL Frequency Synthesizer

Figure 3-15. Block Diagram of PLL Frequency Synthesizer

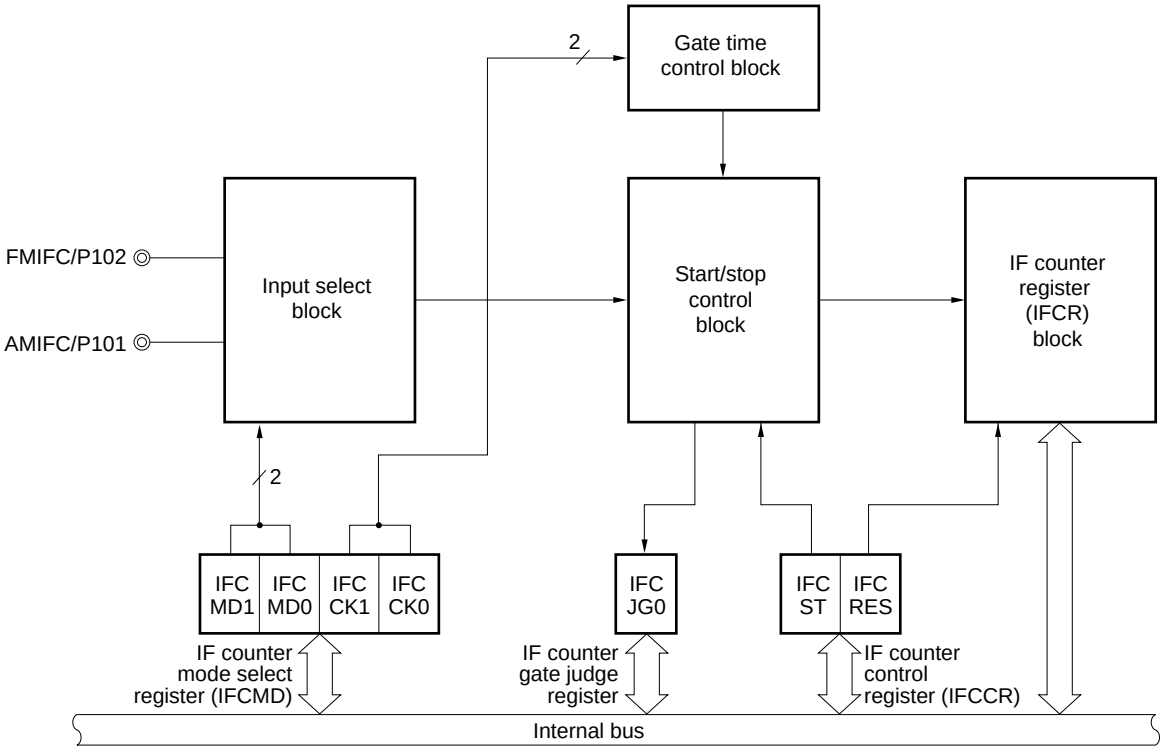


Notes 1. These are external circuits.

2. When the IEBus controller of the μPD178096 and 178098 is used, the 4.5-MHz crystal resonator cannot be used. Use the 6.3-MHz crystal resonator.

3.9 Frequency Counter

Figure 3-16. Block Diagram of Frequency Counter



4. INTERRUPT FUNCTION

(1) μPD178076 and 178078

The μPD178076 and 178078 have the following three types and 22 sources of interrupts:

- Non-maskable : 1[Note]
- Maskable : 21[Note]
- Software : 1

Note Two types of watchdog interrupt sources (INTWDT), non-maskable and maskable, are available, and either of them can be selected.

Table 4-1. Interrupt Sources (μPD178076 and 178078) (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTP7			0014H	
	9	INTCSI0	End of transfer by serial interface 0	Internal	0016H	(B)
	10	INTCSI1	End of transfer by serial interface 1		0018H	
	11	INTCSI3	End of transfer by serial interface 3		001AH	
	12	INTTM50	Generation of coincidence signal of 8-bit timer/event counter 50		001CH	
	13	INTTM51	Generation of coincidence signal of 8-bit timer/event counter 51		001EH	
	14	INTSER0	Reception error of serial interface UART0		0020H	
	15	INTSR0	End of reception by serial interface UART0		0022H	
	16	INTST0	End of transmission by serial interface UART0		0024H	
	17	INTBTM0	Generation of coincidence signal of basic timer		0026H	

Notes 1. If two or more maskable interrupts occur at the same time, they are acknowledged or kept pending according to their default priorities. The default priority 0 is the highest, while 22 is the lowest.

2. (A) to (E) under the heading Basic Configuration Type corresponds to (A) to (E) in Figure 4-1.

Table 4-1. Interrupt Sources (μPD178076 and 178078) (2/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	18	INTTM00	Generation of signal indicating coincidence between 16-bit timer counter (TM0) and capture/compare register (CR00) (when CR00 is used as compare register)	Internal	0028H	(B)
			Detection of input edge of TI00/P32 pin (when CR00 is used as capture register)	External		(D)
	19	INTTM01	Generation of signal indicating coincidence between 16-bit timer counter (TM0) and capture/compare register (CR01) (when CR01 is used as compare register)	Internal	002AH	(B)
			Detection of input edge of TI01/P33 pin (when CR01 is used as capture register)	External		(D)
	20	–	–	–	Note 3	–
	21	–	–		Note 3	
	22	INTAD	End of conversion by A/D converter	Internal	0030H	(B)
Software	–	BRK	Execution of BRK instruction	–	003EH	(E)

Notes 1. If two or more maskable interrupts occur at the same time, they are acknowledged or kept pending according to their default priorities. The default priority 0 is the highest, while 22 is the lowest.

2. (A) to (E) under the heading Basic Configuration Type corresponds to (A) to (E) in Figure 4-1.

3. There are no interrupt sources corresponding to vector addresses 002CH and 002EH.

(2) μPD178096 and 178098

The μPD178096 and 178098 have the following three types and 21 sources of interrupts:

- Non-maskable : 1[Note]
- Maskable : 20[Note]
- Software : 1

Note Two types of watchdog interrupt sources (INTWDT), non-maskable and maskable, are available, and either of them can be selected.

Table 4-2. Interrupt Sources (μPD178096 and 178098) (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTP7			0014H	
	9	INTCSI0	End of transfer by serial interface 0	Internal	0016H	(B)
	10	INTCSI1	End of transfer by serial interface 1		0018H	
	11	INTCSI3	End of transfer by serial interface 3		001AH	
	12	INTTM50	Generation of coincidence signal of 8-bit timer/event counter 50		001CH	
	13	INTTM51	Generation of coincidence signal of 8-bit timer/event counter 51		001EH	
	14	–	–	–	Note 3	–
	15	–	–		Note 3	
	16	–	–		Note 3	
	17	INTBTM0	Generation of coincidence signal of basic timer	Internal	0026H	(B)

Notes 1. If two or more maskable interrupts occur at the same time, they are acknowledged or kept pending according to their default priorities. The default priority 0 is the highest, while 22 is the lowest.

2. (A) to (E) under the heading Basic Configuration Type corresponds to (A) to (E) in Figure 4-1.

3. There are no interrupt sources corresponding to vector addresses 0020H, 0022H, and 0024H.

Table 4-2. Interrupt Sources (μPD178096 and 178098) (2/2)

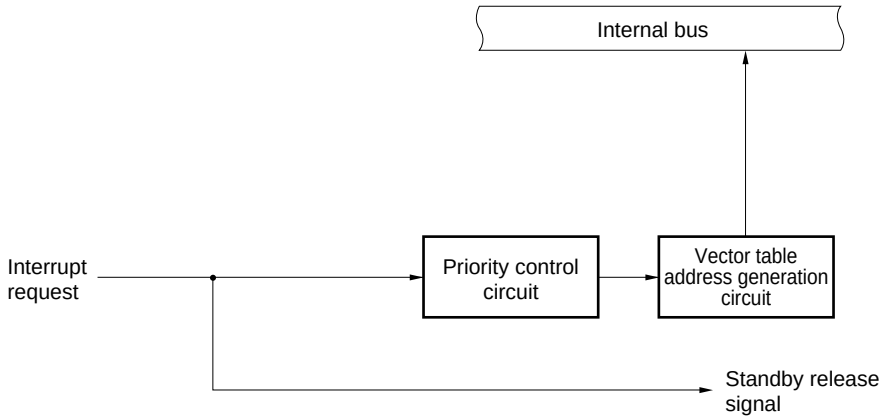
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	18	INTTM00	Generation of signal indicating coincidence between 16-bit timer counter (TM0) and capture/compare register (CR00) (when CR00 is used as compare register)	Internal	0028H	(B)
			Detection of input edge of TI00/P32 pin (when CR00 is used as capture register)	External		(D)
	19	INTTM01	Generation of signal indicating coincidence between 16-bit timer counter (TM0) and capture/compare register (CR01) (when CR01 is used as compare register)	Internal	002AH	(B)
			Detection of input edge of TI01/P33 pin (when CR01 is used as capture register)	External		(D)
	20	INTIE1	IEBus0 data access request	Internal	002CH	(B)
	21	INTIE2	IEBus0 communication error and start/end of communication		002EH	
	22	INTAD	End of conversion by A/D converter AD1		0030H	(B)
Software	–	BRK	Execution of BRK instruction	–	003EH	(E)

Notes 1. If two or more maskable interrupts occur at the same time, they are acknowledged or kept pending according to their default priorities. The default priority 0 is the highest, while 22 is the lowest.

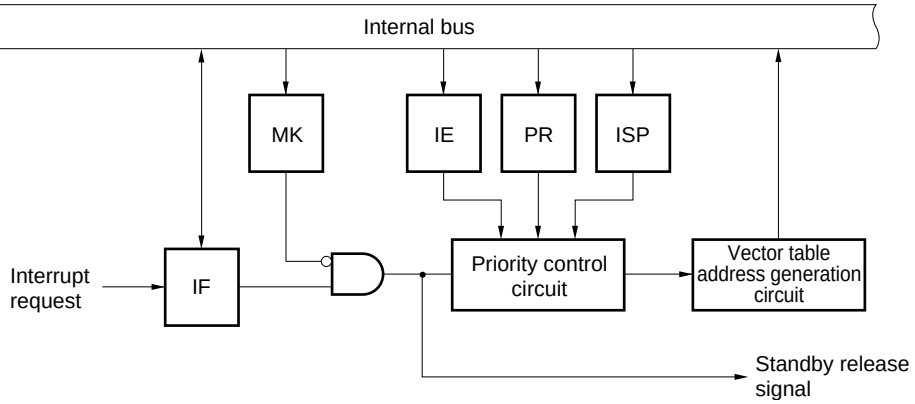
2. (A) to (E) under the heading Basic Configuration Type corresponds to (A) to (E) in Figure 4-1.

Figure 4-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 through INTP7)

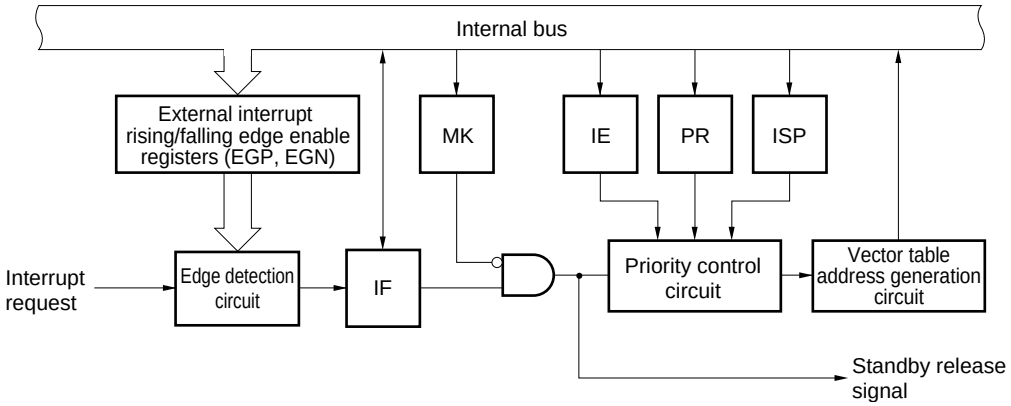
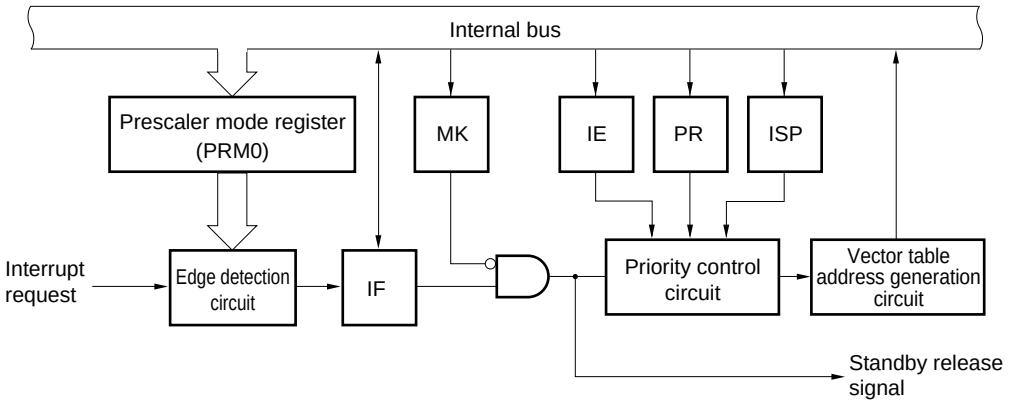
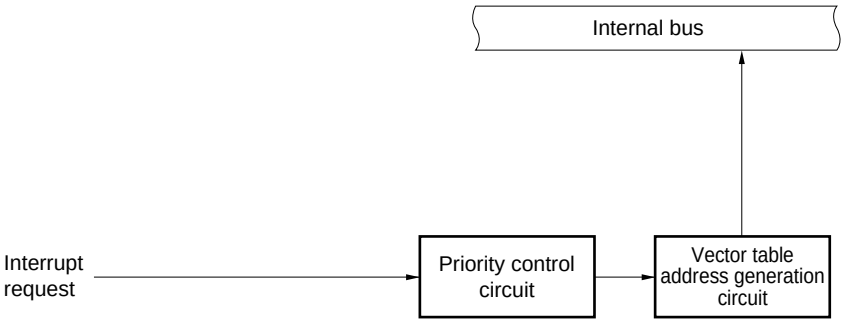


Figure 4-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupts (INTTM00, INTTM01)



(E) Software interrupt



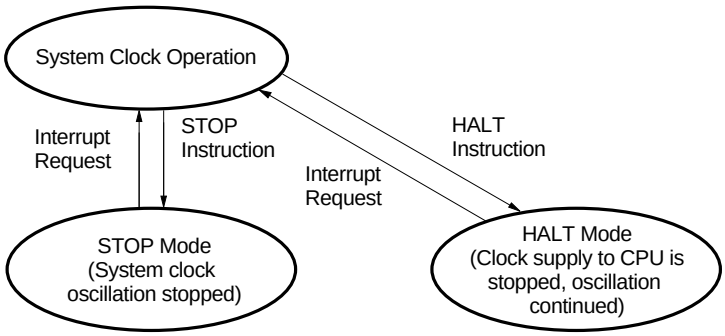
Remark IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

5. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operating clock is stopped.
  The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The system clock oscillation is stopped. All operations by the system clock are stopped and current consumption can be considerably reduced.

Figure 5-1. Standby Function



6. RESET FUNCTION

There are the following three reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer hang-up time detection
- Internal reset by Power-On Clear (POC).

7. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B,C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +6.0	V
	V_{DD}PORT			–0.3 to V_{DD} + 0.3 Note 1	V
	AV_{DD}			–0.3 to V_{DD} + 0.3 Note 1	V
	V_{DD}PLL			–0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	Excluding P130 to P137		–0.3 to V_{DD} + 0.3	V
Output breakdown voltage	V_{BDS}	P130-P137	N-ch open drain	16	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin		–8	mA
★		Total of P00-P01, P20-P27, P50-P57, and P70-P73		–15	mA
★		Total of P02-P07, P30-P37, P40-P47, P60-P67, P74-P77, and P120-P124		–15	mA
		Total of P100-P102		–10	mA
Low-level output current	I_{OL} Note 2	1 pin	Peak value	16	mA
			r.m.s	8	mA
★		Total of P00-P01, P20-P27, P50-P57, and P70-P73	Peak value	30	mA
			r.m.s	15	mA
★		Total of P02-P07, P30-P37, P40-P47, P60-P67, P74-P77, P120-P124, and P130-P137	Peak value	30	mA
			r.m.s	15	mA
		Total of P100-102	Peak value	20	mA
			r.m.s	10	mA
Operating temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–55 to +125	°C

★ **Notes 1.** Keep the voltage at V_{DD}PORT, AV_{DD}, and V_{DD}PLL same as that at the V_{DD} pin.

2. Calculate the r.m.s as follows: [r.m.s] = [Peak value] x $\sqrt{\text{Duty}}$

Caution If the rated value of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, are the values exceeding which the product may be physically damaged. Be sure to use the product with these ratings never being exceeded.

Remark Unless otherwise specified, the characteristics of a multiplexed pin are the same as those of the corresponding port pin.

Recommended Supply Voltage Ranges (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD1}	When CPU and PLL are operating	4.5	5.0	5.5	V
	V_{DD2}	When CPU is operating and PLL is stopped	3.5	5.0	5.5	V
Data retention voltage	V_{DDR}	When crystal oscillation stops	2.3		5.5	V
Output breakdown voltage	V_{BDS}	P130-P137 (N-ch open drain)			15	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P10-P17, P21, P23, P30, P31, P36, P37, P40-P47, P50-P57, P60-P67, P71, P73, P75-P77, P100-P102, P120, P122-P124		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P07, P20, P22, P24-P27, P32-P35, P70, P72, P74, P121, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	P10-P17, P21, P23, P30, P31, P36, P37, P40-P47, P50-P57, P60-P67, P71, P73, P75-P77, P100-P102, P120, P122-P124		0		0.3 V_{DD}	V
	V_{IL2}	P00-P07, P20, P22, P24-P27, P32-P35, P70, P72, P74, P121, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
High-level output voltage	V_{OH1}	P00-P07, P20-P24, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P100-P102, P120-P124	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
	V_{OH2}	EO0, EO1	V_{DD} = 4.5 to 5.5 V, I_{OH} = –3 mA	V_{DD} – 1.0			V
Low-level output voltage	V_{OH1}	P00-P07, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P100-P102, P120-P124, P130-P137,	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1 mA			1.0	V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OL} = 100 μA			0.5	V
★	V_{OL2}	EO0, EO1	V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA			1.0	V
High-level input leakage current	I_{LIH}	P00-P07, P10-P17, P20-P24, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P100-P102, P120-P124, $\overline{\text{RESET}}$	V_I = V_{DD}			3	μA

Remark Unless otherwise specified, the characteristics of a multiplexed pin are the same as those of the corresponding port pin.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level input leakage current	I_{LIL}	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P100-P102, P120-P124, $\overline{\text{RESET}}$	V_I = 0 V			–3	μA
Output off leakage current	I_{LOH1}	P130-P137	V_O = 15 V			–3	μA
	I_{LOL1}	P130-P137	V_O = 0 V			3	μA
	I_{LOH2}	P25-P27 (at N-ch open drain I/O)	V_O = V_{DD}			–3	μA
	I_{LOL2}	P25-P27 (at N-ch open drain I/O)	V_O = 0 V			3	μA
	I_{LOH3}	EO0, EO1	V_O = V_{DD}			–3	μA
	I_{LOL3}	EO0, EO1	V_O = 0 V			3	μA
Supply current[Note]	I_{DD1}	When CPU is operating and PLL is stopped. Sine wave input to X1 pin V_I = V_{DD}	fx = 4.5 MHz (μPD178076, 178078)		2.5	15	mA
	I_{DD2}		fx = 6.3 MHz (μPD178076, 178078, 178096, 178098)		4.0	20	mA
★	I_{DD3}	In HALT mode with PLL stopped. Sine wave input to X1 pin V_I = V_{DD}	fx = 4.5 MHz (μPD178076, 178078)		0.2	0.8	mA
★	I_{DD4}		fx = 6.3 MHz (μPD178076, 178078, 178096, 178098)		0.3	1.0	mA
Data retention voltage	V_{DDR1}	When crystal resonator is oscillating		3.5		5.5	V
	V_{DDR2}	When crystal oscillation is stopped	Power-failure detection function	2.2			V
	V_{DDR3}		Data memory retained	2.0			V
Data retention current	I_{DDR1}	When crystal oscillation is stopped	T_A = 25°C, V_{DD} = 5 V		2.0	4.0	μA
	I_{DDR2}				2.0	20	μA

Note Excluding AV_{DD} current and V_{DD}PLL current.

Remarks 1. fx: System clock oscillation frequency

2. Unless otherwise specified, the characteristics of a multiplexed pin are the same as those of the corresponding port pin.

Reference Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	Supply current	I_{DD5}	When CPU and PLL are operating. Sine wave input to VCOH pin At f_{IN} = 160 MHz, V_{IN} = 0.15 V_{P-P}		5		mA

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	At f_X = 6.3 MHz	0.32		5.08	μs
		At f_X = 4.5 MHz**Note 1**	0.44		7.11	μs
TI00, TI01 input high-/low-level widths	t_{TIH0}, t_{TIL0}		4/fsam**Note 2**			s
TI50, TI51 input frequency	f_{TI5}				2	MHz
TI50, TI51 input high-/low-level widths	t_{TIH5}, t_{TIL5}		200			ns
Interrupt input high-/low-level widths	t_{INTH}, t_{INTL}	INTP0-INTP7	1			μs
$\overline{\text{RESET}}$ pin low-level width	t_{RSL}		10			μs

Notes 1. When the IEBus controller of the μPD178096 and 178098 is used, the 4.5-MHz crystal resonator cannot be used. Use the 6.3-MHz crystal resonator.

2. f_{sam} = f_X/2, f_X/4, f_X/64 selectable by bits 0 and 1 (PRM00 and PRM01) of the prescaler mode register 0 (PRM0). However, f_{sam} = f_X/8 when the valid edge of TI00 is selected as the count clock.

(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)

(a) Serial interface 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	$t_{KCY1}/2$ – 50			ns
			$t_{KCY1}/2$ – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF Note			300	ns

Note C is the load capacitance of $\overline{SCK0}$ and SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF Note			300	ns
$\overline{SCK0}$ at rising or falling edge time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 5.5 V		$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO3}	R = 1 kΩ C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1$\downarrow$ from $\overline{SCK0}\uparrow$	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1$\downarrow$	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of $\overline{SCK0}$, SB0 and SB1 output line.

(iv) SBI mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 5.5 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO4}	R = 1 kΩ C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1$\downarrow$ from $\overline{SCK0}\uparrow$	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1$\downarrow$	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ at rising or falling edge time	t_{R4}, t_{F4}					1000	ns

Note R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ		1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}	C = 100 pF Note		$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		V_{DD} = 4.5 to 5.5 V	300			ns
				350			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}			0		300	ns

Note R and C are the load resistance and load capacitance of $\overline{SCK0}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ	V_{DD} = 4.5 to 5.5 V	0		300	ns
		C = 100 pF Note		0		500	ns
$\overline{SCK0}$ at rising or falling edge time	t_{R6}, t_{F6}					1000	ns

Note R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(vii) I²C Bus mode (SCL ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY7}	R = 1 kΩ		10			μs
SCL high-level width	t_{KH7}	C = 100 pF Note		t_{KCY7} – 160			ns
SCL low-level width	t_{KL7}			t_{KCY7} – 50			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK7}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI7}			0			ns
SDA0, SDA1 output delay time (from SCL↓)	t_{KSO7}		V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of SCL, SDA0 and SDA1 output line.

(viii) I²C Bus mode (SCL ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY8}			1000			ns
SCL high-/low-level width	t_{KH8}, t_{KL8}			400			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK8}			200			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI8}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO8}	R = 1 kΩ	V_{DD} = 4.5 to 5.5 V	0		300	ns
		C = 100 pF Note		0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns
SCL at rising or falling edge time	t_{R8}, t_{F8}					1000	ns

Note R and C are the load resistance and load capacitance of SDA0 and SDA1 output line.

(b) Serial interface 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}, t_{KL9}		$t_{KCY9}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK9}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI9}		400			ns
SO1 output delay time (from $\overline{SCK1}\downarrow$)	t_{KSO9}	C = 100 pF Note			300	ns

Note C is the load capacitance of $\overline{SCK1}$ and SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI10}		400			ns
SO1 output delay time (from $\overline{SCK1}\downarrow$)	t_{KSO10}	C = 100 pF Note			300	ns
$\overline{SCK1}$ at rising or falling edge time	t_{R10}, t_{F10}				1000	ns

Note C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY11}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH11}, t_{KL11}		$t_{KCY11}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK11}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI11}		400			ns
SO1 output delay time (from $\overline{SCK1}\downarrow$)	t_{KSO11}	C = 100 pF Note			300	ns
STB$\uparrow$ from $\overline{SCK1}\uparrow$	t_{SBD}		$t_{KCY11}/2 - 100$		$t_{KCY11}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY11}/2 - 30$		$t_{KCY11}/2 + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}		100			ns
$\overline{SCK1}\downarrow$ from busy inactive	t_{SPS}		200			ns

Note C is the load capacitance of SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY12}		800			ns
$\overline{SCK1}$ high/low-level width	t_{KH12}, t_{KL12}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK12}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI12}		400			ns
SO1 output delay time (from $\overline{SCK1}\downarrow$)	t_{KSO12}	C = 100 pF Note			300	ns
$\overline{SCK1}$ at rising or falling edge time	t_{R12}, t_{F12}				1000	ns

Note C is the load capacitance of SO1 output line.

(c) Serial interface 3

(i) 3-wire serial I/O mode ($\overline{SCK3}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY13}		800			ns
$\overline{SCK3}$ high/low-level width	t_{KH13}, t_{KL13}		$t_{KCY13}/2 - 50$			ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	t_{SIK13}		100			ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	t_{KSI13}		400			ns
SO3 output delay time (from $\overline{SCK3}\downarrow$)	t_{KSO13}	C = 100 pF Note			300	ns

Note C is the load capacitance of $\overline{SCK3}$ and SO3 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK3}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY14}		800			ns
$\overline{SCK3}$ high/low-level width	t_{KH14}, t_{KL14}		400			ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	t_{SIK14}		100			ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	t_{KSI14}		400			ns
SO3 output delay time (from $\overline{SCK3}\downarrow$)	t_{KSO14}	C = 100 pF Note			300	ns
$\overline{SCK3}$ at rising or falling edge time	t_{R14}, t_{F14}				1000	ns

Note C is the load capacitance of SO3 output line.

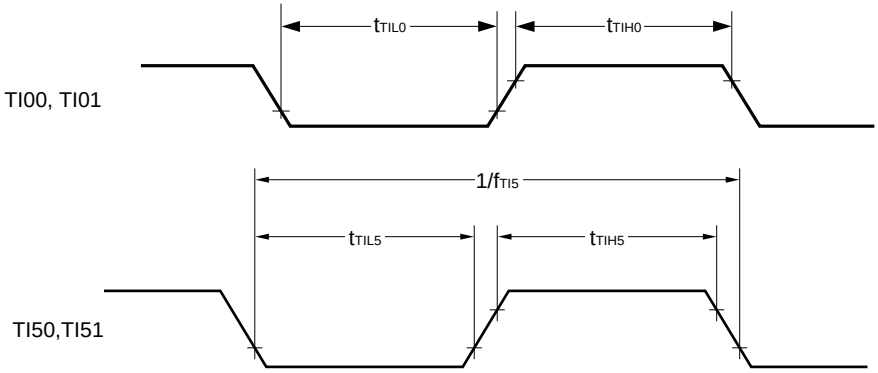
(d) Serial interface UART0 (Dedicated baud rate generator output)Note

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					38400	bps

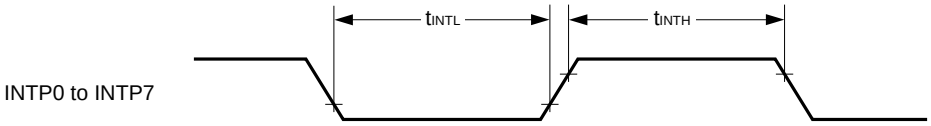
Note μPD178076 and 178078 only.

AC Timing Test Point (Excluding X1 Input)

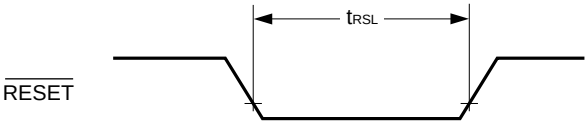
TI Timing



Interrupt Input Timing

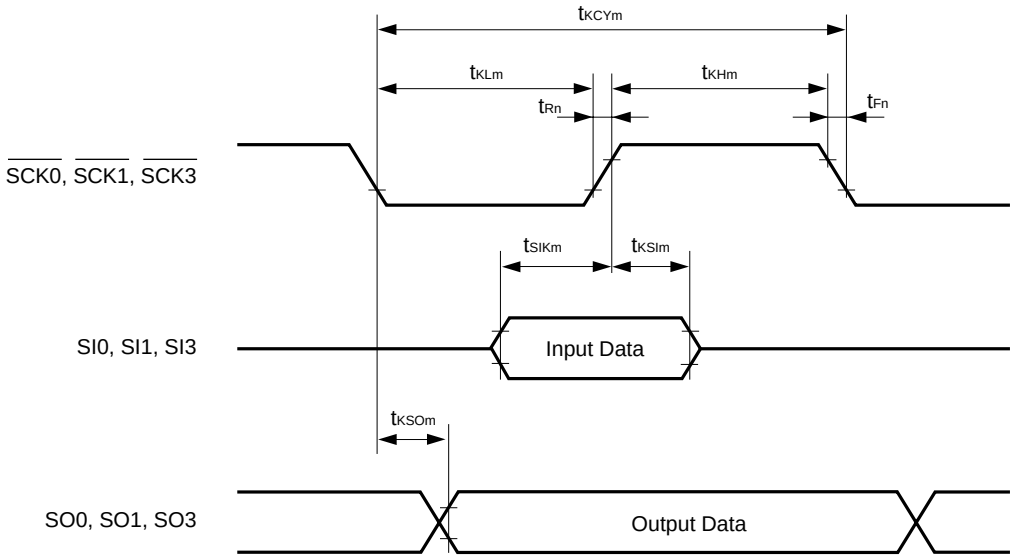


$\overline{\text{RESET}}$ Input Timing



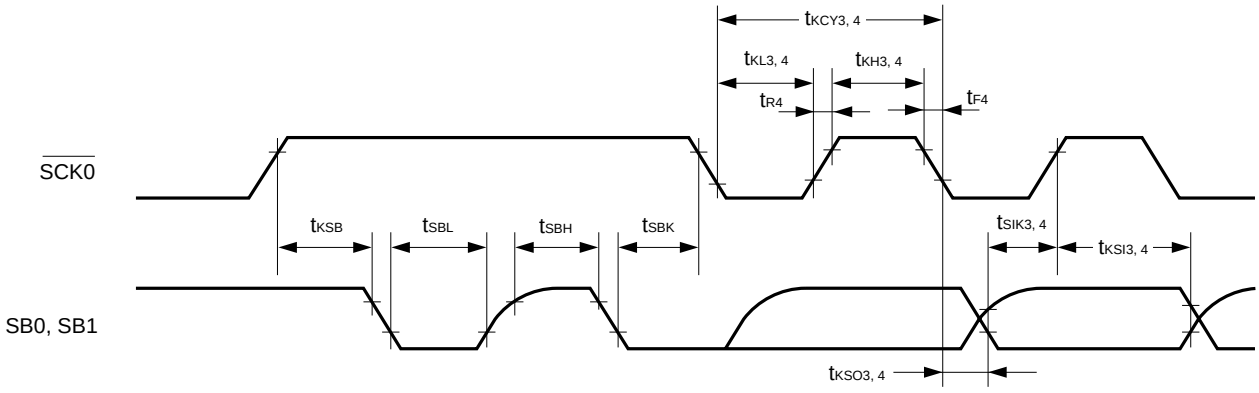
Serial Transfer Timing

3-wire serial I/O mode:

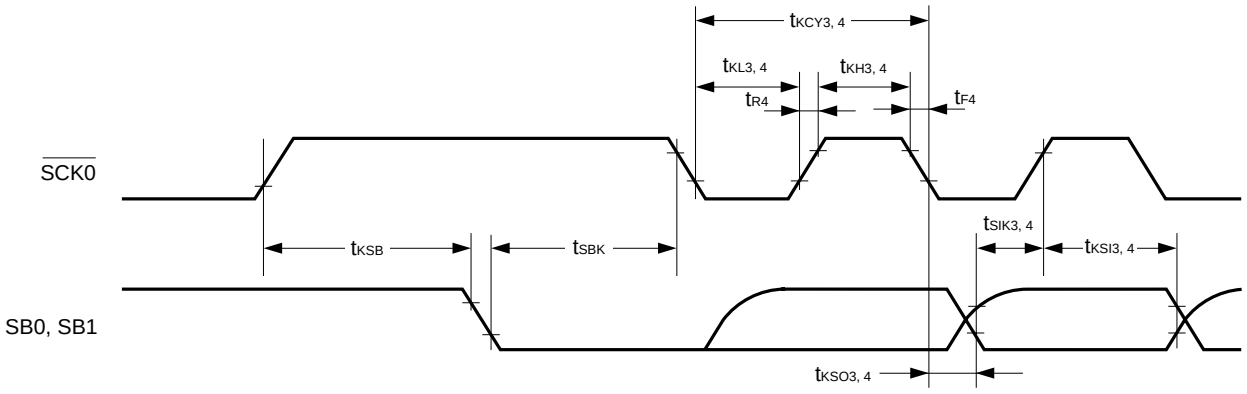


Remark m = 1, 2, 9, 10, 13, 14
n = 2, 10, 14

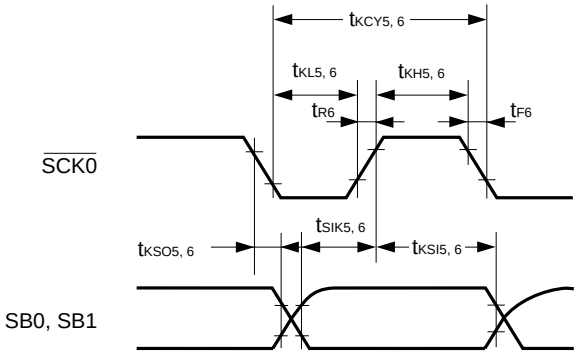
SBI mode (bus release signal transfer):



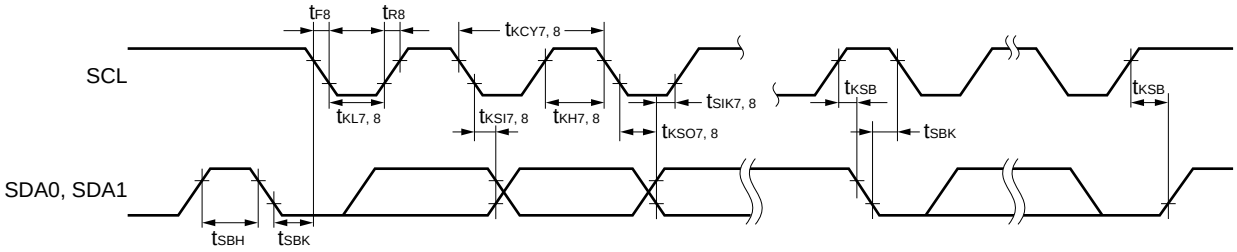
SBI mode (command signal transfer):



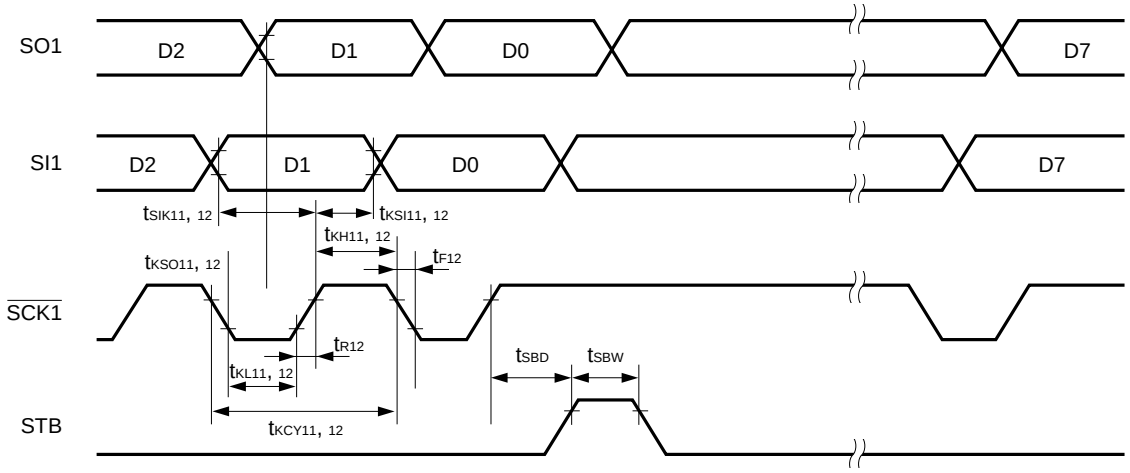
2-wire serial I/O mode:



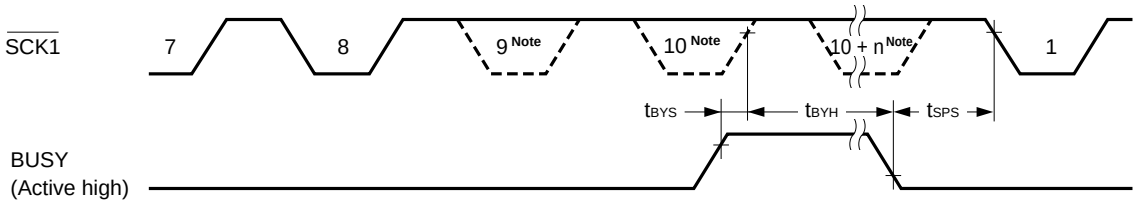
I²C bus mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

★ **IEBus Controller Characteristics[Note 1] (T_A = –40 to +85°C, V_{DD} = 3.5 to 5.5 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus system clock frequency	f_s	Fixed to mode 1		6.3[Note 2]		MHz

Notes 1. μPD178096 and 178098 only.

2. Although the system clock frequency is 6.0 MHz in the IEBus standard, in these products, normal operation is guaranteed at 6.3 MHz.

Remark 6.0 MHz and 6.3 MHz cannot both be used as the IEBus system clock frequency.

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
★ Total conversion error[Notes 1, 2]		V_{DD} = 4.5 to 5.5 V			±1.0	%FSR
★					±1.4	%FSR
Conversion time	t_{CONV}		15.2		45.7	μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Notes 1. Excluding quantization error (±0.2%FSR)

2. This value is indicated as a ratio to the full-scall value.

PLL Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN1}	VCOL pin, MF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.5		3.0	MHz
	f_{IN2}	VCOL pin, HF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	10		40	MHz
	f_{IN3}	VCOH pin, VHF mode, sine wave input, V_{IN} = 0.15 V_{P-P}	60		130	MHz
	f_{IN4}	VCOH pin, VHF mode, sine wave input, V_{IN} = 0.3 V_{P-P}	40		160	MHz

Remark The above values are the result of NEC's evaluation of the device. If the device is likely to be affected by noise in your application, it is recommended to use the device at a voltage higher than the above values.

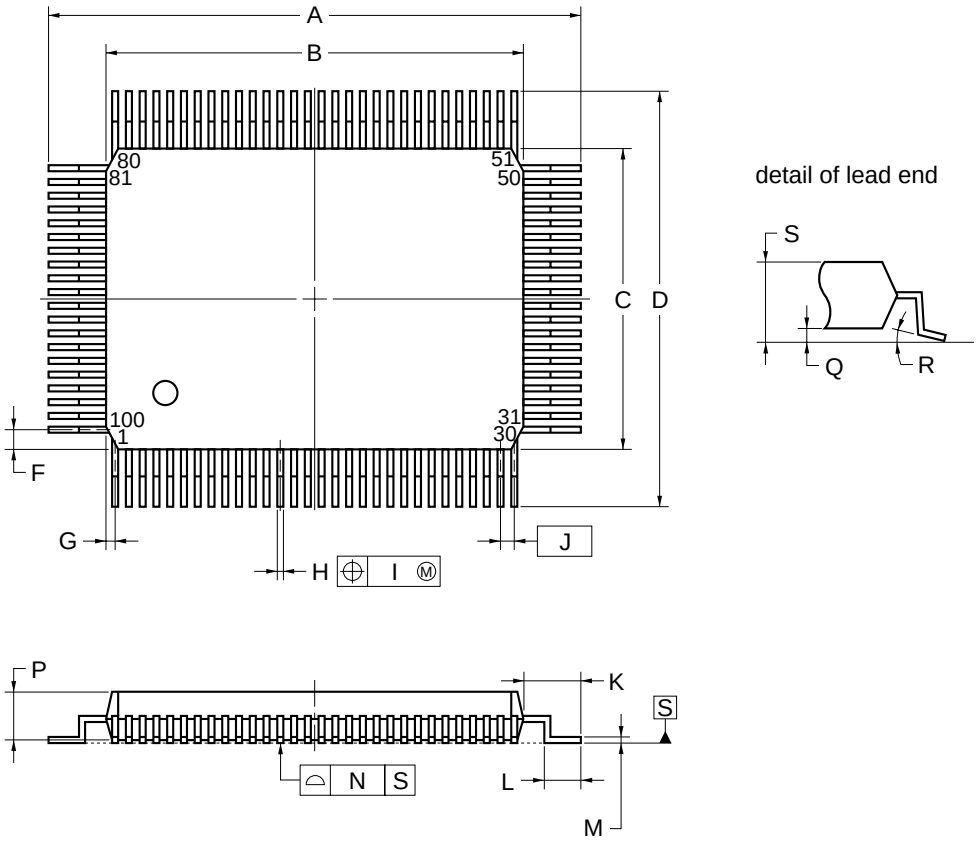
IFC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{IN5}	AMIFC pin, AMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.4		0.5	MHz
	f_{IN6}	FMIFC pin, FMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	10		11	MHz
	f_{IN7}	FMIFC pin, AMIF count mode, sine wave input, V_{IN} = 0.15 V_{P-P}	0.4		0.5	MHz

Remark The above values are the result of NEC's evaluation of the device. If the device is likely to be affected by noise in your application, it is recommended to use the device at a voltage higher than the above values.

9. PACKAGE DRAWING

★ **100-PIN PLASTIC QFP (14x20)**



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

10. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.
For soldering methods and conditions other than those recommended, consult NEC.

Table 10-1. Soldering Conditions for Surface-Mount Type

μPD178076GF-XXX-3BA: 100-pin plastic QFP (14 × 20)
μPD178078GF-XXX-3BA: 100-pin plastic QFP (14 × 20)
μPD178096GF-XXX-3BA: 100-pin plastic QFP (14 × 20)
μPD178098GF-XXX-3BA: 100-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec max. (210°C min.), Number of times: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 sec max. (200°C min.), Number of times: 3 max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec max., Number of times: 1, Preheating temperature: 120°C max., (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 sec max (per device side)	–

Caution Do not use two or more soldering methods in combination (except partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for development of systems using the μPD178078 and 178098 subseries.

Language processor software

RA78K/0[Notes 1, 2, 3]	Assembler package common to 78K/0 series
CC78K/0[Notes 1, 2, 3]	C compiler package common to 78K/0 series
DF178098[Notes 1, 2, 3]	Device file for μPD178078 subseries and μPD178098 subseries
CC78K0-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0 series

Flash memory writing tools

Fashpro III (Part number: FL-PR3[Note 4], PG-FL3)	Dedicated flash programmer
★ FA-100GF-3BA[Note 4]	Flash programmer adapter

Debugging tools

- **When in-circuit emulator IE-78K0-NS is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board for enhancing and expanding the IE-78K0-NS function
IE-70000-98-IF-C	Interface adapter necessary when PC-9800 series (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable necessary when a notebook-type PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter necessary when a IBM PC/AT™ compatible machine is used as host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-178098-NS-EM1	Emulation board to emulate μPD178078 and 178098 subseries
NP-100GF[Note 4]	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket mounted on board of target system created for 100-pin plastic QFP (GF-3BA type)
SM78K0[Notes 1, 2]	System simulator common to 78K/0 series
ID78K0-NS[Notes 1, 2]	Integrated debugger common to 78K/0 series
DF178098[Notes 1, 2, 3]	Device file for μPD178078 subseries and μPD178098 subseries

Notes 1. PC-9800 series (Japanese Windows™) based
2. IBM PC/AT compatible machine (Japanese/English windows) based
3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based, NEWS™ (NEWS-OS™) based
4. Products of Naito Densei Machida Mfg. Co., Ltd. (Tel: 044-822-3813).

Remark Use the RA78K0, CC78K0, and SM78K0 in combination with the DF178098.

• **When in-circuit emulator IE-78001-R-A is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 series
IE-70000-98-IF-C	Interface adapter necessary when PC-9800 series (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter necessary when IBM PC/AT compatible machine is used as host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when EWS is used as host machine
IE-178098-NS-EM1	Emulation board to emulate μPD178078 and 178098 subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-178098-NS-EM1 on IE-78001-R-A
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket mounted on board of target system created for 100-pin plastic QFP (GF-3BA type)
SM78K0 Notes 1, 2	System simulator common to 78K/0 series
ID78K0 Notes 1, 2	Integrated debugger common to 78K/0 series
DF178098 Notes 1, 2, 3	Device file for μPD178078 subseries and μPD178098 subseries

Real-time OS

RX78K/0 Notes 1, 2, 3	Real-time OS for 78K/0 series
MX78K0 Notes 1, 2, 3	OS for 78K/0 series

Notes 1. PC-9800 series (Japanese Windows) based
2. IBM PC/AT compatible machine (Japanese/English windows) based
3. HP9000 series 700 (HP-UX) based, SPARCstation (SunOS, Solaris) based, NEWS (NEWS-OS) based

Remark Use the SM78K0 in combination with the DF178098.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device Documents

Title		Document No.	
		Japanese	English
μPD178076, 178078, 178096, 178098 Data Sheet		U12885J	This document
★ μPD178F098 Data Sheet		U12920J	U12920E
μPD178078, 178098 Subseries User's Manual		U12790J	U12790E
78K/0 Series User's Manual - Instruction		U12326J	U12326E
78K/0 Series Application Note	Basics (I)	U12704J	U12704E

Development Tool Documents (User's Manual)

Title		Document No.	
		Japanese	English
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
★ IE-78001-R-A		U14142J	To be prepared
★ IE-78K0-NS		U13731J	U13731E
★ IE-178098-NS-EM1		U14013J	U14013E
EP-78064		EEU-934	EEU-1469
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
ID78K0-NS Integrated Debugger Windows Based	Reference	U12900J	U12900E
★	Operation	U14379J	To be prepared

Caution The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.

Related Documents for Embedded Software (User's Manual)

Title		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Fundamental	U11537J	U11537E
	Installation	U11536J	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257J	U12257E

Other Documents

Title	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Guides on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality/Reliability Handbook	C12769J	—
Microcomputer Product Series Guide	U11416J	—

Caution The contents of the above documents are subject to change without notice. Ensure that the latest versions are used in design work, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 408-588-6130
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