

## 4M-BIT CMOS FAST SRAM 256K-WORD BY 16-BIT

### Description

The μPD444016L is a high speed, low power, 4,194,304 bits (262,144 words by 16 bits) CMOS static RAM.

Operating supply voltage is 3.3 V ± 0.3 V.

The μPD444016L is packaged in 44-pin plastic SOJ and 44-pin plastic TSOP (II).

### Features

- 262,144 words by 16 bits organization
- Fast access time : 8, 10, 12 ns (MAX.)
- Byte data control : /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Output Enable input for easy application
- Single +3.3 V power supply

### Ordering Information

| Part number          | Package                                      | Access time<br>ns (MAX.) | Supply current mA (MAX.) |            |
|----------------------|--|--------------------------|--------------------------|------------|
|                      |  |                          | At operating             | At standby |
| μPD444016LLE-A8      | 44-pin plastic SOJ<br>(10.16 mm (400))       | 8                        | 210                      | 5          |
| μPD444016LLE-A10     |  | 10                       | 190                      |            |
| μPD444016LLE-A12     |  | 12                       | 180                      |            |
| μPD444016LG5-A8-7JF  | 44-pin plastic TSOP (II)<br>(10.16 mm (400)) | 8                        | 210                      |            |
| μPD444016LG5-A10-7JF |  | 10                       | 190                      |            |
| μPD444016LG5-A12-7JF |  | 12                       | 180                      |            |

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

# Pin Configuration (Marking Side)

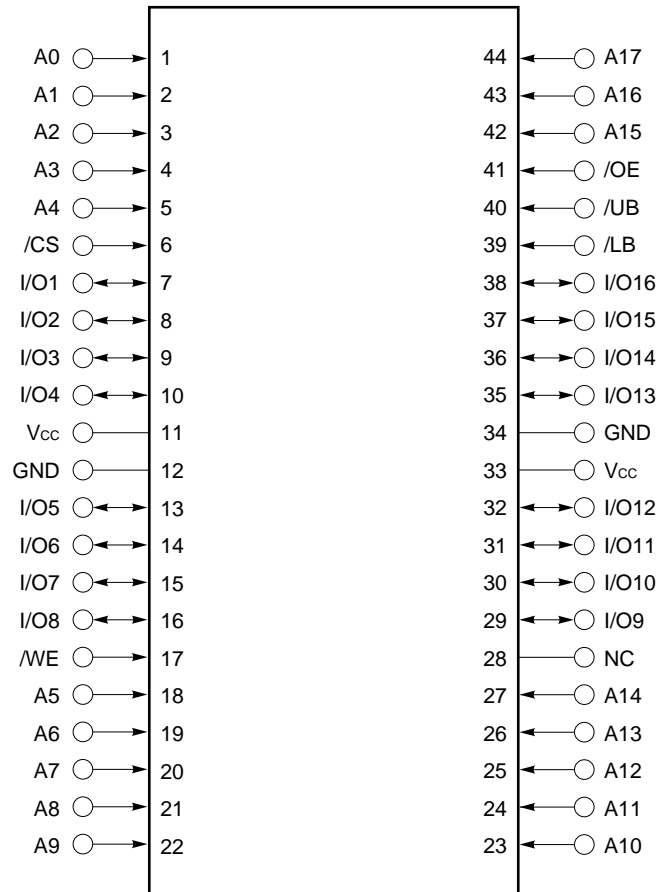
/xxx indicates active low signal.

## 44-pin plastic SOJ (10.16 mm (400))

[ μPD444016LLE ]

## 44-pin plastic TSOP (II) (10.16 mm (400)) (Normal bent)

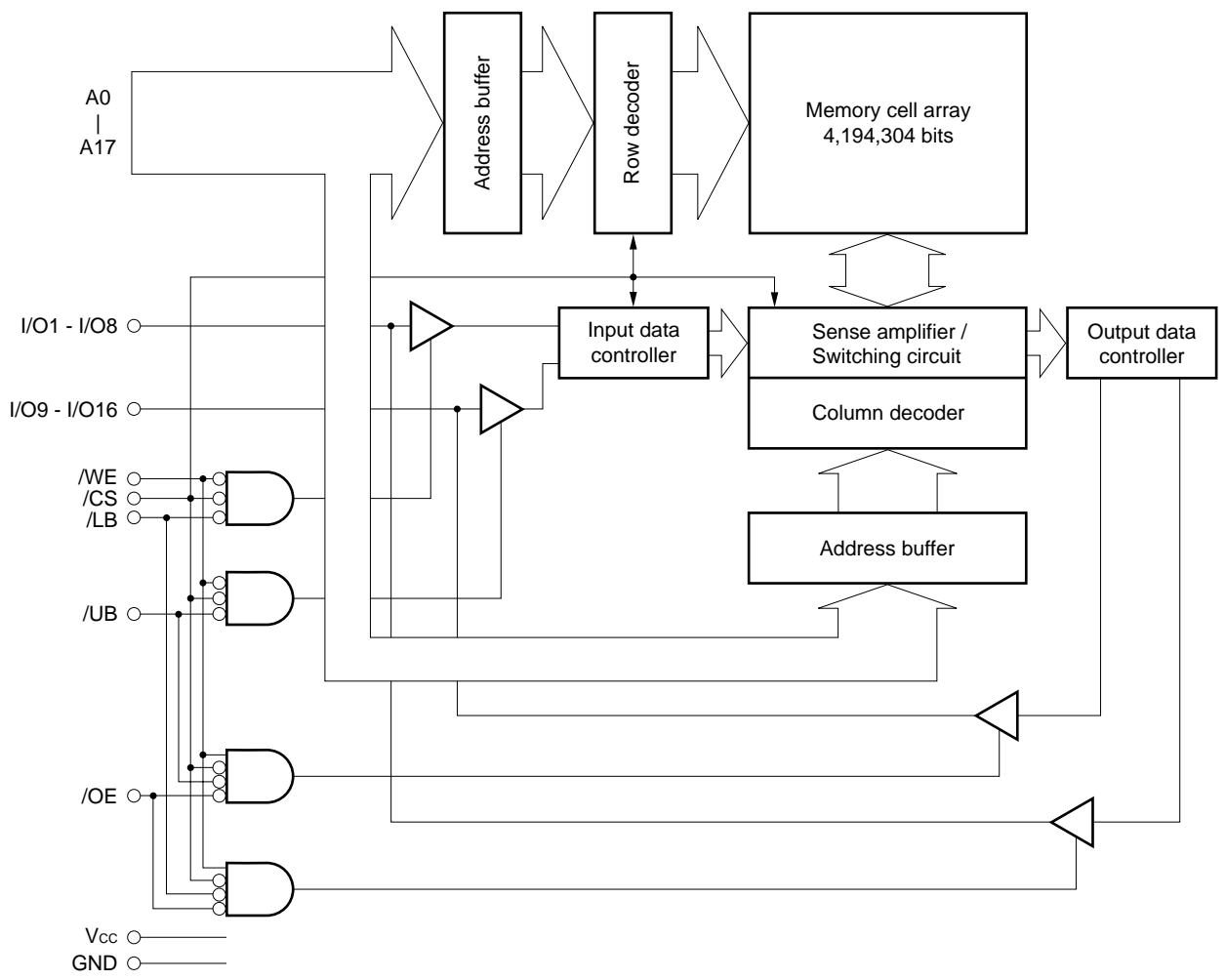
[ μPD444016LG5-xxx-7JF ]



- A0 - A17 : Address Inputs
- I/O1 - I/O16 : Data Inputs / Outputs
- /CS : Chip Select
- /WE : Write Enable
- /OE : Output Enable
- /LB, /UB : Byte data select
- Vcc : Power supply
- GND : Ground
- NC : No connection

**Remark** Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

| /CS | /OE | /WE | /LB | /UB | Mode           | I/O              |                  | Supply current  |
|-----|-----|-----|-----|-----|----------------|------------------|------------------|-----------------|
|     |     |     |     |     |                | I/O1 - I/O8      | I/O9 - I/O16     |                 |
| H   | ×   | ×   | ×   | ×   | Not selected   | High impedance   | High impedance   | I <sub>SB</sub> |
| L   | L   | H   | L   | L   | Read           | D <sub>OUT</sub> | D <sub>OUT</sub> | I <sub>CC</sub> |
|     |     |     | L   | H   |                | D <sub>OUT</sub> | High impedance   |                 |
|     |     |     | H   | L   |                | High impedance   | D <sub>OUT</sub> |                 |
| L   | ×   | L   | L   | L   | Write          | D <sub>IN</sub>  | D <sub>IN</sub>  |                 |
|     |     |     | L   | H   |                | D <sub>IN</sub>  | High impedance   |                 |
|     |     |     | H   | L   |                | High impedance   | D <sub>IN</sub>  |                 |
| L   | H   | H   | ×   | ×   | Output disable | High impedance   | High impedance   |                 |
| L   | ×   | ×   | H   | H   |                | High impedance   | High impedance   |                 |

Remark × : Don't care

## Electrical Specifications

## Absolute Maximum Ratings

|   | Parameter                     | Symbol           | Condition | Rating                         | Unit |
|---|-------------------------------|------------------|-----------|--------------------------------|------|
| ★ | Supply voltage                | $V_{CC}$         |           | $-0.5^{\text{Note}}$ to $+4.0$ | V    |
| ★ | Input / Output voltage        | $V_T$            |           | $-0.5^{\text{Note}}$ to $+4.0$ | V    |
|   | Operating ambient temperature | $T_A$            |           | 0 to 70                        | °C   |
|   | Storage temperature           | $T_{\text{stg}}$ |           | $-55$ to $+125$                | °C   |

**Note**  $-2.0$  V (MIN.) (pulse width : 2 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

| Parameter                     | Symbol   | Condition | MIN.                 | TYP. | MAX.         | Unit |
|-------------------------------|----------|-----------|----------------------|------|--------------|------|
| Supply voltage                | $V_{CC}$ |           | 3.0                  | 3.3  | 3.6          | V    |
| High level input voltage      | $V_{IH}$ |           | 2.0                  |      | $V_{CC}+0.3$ | V    |
| Low level input voltage       | $V_{IL}$ |           | $-0.3^{\text{Note}}$ |      | +0.8         | V    |
| Operating ambient temperature | $T_A$    |           | 0                    |      | 70           | °C   |

**Note**  $-2.0$  V (MIN.) (pulse width : 2 ns)

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

| Parameter                 | Symbol    | Test condition   | MIN. | TYP. | MAX. | Unit          |
|---------------------------|-----------|--|------|------|------|---------------|
| Input leakage current     | $I_{LI}$  | $V_{IN} = 0\text{ V to }V_{CC}$  | -2   |      | +2   | $\mu\text{A}$ |
| Output leakage current    | $I_{LO}$  | $V_{I/O} = 0\text{ V to }V_{CC}$ , $/CS = V_{IH}$ or $/OE = V_{IH}$<br>or $/WE = V_{IL}$ or $/LB = V_{IH}$ or $/UB = V_{IH}$ | -2   |      | +2   | $\mu\text{A}$ |
| Operating supply current  | $I_{CC}$  | $/CS = V_{IL}$ ,<br>Cycle time : 8 ns  |      |      | 210  | mA            |
|                           |           | $I_{I/O} = 0\text{ mA}$ ,<br>Cycle time : 10 ns  |      |      | 190  |               |
|                           |           | Minimum cycle time<br>Cycle time : 12 ns   |      |      | 180  |               |
| Standby supply current    | $I_{SB}$  | $/CS = V_{IH}$ , $V_{IN} = V_{IH}$ or $V_{IL}$   |      |      | 40   | mA            |
|                           | $I_{SB1}$ | $/CS \geq V_{CC} - 0.2\text{ V}$ ,<br>$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$                      |      |      | 5    |               |
| High level output voltage | $V_{OH}$  | $I_{OH} = -4.0\text{ mA}$  | 2.4  |      |      | V             |
| Low level output voltage  | $V_{OL}$  | $I_{OL} = +8.0\text{ mA}$  |      |      | 0.4  | V             |

**Remarks 1.**  $V_{IN}$  : Input voltage $V_{I/O}$  : Input / Output voltage**2.** These DC characteristics are in common regardless of package types.**Capacitance ( $T_A = 25\text{ }^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )**

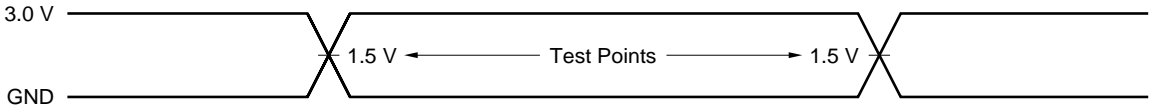
| Parameter                  | Symbol    | Test condition         | MIN. | TYP. | MAX. | Unit |
|----------------------------|-----------|------------------------|------|------|------|------|
| Input capacitance          | $C_{IN}$  | $V_{IN} = 0\text{ V}$  |      |      | 6    | pF   |
| Input / Output capacitance | $C_{I/O}$ | $V_{I/O} = 0\text{ V}$ |      |      | 8    | pF   |

**Remarks 1.**  $V_{IN}$  : Input voltage $V_{I/O}$  : Input / Output voltage**2.** These parameters are periodically sampled and not 100% tested.

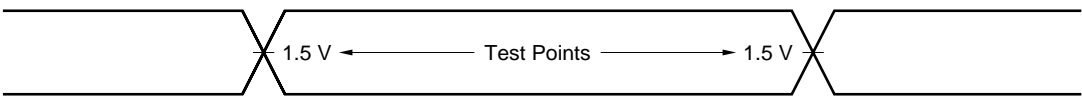
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)



Output Waveform



Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2**.

Figure 1

( $t_{AA}$ ,  $t_{ACS}$ ,  $t_{OE}$ ,  $t_{ABD}$ ,  $t_{OH}$ )

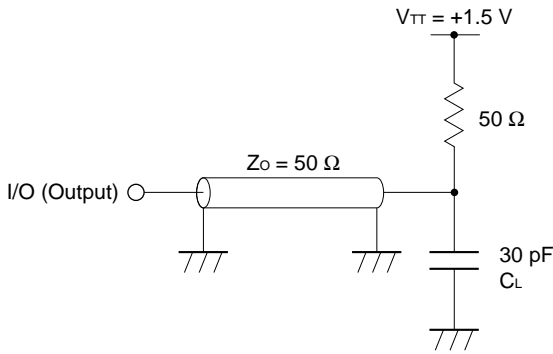
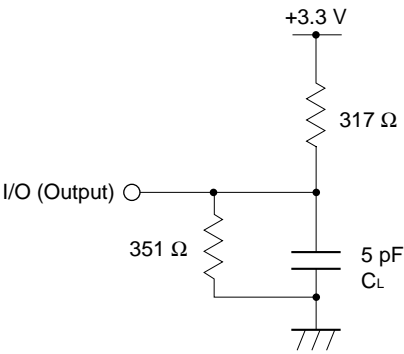


Figure 2

( $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{BLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{BHZ}$ ,  $t_{WHZ}$ ,  $t_{OW}$ )



**Remark** C<sub>L</sub> includes capacitances of the probe and jig, and stray capacitances.

# Read Cycle

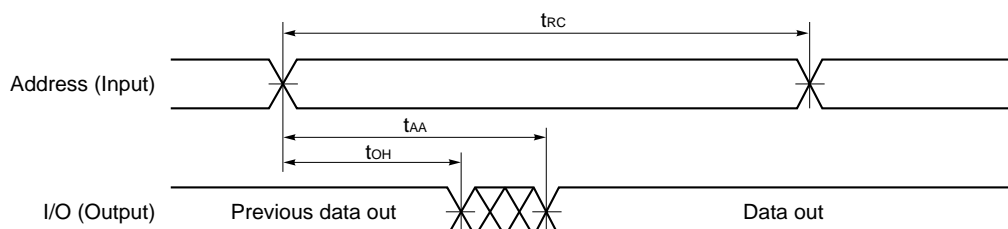
| Parameter                                 | Symbol           | μPD444016L-A8 |      | μPD444016L-A10 |      | μPD444016L-A12 |      | Unit | Notes |
|---|------------------|---------------|------|----------------|------|----------------|------|------|-------|
|   |                  | MIN.          | MAX. | MIN.           | MAX. | MIN.           | MAX. |      |       |
| Read cycle time                           | t <sub>RC</sub>  | 8             |      | 10             |      | 12             |      | ns   |       |
| Address access time                       | t <sub>AA</sub>  |               | 8    |                | 10   |                | 12   | ns   | 1     |
| /CS access time                           | t <sub>ACS</sub> |               | 8    |                | 10   |                | 12   | ns   |       |
| /OE access time                           | t <sub>OE</sub>  |               | 4    |                | 5    |                | 6    | ns   |       |
| /LB, /UB access time                      | t <sub>ABD</sub> |               | 4    |                | 5    |                | 6    | ns   |       |
| Output hold from address change           | t <sub>OH</sub>  | 3             |      | 3              |      | 3              |      | ns   |       |
| /CS to output in low impedance            | t <sub>CLZ</sub> | 3             |      | 3              |      | 3              |      | ns   | 2, 3  |
| /OE to output in low impedance            | t <sub>OLZ</sub> | 0             |      | 0              |      | 0              |      | ns   |       |
| /LB, /UB to output in low impedance       | t <sub>BLZ</sub> | 0             |      | 0              |      | 0              |      | ns   |       |
| /CS to output in high impedance           | t <sub>CHZ</sub> |               | 4    |                | 5    |                | 6    | ns   |       |
| /OE to output hold in high impedance      | t <sub>OHZ</sub> |               | 4    |                | 5    |                | 6    | ns   |       |
| /LB, /UB to output hold in high impedance | t <sub>BHZ</sub> |               | 4    |                | 5    |                | 6    | ns   |       |

**Notes 1.** See the output load shown in **Figure 1**.

2. Transition is measured at  $\pm 200$  mV from steady-state voltage with the output load shown in **Figure 2**.
3. These parameters are periodically sampled and not 100% tested.

**Remark** These AC characteristics are in common regardless of package types.

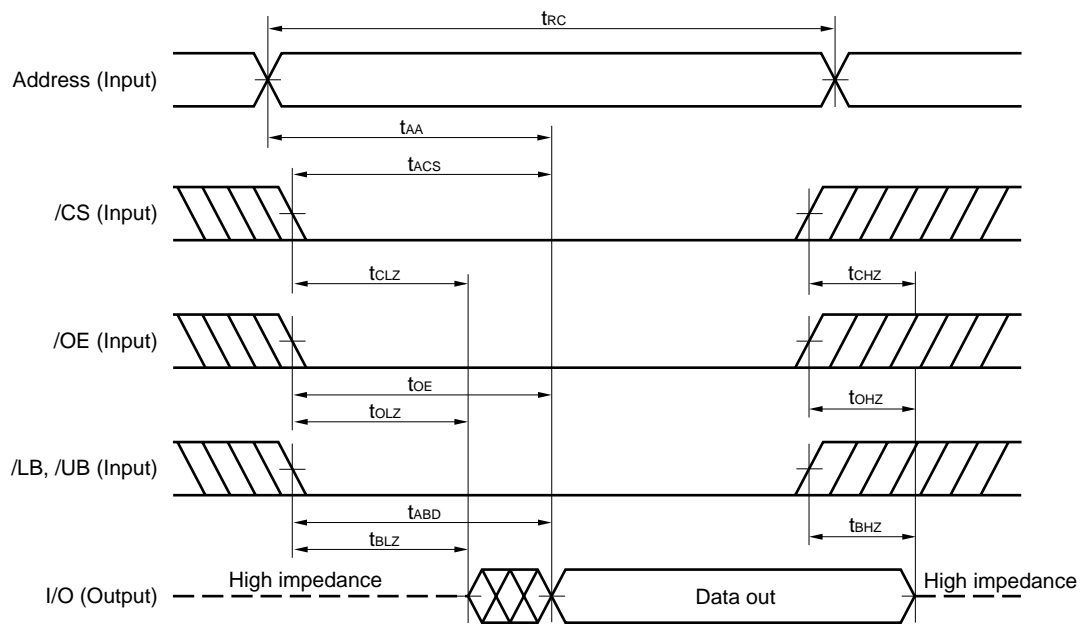
## Read Cycle Timing Chart 1 (Address Access)



**Remarks 1.** In read cycle, /WE should be fixed to high level.

**2.** /CS = /OE = /LB (or /UB) = V<sub>IL</sub>

Read Cycle Timing Chart 2 (/CS Access)



**Caution** Address valid prior to or coincident with /CS low level input.

**Remark** In read cycle, /WE should be fixed to high level.



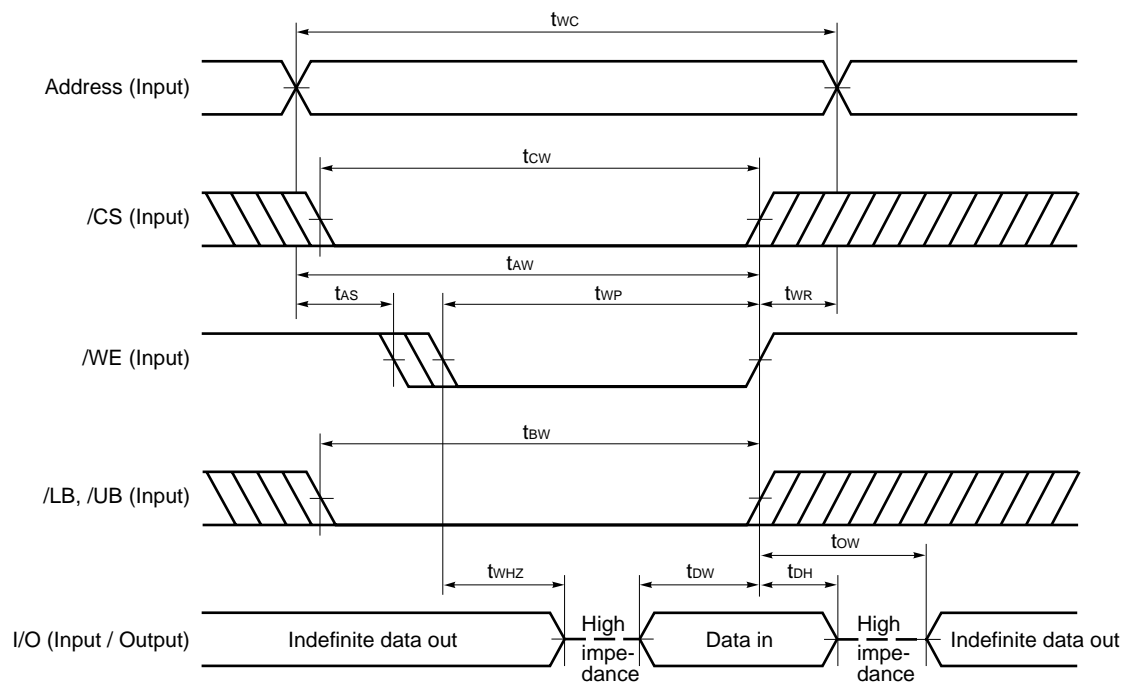
**Write Cycle**

| Parameter                       | Symbol           | $\mu$ PD444016L-A8 |      | $\mu$ PD444016L-A10 |      | $\mu$ PD444016L-A12 |      | Unit | Notes |
|---------------------------------|------------------|--------------------|------|---------------------|------|---------------------|------|------|-------|
|                                 |                  | MIN.               | MAX. | MIN.                | MAX. | MIN.                | MAX. |      |       |
| Write cycle time                | t <sub>WC</sub>  | 8                  |      | 10                  |      | 12                  |      | ns   |       |
| /CS to end of write             | t <sub>CW</sub>  | 6                  |      | 7                   |      | 8                   |      | ns   |       |
| Address valid to end of write   | t <sub>AW</sub>  | 6                  |      | 7                   |      | 8                   |      | ns   |       |
| Write pulse width               | t <sub>WP</sub>  | 6                  |      | 7                   |      | 8                   |      | ns   |       |
| /LB, /UB to end of write        | t <sub>BW</sub>  | 6                  |      | 7                   |      | 8                   |      | ns   |       |
| Data valid to end of write      | t <sub>DW</sub>  | 4                  |      | 5                   |      | 6                   |      | ns   |       |
| Data hold time                  | t <sub>DH</sub>  | 0                  |      | 0                   |      | 0                   |      | ns   |       |
| Address setup time              | t <sub>AS</sub>  | 0                  |      | 0                   |      | 0                   |      | ns   |       |
| Write recovery time             | t <sub>WR</sub>  | 0                  |      | 0                   |      | 0                   |      | ns   |       |
| /WE to output in high impedance | t <sub>WHZ</sub> |                    | 4    |                     | 5    |                     | 6    | ns   | 1, 2  |
| Output active from end of write | t <sub>OW</sub>  | 3                  |      | 3                   |      | 3                   |      | ns   |       |

**Notes** 1. Transition is measured at  $\pm 200$  mV from steady-state voltage with the output load shown in **Figure 2**.

2. These parameters are periodically sampled and not 100% tested.

**Remark** These AC characteristics are in common regardless of package types.

**Write Cycle Timing Chart 1 (/WE Controlled)**

**Cautions** 1. /CS or /WE should be fixed to high level during address transition.

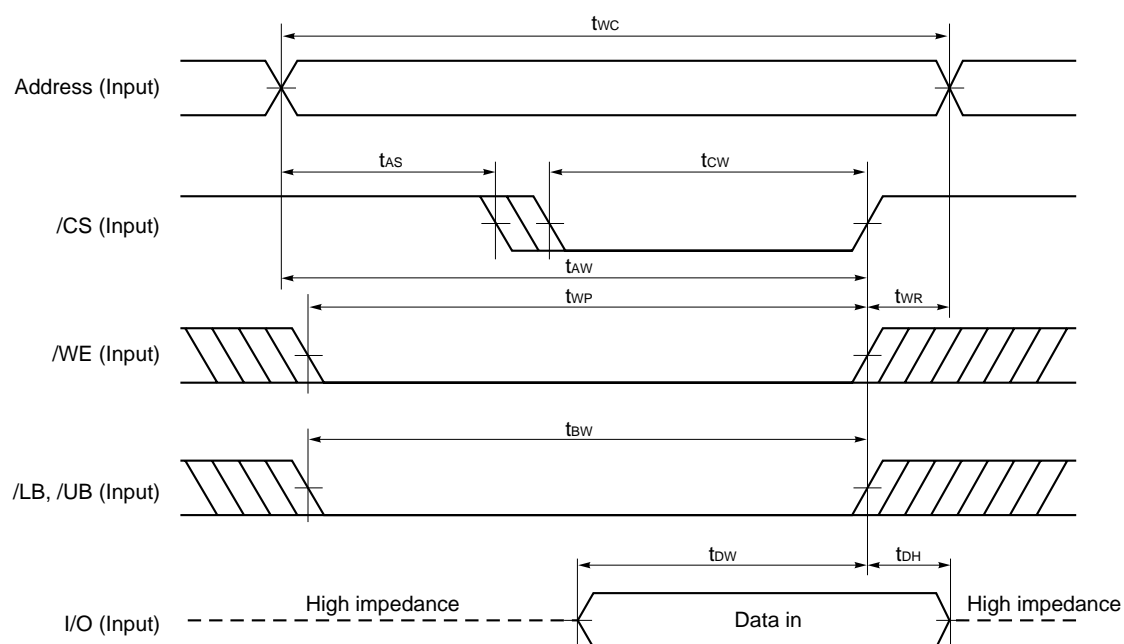
★

2. Do not input data to the I/O pins while they are in the output state.

**Remarks** 1. Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

2. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CS Controlled)



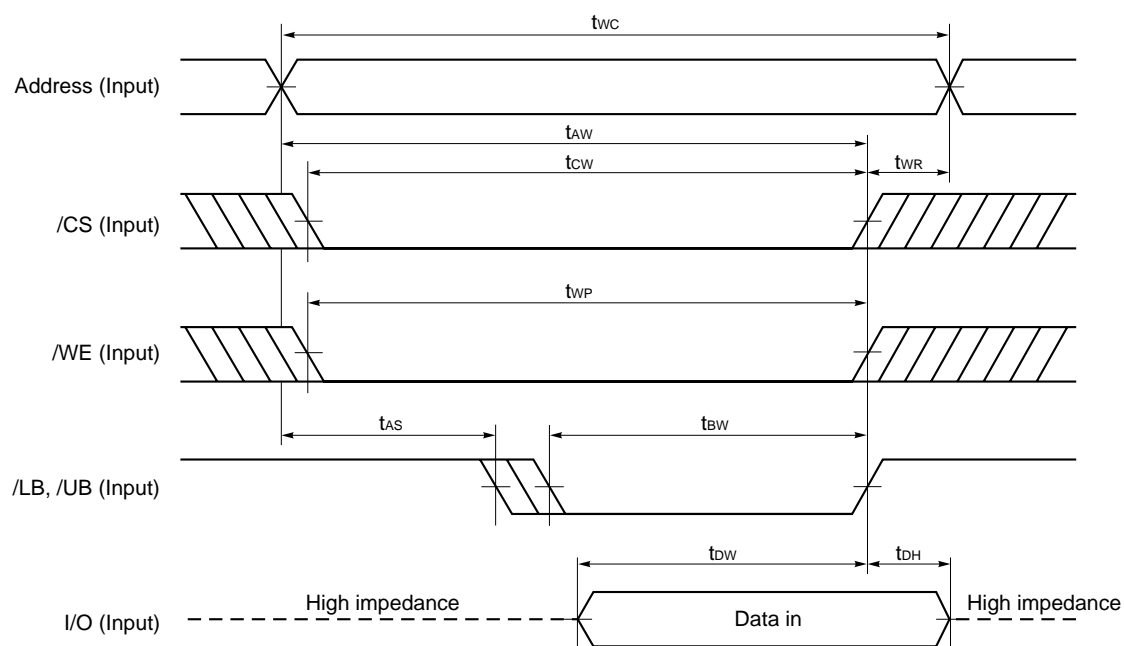
**Cautions** 1. /CS or /WE should be fixed to high level during address transition.

★

2. Do not input data to the I/O pins while they are in the output state.

**Remark** Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Write Cycle Timing Chart 3 (/LB, /UB Controlled)



**Cautions** 1. /CS or /WE should be fixed to high level during address transition.

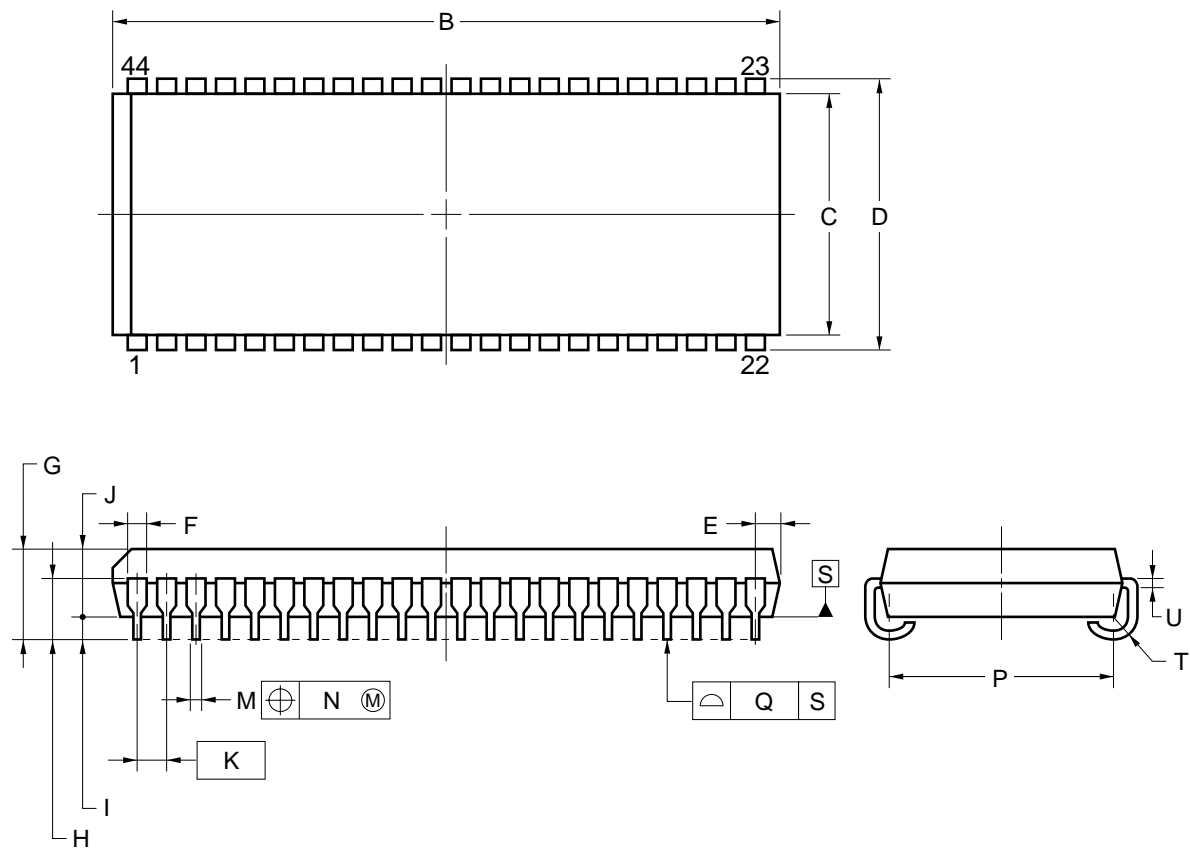
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2. Do not input data to the I/O pins while they are in the output state.

**Remark** Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Package Drawings

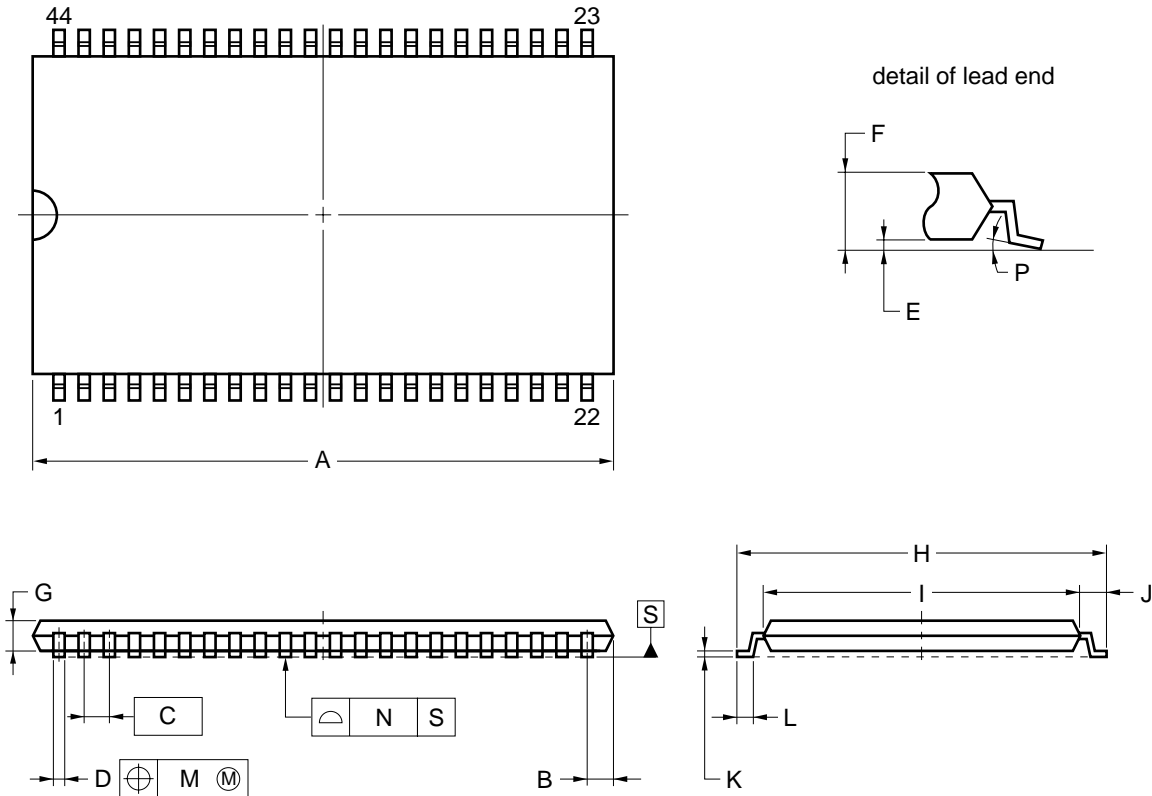
44-PIN PLASTIC SOJ (10.16 mm (400))



**NOTE**  
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

| ITEM         | MILLIMETERS                             |
|--------------|---|
| B            | 28.73 <sup>+0.20</sup> <sub>-0.35</sub> |
| C            | 10.16                                   |
| D            | 11.18±0.20                              |
| E            | 1.03±0.15                               |
| F            | 0.74                                    |
| G            | 3.5±0.2                                 |
| H            | 2.3±0.2                                 |
| I            | 0.8 MIN.                                |
| J            | 2.6                                     |
| K            | 1.27 (T.P.)                             |
| M            | 0.40±0.10                               |
| N            | 0.12                                    |
| P            | 9.4±0.20                                |
| Q            | 0.10                                    |
| T            | R 0.85                                  |
| U            | 0.20 <sup>+0.10</sup> <sub>-0.05</sub>  |
| P44LE-400A-1 |   |

44-PIN PLASTIC TSOP (II) (10.16 mm (400))



**NOTE**  
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                               |
|------|---|
| A    | 18.63 MAX.                                |
| B    | 0.93 MAX.                                 |
| C    | 0.8 (T.P.)                                |
| D    | 0.32 <sup>+0.08</sup> <sub>-0.07</sub>    |
| E    | 0.1±0.05                                  |
| F    | 1.2 MAX.                                  |
| G    | 0.97                                      |
| H    | 11.76±0.2                                 |
| I    | 10.16±0.1                                 |
| J    | 0.8±0.2                                   |
| K    | 0.145 <sup>+0.025</sup> <sub>-0.015</sub> |
| L    | 0.5±0.1                                   |
| M    | 0.13                                      |
| N    | 0.10                                      |
| P    | 3° <sup>+7°</sup> <sub>-3°</sub>          |

S44G5-80-7JF5-1

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD444016L.

**Types of Surface Mount Device**

$\mu$ PD444016LLE : 44-pin plastic SOJ (10.16 mm (400))

$\mu$ PD444016LG5-7JF : 44-pin plastic TSOP (II) (10.16 mm (400)) (Normal bent)

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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