

# MOS INTEGRATED CIRCUIT

# $\mu$ PD4632312A-X

## 32M-BIT CMOS MOBILE SPECIFIED RAM

## 2M-WORD BY 16-BIT

## EXTENDED TEMPERATURE OPERATION

### Description

The  $\mu$ PD4632312A-X is a high speed, low power, 33,554,432 bits (2,097,152 words by 16 bits) CMOS Mobile Specified RAM featuring Low Power Static RAM compatible function and pin configuration.

The  $\mu$ PD4632312A-X is fabricated with advanced CMOS technology using one-transistor memory cell.

The  $\mu$ PD4632312A-X is packed in 48-pin TAPE FBGA.

### Features

- 2,097,152 words by 16 bits organization
- Fast access time: 60, 65, 75, 85 ns (MAX.)
- Fast page access time: 18, 25, 30 ns (MAX.)
- Byte data control: /LB (I/O0 to I/O7), /UB (I/O8 to I/O15)
- Low voltage operation: 2.7 to 3.1 V (-B60X, -B65X)  
2.7 to 3.1 V (Chip), 1.65 to 2.1 V (I/O) (-BE75X, -BE85X)
- Operating ambient temperature:  $T_A = -25$  to  $+85$  °C
- Output Enable input for easy application
- Chip Enable input: /CS pin
- Standby Mode input: MODE pin
- Standby Mode1: Normal standby (Memory cell data hold valid)
- Standby Mode2: Density of memory cell data hold is variable

	μPD4632312A	Access time ns (MAX.)	Operating supply voltage V		Operating ambient temperature °C	Supply current					
						At operating mA (MAX.)	At standby μA (MAX.)				
			Density of data hold								
			32M bits	16M bits			8M bits	4M bits	0M bit		
★	-B60X <sup>Note</sup> , -B65X	60, 65	2.7 to 3.1	–	–25 to +85	50	100	70	60	50	30
★	-BE75X <sup>Note</sup> , -BE85X <sup>Note</sup>	75, 85	2.7 to 3.1	1.65 to 2.1		45					

**Note** Under development

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## Ordering Information

★	Part number	Package	Access time ns (MAX.)	Operating supply voltage V		Operating temperature °C
				Chip	I/O	
	μPD4632312AF9-B60X-BC2 <small>Note</small>	48-pin TAPE FBGA (8 x 6)	60	2.7 to 3.1	–	–25 to +85
	μPD4632312AF9-B65X-BC2		65			
	μPD4632312AF9-BE75X-BC2 <small>Note</small>		75	2.7 to 3.1	1.65 to 2.1	
μPD4632312AF9-BE85X-BC2 <small>Note</small>	85					

**Note** Under development

Pin Configurations

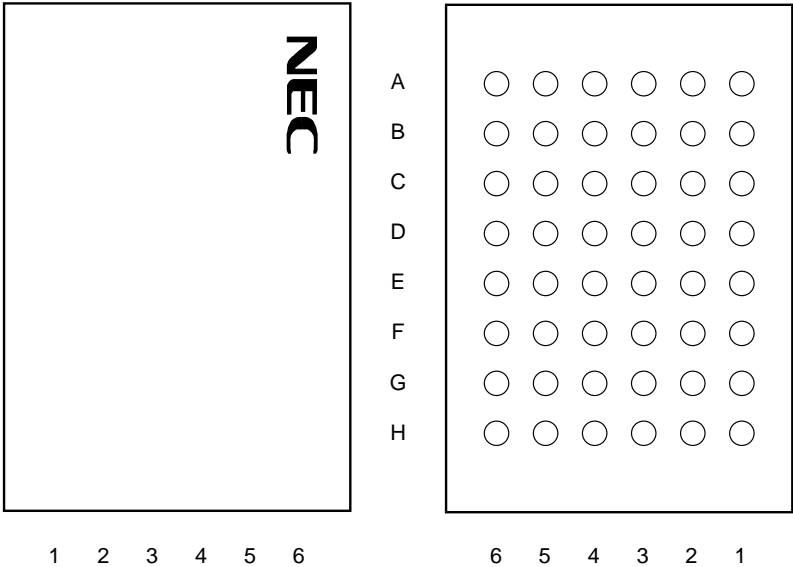
/xxx indicates active low signal.

48-pin TAPE FBGA (8 x 6)

[ μPD4632312AF9-B60X-BC2 ]  
[ μPD4632312AF9-B65X-BC2 ]

Top View

Bottom View



	1	2	3	4	5	6
A	/LB	/OE	A0	A1	A2	MODE
B	I/O8	/UB	A3	A4	/CS	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	GND	I/O11	A17	A7	I/O3	Vcc
E	Vcc	I/O12	NC	A16	I/O4	GND
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	A19	A12	A13	/WE	I/O7
H	A18	A8	A9	A10	A11	A20

	6	5	4	3	2	1
A	MODE	A2	A1	A0	/OE	/LB
B	I/O0	/CS	A4	A3	/UB	I/O8
C	I/O2	I/O1	A6	A5	I/O10	I/O9
D	Vcc	I/O3	A7	A17	I/O11	GND
E	GND	I/O4	A16	NC	I/O12	Vcc
F	I/O6	I/O5	A15	A14	I/O13	I/O14
G	I/O7	/WE	A13	A12	A19	I/O15
H	A20	A11	A10	A9	A8	A18

- A0 to A20

: Address inputs
- I/O0 to I/O15

: Data inputs / outputs
- /CS

: Chip select
- MODE

: Standby mode
- /WE

: Write enable
- /OE

: Output enable
- /LB, /UB

: Byte data select
- Vcc

: Power supply
- GND

: Ground
- NC <sup>Note</sup>

: No connection

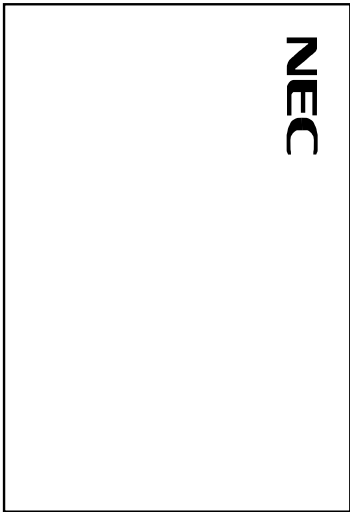
**Note** Some signals can be applied because this pin is not internally connected.

**Remark** Refer to **Package Drawing** for the index mark.

48-pin TAPE FBGA (8 x 6)

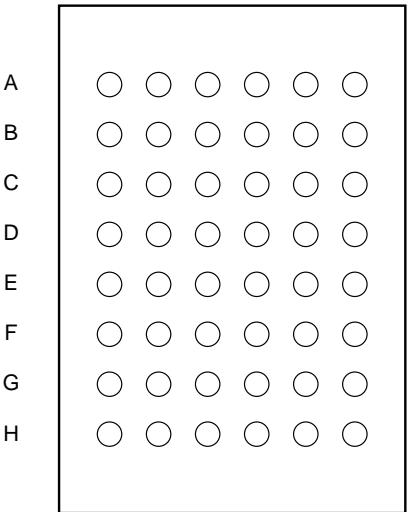
[ μPD4632312AF9-BE75X-BC2 ]  
[ μPD4632312AF9-BE85X-BC2 ]

Top View



1 2 3 4 5 6

Bottom View



6 5 4 3 2 1

	1	2	3	4	5	6
A	/LB	/OE	A0	A1	A2	MODE
B	I/O8	/UB	A3	A4	/CS	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	GND	I/O11	A17	A7	I/O3	Vcc
E	VccQ	I/O12	NC	A16	I/O4	GND
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	A19	A12	A13	/WE	I/O7
H	A18	A8	A9	A10	A11	A20

	6	5	4	3	2	1
A	MODE	A2	A1	A0	/OE	/LB
B	I/O0	/CS	A4	A3	/UB	I/O8
C	I/O2	I/O1	A6	A5	I/O10	I/O9
D	Vcc	I/O3	A7	A17	I/O11	GND
E	GND	I/O4	A16	NC	I/O12	VccQ
F	I/O6	I/O5	A15	A14	I/O13	I/O14
G	I/O7	/WE	A13	A12	A19	I/O15
H	A20	A11	A10	A9	A8	A18

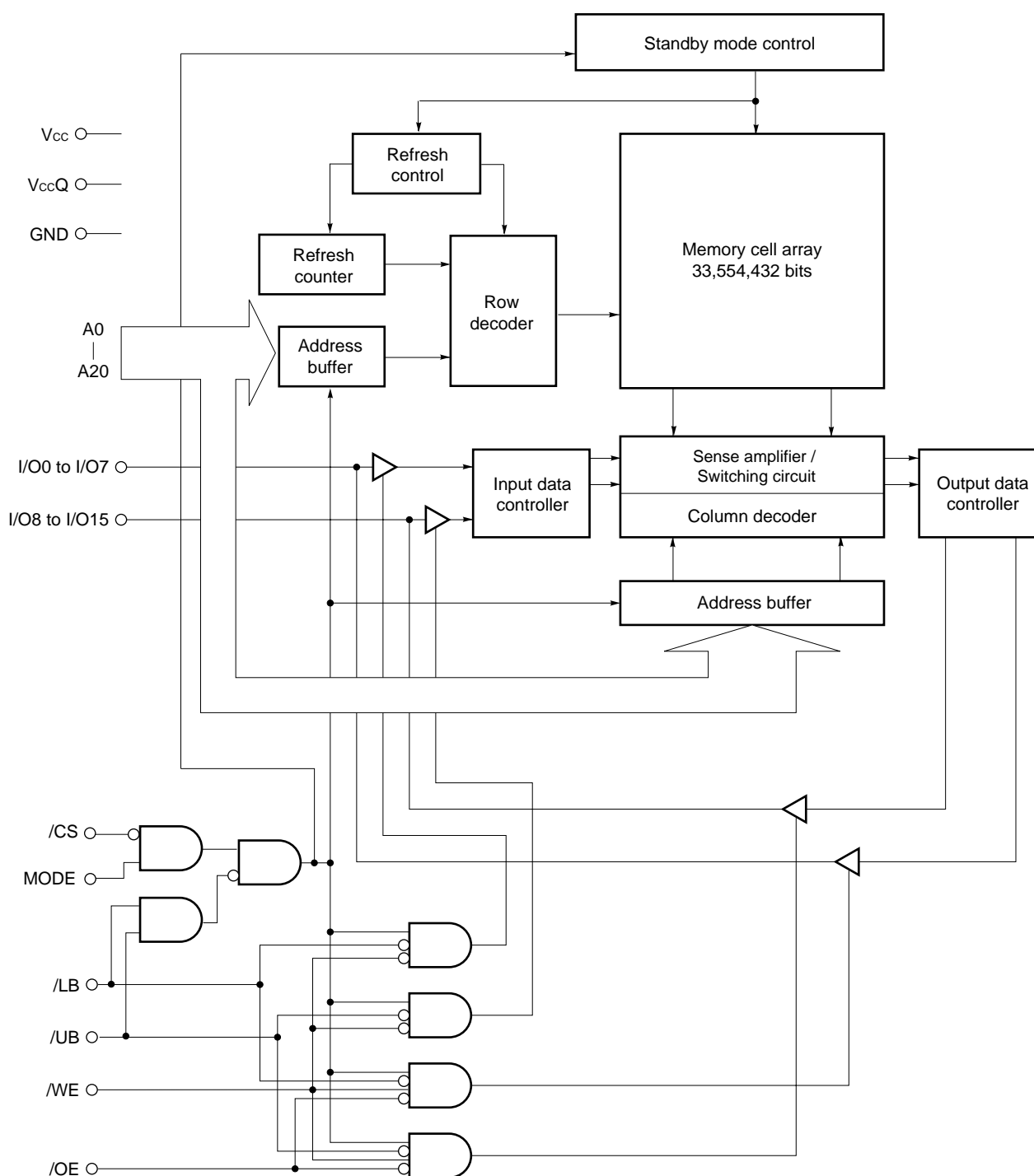
A0 to A20 : Address inputs  
I/O0 to I/O15 : Data inputs / outputs  
/CS : Chip Select  
MODE : Standby mode  
/WE : Write enable

/OE : Output enable  
/LB, /UB : Byte data select  
Vcc : Power supply  
VccQ : Input / Output power supply  
GND : Ground  
NC <sup>Note</sup> : No connection

**Note** Some signals can be applied because this pin is not internally connected.

**Remark** Refer to **Package Drawing** for the index mark.

# Block Diagram



**Remark**  $V_{CCQ}$  is the input / output power supply for -BE75X and -BE85X.

Truth Table

/CS	MODE	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O0 to I/O7	I/O8 to I/O15	
H	H	×	×	×	×	Not selected (Standby Mode 1)	High-Z	High-Z	I <sub>SB1</sub>
×	H	×	×	H	H	Not selected (Standby Mode 1)	High-Z	High-Z	
×	L	×	×	×	×	Not selected (Standby Mode 2) <sup>Note</sup>	High-Z	High-Z	I <sub>SB2</sub>
L	H	H	H	×	×	Output disable	High-Z	High-Z	I <sub>CCA</sub>
		L	H	L	L	Word read	D <sub>OUT</sub>	D <sub>OUT</sub>	
				L	H	Lower byte read	D <sub>OUT</sub>	High-Z	
				H	L	Upper byte read	High-Z	D <sub>OUT</sub>	
		H	L	L	L	Word write	D <sub>IN</sub>	D <sub>IN</sub>	
				L	H	Lower byte write	D <sub>IN</sub>	High-Z	
				H	L	Upper byte write	High-Z	D <sub>IN</sub>	

**Note** MODE pin must be fixed to high level except Standby Mode 2. (refer to **2.3 Standby Mode Status Transition**).

**Remark** ×: V<sub>IH</sub> or V<sub>IL</sub>, H: V<sub>IH</sub>, L: V<sub>IL</sub>

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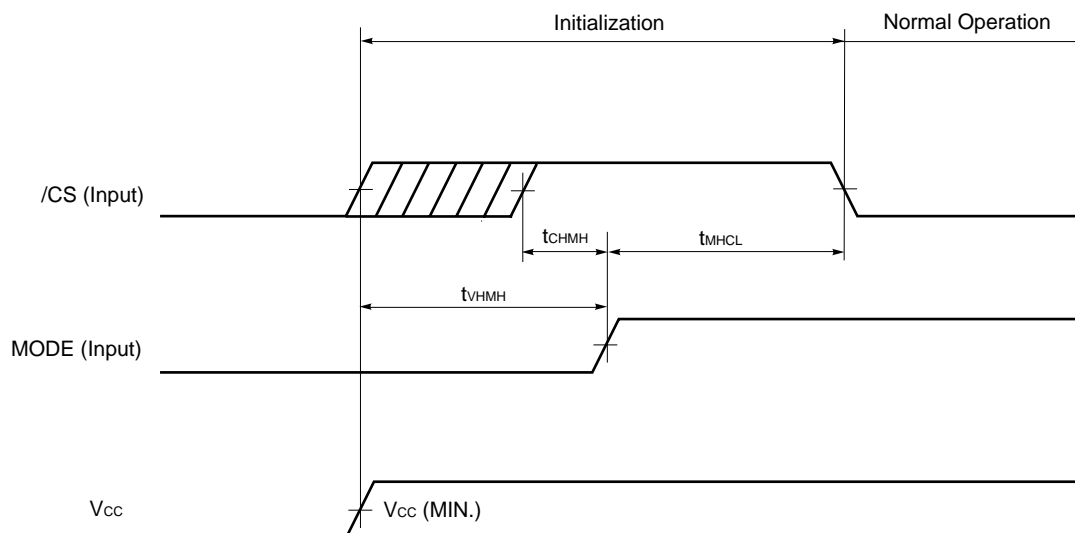
## 1. Initialization

Initialize the μPD4632312A-X at power application using the following sequence to stabilize internal circuits.

- (1) Following power application, make MODE high level after fixing MODE to low level for the period of  $t_{VHMH}$ . Make /CS high level before making MODE high level.
- (2) /CS and MODE are fixed to high level for the period of  $t_{MHCL}$ .

Normal operation is possible after the completion of initialization.

Figure1-1. Initialization Timing Chart



**Cautions 1. Make MODE low level when starting the power supply.**

2.  $t_{VHMH}$  is specified from when the power supply voltage reaches the prescribed minimum value ( $V_{CC} (MIN.)$ ).

### Initialization Timing

Parameter	Symbol	MIN.	MAX.	Unit
Power application to MODE low level hold	$t_{VHMH}$	50		$\mu s$
/CS high level to MODE high level	$t_{CHMH}$	0		ns
Following power application MODE high level hold to /CS low level	$t_{MHCL}$	200		$\mu s$



## 2. Partial Refresh

### 2.1 Standby Mode

In addition to the regular standby mode (Standby Mode 1) with a 32M bits density, Standby Mode 2, which performs partial refresh, is also provided.

### 2.2 Density Switching

In Standby Mode 2, the densities that can be selected for performing refresh are 16M bits, 8M bits, 4M bits, and 0M bit.

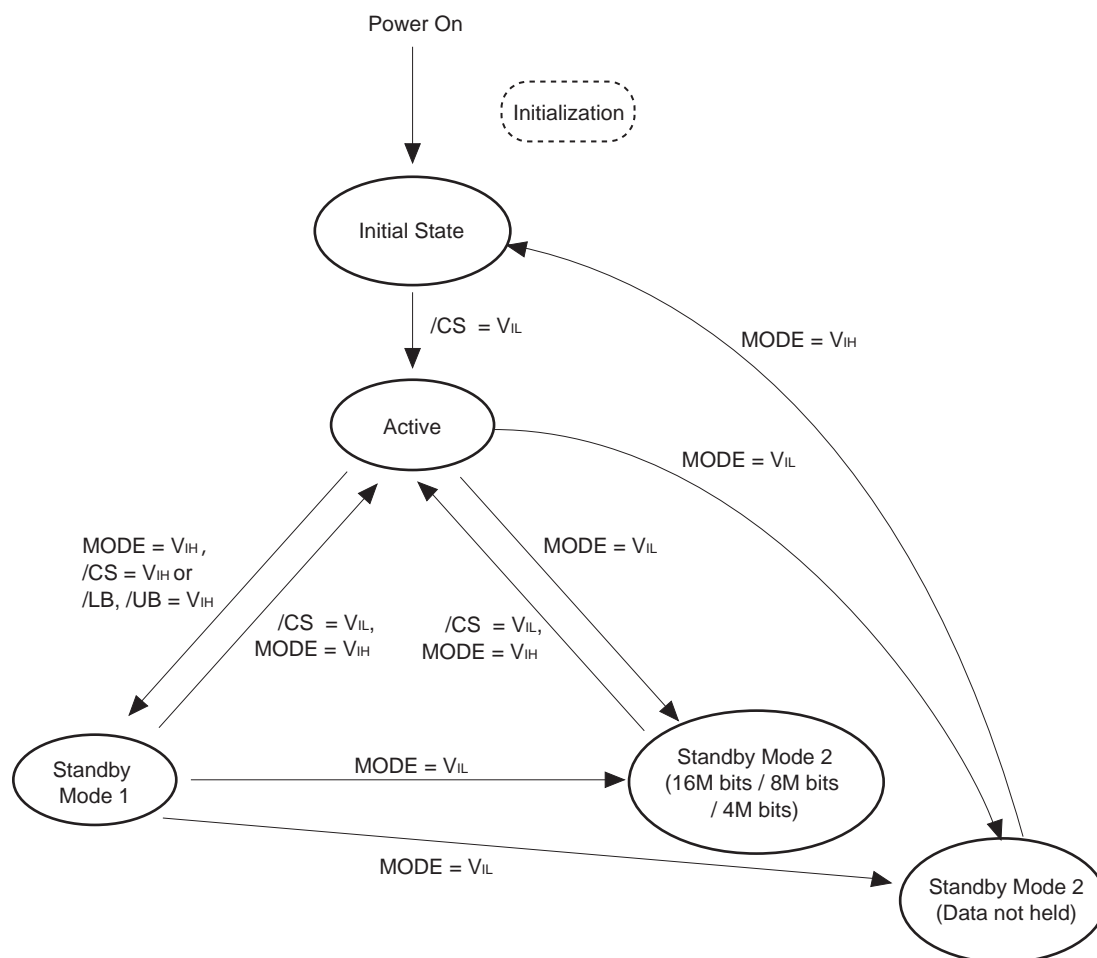
The density for performing refresh can be set with the mode register. Once the refresh density has been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application. (For how to perform mode register settings, refer to section **4. Mode Register Settings**.)

### 2.3 Standby Mode Status Transition

In Standby Mode 1, MODE and /CS are high level, or MODE, /LB and /UB are high level. In Standby Mode 2, MODE is low level. In Standby Mode 2, if 0M bit is set as the density, it is necessary to perform initialization the same way as after applying power, in order to return to normal operation from Standby Mode 2. When the density has been set to 16M bits, 8M bits, or 4M bits in Standby Mode 2, it is not necessary to perform initialization to return to normal operation from Standby Mode 2.

For the timing charts, refer to **Figure 6-14. Standby Mode 2 (data hold: 16M bits / 8M bits / 4M bits) Entry / Exit Timing Chart**, **Figure 6-15. Standby Mode 2 (data not held) Entry / Exit Timing Chart**.

Figure 2-1. Standby Mode State Machine



## 2.4 Addresses for Which Partial Refresh Is Supported

Data hold density	Correspondence address
16M bits	000000H to 0FFFFFFH
8M bits	000000H to 07FFFFFFH
4M bits	000000H to 03FFFFFFH

### 3. Page Read Operation

#### 3.1 Features of Page Read Operation

Features	8 Words Mode
Page length	8 words
Page read-corresponding addresses	A2, A1, A0
Page read start address	Don't care
Page direction	Don't care
Interrupt during page read operation	Enabled <sup>Note</sup>

**Note** An interrupt is output when /CS = H or in case A3 or a higher address changes.

#### 3.2 Page Length

8 words is supported as the page lengths.

#### 3.3 Page-Corresponding Addresses

The page read-enabled addresses are A2, A1, and A0. Fix addresses other than A2, A1, and A0 during page read operation.

#### 3.4 Page Start Address

Since random page read is supported, any address (A2, A1, A0) can be used as the page read start address.

#### 3.5 Page Direction

Since random page read is possible, there is not restriction on the page direction.

#### 3.6 Interrupt during Page Read Operation

When generating an interrupt during page read, either make /CS high level or change A3 and higher addresses.

#### 3.7 When page read is not used

Since random page read is supported, even when not using page read, random access is possible as usual.

## 4. Mode Register Settings

The partial refresh density can be set using the mode register. Since the initial value of the mode register at power application is undefined, be sure to set the mode register after initialization at power application. When setting the density of partial refresh, data before entering the partial refresh mode is not guaranteed. (This is the same for re-setup.) However, since partial refresh mode is not entered unless MODE = L when partial refresh is not used, it is not necessary to set the mode register. Moreover, when using page read without using partial refresh, it is not necessary to set the mode register.

### 4.1 Mode Register Setting Method

The mode register setting mode can be entered by successively writing two specific data after two continuous reads of the highest address (1FFFFFFH). The mode register setting is a continuous four-cycle operation (two read cycles and two write cycles).

Commands are written to the command register. The command register is used to latch the addresses and data required for executing commands, and it does not have an exclusive memory area.

For the timing chart and flow chart, refer to **Figure 6-12. Mode Register Setting Timing Chart**, **Figure 6-13. Mode Register Setting Flow Chart**.

Table 4-1. shows the commands and command sequences.

**Table 4-1. Command sequence**

Command sequence	1st bus cycle (Read cycle)		2nd bus cycle (Read cycle)		3rd bus cycle (Write cycle)		4th bus cycle (Write cycle)	
	Address	Data	Address	Data	Address	Data	Address	Data
Partial refresh density	1FFFFFFH	–	1FFFFFFH	–	1FFFFFFH	00H	1FFFFFFH	04H
16M bits	1FFFFFFH	–	1FFFFFFH	–	1FFFFFFH	00H	1FFFFFFH	04H
8M bits	1FFFFFFH	–	1FFFFFFH	–	1FFFFFFH	00H	1FFFFFFH	05H
4M bits	1FFFFFFH	–	1FFFFFFH	–	1FFFFFFH	00H	1FFFFFFH	06H
0M bit	1FFFFFFH	–	1FFFFFFH	–	1FFFFFFH	00H	1FFFFFFH	07H

4th bus cycle (Write cycle)

I/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode Register setting	0	0	0	0	0	0	0	0	0	0	0	0	0	PL	PD	

Page length	1	8 words
-------------	---	---------

Partial refresh density	I/O1	I/O0	Density
	0	0	16M bits
	0	1	8M bits
	1	0	4M bits
	1	1	0M bit

#### 4.2 Cautions for Setting Mode Register

Since, for the mode register setting, the internal counter status is judged by toggling /CS and /OE, toggle /CS at every cycle during entry (read cycle twice, write cycle twice), and toggle /OE like /CS at the first and second read cycles.

If incorrect addresses or data are written, or if addresses or data are written in the incorrect order, the setting of the mode register are not performed correctly.

When the highest address (1FFFFH) is read consecutively three or more times, the mode register setting entries are cancelled.

Once the refresh density has been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application.

For the timing chart and flow chart, refer to **Figure 6-12. Mode Register Setting Timing Chart**, **Figure 6-13. Mode Register Setting Flow Chart**.

## 5. Electrical Specifications

### Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			-B60X, -B65X	-BE75X, -BE85X	
Supply voltage	V <sub>CC</sub>		-0.5 <sup>Note</sup> to +4.0	-0.5 <sup>Note</sup> to +4.0	V
Input / Output supply voltage	V <sub>CCQ</sub>		—	-0.5 <sup>Note</sup> to +4.0	V
Input / Output voltage	V <sub>I</sub>		-0.5 <sup>Note</sup> to V <sub>CC</sub> + 0.4 (4.0 V MAX.)	-0.5 <sup>Note</sup> to V <sub>CCQ</sub> + 0.4 (4.0 V MAX.)	V
Operating ambient temperature	T <sub>A</sub>		-25 to +85	-25 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	-55 to +125	°C

**Note** -1.0 V (MIN.) (Pulse width: 30 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

Parameter	Symbol	Condition	-B60X, -B65X		-BE75X, -BE85X		Unit
			MIN.	MAX.	MIN.	MAX.	
Supply voltage	V <sub>CC</sub>		2.7	3.1	2.7	3.1	V
Input / Output supply voltage	V <sub>CCQ</sub>		—	—	1.65	2.1	V
High level input voltage	V <sub>IH</sub>		0.8V <sub>CC</sub>	V <sub>CC</sub> +0.3	0.8V <sub>CCQ</sub>	V <sub>CCQ</sub> +0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>	0.2V <sub>CC</sub>	-0.3 <sup>Note</sup>	0.2V <sub>CCQ</sub>	V
Operating ambient temperature	T <sub>A</sub>		-25	+85	-25	+85	°C

**Note** -0.5 V (MIN.) (Pulse width: 30 ns)

### Capacitance (T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			8	pF
Input / Output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			10	pF

**Remarks** 1. V<sub>IN</sub>: Input voltage, V<sub>I/O</sub>: Input / Output voltage  
 2. These parameters are not 100% tested.

## DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Parameter	Symbol	Test condition	Density of data hold	-B60X, -B65X			Unit
				MIN.	TYP.	MAX.	
Input leakage current	$I_{LI}$	$V_{IN} = 0\text{ V to }V_{CC}$		-1.0		+1.0	$\mu\text{A}$
I/O leakage current	$I_{LO}$	$V_{I/O} = 0\text{ V to }V_{CC}$ , $/CS = V_{IH}$ or $/WE = V_{IL}$ or $/OE = V_{IH}$		-1.0		+1.0	$\mu\text{A}$
★ Operating supply current	$I_{CCA}$	$/CS = V_{IL}$ , Minimum cycle time, $I_{I/O} = 0\text{ mA}$				50	mA
★ Standby supply current	$I_{SB1}$	$/CS \geq V_{CC} - 0.2\text{ V}$ , $MODE \geq V_{CC} - 0.2\text{ V}$	32M bits			100	$\mu\text{A}$
★	$I_{SB2}$	$/CS \geq V_{CC} - 0.2\text{ V}$ , $MODE \leq 0.2\text{ V}$	16M bits			70	
★			8M bits			60	
★			4M bits			50	
★			0M bit			30	
High level output voltage	$V_{OH}$	$I_{OH} = -0.5\text{ mA}$		$0.8V_{CC}$			V
Low level output voltage	$V_{OL}$	$I_{OL} = 1\text{ mA}$				$0.2V_{CC}$	V

**Remark**  $V_{IN}$ : Input voltage,  $V_{I/O}$ : Input / Output voltage

## DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition	Density of data hold	-BE75X, -BE85X			Unit
				MIN.	TYP.	MAX.	
Input leakage current	$I_{LI}$	$V_{IN} = 0\text{ V to }V_{CCQ}$		-1.0		+1.0	$\mu\text{A}$
I/O leakage current	$I_{LO}$	$V_{I/O} = 0\text{ V to }V_{CCQ}$ , $/CS = V_{IH}$ or $/WE = V_{IL}$ or $/OE = V_{IH}$		-1.0		+1.0	$\mu\text{A}$
★ Operating supply current	$I_{CCA}$	$/CS = V_{IL}$ , Minimum cycle time, $I_{I/O} = 0\text{ mA}$				45	mA
★ Standby supply current	$I_{SB1}$	$/CS \geq V_{CCQ} - 0.2\text{ V}$ , $MODE \geq V_{CCQ} - 0.2\text{ V}$	32M bits			100	$\mu\text{A}$
★	$I_{SB2}$	$/CS \geq V_{CCQ} - 0.2\text{ V}$ , $MODE \leq 0.2\text{ V}$	16M bits			70	
★			8M bits			60	
★			4M bits			50	
★			0M bit			30	
High level output voltage	$V_{OH}$	$I_{OH} = -0.5\text{ mA}$		$0.8V_{CCQ}$			V
Low level output voltage	$V_{OL}$	$I_{OL} = 1\text{ mA}$				$0.2V_{CCQ}$	V

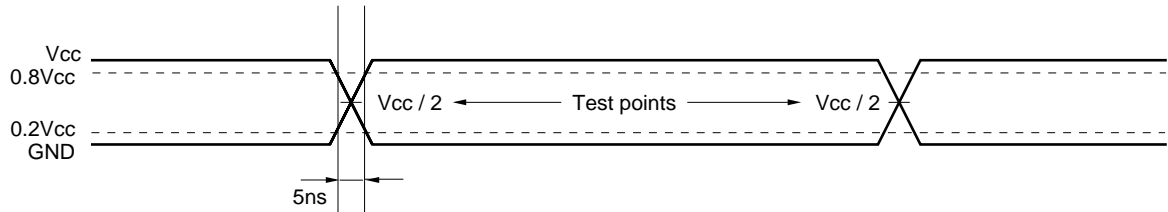
**Remark**  $V_{IN}$ : Input voltage,  $V_{I/O}$ : Input / Output voltage

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

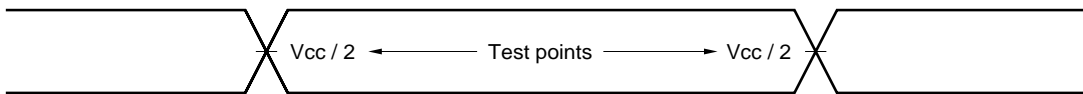
AC Test Conditions

[ -B60X, -B65X ]

Input Waveform (Rise and Fall Time ≤ 5 ns)

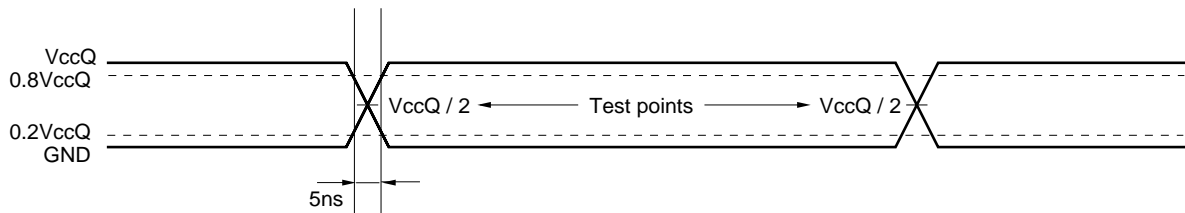


Output Waveform

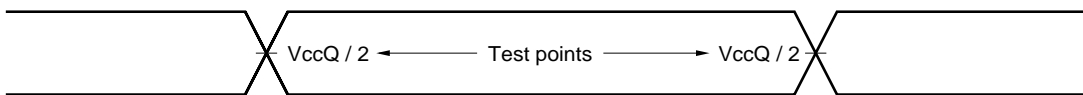


[ -BE75X, -BE85X ]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics directed with the note should be measured with the output load shown in Figure 5-1, Figure 5-2.

Figure 5-1.

[ -B60X, -B65X ]

CL: 30 pF

5 pF (tCLZ, tOLZ, tBLZ, tCHZ, tOHZ, tBHZ)

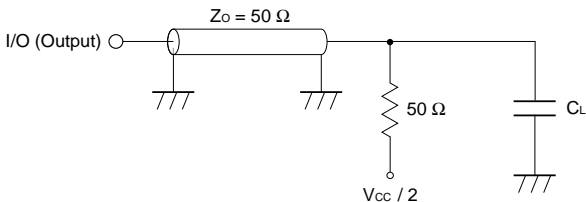
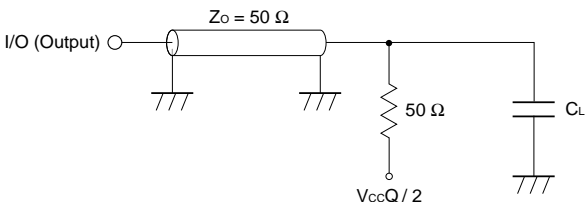


Figure 5-2.

[ -BE75X, -BE85X ]

CL: 30 pF

5 pF (tCLZ, tOLZ, tBLZ, tCHZ, tOHZ, tBHZ)



**Remark**  $C_L$  includes capacitance of the probe and jig, and stray capacitance.



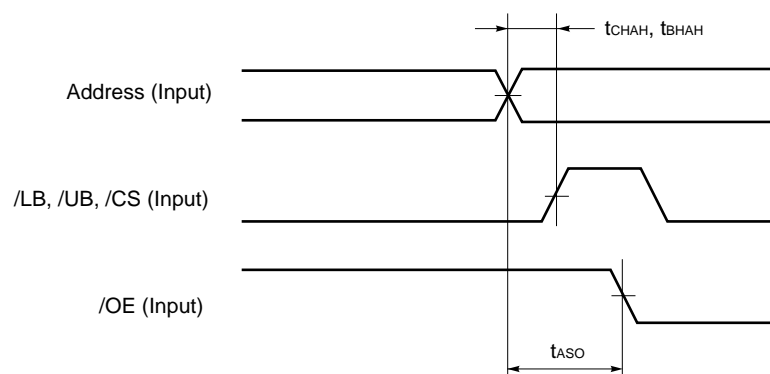
## Read Cycle

Parameter	Symbol	-B60X		-B65X		-BE75X		-BE85X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	$t_{RC}$	65		65		75		85		ns	1
Address access time	$t_{AA}$		60		65		75		85	ns	
/CS access time	$t_{ACS}$		63		65		75		85	ns	
/OE to output valid	$t_{OE}$		45		45		50		55	ns	
/LB, /UB to output valid	$t_{BA}$		63		65		75		85	ns	
Output hold from address change	$t_{OH}$	5		5		5		5		ns	
Page read cycle time	$t_{PRC}$	18		18		25		30		ns	
Page access time	$t_{PAA}$		18		18		25		30	ns	
/CS to output in low impedance	$t_{CLZ}$	10		10		10		10		ns	2
/OE to output in low impedance	$t_{OLZ}$	5		5		5		5		ns	
/LB, /UB to output in low impedance	$t_{BLZ}$	5		5		5		5		ns	
/CS to output in high impedance	$t_{CHZ}$		25		25		25		25	ns	
/OE to output in high impedance	$t_{OHZ}$		25		25		25		25	ns	
/LB, /UB to output in high impedance	$t_{BHZ}$		25		25		25		25	ns	
Address set to /OE low level	$t_{ASO}$	0		0		0		0		ns	
/OE high level to address hold	$t_{OHAH}$	-5		-5		-5		-5		ns	
/CS high level to address hold	$t_{CHAH}$	0		0		0		0		ns	3
/LB, /UB high level to address hold	$t_{BHAH}$	0		0		0		0		ns	3, 4
/CS low level to /OE low level	$t_{CLOL}$	0	10,000	0	10,000	0	10,000	0	10,000	ns	5
★ /OE low level to /CS high level	$t_{OLCH}$	45		45		50		55		ns	
/CS high level pulse width	$t_{CP}$	10		10		10		10		ns	
/LB, /UB high level pulse width	$t_{BP}$	10		10		10		10		ns	
/OE high level pulse width	$t_{OP}$	2	10,000	2	10,000	2	10,000	2	10,000	ns	5

**Notes** 1. Output load: 30 pF

2. Output load: 5 pF

3. When  $t_{ASO} \geq |t_{CHAH}|, |t_{BHAH}|$ ,  $t_{CHAH}$  and  $t_{BHAH}$  (MIN.) are -15 ns.



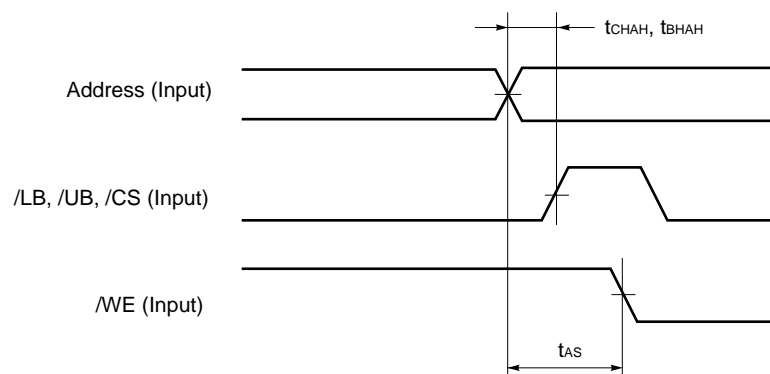
4.  $t_{BHAH}$  is specified from when both /LB and /UB become high level.

5.  $t_{CLOL}$  and  $t_{OP}$  (MAX.) are applied while /CS is being hold at low level.

# Write Cycle

Parameter	Symbol	-B60X		-B65X		-BE75X		-BE85X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	$t_{WC}$	65		65		75		85		ns	
/CS to end of write	$t_{CW}$	55		55		60		70		ns	
Address valid to end of write	$t_{AW}$	55		55		60		70		ns	
/LB, /UB to end of write	$t_{BW}$	55		55		60		70		ns	
Write pulse width	$t_{WP}$	50		50		55		60		ns	
Write recovery time	$t_{WR}$	0		0		0		0		ns	
/CS pulse width	$t_{CP}$	10		10		10		10		ns	
/LB, /UB high level pulse width	$t_{BP}$	10		10		10		10		ns	
/WE high level pulse width	$t_{WHP}$	10		10		10		10		ns	
Address setup time	$t_{AS}$	0		0		0		0		ns	
/OE high level to address hold	$t_{OHAH}$	-5		-5		-5		-5		ns	
/CS high level to address hold	$t_{CHAH}$	0		0		0		0		ns	1
/LB, /UB high level to address hold	$t_{BHAH}$	0		0		0		0		ns	1, 2
Data valid to end of write	$t_{DW}$	30		30		35		35		ns	
Data hold time	$t_{DH}$	0		0		0		0		ns	
/OE high level to /WE set	$t_{OES}$	0	10,000	0	10,000	0	10,000	0	10,000	ns	3
/WE high level to /OE set	$t_{OEH}$	10	10,000	10	10,000	10	10,000	10	10,000	ns	

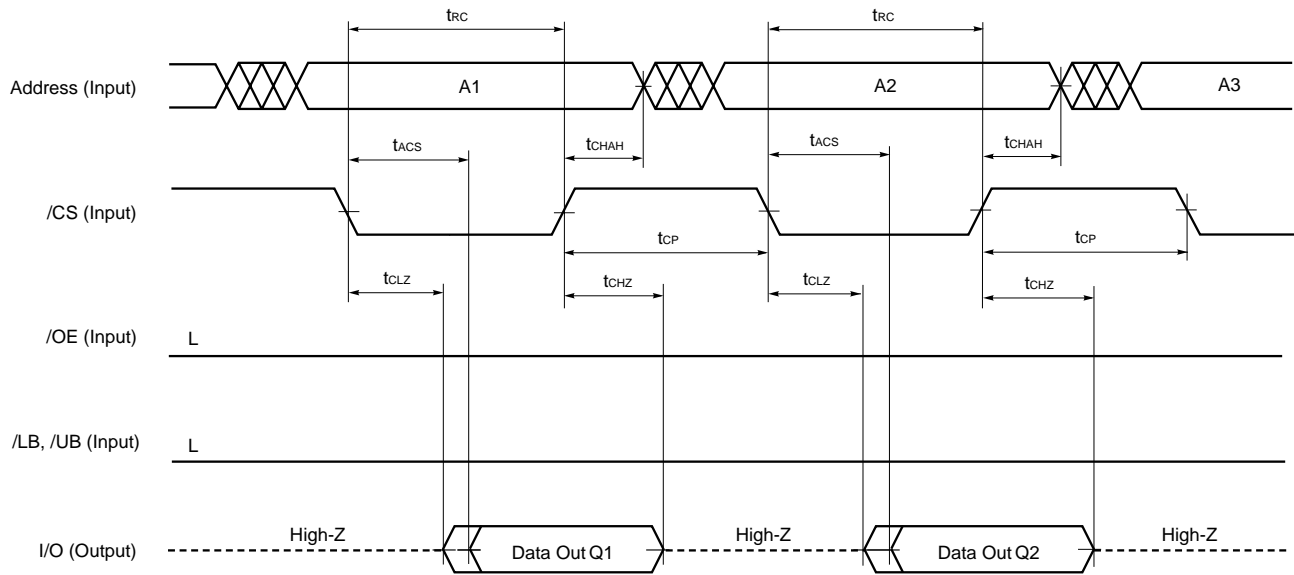
**Notes 1.** When  $t_{AS} \geq |t_{CHAH}|, |t_{BHAH}|$  and  $t_{CP} \geq 18$  ns,  $t_{CHAH}$  and  $t_{BHAH}$  (MIN.) are -15 ns.



- $t_{BHAH}$  is specified from when both /LB and /UB become high level.
- $t_{OES}$  and  $t_{OEH}$  (MAX.) are applied while /CS is being hold at low level.

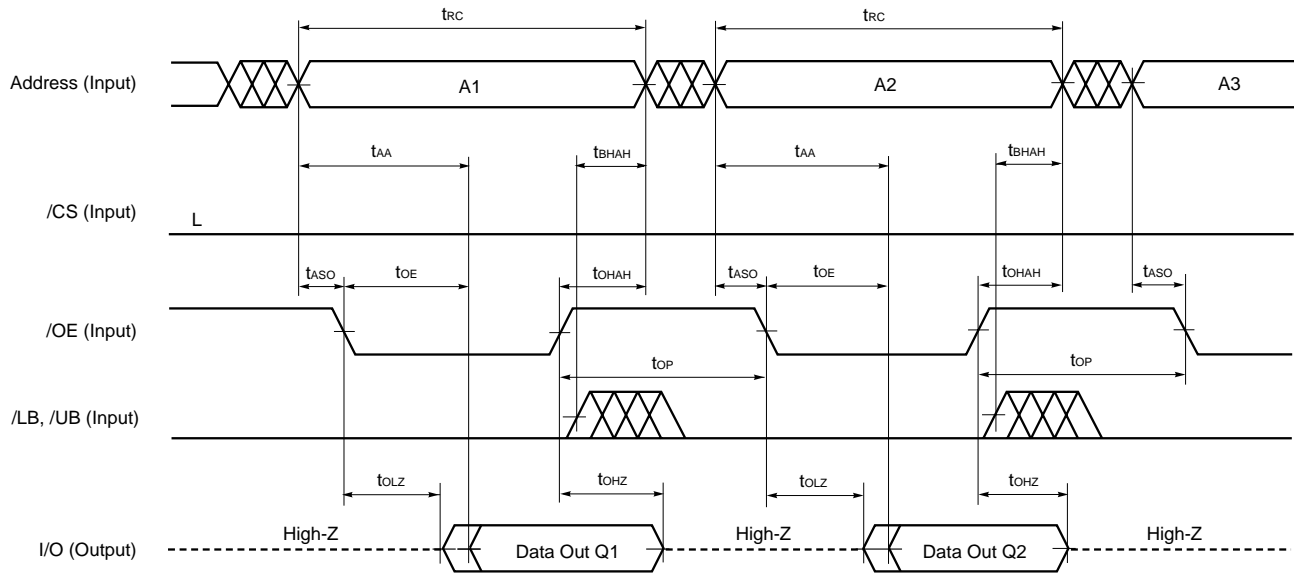
## 6. Timing Charts

Figure 6-1. Read Cycle Timing Chart 1 (/CS Controlled)



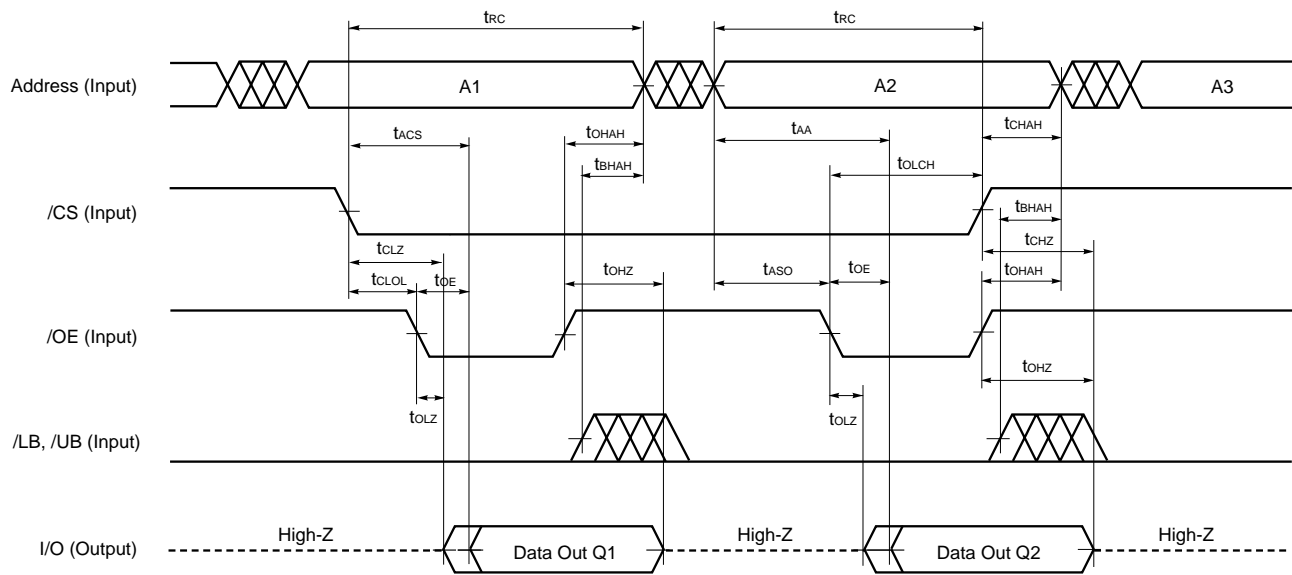
**Remark** In read cycle, MODE and /WE should be fixed to high level.

Figure 6-2. Read Cycle Timing Chart 2 (/OE Controlled)



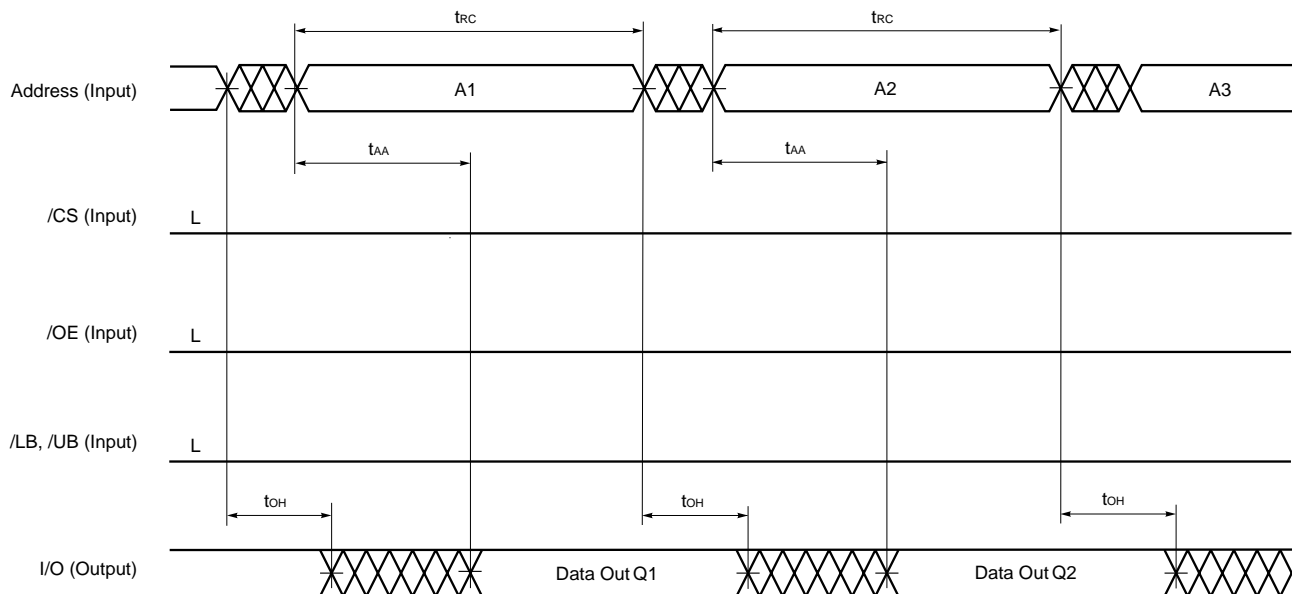
**Remark** In read cycle, MODE and /WE should be fixed to high level.

Figure 6-3. Read Cycle Timing Chart 3 (/CS, /OE Controlled)



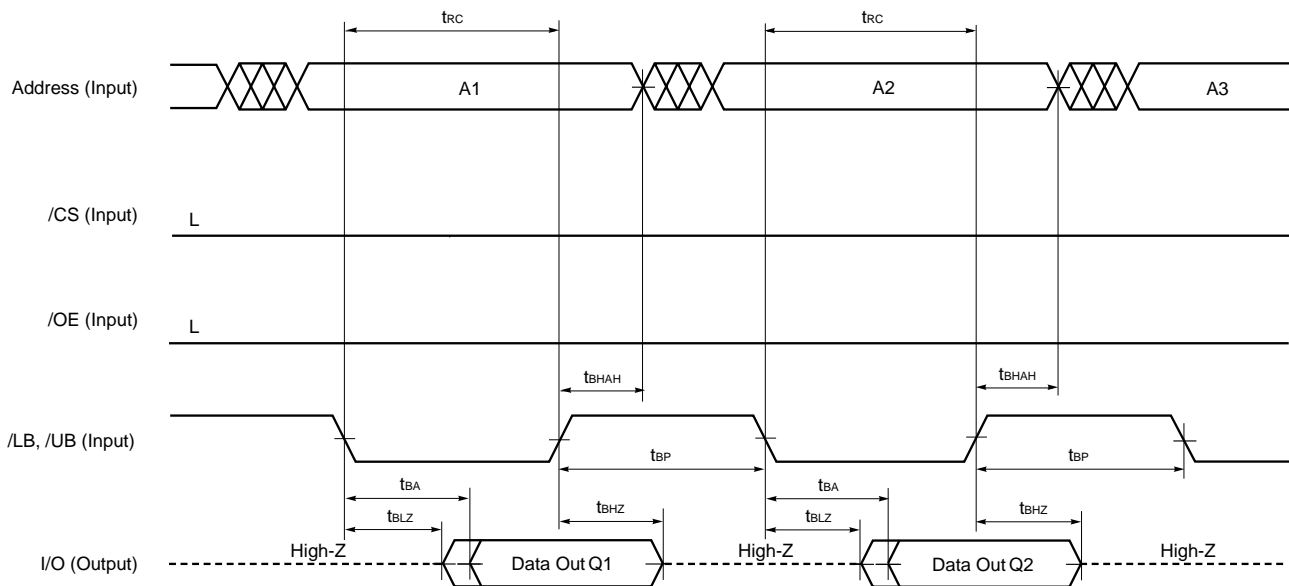
**Remark** In read cycle, MODE and /WE should be fixed to high level.

Figure 6-4. Read Cycle Timing Chart 4 (Address Controlled)



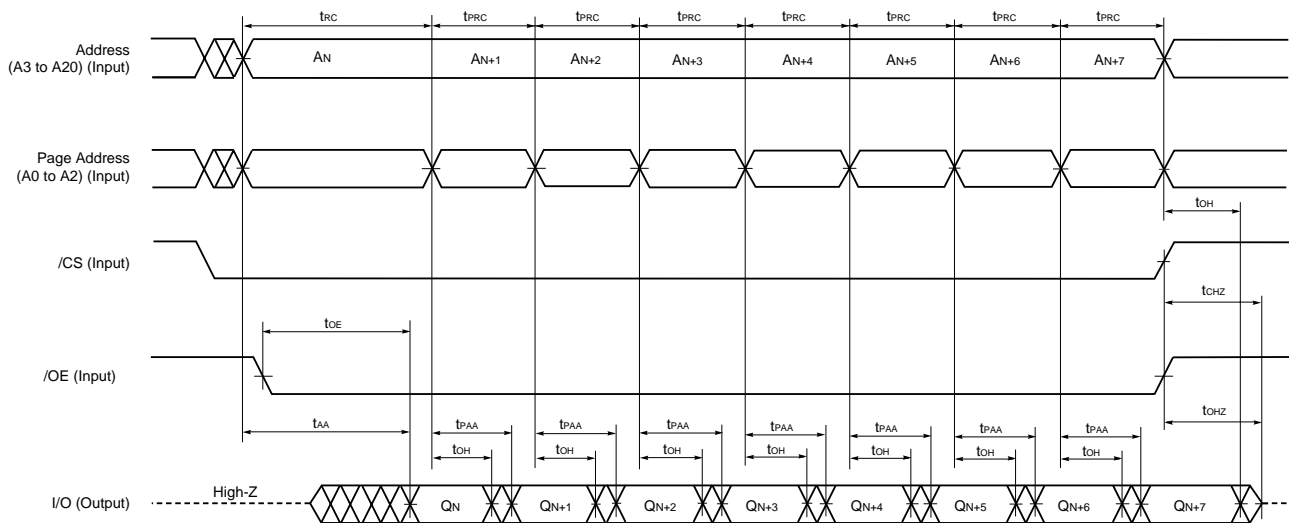
**Remark** In read cycle, MODE and /WE should be fixed to high level.

Figure 6-5. Read Cycle Timing Chart 5 (/LB, /UB Controlled)



**Remark** In read cycle, MODE and /WE should be fixed to high level.

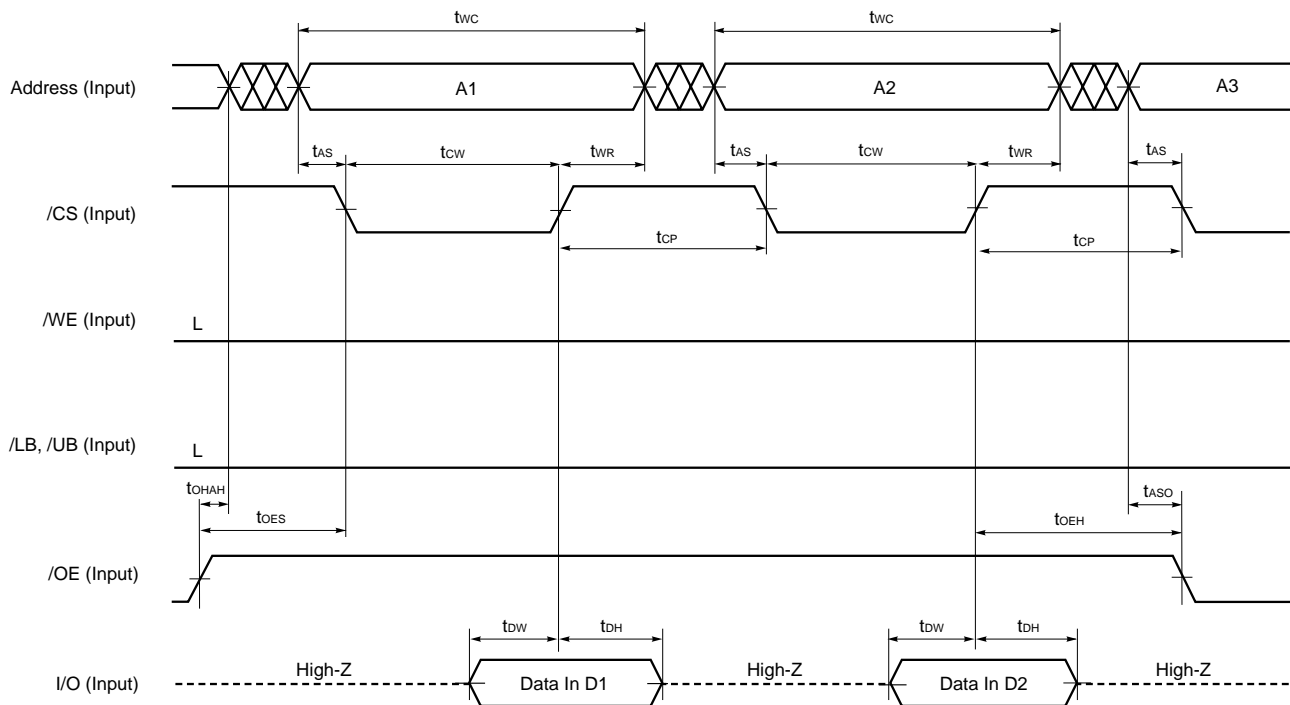
Figure 6-6. Page Read Cycle Timing Chart



**Remarks 1.** In read cycle, MODE and /WE should be fixed to high level.

**2.** /LB and /UB are low level.

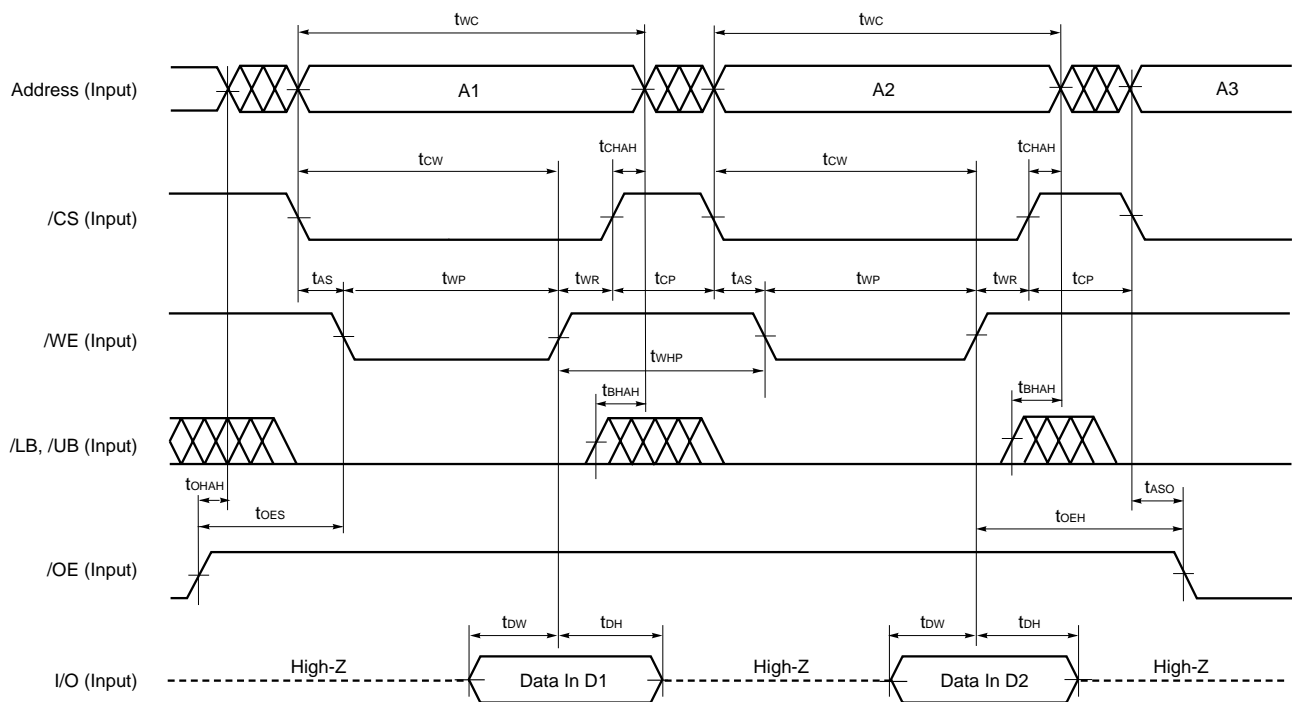
Figure 6-7. Write Cycle Timing Chart 1 (/CS Controlled)



- Cautions**
1. During address transition, at least one of pins  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$ , or both of  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  pins should be inactivated.
  2. Do not input data to the I/O pins while they are in the output state.
  3. In write cycle,  $\text{MODE}$  and  $\overline{\text{OE}}$  should be fixed to high level.

**Remark** Write operation is done during the overlap time of a low level  $\overline{\text{CS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{LB}}$  and/or  $\overline{\text{UB}}$ .

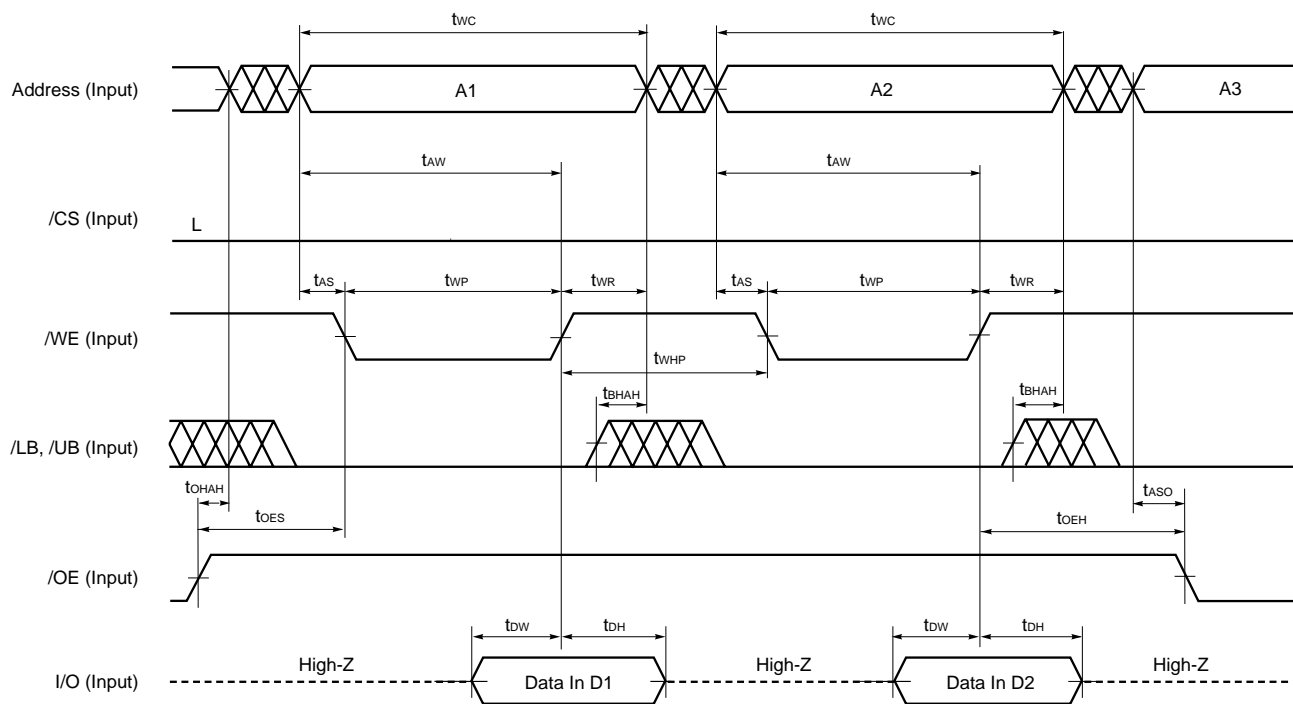
Figure 6-8. Write Cycle Timing Chart 2 (/WE Controlled)



- Cautions**
1. During address transition, at least one of pins  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$ , or both of  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  pins should be inactivated.
  2. Do not input data to the I/O pins while they are in the output state.
  3. In write cycle,  $\text{MODE}$  and  $\overline{\text{OE}}$  should be fixed to high level.

**Remark** Write operation is done during the overlap time of a low level  $\overline{\text{CS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{LB}}$  and/or  $\overline{\text{UB}}$ .

Figure 6-9. Write Cycle Timing Chart 3 (/WE Controlled)

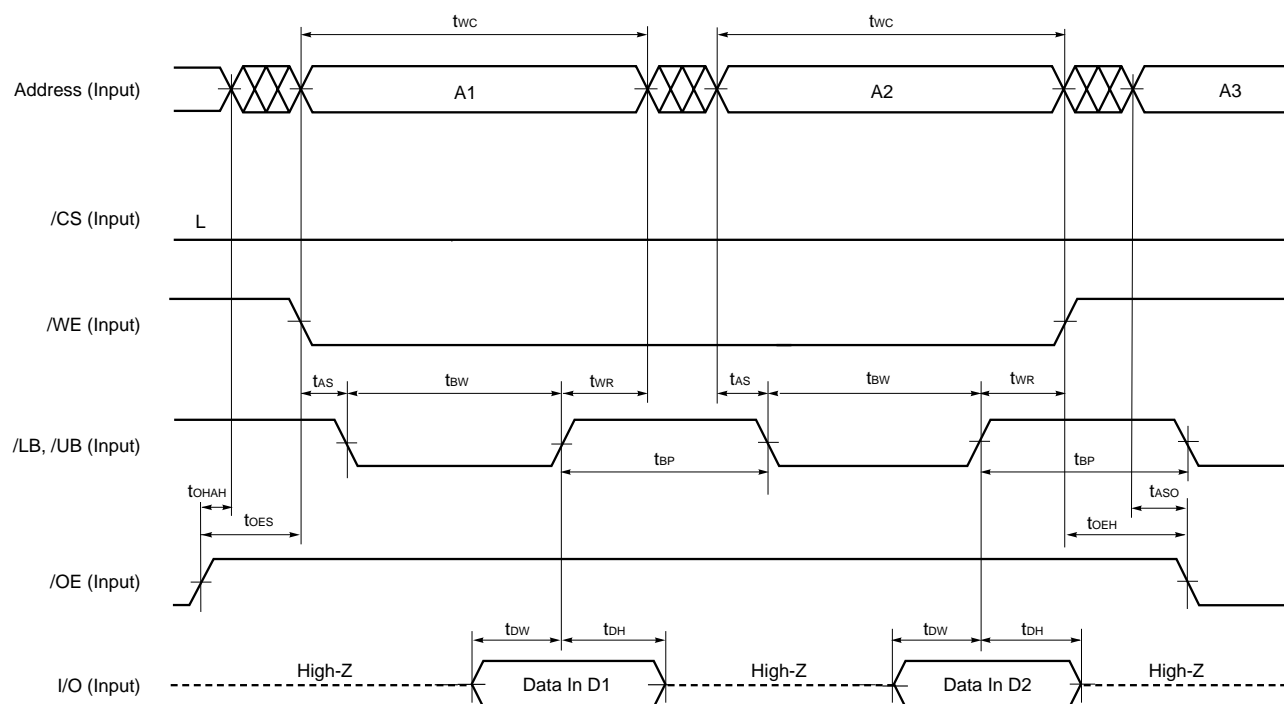


- Cautions**
1. During address transition, at least one of pins  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$ , or both of  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  pins should be inactivated.
  2. Do not input data to the I/O pins while they are in the output state.
  3. In write cycle,  $\text{MODE}$  and  $\overline{\text{OE}}$  should be fixed to high level.

**Remark** Write operation is done during the overlap time of a low level  $\overline{\text{CS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{LB}}$  and/or  $\overline{\text{UB}}$ .



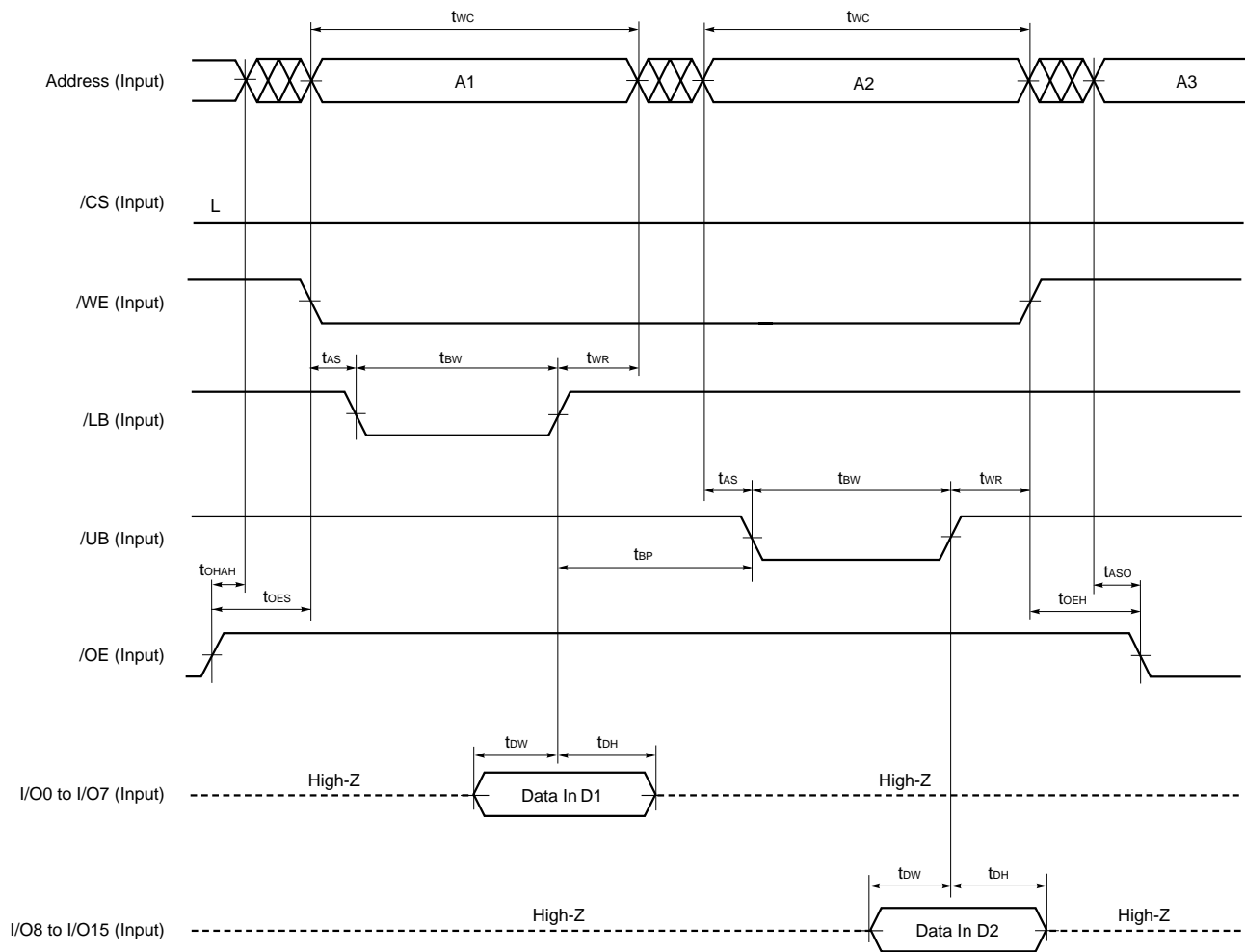
Figure 6-10. Write Cycle Timing Chart 4 (/LB, /UB Controlled)



- Cautions**
1. During address transition, at least one of pins /CS and /WE, or both of /LB and /UB pins should be inactivated.
  2. Do not input data to the I/O pins while they are in the output state.
  3. In write cycle, MODE and /OE should be fixed to high level.

**Remark** Write operation is done during the overlap time of a low level /CS, /WE, /LB and/or /UB.

Figure 6-11. Write Cycle Timing Chart 5 (/LB, /UB Independent Controlled)



- Cautions**
1. During address transition, at least one of pins /CS and /WE, or both of /LB and /UB pins should be inactivated.
  2. Do not input data to the I/O pins while they are in the output state.
  3. In write cycle, MODE and /OE should be fixed to high level.

**Remark** Write operation is done during the overlap time of a low level /CS, /WE, /LB and/or /UB.

Figure 6-12. Mode Register Setting Timing Chart

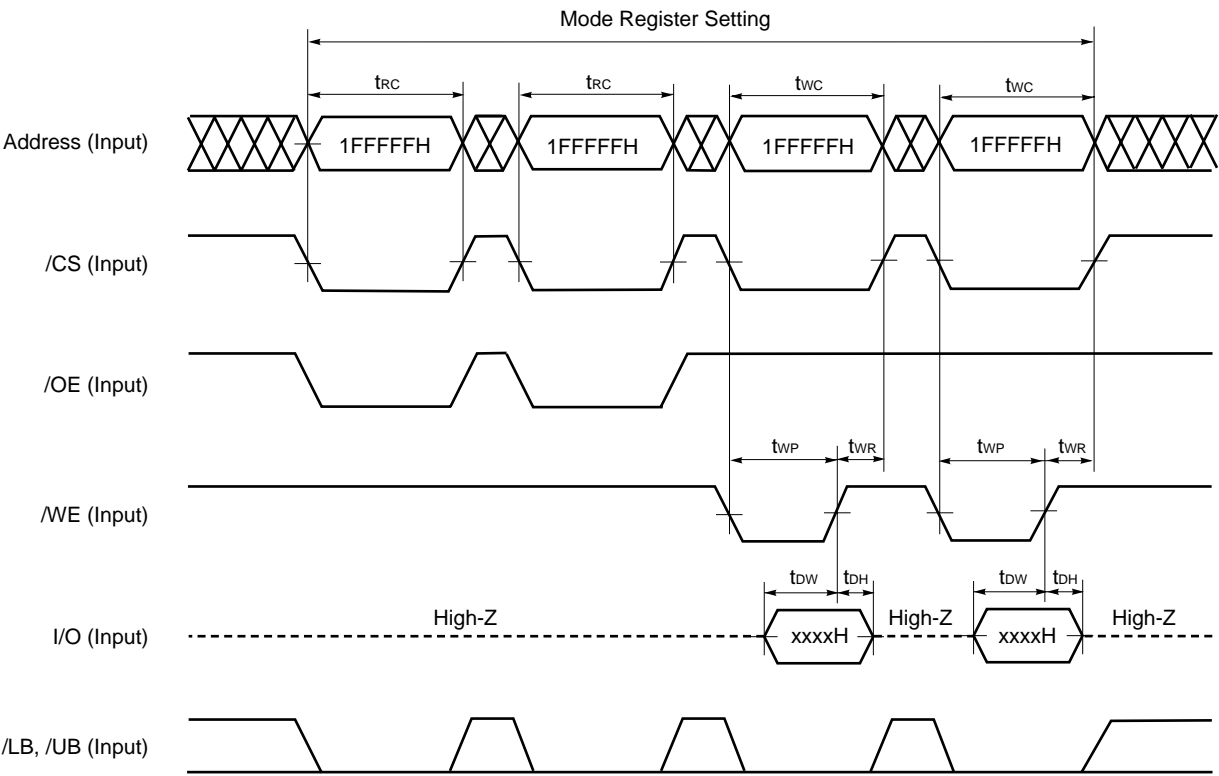
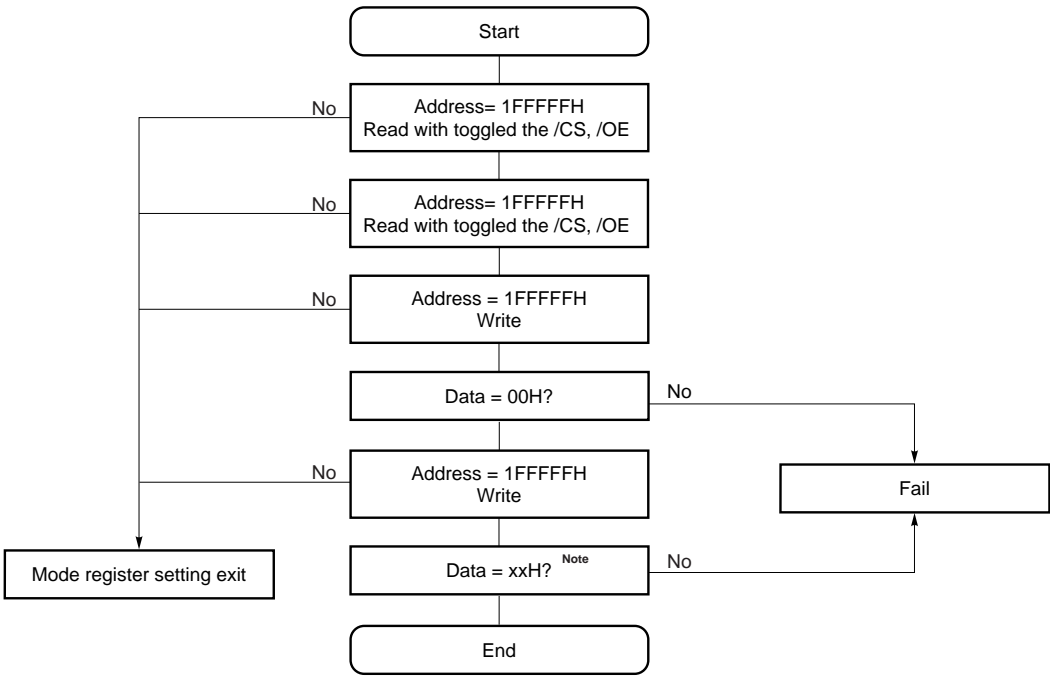


Figure 6-13. Mode Register Setting Flow Chart



**Note** xxH = 04H, 05H, 06H, 07H

Figure 6-14. Standby Mode 2 (data hold: 16M bits / 8M bits / 4M bits) Entry / Exit Timing Chart

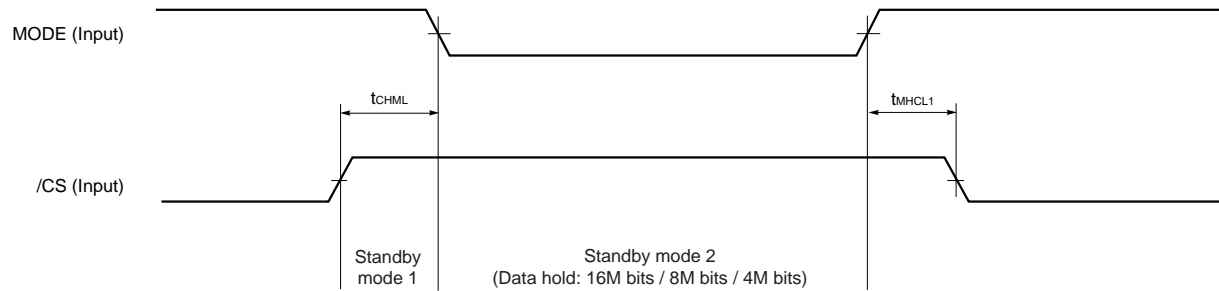
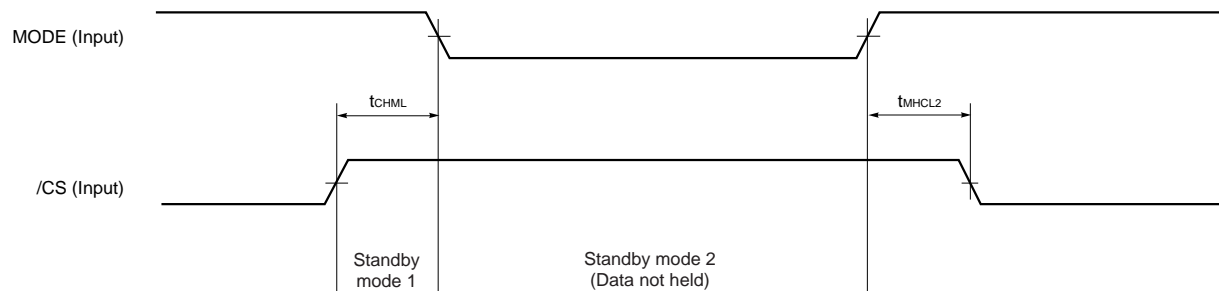


Figure 6-15. Standby Mode 2 (data not held) Entry / Exit Timing Chart



#### Standby Mode 2 Entry / Exit Timing

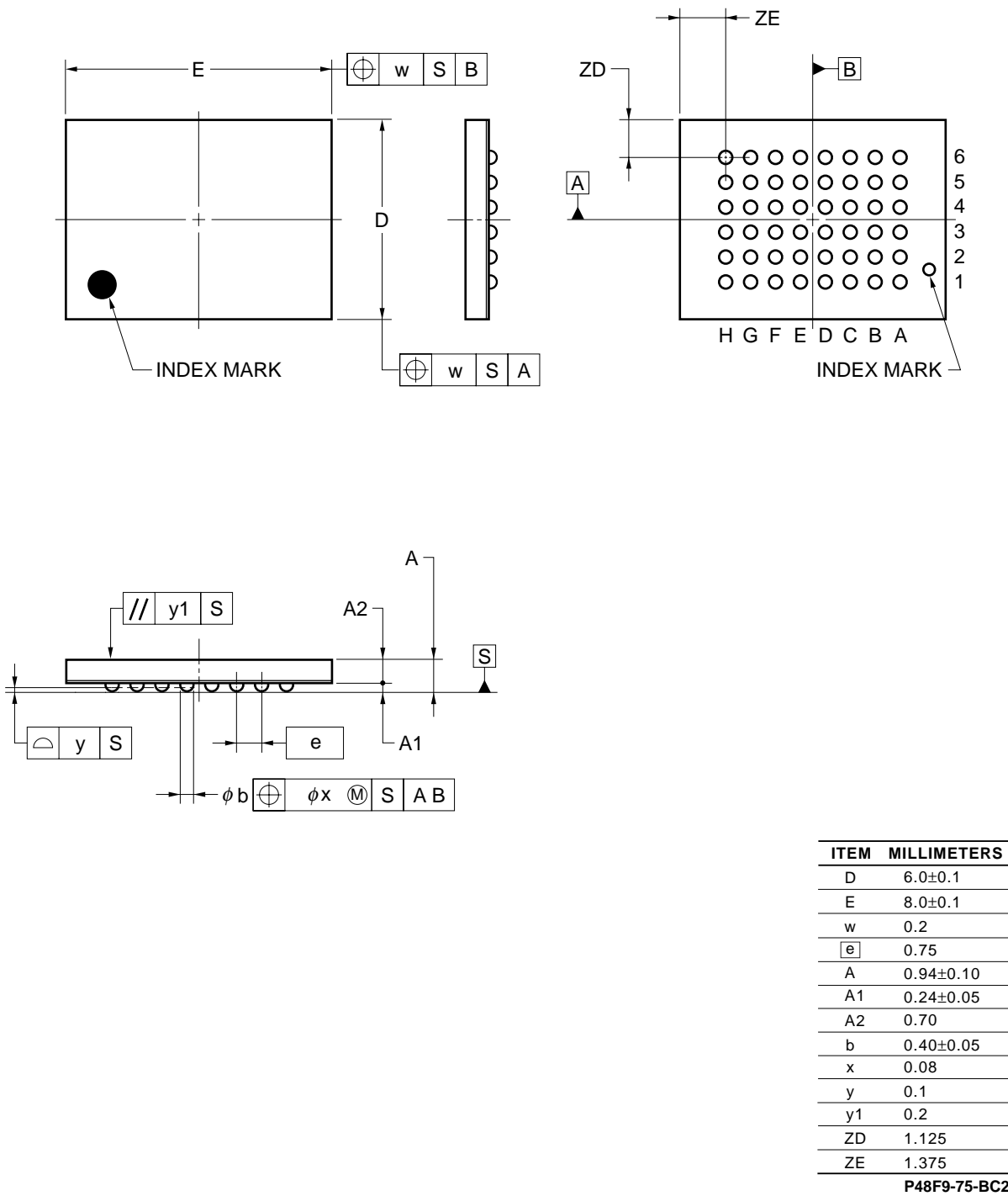
Parameter	Symbol	MIN.	MAX.	Unit	Note
Standby mode 2 entry /CS high level to MODE low level	$t_{CHML}$	0		ns	
Standby mode 2 exit to normal operation MODE high level to /CS low level	$t_{MHCL1}$	30		ns	1
Standby mode 2 exit to normal operation MODE high level to /CS low level	$t_{MHCL2}$	200		μs	2

**Notes** 1. This is the time it takes to return to normal operation from Standby Mode 2 (data hold: 16M bits / 8M bits / 4M bits).

2. This is the time it takes to return to normal operation from Standby Mode 2 (data not held).

7. Package Drawing

48-PIN TAPE FBGA (8x6)



## 8. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the  $\mu$ PD4632312A-X.

### Type of Surface Mount Device

$\mu$ PD4632312AF9-BC2: 48-pin TAPE FBGA (8 x 6)

## 9. Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
5th edition/ Jan. 2003	pp.1, 2	pp.1, 2	Addition	Features, Ordering Information	-B60X: The note under development was added.
	pp.1, 15	pp.1, 15	Modification	Features, DC Characteristics	Operating supply current (MAX.): -B65X: 45 mA → 50 mA -BE75X, -BE85X: 40 mA → 45 mA Standby supply current (MAX.): Density of data hold 32M bits: 70 μA → 100 μA 16M bits: 50 μA → 70 μA 8M bits: 45 μA → 60 μA 4M bits: 42 μA → 50 μA 0M bit : 10 μA → 30 μA
	p.17	p.17	Modification	Read Cycle	t <sub>OLCH</sub> (MIN.): -BE75X: 45 ns → 50 ns -BE85X: 45 ns → 55 ns

[MEMO]



[MEMO]

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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