

Description

The NL82721 is a 128K bit Ternary Synchronous Content Addressable Memory. The NL82721 device performs high-speed parallel search operations on memory tables. Its primary application is as an address filter or an address translator for Fast Ethernet, Gigabit Ethernet, and ATM switches.

NL82721 has a mask word associated with every memory word. This enables the user to effectively store a “don’t care” state for compare operations (in addition to ‘0’ and ‘1’) making it a Ternary CAM. This device is ideal for enabling policy enforcement and packet classification for differentiated services in edge, campus and enterprise networking applications.

Features

- 1K x 128 Synchronous Ternary CAM Architecture
- 1K x 128 Local Mask Words allow masking of each CAM word on a bit by bit basis.
- Single cycle “Learn” instruction for easy table updates
- Match Flag times: 18/22 ns
- CAM Index output (flow through mode): 21/25 ns
- CAM Index output (pipelined mode): 10/12 ns
- Depth-expansion with no glue logic required
- Sustained 64-bit searches of up to 40 Million/Second (128-bit search rate of 20 Million/Second)
- Separate 64-bit Comparand I/O bus, 64-bit Results bus and 14-bit Instruction bus
- Two validity bits (Skip and Empty) for each location define the location as Valid, Skip, Empty or RAM
- Two 128-bit wide Mask Registers for easy masking of compare or write operations
- Single cycle execution of all instructions
- 3.3V TTL CMOS; 292-pin PBGA Package

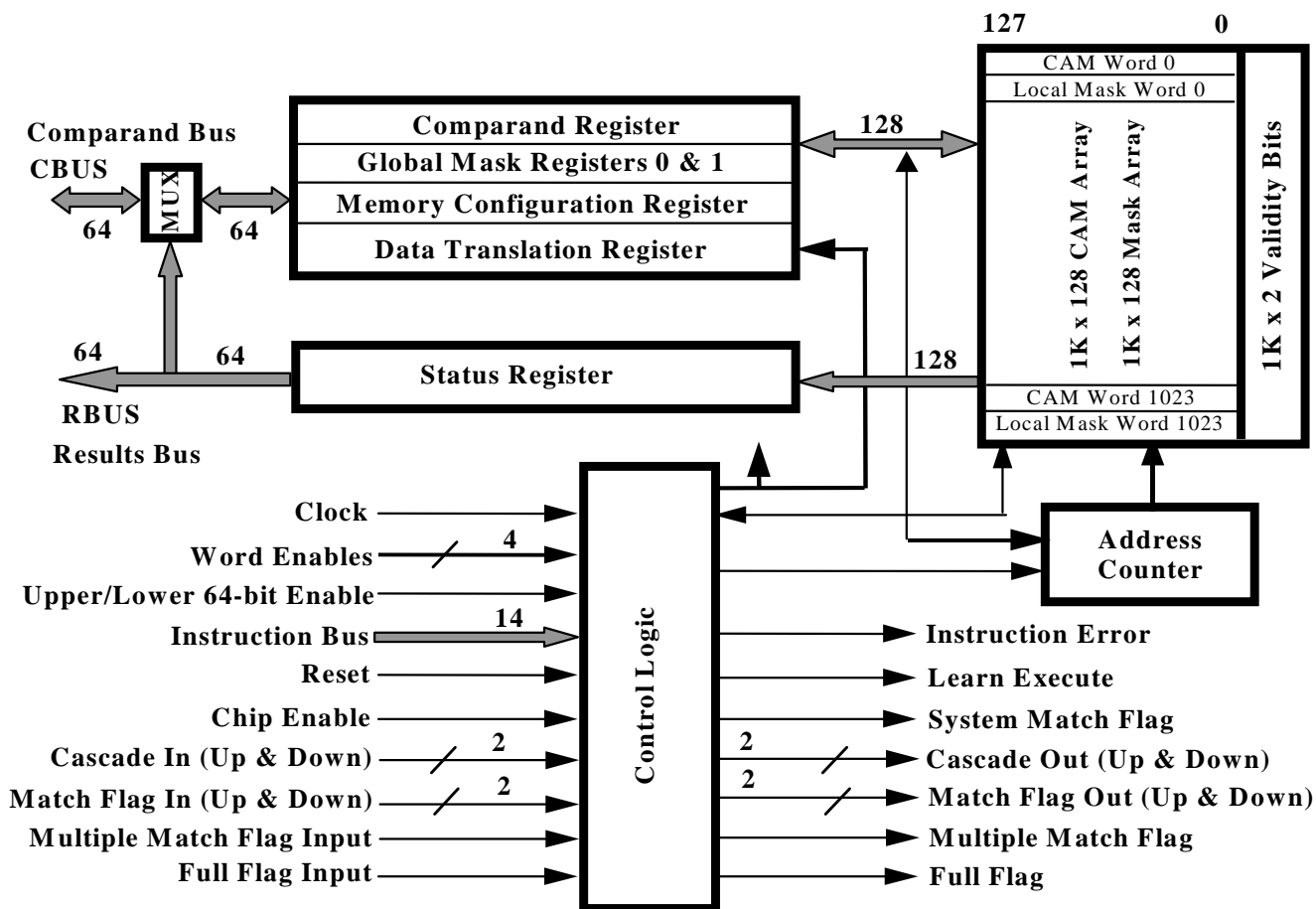


Figure 1 NL82721 Block Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	CBUS02	CBUS04	CBUS06	CBUS10	CBUS12	CBUS15	CBUS18	CBUS21	CBUS24	CBUS25	CBUS27	CBUS30	CBUS32	CBUS35	CBUS37	CBUS42	CBUS43	CBUS47	CBUS49	CBUS50
B	CBUS01	CBUS05	CBUS07	CBUS08	CBUS11	CBUS14	CBUS17	CBUS20	CBUS22	CBUS26	CBUS28	CBUS31	CBUS34	CBUS36	CBUS38	CBUS41	CBUS44	CBUS46	CBUS48	CBUS51
C	CBUS00	CBUS03	GND	CBUS09	CBUS13	VDD	CBUS16	CBUS19	CBUS23	VDD	CBUS29	CBUS33	CBUS39	VDD	CBUS40	CBUS45	GND	CBUS52	CBUS53	CBUS54
D	IBUS02	IBUS00	/RST	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	GND	CBUS55	CBUS56
E	IBUS04	IBUS03	IBUS01	GND													GND	CBUS58	CBUS57	CBUS59
F	IBUS07	IBUS06	IBUS05	VDD													VDD	VDD	CBUS60	CBUS61
G	IBUS09	IBUS08	VDD	VDD													VDD	(NC)	CBUS63	CBUS62
H	IBUS12	IBUS11	IBUS10	GND									GND				GND	(NC)	(NC)	(NC)
J	/CE	CLK	IBUS13	GND								GND	GND				GND	(NC)	(NC)	(NC)
K	ULEN	/WEN2	/WEN3	VDD								GND	GND				VDD	VDD	(NC)	(NC)
L	/WEN1	/WEN0	VDD	VDD								GND	GND				VDD	(NC)	(NC)	(NC)
M	/FF1	/MMF1	/MFUI	GND								GND	GND				GND	(NC)	(NC)	(NC)
N	CSCUI	/MFDI	CSCDI	GND								GND	GND				GND	(NC)	(NC)	(NC)
P	(NC)	CSCUO	/MFUO	VDD													VDD	VDD	(NC)	RBUS62
R	CSCDO	/MFD0	VDD	VDD													VDD	RBUS63	RBUS60	RBUS61
T	(NC)	/SMF	/LEX	GND													GND	RBUS58	RBUS57	RBUS59
U	/MMF	/FF	/IERR	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	VDD	VDD	GND	GND	GND	RBUS55	RBUS56
V	RBUS00	RBUS01	GND	RBUS09	RBUS13	VDD	RBUS16	RBUS19	RBUS23	VDD	RBUS29	RBUS33	RBUS39	VDD	RBUS40	RBUS45	GND	RBUS52	RBUS53	RBUS54
W	RBUS02	RBUS03	RBUS06	RBUS08	RBUS11	RBUS14	RBUS17	RBUS20	RBUS22	RBUS26	RBUS28	RBUS31	RBUS34	RBUS36	RBUS38	RBUS41	RBUS44	RBUS46	RBUS48	RBUS51
Y	RBUS04	RBUS05	RBUS07	RBUS10	RBUS12	RBUS15	RBUS18	RBUS21	RBUS24	RBUS25	RBUS27	RBUS30	RBUS32	RBUS35	RBUS37	RBUS42	RBUS43	RBUS47	RBUS49	RBUS50
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Figure 2 NL82721 Ball Assignment (292 PBGA, Top View)

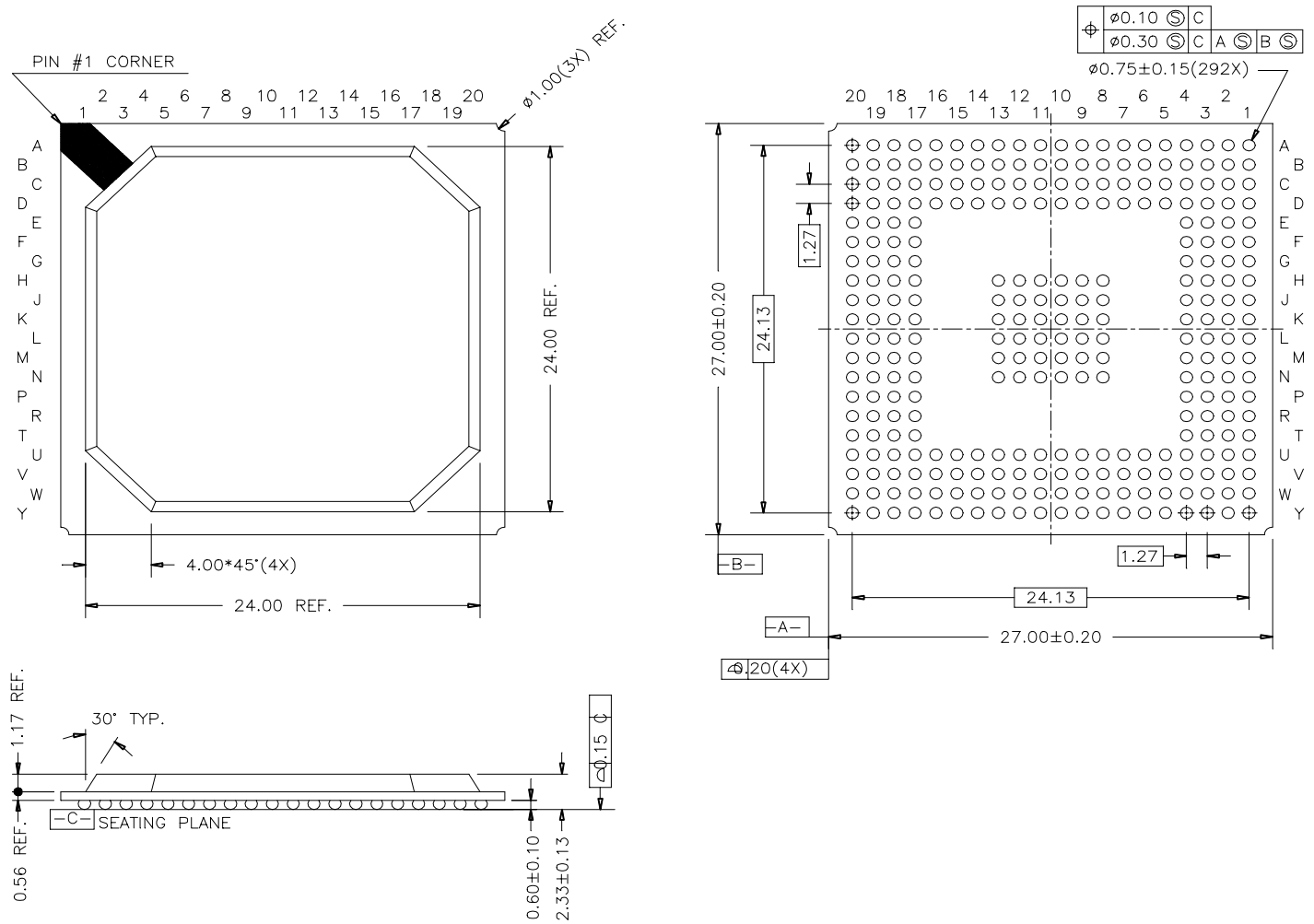


Figure 3: 292 PBGA Package Dimensions

1.0 Functional Description

The NL82721 is a Synchronous Content Addressable Memory (IPCAM™) designed for use as an address filter or an address translator in 100/1000 Mb/s Ethernet switches and routers. This device can also be used to implement fast routing tables in Internet Protocol (IP) switches. The NL82721 has a total associative memory capacity of 128K bits organized as 1K x 128 bits.

Each 128-bit memory word has associated with it a 128-bit local mask word that is used during compare operation. In contrast to global masks, these local mask words are used only with their associated word. This local mask is used only for compare instructions and is always used (not deselectable as global masks). This provides masking on an individual bit basis and hence Ternary CAM capability. This masking on a per bit basis capability is useful to store subnet masks in Internet Protocol (IP). The NL82721 is thus referred to as IPCAM™.

A bi-directional 64-bit Comparand Bus (CBUS) enables all internal registers and memory to be accessed. An output only, 64-bit Results Bus (RBUS) provides status information after a compare operation. A 14-bit Instruction Bus (IBUS) allows instructions to be presented to the device once every cycle. All operations on the device are timed synchronously with the rising edge of a free running clock.

The Comparand Register (CR) is a 128-bit register that enables the user to write the comparand data (key) and compare it with the contents of memory. This is the only register that enables a user to store and compare data with memory.

The NL82721 has two Global Mask Registers (GMR1-GMR0) that can each be selected on an operation by operation basis for write or compare operations. For a write operation, when the bits in these registers are programmed with '1's, the corresponding bits in memory will be masked, i.e. will not be written into. For compare operations, the corresponding bits in the associative data word will be forced to a match.

The 16-bit Device Configuration Register (DCR) enables the user to configure the device operation. One can configure the RBUS to be in pipeline or flow through mode, RBUS to output the upper or the lower 64 bits of the Status Register, Address Counter to be incremented automatically during write and so on. See Table 3d for a complete list.

The Memory Configuration Register (MCR) is a 128-bit wide register used as a mask during Compare instruction cycles. It provides compare masking capability in addition to the global masks. This memory configuration register is always used during comparison as opposed to the global mask registers, which may or may not be selected during comparison. After reset, all bits are '0' indicating no masking of any bits during comparison.

The Data Translation Register (DTR) is a 128-bit register that allows manipulation of data stored in it.

The Status Register (SR) holds status information after compare, read, write or copy operations.

A 10-bit Address Counter (ACR) supplies the address to the memory array. This counter may be loaded with any valid start address and can be configured to increment once every cycle for read or write operations. This allows data to be loaded into or read out of the memory continuously.

An Upper 64-bit/Lower 64-bit enable pin (ULEN) allows accesses to either the upper 64-bits or the lower 64-bits of the 128-bit words of memory and registers.

Four Word Enable (/WEN3-/WEN0) inputs allow access to the internal registers and memory on 16-bit boundaries. These inputs also allow for bus matching on the CBUS with no glue logic.

The NL82721 has "Learn" instructions that enable the user to automatically update the memory when a "No Match" is obtained on a comparison. The comparand data is written into the Next Free Address and this address is output on the RBUS. The Learn Execute pin (/LEX) asserts an active low when a Learn instruction is executed and a memory update takes place.

The NL82721 can be clocked up to frequencies of 40MHz with a free running clock. A Chip Enable (/CE) input allows the device to be selected or deselected similar to any memory device. The device has flag inputs and outputs that enable depth cascading with no glue logic. The Instruction Error pin (/IERR) asserts an active low when erroneous Opcodes are presented to the device.

2.0 Pin Description

2.1 Clock (CLK)

This is a free running clock that is used to time all transactions on the CAM. The rising edge of the clock is the timing reference.

2.2 Chip Enable (/CE)

This is a synchronous input that selects the device for all operations, when asserted low. When asserted high, the device is deselected and is in idle mode. In idle mode, the CBUS and the RBUS are high-z. For single device operation, when the device is deselected (/CE asserted high) the Match, Multiple Match and System Match Flags are high and Full Flag is low. For depth cascaded devices, the deselected devices will pass the flag input states through to the flag outputs. When /CE is taken from a "1" to a "0" (idle to active), a NOP is necessary for the device (and the devices in the cascade chain, if applicable) to be activated except in the case of a Comparand Register access. The user may access the Comparand Register in the same cycle as /CE transitions from "1" to "0" (Idle to active). See Table 1.

2.3 Reset (/RST)

This is an asynchronous input and provides the hardware reset for the device. During initialization, this pin must be asserted low for a minimum of *three (3) cycles*. This will set all CAM words to empty, initialize the control logic, and clear all registers. The reset operation must be followed by at least one NOP instruction. Tables 2 and 3a-3g illustrate the state of the part after reset.

2.4 Full Flag Input (/FFI)

This input is provided for depth cascading multiple CAMs. When asserted low, this pin will allow data to be written into the CAM at the next free address (NFA) using the "Write to memory at NFA" instruction provided the device is not full. However, write to memory at address specified by the Address Counter is not affected by full flag input or output. For single device operation, the /FFI pin is tied to ground. For depth cascaded devices, the highest priority device has its /FFI input tied to ground, all other devices in the cascade having the /FFI tied to the Full Flag output (/FF) of the next higher priority device. Refer to the depth cascading section for more details.

2.5 Match Flag Up Input (/MFUI)

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices, the lowest priority device has its /MFUI pin connected to VDD. All other devices in the cascade have their /MFUI pin tied to the Match Flag Up Output (/MFUO) of the next Lower priority device. Refer to the depth cascading section for more details.

2.6 Match Flag Down Input (/MFDI)

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices, the highest Priority device has its /MFDI pin connected to VDD. All other devices in the cascade have their /MFDI pin tied to the Match Flag Down Output (/MFDO) of the next higher priority device. Refer to the depth cascading section for more details.

2.7 Multiple Match Flag Input (/MMFI)

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices the highest priority device has its /MMFI tied to VDD. All other devices in the cascade have their /MMFI pin tied to the Multiple Match Flag (/MMF) of the next higher Priority device. Refer to the depth cascading section for more details.

2.8 Cascade Down Input (CSCDI)

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to ground. For depth cascaded devices the highest priority device has its CSCDI connected to ground. All other devices in the cascade have their CSCDI pin tied to the CSCDO of the next higher priority device. Refer to the depth cascading section for more details.

2.9 Cascade Up Input (CSCUI)

This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to ground. For depth cascaded devices the lowest Priority device has its CSCUI connected to ground. All other devices in the cascade have their CSCUI pin tied to the CSCUI of the next lower priority device. Refer to the depth expansion section for more details.

2.10 Upper/Lower 64-bit enable (ULEN)

This is a synchronous input and enables access to the upper 64-bits or the lower 64-bits of the 128-bit memory, Memory Configuration, Global Mask, Comparand, Data Translation and Status Registers. When ULEN is high, it enables access to the upper 64 bits of the 128 bits; when it is low, it enables access to the lower 64 bits of the 128 bits.

2.11 Word Enable (/WEN_0,1,2,3)

This is a synchronous input and enables access to the CAM array and all the registers with 16-bit granularity. For 64-bit entities in the CAM, /WEN_3 enables access to bits 63-48, /WEN_2 to bits 47-32, /WEN_1 to bits 31-16 and /WEN_0 to bits 15-0. These control pins are effective only for read and write to memory and the registers; for all other operations they are a "don't care".

2.12 Instruction Bus (IBUS_{13..IBUS₀})

This is a synchronous 14-bit bus that provides the operation code (Opcode) to the CAM.

2.13 Comparand Bus (CBUS_{63..CBUS₀})

This is a 64-bit synchronous I/O bus that conveys data to and from the memory and the registers.

2.14 Instruction Error (/IERR)

This is a synchronous output and will be asserted low whenever an erroneous Opcode is detected. An erroneous Opcode is one that does not conform to the listed Opcodes for the IPCAM™. In a depth cascade all devices will provide the Instruction Error output. The user is advised against issuing erroneous Opcodes, as the results will be non-deterministic.

2.15 Learn Execute (/LEX)

This is a synchronous output and is asserted for one cycle, every time a Learn Instruction is executed and a memory update takes place. For all other instructions it is high-z. In depth cascaded devices, all the Learn Execute pins are tied together to provide the System Learn Execute indication. This pin needs an external pull-up resistor if used. This is an open drain output.

2.16 Cascade Down Output (CSCDO)

This output is provided for depth cascading multiple CAMs. For single device operation this pin must be left unconnected. For depth cascaded devices, the highest priority device has its CSCDO connected to the CSCDI of the next lower priority device. Refer to the depth expansion section for more details.

2.17 Cascade Up Output (CSCUO)

This output is provided for depth cascading multiple CAMs. For single device operation this pin must be left unconnected. For depth cascaded devices, the lowest priority device has its CSCUO connected to the CSCUI of the next higher priority device. Refer to the depth expansion section for more details.

2.18 Full Flag (/FF)

This is a synchronous output and is updated after Learn, Write to Memory, Copy to Memory, set VBITs or Set Full Flag operations. After reset, this pin is high. When the device is full, /FF is asserted low. For depth cascaded devices, /FF is connected to /FFI of the next lower priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /FFI through to /FF.

2.19 Match Flag Up Output (/MFUO)

This synchronous output is provided for depth cascading CAMs. This output is updated for all compare operations. After reset, /MFUO is high. For depth cascaded devices, the /MFUO of a device is connected to the /MFUI of the next higher priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /MFUI through to /MFUO.

2.20 Match Flag Down Output (/MFDO)

This synchronous output is provided for depth cascading CAMs. This output is updated for all compare operations. After reset, /MFDO is high. For depth cascaded devices, the /MFDO of a device is connected to the /MFDI of the next lower priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /MFDI through to /MFDO.

2.21 System Match Flag (/SMF)

This synchronous output provides the System Match Flag (either for single device or cascaded devices). This output is updated for all compare operations. After reset /SMF is high. Functionally this output is identical to /MFDO. When cascading, the /SMF is provided by the lowest priority CAM. The /SMF from all other CAMs in the cascade may be left unconnected.

2.22 Multiple Match Flag (/MMF)

This synchronous output provides the Multiple Match Flag (either for single device or cascaded devices). This output is updated for all compare operations. After reset /MMF is high. In depth cascaded systems the lowest priority device provides the /MMF. For cascaded devices, when single device mode is selected, the deselected devices pass /MMFI through to /MMF.

2.23 Results Bus (RBUS₆₃..RBUS₀)

This is a 64-bit synchronous bus (RBUS) that outputs the results of a Compare operation including the "Learn" type

Compare operation. During a compare operation, when there is no match, RBUS is High-Z. For a compare operation, when there is a match, this bus outputs the CAM index of the Highest Priority Match (HPM), the Device ID, status of the flags and a portion of the memory at the HPM address.

For a "Learn" type compare operation, when there is no match, this bus outputs the Next Free Address (NFA), the Device ID and the status of the flags. When there is a match, the RBUS outputs the CAM index of the HPM, the Device ID and the status of the flags. The memory data field for the "Learn" type compare operation is a "don't care".

The following describes the RBUS format:

The CAM index of HPM or the NFA will be output on RBUS[63] through RBUS[52]. The lower 12 bits of Device ID are output on RBUS[51] through RBUS[40]. Bits RBUS[39] through RBUS[37] are reserved and will read '0'. RBUS[36] is the match flag status of the chip. RBUS[35] is the multiple match flag status of the chip. RBUS[34] is the full flag status of the chip. RBUS[33] and RBUS[32] will reflect the state of validity bits - skip and empty respectively, when a Compare operation including the "Learn" type compare operation is issued referencing to the validity bits.

RBUS[31] through RBUS[0] reflect a portion of memory at the HPM address.

The RBUS can be selected to output in the format of either the upper or the lower 64 Bits of the Status Register. NL82721 reflects the format of the lower 64 bits of the Status Register on RBUS as default after reset (See Figure 3). Programming the Device Configuration Register selects this format.

The IPCAM™ device can be set to operate in either **flow through** or **pipeline** mode. In the flow through mode the results of a compare instruction are output on RBUS in the same cycle with zero cycle latency. In the pipelined mode the results of a compare instruction are output on RBUS in the following cycle. However, the Match Flag is available in flow through mode only and is output in the current clock cycle. The format of the RBUS data in the pipeline mode is the same as described above for the flow through mode.

The user can program bit b7 in the Device Configuration Register to setup the RBUS to be in pipeline or flow through mode. When bit b7 is set to '1' the RBUS will operate in pipeline mode. When this bit is set to '0' the RBUS will operate in flow through mode. **The default mode after reset is the flow through mode.**

Table 1: Logical State of the Outputs with /CE high

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results bus	RBUS	High-Z
Match Flag Down Output	/MFDO	Same as Match Flag Down Input (/MFDI)
Match Flag Up Output	/MFUO	Same as Match Flag Up Input (/MFUI)
System Match Flag	/SMF	Same as Match Flag Down Input (/MFDI)
Multiple Match Flag	/MMF	Same as Multiple Match Flag Input (/MMFI)
Full Flag	/FF	Same as Full Flag Input (/FFI).
Instruction Error	/IERR	High
Learn Execute	/LEX	High-Z (If used, needs pull-up resistor to VDD)

Table 2: Logical State of the Outputs after Hardware or Software Reset

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results Bus	RBUS	High-Z
Match Flag Down Output	/MFDO	High
Match Flag Up Output	/MFUO	High
System Match Flag	/SMF	High
Multiple Match Flag	/MMF	High
Full Flag	/FF	High
Instruction Error	/IERR	High
Learn Execute	/LEX	High-Z (If used, needs pull up resistor to VDD)

Table 3a: Address Counter, NFAR, and HPM Registers after Hardware or Software Reset

b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0

Table 3b: Status Register after Hardware or Software Reset (Bits 63-0)

b63	b52	b51	b40	b39	b37	b36	b35	b34	b33	b32	b31	b0
CAM Address		Device ID		RSV	MF	MMF	FF	S	E	Memory Data		
0 0 0 Hex ^a		0 0 0 Hex ^b		000	1	1	1	0	1	0000 0000 Hex		

a The highest two significant bits (b63, b62) of the 12 bit CAM address always read "00".

b Only the lower 12-bits of the Device ID Register will appear. This field is unchanged after software reset.

Table 3c: Status Register after Hardware or Software Reset (Bits 127-64)

b127	b64
Memory Data	
0000 0000 0000 0000 Hex	

Table 3d: Device Configuration Register (DCR) after Hardware or Software Reset

b15	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type		802.3 <-> 802.5	P/FL	SR ^d	RSV	ACNT	RSV	RSV	RSV	C_MAP
001 1001 ^c Hex		0	0	0	0	0	0	0	0	0

c 001 1001 indicates a 1K x 128 IPCAM™. This entry is read only.

d Selects between the upper and the lower 64 bits of the Status Register

Table 3e: Memory Configuration, Global Mask Registers after Hardware or Software Reset

b127									b0
0000 0000 0000 0000 0000 0000 0000 0000 Hex									

Table 3f: Device ID Register after Hardware Reset (Device ID is not altered by Software Reset)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3g: State of the IPCAM™ after Hardware or Software Reset

#	Memory, Registers and Outputs	Status after Hardware Reset	Status after Software Reset
1	Device ID Register	All bits reset to '0'	Remains unchanged
2	Memory Configuration Register	All bits reset to '0'	All bits reset to '0'
3	Address Counter	All bits reset to '0'	All bits reset to '0'
4	Next Free Address Register	All bits reset to '0'	All bits reset to '0'
5	Global Mask Registers	All bits reset to '0'	All bits reset to '0'
6	Data Translation Register	All bits reset to '0'	All bits reset to '0'
7	Status Register	See table 3b & 3c	See table 3b & 3c
8	Device Configuration Register	See table 3d	See table 3d
9	Memory ^a	Unknown	Unknown
10	VBITs in Memory	Skip=0; Empty=1	Skip=0; Empty=1
11	Full Flag	Reset to '1'	Reset to '1'
12	Comparand Bus (CBUS)	High-Z	High-Z
13	Results Bus (RBUS)	High-Z	High-Z
14	Match Flag Down Output (/MFDO)	High	High
15	Match Flag Up Output (/MFUO)	High	High
16	System Match Flag (/SMF)	High	High
17	Multiple Match Flag (/MMF)	High	High
18	Cascade Up Output (CSCUO)	High	High
19	Cascade Down Output (CSCDO)	High	High

a Memory indicates CAM Words and Local Mask Words.

Table 3h: CBUS State under Operating Mode and Control Inputs

Control Inputs State	Comparand Bus (CBUS) State
Reset (/RST) = Low	High-Z
Chip Enable (/CE) = High	High-Z
Chip Enable (/CE) = Low	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z

Global Device Mode Operation, /RST='1', /CE='0'	
Highest Priority Device (/MFDI='1' & /MFDO='0')	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
Device with Next Free Address (/FFI='0' & /FF='1')	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
All Other Devices	High-Z

Single Device Mode Operation, /RST='1', /CE='0'	
Selected Device (Device with Matching Device ID)	/WEN_X that are '0' enable corresponding 16-bits; others are High-Z
All Other Devices	High-Z

Table 3i: Device Configuration Register Format

b15 b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type	802.3-802.5	FL/P	SR	RSV	ACNT	RSV	RSV	RSV	C_MAP

Notes:

- b15-b9** CAM Type field. Reads “001 1001” for 1K x 128 IPCAM™. This CAM Type field is read only.
- b8** When set to ‘1’ this bit enables **802.3 <-> 802.5 translation**. When set to ‘0’ this bit disables translation. This bit is set to ‘0’ after reset (Hardware or Software)
- b7** When this bit is set to ‘1’ the RBUS operates in **Pipeline mode**. When this bit is set to ‘0’ the RBUS operates in **Flow through mode**. This bit is set to ‘0’ after reset. (Hardware or Software)
- b6** Selects between the upper and the lower 64 bits of the Status Register. When this bit set to ‘1’, RBUS reflects the upper 64-bits (bit127-bit64) of the Status Register; when set to ‘0’, RBUS reflects the lower 64 bits (b63-b0) of the Status Register. This bit is set to ‘0’ after reset (Hardware or Software).
- b5** Reserved. Will read ‘0’.
- b4** When set to ‘1’ this bit enables the **Address counter** to be **incremented**. When set to ‘0’ it disables the address counter incrementing. This bit is set to ‘0’ after reset. (Hardware or Software)
- b3-b1** Reserved. Will read ‘0’.
- b0** This is the C_MAP bit. This enables the user to map different regions of memory onto the upper and lower 64-bits of the Status Register. Please see chart below for details. After reset this bit is set to ‘0’ (Hardware or Software).

Table 3j: Status Register Format (Bits 63-0)

b63	b52	b51	b40	b39 b37	b36	b35	b34	b33	b32	b31	b0
CAM Index		Device ID		RSV	MF	MMF	FF	S	E	Memory Data	

Notes:

- b63-b52** CAM Index field. Updated after all compare instructions. Updated with Highest Priority Match (HPM) index when there is a match; updated with Next Free Address if there is no match and is a “Learn” type compare operation. The highest significant bits (b63, b62) will always read “00”.
- b51-b40** Lower 12 bits of the 16-bit Device ID. Updated when Device ID is written.
- b39-b37** Reserved; will read ‘000’.
- b36** Match flag. Updated after all compare operations; reflects the internal match flag status.
- b35** Multiple match flag. Updated after all compare operations; reflects the internal multiple match flag status.
- b34** Full flag. Updated after write to memory, copy to memory, set VBITs or learn (compare) instructions; reflects internal full flag status.
- b33-b32** VBITs (skip and empty). Updated for all compare operations with the type of word compared; updated with the settings of VBITs after write to memory or copy to memory; updated with the type of word read for memory read operations; updated with VBITs after set VBITs operation.
- b31-b0** Updated after all compare operations with the exception of “Learn” type compare operations. Reflects portion of the memory at HPM address.

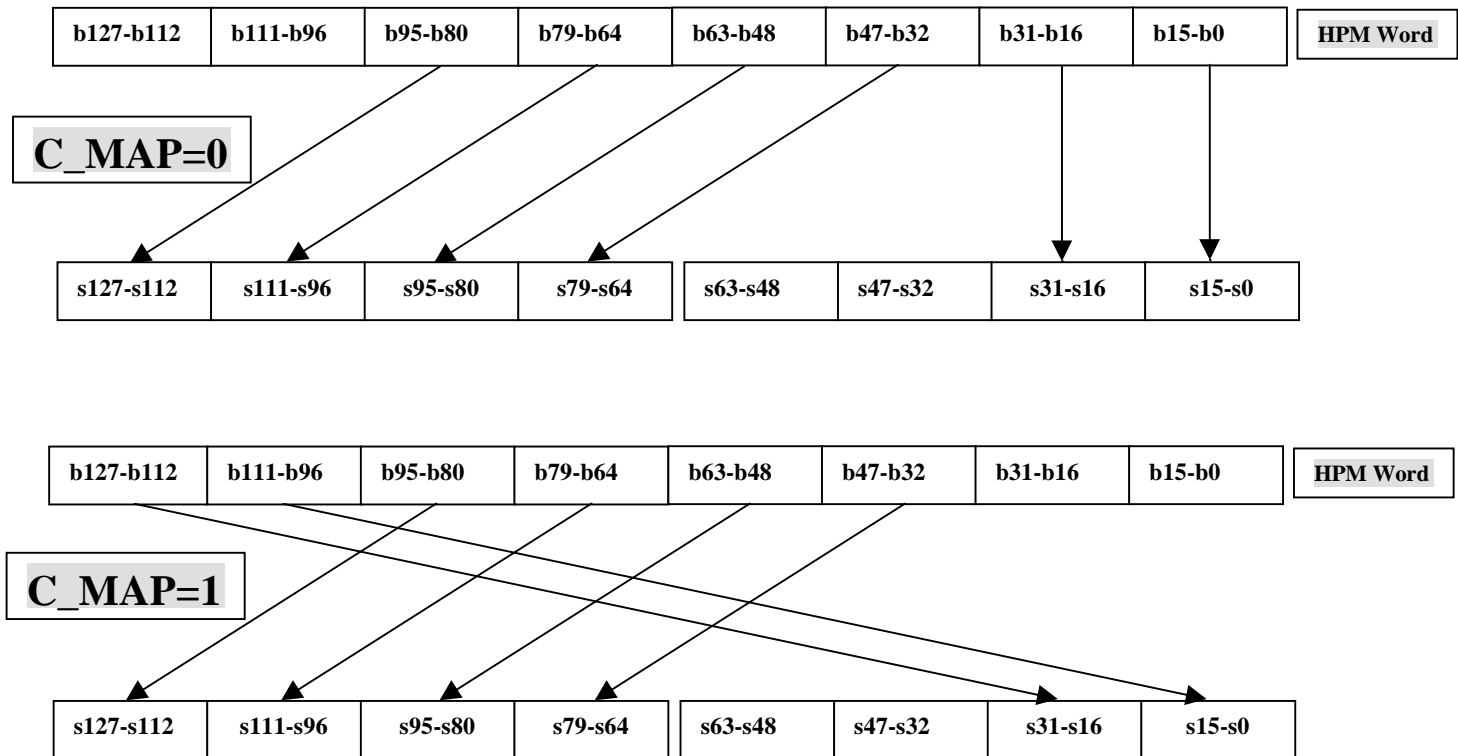
Table 3k: Status Register Format (Bits 127-64)

b127	b64
Memory Data	

Notes:

- b127-b64** Updated after all compare operations with the exception of learn operations. Reflects portion of the memory of HPM address.

Figure 4 Status Register and RBUS Mapping



3.0 IPCAM™ Internal Registers

3.1 Status Register

The 1K x 128 IPCAM™ device has a Status Register labeled SR. This register holds the results of Compare, Read, Write or Copy operations. After a comparison, the RBUS outputs results of either the upper 64-bits or the lower 64-bits of the 128-bit Status Register depending on bit-6 setting in the Device Configuration Register. The user can also access the Status Register from the CBUS by executing a “read status register” instruction. The tables 3b and 3c describe the contents of this register after reset. Tables 3j and 3k describe the contents of this register after all other operations.

3.2 Memory Configuration Register (MCR)

The Memory Configuration Register (MCR) is a 128-bit wide register that is used as a mask during compare instruction cycles. It provides compare masking capability in addition to the global masks. This MCR is always used during comparison as opposed to the Global Mask Registers, which may or may not be selected during comparison. After reset, all bits are ‘0’ indicating no masking of any bits during comparison. While Global Mask Registers may be used for write and compare operations, the MCR is used only for compare operations.

3.3 Comparand Register (CR)

The Comparand Register (CR) is a 128-bit register for loading the comparand (key) data into the device for compare and other operations. This data is also used during Learn instructions to update the memory with new words (keys). The ULEN pin enables the user to load the lower 64-bit or the higher 64-bit of the comparand. For bus widths of 16 or 32 bits, the Word Enable (/WEN3-/WEN0) inputs enable the user to load data into the CR and then compare its contents with the contents of memory. This feature enables the IPCAM™ to interface to buses that are 16, 32 and 64-bit wide seamlessly. This is the only register that enables the user to store and compare data with memory.

3.4 Global Mask Registers (GMR)

There are two 128-bit Global Mask Registers (GMR) that may be used either to mask compares or to mask data during memory writes. Each GMR may be selected on a cycle by cycle basis by specifying the GMR address in the instruction. All GMRs allow for a single bit to be shifted left or right to support proximity matching algorithms.

For compare instructions calling for a masked compare, if a mask bit is '1', the corresponding bits in the memory will not enter the compare operation. If a mask bit is '0', the corresponding bits in the memory will enter the compare operation.

For memory write instructions calling for a masked write, if a mask bit is '1', the corresponding bits in the memory will not be altered. If a mask bit is '0', the corresponding bits in the memory will be written to.

3.5 Data Translation Register (DTR)

The Data Translation Register (DTR) is a 128-bit register for performing data manipulations in the IPCAM™. The operations are done in the upper or the lower 64 bits and is selected by ULEN input. The operations are listed below.

1. 32-bit swap
2. 16-bit swap
3. 16-bit shift
4. 1-bit shift

3.6 Highest Priority Match Index Register (HPMR)

This register holds the address of the highest priority match. This register is updated after all compare operations. See table 3a.

3.7 Next Free Address Register (NFAR)

This register holds the address of next free address in the array. This is updated for all write to memory, copy to memory, set VBITs and learn (compare) instructions. See table 3a and section 5.

3.8 Device Configuration Register (DCR)

This register holds the programmable bits for selecting modes of operation of the CAM device. This register includes a field (read only) indicating the type of device. For details, see table 3i.

3.9 Device ID Register (DIDR)

This register holds the Device ID value. This register is written into as part of initialization sequence. This register is reset only during hardware reset. Software reset instruction does not alter this register. See table 3f.

4.0 CAM Address Counter (ACR)

The CAM Address Counter (ACR) in the IPCAM™ allows a user to perform read, write or copy operations continuously. The user may set the start address in the counter and program the Device Configuration Register to increment the counter after write, read or copy operations. The ACR is set to increment by setting bit b4 in the Device Configuration Register to a '1'. When the counter is set **not to increment**, (bit b4='0'), then the counter address will not increment even for instructions that specify that the Address Counter be incremented.

When the CAM Address Counter is **set to increment** in the Device Configuration Register, the counter will be incremented after any of the following instructions are executed:

1. Copy operations to and from memory that reference the Address Counter.
2. Set VBITs to either Valid, Empty, Skip or RAM at the address indicated by the Address Counter.
3. Write to memory and set VBITs to Valid, Empty, Skip or RAM at the address indicated by the Address Counter.
4. Write to memory masked by Global Mask Register, set VBITs to Valid, Skip or RAM at the address indicated by the Address Counter.
5. Write to Local Mask Word and increment counter.
6. Read memory at address indicated by the Address Counter and increment Address Counter.
7. Read Local Mask Word and increment counter.

The following memory operations that reference the Address Counter **do not increment** the Address Counter even if b4 in the Configuration Register is set to '1' (Increment):

1. Write to memory, no change to VBITs.
2. Write to memory masked by Global Mask Register, no change to VBITs.
3. Read memory (CAM Word).
4. Read Local Mask Word.

These restrictions should be kept in mind when interfacing IPCAM™ to buses smaller than 64-bit wide. In NL82721 device, the external interface is 64-bit wide and the internal words are 128-bit wide. Thus it takes the user two clock cycles to complete the load. This should be kept in mind when issuing instructions that increment the Address Counter after write instructions.

5.0 Next Free Address Register (NFAR)

The Next Free Address Register (NFAR) holds the address of the memory word that has its VBITs set to empty, and that is numerically closest to zero. This is noted as the Next Free Address (NFA). This address is generated from the output of the priority encoder in the IPCAM™. When the CAM has no empty locations, the NFAR holds the address of the last empty location before the device became full.

The following operations will update the NFAR:

1. Write to Memory (CAM Word) at NFA; set VBITs to Valid, Skip or RAM.
2. Set VBITs to empty at the Address indicated by the Address Counter.
3. Set VBITs to empty at HPM address.
4. Set VBITs to empty at all matching locations.
5. Copy operations that reference the NFA.
6. Learn.

The NFAR will **not be updated** for the following:

1. Write to memory (CAM Word) at NFA; no change to VBITs.
2. Write to Local Mask Word at NFA.

These restrictions should be kept in mind when interfacing IPCAM™ to buses smaller than 64-bit wide. In NL82721 device, the external interface is 64-bit wide and the internal words are 128-bit wide. Thus it takes the user two clock cycles to complete the load. This should be kept in mind when issuing instructions that increment Address Counter after write instructions.

6.0 Validity Bits

Every location in the memory array has a corresponding skip and empty bit associated with it. These are referred to as VBITs. These bits can be written to or read from just like locations in memory. These VBITs group memory words into four different categories (See table 5). Any compare instruction indicates the type of words to be searched during the cycle and only words belonging to that group participate in the search operation; all other words not belonging to the group do not participate in the match operation (indicate a no match). The Skip state allows a user to temporarily skip comparisons of certain CAM words. After hardware/software reset all words belong to the “Empty” group.

When the Skip and Empty bits are set to reflect the Valid state for a particular word, then that particular word will take part in Compare operations only when the compare operation with VBITs set to valid instruction is executed.

When the Skip and Empty bits are set to reflect the Skip state for a particular word, then that particular word will take part in compare operations only when the compare operation with VBITs set to Skip instruction is executed.

When the Skip and Empty bits are set to reflect the RAM state for a particular word, then that particular word will take part in compare operations only when the compare operation with VBITs set to RAM instruction is executed.

When a write operation is performed and the instruction calls for setting the written word to Valid, Skip or RAM, the Status Register is updated with the type of word added. Bits 32 and 33 of the Status Register reflect this. When a CAM array Read operation is performed, the VBITs corresponding to the word read are updated in bits 33-32 in the Status Register.

Table 5: Validity Bit (VBITs) Encoding

Option	Skip (S)	Empty (E)	Word Type
1	0	0	Valid
2	0	1	Empty
3	1	0	Skip
4	1	1	RAM

7.0 IEEE 802.3 / 802.5 Mapping

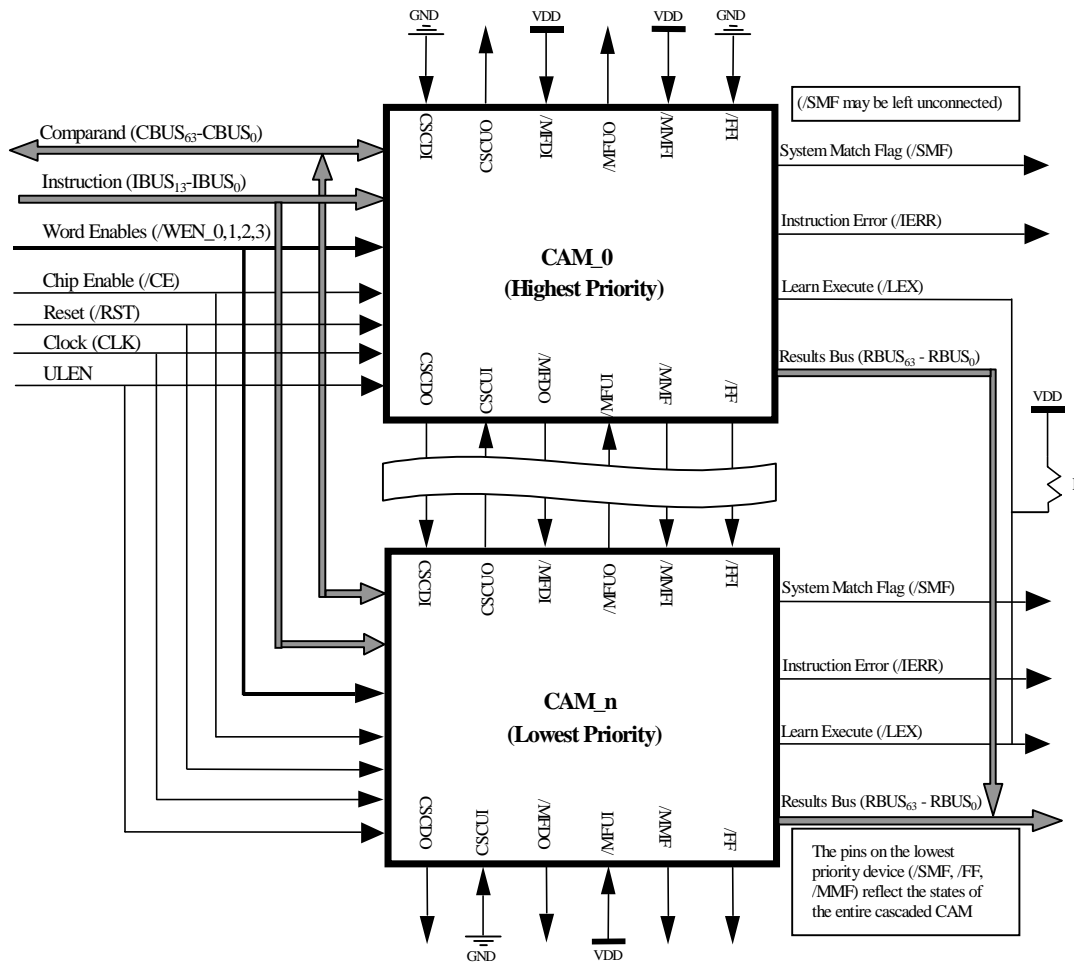
To support the symmetrical mapping between the address formats of IEEE 802.3 and IEEE 802.5, the IPCAM™ provides a bit translation facility. The user can program bit b8 to a ‘1’ in the Device Configuration Register to enable translation. When this bit is set to ‘0’ it will disable translation. After reset, bit b8 is ‘0’ indicating no translation. This translation is applicable only for writing.

The nth bit, D (n), maps to the xth output bit, Q (x), through the following expressions:

$$\begin{aligned}
 D(n) &= Q(7-n) \text{ for } 0 \leq n \leq 7, \\
 D(n) &= Q(23-n) \text{ for } 8 \leq n \leq 15, \\
 D(n) &= Q(39-n) \text{ for } 16 \leq n \leq 23, \\
 D(n) &= Q(55-n) \text{ for } 24 \leq n \leq 31, \\
 D(n) &= Q(71-n) \text{ for } 32 \leq n \leq 39, \\
 D(n) &= Q(87-n) \text{ for } 40 \leq n \leq 47, \\
 D(n) &= Q(103-n) \text{ for } 48 \leq n \leq 55, \\
 D(n) &= Q(119-n) \text{ for } 56 \leq n \leq 63, \\
 D(n) &= Q(135-n) \text{ for } 64 \leq n \leq 71, \\
 D(n) &= Q(151-n) \text{ for } 72 \leq n \leq 79, \\
 D(n) &= Q(167-n) \text{ for } 80 \leq n \leq 87, \\
 D(n) &= Q(183-n) \text{ for } 88 \leq n \leq 95, \\
 D(n) &= Q(199-n) \text{ for } 96 \leq n \leq 103, \\
 D(n) &= Q(215-n) \text{ for } 104 \leq n \leq 111, \\
 D(n) &= Q(231-n) \text{ for } 112 \leq n \leq 119, \\
 D(n) &= Q(247-n) \text{ for } 120 \leq n \leq 127
 \end{aligned}$$

This mapping above does not apply to 16-bit registers (Address Counter, Device ID and Device Configuration).

8.0 Depth Cascading the IPCAM™



Depth cascading of the IPCAM™ is accomplished by connecting them as shown above and described below.

1. Connect /FFI of the highest priority device to '0'.
2. Connect /MMFI of the highest priority device to '1'.
3. Connect /MMFI of the highest priority device to '1'.
4. Connect /CSCDI of the highest priority device to '0'.
5. Connect /MFUI of the lowest priority device to '1'.
6. Connect /CSCUI of the lowest priority device to '0'.
7. Connect /FF of each device to /FFI of the next lower priority device (except lowest priority device).
8. Connect /MFDI of each device to /MFDI of the next lower priority device (except lowest priority device).
9. Connect /MMF of each device to /MMFI of the next lower priority device (except lowest priority device).
10. Connect /CSCDI of each device to /CSCDI of the next lower priority device (except lowest priority device).
11. Connect /MFUI of each device to /MFUI of the next higher priority device (except highest priority device).
12. Connect /CSCUI of each device to /CSCUI of the next higher priority device (except highest priority device).

The System Match Flag (/SMF) is generated by the lowest priority device and is the logical OR of all the match flags

in the cascade. The /SMF from all other devices indicate the match flag status up to that point and may be left unconnected.

The System Multiple Match Flag is the Multiple Match Flag (/MMF) of the lowest priority device. This flag is asserted whenever more than one device in the cascade has a match and/or one or more devices in the cascade have a multiple match.

After compare, should a match occur in more than one device in the cascade, the device with a match that is the highest priority device will drive RBUS. The highest priority device is the one with /MFDI high and /MFDI low.

When devices are cascaded and are operating in Global Mode, Read instructions are executed by the highest priority device. All other device will treat this as a NOP.

When the devices are cascaded and are operating in Single Device Mode, Read instructions are executed by the selected device. All other (deselected) devices treat this as a NOP.

9.0 Initializing the IPCAM™

The IPCAM™ needs to be initialized after power up for proper operation. The following steps show how to initialize the IPCAM™ for single device and for depth cascaded devices. Please refer to section 8 for details on depth cascading.

9.1 Single Device Initialization

1. Assert /RST pin low for a minimum of three cycles.
2. Execute NOP instruction (at least once).
3. Write to Device ID Register (any 16-bit value).
4. Select Single device mode (Device ID input on CBUS₁₅:CBUS₀).

The IPCAM™ device is now ready for memory write, local mask write, compare and other operations.

9.2 Depth Cascaded Devices Initialization

1. Assert /RST pin low for a minimum of three cycles.
2. Execute NOP instruction (at least once).
3. Write to Device ID Register (any 16-bit value).
4. Set Full Flag.
5. Write to Device ID Register (any 16-bit value).
6. (Repeat 4 & 5 until all devices have ID written).
7. Execute software Reset.
8. Execute NOP instruction (atleast once).

The device IDs must all be unique for proper operation. At step 3, the first device has the ID written; at step 5, the second device has the ID written and so on. The IPCAM™ device is now ready for memory write, local mask write, compare and other operations.

The NL82721 device has a 128-bit local mask word associated with each 128-bit memory word. The contents of these local mask words and memory words are in unknown state after reset. **Thus it is necessary to write to the CAM memory words and Local Mask Words before issuing compare instructions.**

10.0 Writing to the CAM Array

After initialization, the user can write into the IPCAM™ array in many ways. Two common methods of accomplishing this are described below:

10.1 Writing to Memory: Option 1

One method of writing into the CAM array is to execute “Write to mask word at Next Free Address” instruction followed by “Write to CAM Word at Next Free Address

and set VBITs” repeatedly until the memory is full or all data is written into the CAMs. The write operation begins in the device with /FFI = 0 and /FF=1, continues until all locations have been written into (no EMPTY locations remain). When the last empty location has been written to, the /FF of that device will assert a ‘0’ preventing any further “Write to memory at NFA” operations from occurring in that device. This will then enable the next lower priority device in the cascade to accept “Write to memory at NFA” operation. This continues until the last device in the chain becomes full and asserts /FF pin low, indicating that all the CAM devices are now full, and no empty locations remain. The steps involved in this method are as follows:

1. Write to local mask word at next free address (NFA) the first 64 bits (ULEN=1).
2. Write to local mask word at NFA the second 64 bits (ULEN=0).
3. Write to memory at NFA the first 64 bits (ULEN=1).
4. Write to memory at NFA the second 64 bits and set VBITs (ULEN=0).
5. Repeat steps 1-4 until the device/s are full (/FF =0 for the device or the cascade chain).

10.2 Writing to the Memory: Option 2

Another method of writing to the CAM is to use the address from the internal Address Counter as opposed to the NFAR. The steps involved in this method are as follows:

1. Select Single Device Mode (with device ID on CBUS₁₅:CBUS₀ as input data).
2. Write to local mask word at address from the Address Counter (ACR) the first 64-bits (ULEN=1).
3. Write to local mask word at address from ACR the second 64-bits (ULEN=0).
4. Write to memory at address from ACR the first 64-bits (ULEN=1).
5. Write to memory at address from ACR the second 64-bits (ULEN=0) and set VBITs.
6. Steps 2-5 are repeated until the devices are full (/FF=0 for single device or cascade chain).
7. Select Global Device Mode

The above sections 10.1 and 10.2 show two of many possible ways of writing to the Memory Array.

When interfacing the SyncCAM® to a bus smaller than 64-bits and updating memory in segments (16/32-bits), the user is advised to execute either “Write to memory at NFA, no change to VBIT” or “Write to memory, no change to VBIT” followed by “Write to memory at NFA and set VBIT” or “Write to memory and set VBIT”.

11.0 Electrical Characteristics

11.1 Absolute Maximum Ratings ⁽¹⁾

Supply voltage to GND	-0.5 to +4.6V
DC output voltage (Vout)	-0.5 to VDD + 0.5V ⁽²⁾
DC output current	50mA ⁽³⁾
T _{BIAS} Temperature under bias	-40°C to +85°C
T _{STG} Storage temperature	-65°C to +150°C

Notes:

1. Stresses greater than ABSOLUTE MAXIMUM RATINGS will cause permanent damage to the device, resulting in functional or reliability type failures.
2. -2.0V for 10 ns, measured at the 50% point.
3. Per output, one at a time, one-second duration.

11.2 Power Supply Characteristics

Symbol	Parameter	Test Conditions	40 MHz	33 MHz	Unit
			Max.	Max.	
I _{DDO}	Operating Current	t _{CYC} = t _{CYC} (min)	700	650	mA
I _{RM}	Idle Mode Current	/CE = '1'	90	90	mA

11.3 Capacitance

Symbol	Parameter	Max.	Unit	Notes
C _{IN}	Input Capacitance	6	pF	f=1MHz, V _{IN} =0V
C _{OUT}	Output Capacitance	8	pF	f=1MHz, V _{OUT} =0V

11.4 DC Electrical Characteristics over Operating Range (T_A = 0°C - 70°C, VDD = 3.3V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Max.	UNIT
V _{IH}	Input HIGH Voltage	Logic high for all Inputs	2.2	VDD + 0.5	V
V _{IL}	Input LOW Voltage	Logic low for all Inputs	-0.5	0.8	V
V _{OH}	Output HIGH Voltage	I _{OH} = -4mA, VDD = Min.	2.4	-	V
V _{OL}	Output LOW Voltage	I _{OL} = 4mA, VDD = Min.	-	0.4	V
I _{LI}	Input Leakage	VDD = 3.47V; GND ≤ V _{IN} ≤ VDD	-5	5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ VDD	-10	10	μA

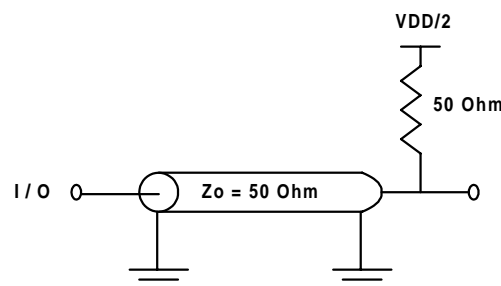
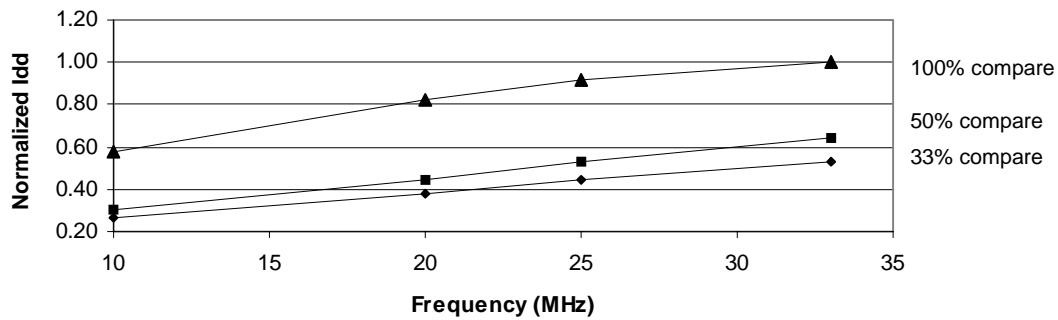


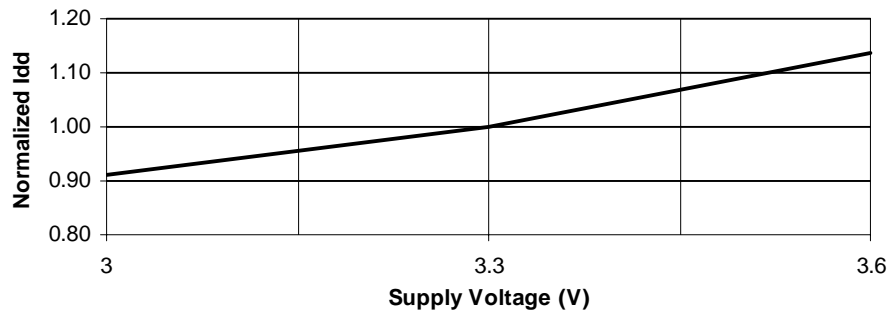
Figure 5 AC Test Conditions

11.5 Power De-rating Curves

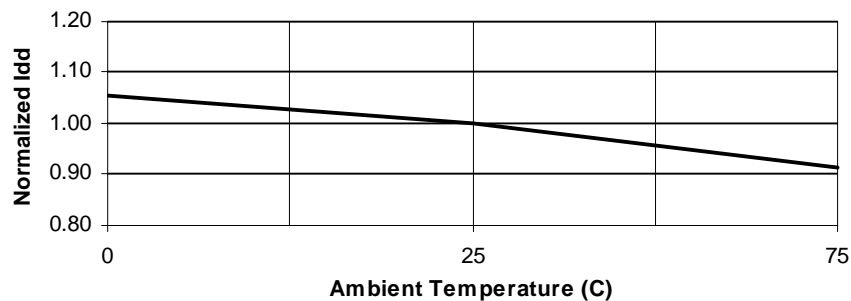
Normalized Dynamic Supply Current vs. Clock Frequency
Max Vdd=3.6V, 25 Deg C, Compare Cycles



Normalized Dynamic Supply Current vs. Supply Voltage
25 Deg C, 100% Compare



Normalized Dynamic Supply Current vs. Ambient Temp.
Vdd=3.3V, 100% Compare



12.0 AC Timing Parameters

12.1 AC Timing Parameters; Single Device (VDD = 3.3V +- 5%, TA=0°C – 70°C)

#	Parameter	Type	Description	40MHz		33 MHz	
				Min	Max	Min	Max
1	t _{CYC}		Cycle	25		30	
2	t _{CYH}		Cycle high	11.5		13.5	
3	t _{CYL}		Cycle low	11.5		13.5	
4	t _{CSU}	IN	Chip Enable Set-up	4		5	
5	t _{CHD}	IN	Chip Enable Hold	0		0	
6	t _{WNSU}	IN	Word Enable Set-up	4		5	
7	t _{WNH}	IN	Word Enable Hold	0		0	
8	t _{ULSU}	IN	ULEN Setup	4		5	
9	t _{ULHD}	IN	ULEN Hold	0		0	
10	t _{DSU}	IN	Data Setup	4		5	
11	t _{DHD}	IN	Data Hold	0		0	
12	t _{INSU}	IN	Instruction Setup	4		5	
13	t _{INHD}	IN	Instruction Hold	0		0	
14	t _{RB1}	OUT	RBUS Output (Pipeline Mode)		10		12
15	t _{RB2}	OUT	RBUS Output Hold (Pipeline Mode)	1		1	
16A	t _{RB3}	OUT	RBUS Output (Index Compare in Flow Through Mode)		21		25
16B	t _{RB3}	OUT	RBUS Output (Index Learn in Flow Through Mode)		23.5		27
17A	t _{RB4}	OUT	RBUS Output (Flags, for Compare data in Flow Through Mode)	---	---		28
17B	t _{RB4}	OUT	RBUS Output (Memory, for Compare data in Flow Through Mode)	---	---		28
17C	t _{RB4}	OUT	RBUS Output (Flags, for Learn data in Flow Through Mode)	---	---		34
18	t _{RBH}	OUT	RBUS Output Hold (Flow Through Mode)	3		3	
19A	t _{CDO}	OUT	CBUS Memory Data Output		22		25
19B	t _{CDO}	OUT	CBUS Register Data Output		12		14
20	t _{CDH}	OUT	CBUS Data Output Hold	3.5		3.5	
23	t _{SMF}	OUT	System Match Flag Assertion and Deassertion	4	18	4	22
24	t _{MMF}	OUT	Multiple Match Flag Assertion and Deassertion	4	21	4	25
26	t _{FF1}	OUT	Full Flag Assertion and Deassertion (Write, Copy instructions)	2	23	2	26
27	t _{FF2}	OUT	Full Flag Assertion and Deassertion (Learn, VBC instructions)	2	30	2	34
28	t _{LEX}	OUT	Learn Execute Assertion and Deassertion	1	21	1	27
29	t _{IER}	OUT	Instruction Error Assertion and Deassertion	2	20	2	23

See important timing notes on next page.

12.2 AC Timing Parameters; Cascaded (VDD = 3.3V +- 5%, TA=0°C – 70°C)

#	Parameter	Type	Description	40MHz		33 MHz	
				Min	Max	Min	Max
21	t _{MFI}	IN	Match Flag Input Setup	4		4	
22	t _{MF}	OUT	Match Flag Assertion and Deassertion (/MFDO, /MFUO)	2	18	2	22
25	t _{FFI}	IN	Full Flag Input Setup	4		4	
30	t _{MMI}	IN	Multiple Match Flag Input Setup	4		4	

1. All timings are with reference to the rising edge of the clock, measured in nano seconds.
2. Output Hold times are guaranteed by design, not tested in production.
3. All timing numbers are for a single device (as opposed to devices in cascade).
4. t_{LEX} and t_{IER} are included for reference only. These parameters are characterized, but not tested in production.
5. t_{RB4B}: A “Learn” instruction may not be immediately followed by a “Write to NFA” instruction because of the possibility that the CAM array is full when the Full Flag has not yet been issued.
6. t_{FFI}: This timing is valid for all instruction sequences except for the following : 1. Compare empty VBits, 2. Set VBITs to Valid at all matching locations.

13.0 1K x 128 IPCAM™ Instruction Set Format

The IPCAM™ Instruction bus is 14-bits wide. It consists of a 11-bit “Opcode field” consisting of bits IBUS₁₃-IBUS₀₃, a 2-bit global mask field “GMSK” consisting of IBUS₀₂ and IBUS₀₁ and a 1-bit comparand field “CDS” consisting of IBUS₀₀.

Instruction Word (Opcode) Format:

IBUS ₁₃	IBUS ₁₂	IBUS ₁₁	IBUS ₁₀	IBUS ₀₉	IBUS ₀₈	IBUS ₀₇	IBUS ₀₆	IBUS ₀₅	IBUS ₀₄	IBUS ₀₃	IBUS ₀₂	IBUS ₀₁	IBUS ₀₀
fn10	fn9	fn8	fn7	fn6	fn5	fn4	fn3	fn2	fn1	fn0	y1	y0	z0
Opcode Field											GMSK		CDS

IBUS₁₃ -- IBUS₀₃: fn10.. fn0 is the Opcode field. This field determines all possible instructions.

Erroneous Opcodes will result in indeterminate state in the IPCAM™.

IBUS₀₂- IBUS₀₁: IBUS₀₂ and IBUS₀₁ select between the two Global Mask Registers; designated as y1 and y0.

Note: y1 is a “Don’t Care” for all instructions except for those which use the Global Mask Registers. For Instructions that use the Global Mask Registers, see the table below:

#	IBUS ₀₂ /y1	IBUS ₀₁ /y0	Selects Global Mask Register
1	1	0	0
2	1	1	1

IBUS₀₀: Selects between Comparand/Data Translation for read/write, designated as z0.

#	z0	Selects
1	0	Comparand Register for read/write
2	1	Data Translation Register read/write

Instruction : [Opcode field][GMSK] [CDS]

xxx xxxx xxxx y1,y0 z0

[Opcode field]: Bits 13 - 3, coded as [w2 w1 w0], w2 is bits 13-11, w1 is bits 10 - 7 and w0 is bits 6 - 3

[GMSK]: Bits 2-1, coded as [y1, y0]

[CDS]: Bit 0, coded as [z0]

14.0 IPCAM™ Instruction Opcodes and Description

14.1 Compare Instructions

Opcode in Hex		Instructions Explanation
#	[Opcode][GMSK][CDS] [w2/1/0][y1 y0][z0]	
1	[610] [X0] [0]	Compare Valid Entries
2	[611] [X0] [0]	Compare Skip Entries
3	[613] [X0] [0]	Compare RAM Entries
4	[614] [y1y0] [0]	Compare Valid Entries using Global Mask Register
5	[615] [y1y0] [0]	Compare Skip Entries using Global Mask Register
6	[617] [y1y0] [0]	Compare RAM Entries using Global Mask Register
7	[618] [X0] [0]	Compare Valid Entries; If No Match, Write Comparand to memory at NFA and set VBITs to Valid
8	[619] [X0] [0]	Compare Skip Entries; If No Match, Write Comparand to memory at NFA and set VBITs to Skip
9	[61B] [X0] [0]	Compare RAM Entries; If No Match, Write Comparand to memory at NFA and set VBITs to RAM
10	[61C] [y1y0] [0]	Compare Valid Entries using Global Mask; If No Match, Write Comparand to memory at NFA and set VBITs to Valid
11	[61D] [y1y0] [0]	Compare Skip Entries using Global Mask; If No Match, Write Comparand to memory at NFA and set VBITs to Skip
12	[620] [X0] [0]	Write to Comparand Register and Compare Valid Entries
13	[621] [X0] [0]	Write to Comparand Register and Compare Skip Entries
14	[623] [X0] [0]	Write to Comparand Register and Compare RAM Entries
15	[624] [y1y0] [0]	Write to Comparand Register and Compare Valid Entries using Global Mask Register
16	[625] [y1y0] [0]	Write to Comparand Register and Compare Skip Entries using Global Mask Register
17	[627] [y1y0] [0]	Write to Comparand Register and Compare RAM Entries using Global Mask Register
18	[628] [X0] [0]	Write to Comparand and Compare Valid Entries. If No Match, copy Comparand to memory at NFA and set VBITs to Valid
19	[629] [X0] [0]	Write to Comparand and Compare Skip Entries. If No Match, copy Comparand to memory at NFA and set VBITs to Skip
20	[62B] [X0] [0]	Write to Comparand and Compare RAM Entries. If No Match, copy Comparand to memory at NFA and set VBITs to RAM
21	[62C] [y1y0] [0]	Write to Comparand and Compare Valid Entries using Global Mask. If No Match, copy Comparand to memory at NFA and set VBITs to Valid
22	[62D] [y1y0] [0]	Write to Comparand and Compare Skip Entries using Global Mask. If No Match, copy Comparand to memory at NFA and set VBITs to Skip
23	[640] [X0] [0]	Compare Valid VBITs
24	[641] [X0] [0]	Compare Skip VBITs
25	[642] [X0] [0]	Compare Empty VBITs
26	[643] [X0] [0]	Compare RAM VBITs

Notes:

- Instructions 7-11, 18-22 are “Learn” Instructions
- X implies a “Don’t Care”

14.2 Write Instructions

1	[000] [X0] [0] H	NOP (No Operation)
2	[001] [X0] [z0] H	Write to Comparand or Data Translation Register
3	[002] [y1y0] [0] H	Write to Global Mask Register
4	[003] [X0] [0] H	Write to Memory at Address Register Location, No Change to VBITs
5	[004] [X0] [0] H	Write to Memory at Address Register Location, Set VBITs to Valid
6	[005] [X0] [0] H	Write to Memory at Address Register Location, Set VBITs to SKIP
7	[006] [X0] [0] H	Write to Memory at Address Register Location, Set VBITs to RAM
8	[007] [y1y0] [0] H	Write to Memory, masked by Global Mask Register, No Change to VBITs
9	[008] [y1y0] [0] H	Write to Memory, masked by Global Mask Register, Set VBITs to Valid
10	[009] [y1y0] [0] H	Write to Memory masked by Global Mask Register, Set VBITs to SKIP
11	[00A] [y1y0] [0] H	Write to Memory masked by Global Mask Register, Set VBITs to RAM
12	[00B] [X0] [0] H	Write to Memory at HPM address, No change to VBITs
13	[00C] [X0] [0] H	Write to Memory at HPM address, Set VBITs to Valid
14	[00D] [X0] [0] H	Write to Memory at HPM Address, Set VBITs to SKIP
15	[00E] [X0] [0] H	Write to Memory at HPM Address, Set VBITs to RAM
16	[013] [X0] [0] H	Write to Memory at NFA, No change to VBITs
17	[014] [X0] [0] H	Write to Memory at NFA, Set VBITs to Valid
18	[015] [X0] [0] H	Write to Memory at NFA, Set VBITs to Skip
19	[016] [X0] [0] H	Write to Memory at NFA, Set VBITs to RAM
20	[01B] [X0] [0] H	Set VBITs to Valid at Address Counter
21	[01C] [X0] [0] H	Set VBITs to Empty at Address Counter
22	[01D] [X0] [0] H	Set VBITs to Skip at Address Counter
23	[01E] [X0] [0] H	Set VBITs to RAM at Address Counter
24	[01F] [X0] [0] H	Set VBITs to Valid at HPM address
25	[020] [X0] [0] H	Set VBITs to Empty, at HPM address
26	[021] [X0] [0] H	Set VBITs to Skip at HPM address
27	[022] [X0] [0] H	Set VBITs to RAM, at HPM address
28	[023] [X0] [0] H	Set VBITs to Valid at all matching address
29	[024] [X0] [0] H	Set VBITs to Empty at all matching address
30	[025] [X0] [0] H	Set VBITs to Skip at all matching address
31	[026] [X0] [0] H	Set VBITs to RAM at all matching address

Notes: 1. All write operations are controlled by ULEN and the four Word Enables.

2. Instructions 28-31 are “VBC” Instructions.

14.3 Copy Instructions

32	[027] [X0] [z0] H	Copy Memory to Comparand Register or Data Translation Register
33	[028] [y1y0] [z0] H	Copy Memory to Comparand Register or Data Translation Register, masked by Global Mask Register
34	[029] [y1y0] [0] H	Copy Memory to Global Mask Register
35	[02A] [y1y0] [0] H	Copy memory at HPM Address to Global Mask Register
36	[02B] [X0] [z0] H	Copy Comparand Register or Data Translation Register to Memory, No change to VBITs
37	[02C] [X0] [z0] H	Copy Comparand Register or Data Translation Register to Memory, Set VBITs to Valid
38	[02D] [X0] [z0] H	Copy Comparand Register or Data Translation Register to Memory, Set VBITs to Skip
39	[02E] [X0] [z0] H	Copy Comparand Register or Data Translation Register to Memory, Set VBITs to RAM
40	[02F] [X0] [z0] H	Copy Comparand Register or Data Translation Register to memory at NFA, Set VBITs to Valid
41	[030] [X0] [z0] H	Copy Comparand Register or Data Translation Register to memory at NFA, Set VBITs to Skip
42	[031] [X0] [z0] H	Copy Comparand Register or Data Translation Register to memory at NFA, Set VBITs to RAM
43	[035] [y1y0] [z0] H	Copy Comparand Register or Data Translation Register to Global Mask Register
44	[03A] [X0] [z0] H	Copy Comparand or Data Translation Register to memory at HPM Address, No change to VBITs.
45	[03B] [X0] [z0] H	Copy Comparand or Data Translation Register to memory at HPM Address, Set VBITs Valid
46	[03C] [X0] [z0] H	Copy Comparand Register or Data Translation Register to memory at HPM Address, Set VBITs Skip
47	[03D] [X0] [z0] H	Copy Comparand or Data Translation Register to memory at HPM Address, Set VBITs to RAM
48	[042] [y1y0] [z0] H	Copy Global Mask Register to Comparand Register or Data Translation Register
49	[043] [y1y0] [0] H	Copy Global Mask Register to Memory, Set VBITs to RAM
50	[044] [y1y0] [0] H	Copy Global Mask Register to memory at HPM Address, Set VBITs to RAM
51	[045] [y1y0] [0] H	Copy Global Mask Register to memory at NFA, Set VBITs to RAM

Notes: All Copy instructions are 128-bit wide operations.

14.4 Special Instructions

52	[046]	[X0]	[0]	H	Write to Memory Configuration Register
53	[047]	[X0]	[0]	H	Write to Device Configuration Register (Data input on CBUS[15:0])
54	[048]	[X0]	[0]	H	Write to Device ID Register (Data input on CBUS[15:0]) ^a
55	[049]	[X0]	[0]	H	Copy Comparand Register to Data Translation Register
56	[04A]	[X0]	[1]	H	Copy Data Translation Register to Comparand Register
57	[04B]	[X0]	[0]	H	Set Full Flag ^a
58	[04C]	[X0]	[0]	H	Select Single Device Mode
59	[04D]	[X0]	[0]	H	Select Global Mode
60	[04E]	[X0]	[0]	H	Software Reset ^b
61	[04F]	[X0]	[0]	H	Write to Address Counter (Data input on CBUS[15:0])

- Notes:
- ^a This instruction will be executed in the device with /FI = 0 and /FF = 1. All other devices will treat this as NOP.
 - ^b A Software instruction must be followed by a NOP instruction.
Copy instructions are 128-bit operations; Write to Memory Configuration Register is controlled by four Word Enables.

14.5 Local Mask Write Instructions

62	[050]	[X0]	[0]	H	Write to Local Mask Word
63	[051]	[X0]	[0]	H	Write to Local Mask Word and Increment Address Counter
64	[052]	[y1y0]	[0]	H	Write to Local Mask Word, masked by Global Mask Register
65	[053]	[X0]	[0]	H	Write to Local Mask Word at Highest Priority Match Location
66	[054]	[X0]	[0]	H	Write to Local Mask Word at Next Free Address
67	[055]	[X0]	[1]	H	Copy Local Mask Word to Comparand Register or Data Translation Register
68	[056]	[y1y0]	[0]	H	Copy Local Mask Word to Comparand or Data Translation Register, masked by Global Mask Register
69	[057]	[y1y0]	[0]	H	Copy Local Mask Word to Global Mask Register
70	[058]	[y1y0]	[0]	H	Copy Global Mask Register to Local Mask Word
71	[059]	[y1y0]	[0]	H	Copy Local Mask Word at Highest Priority Match Location to Global Mask Register
72	[05A]	[y1y0]	[0]	H	Copy Global Mask Register to Local Mask Word at Highest Priority Match Location

Notes: Copy instructions are 128-bit operations; Write to Memory Configuration Register is controlled by four Word Enables.

14.6 Read Operations

73	[200]	[X0]	[0]	H	Read Address Counter (Data output on CBUS[15:0])
74	[201]	[X0]	[0]	H	Read Memory
75	[202]	[X0]	[0]	H	Read Memory and Increment Counter
76	[203]	[X0]	[y]	H	Read Status Register (Data output on CBUS[63:0])
77	[204]	[y1y0]	[0]	H	Read Global Mask Register
78	[205]	[X0]	[y]	H	Read Comparand Register or Data Translation Register
79	[206]	[X0]	[0]	H	Read Next Free Address Register (Device ID output on CBUS[31:16] and NFA on CBUS[15:0])
80	[207]	[X0]	[0]	H	Read Memory at HPM Address
81	[208]	[X0]	[0]	H	Read Memory Configuration Register
82	[209]	[X0]	[0]	H	Read Device Configuration Register (Data output on CBUS[15:0])
83	[20A]	[X0]	[0]	H	Read Device ID Register (Data output on CBUS[31:16])
84	[20B]	[X0]	[0]	H	Read Local Mask Word
85	[20C]	[X0]	[0]	H	Read Local Mask Word and Increment Counter
86	[20D]	[X0]	[0]	H	Read Local Mask Word at HPM location

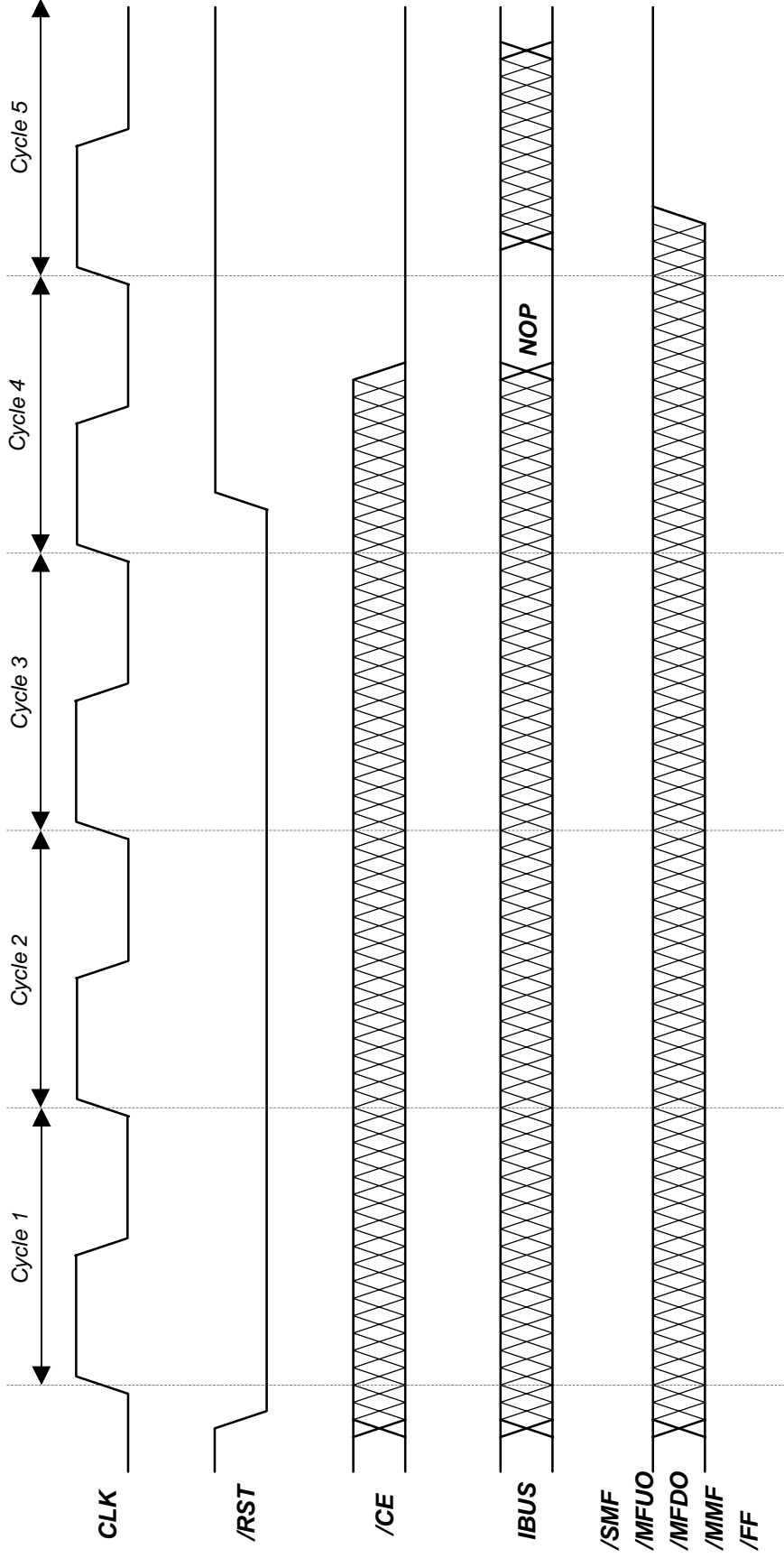
See section on cascading IPCAMs for additional details on Read operation in cascaded devices.

14.7 Data Translation Instructions

87	[500]	[X0]	[1]	H	Swap Long Word 0, 1 in Data Translation Register (32-bit swap)
88	[501]	[X0]	[1]	H	Swap Word 0, 1 in Data Translation Register (16-bit swap)
89	[502]	[X0]	[1]	H	Swap Word 2, 3 in Data Translation Register (16-bit swap)
90	[503]	[X0]	[1]	H	Shift Right 16 bits in Data Translation Register (wrap around)
91	[504]	[X0]	[1]	H	Shift Left 16 bits in Data Translation Register (wrap around)
92	[505]	[X0]	[1]	H	Shift Right 1 bit in Data Translation Register (wrap around)
93	[506]	[X0]	[1]	H	Shift Left 1 bit in Data Translation Register (wrap around)
94	[507]	[y1y0]	[0]	H	Shift Right 1 bit in Global Mask Register (fall off to the right)
95	[508]	[y1y0]	[0]	H	Shift Left 1 bit in Global Mask Register (fall off to the left)

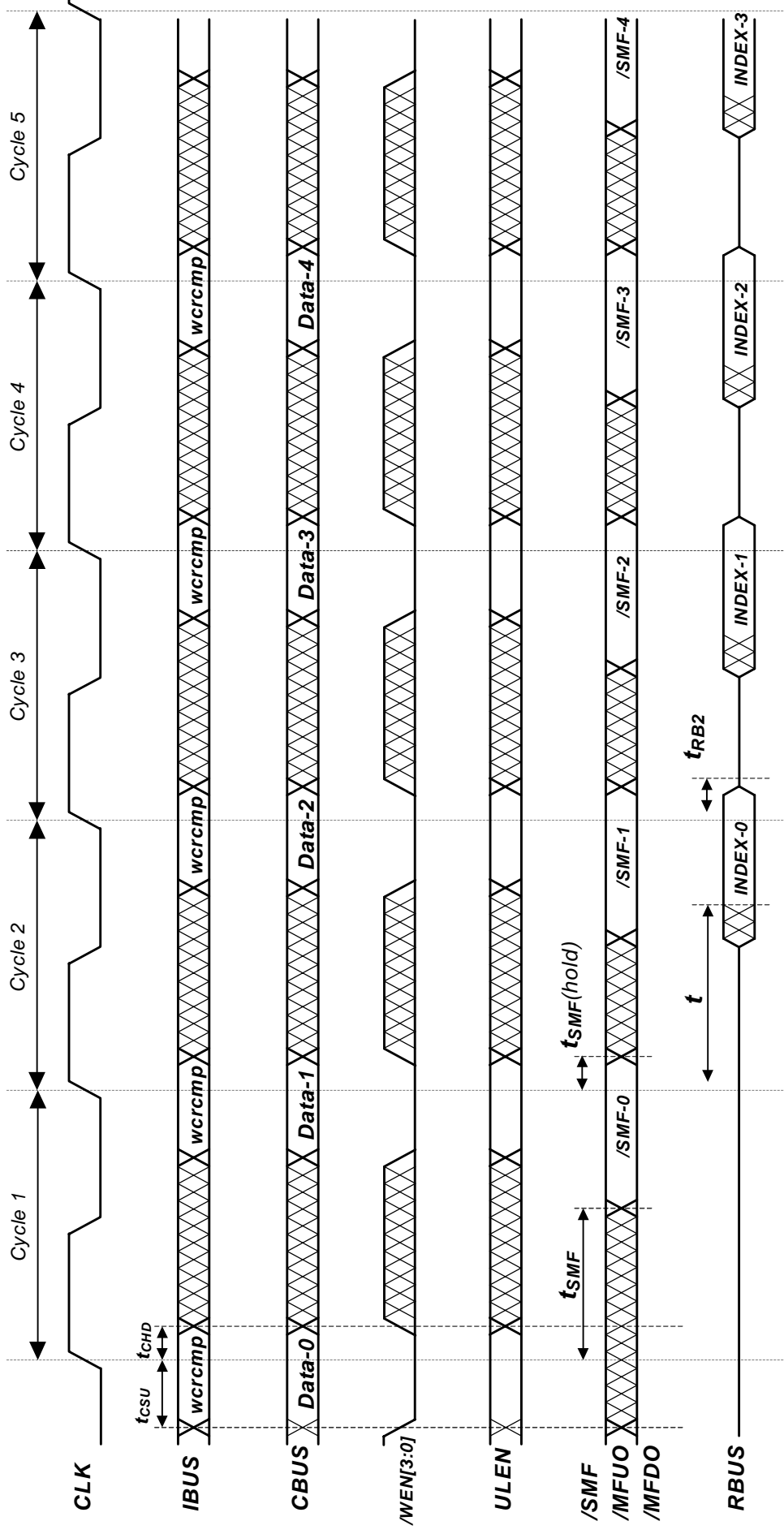
- Notes:
1. Swap/Shift operations in Data Translation Registers are controlled by ULEN input.
 2. Shifts in Global Mask Registers are performed on the 128-bit registers; ULEN input is a don't care.

RESET CYCLE



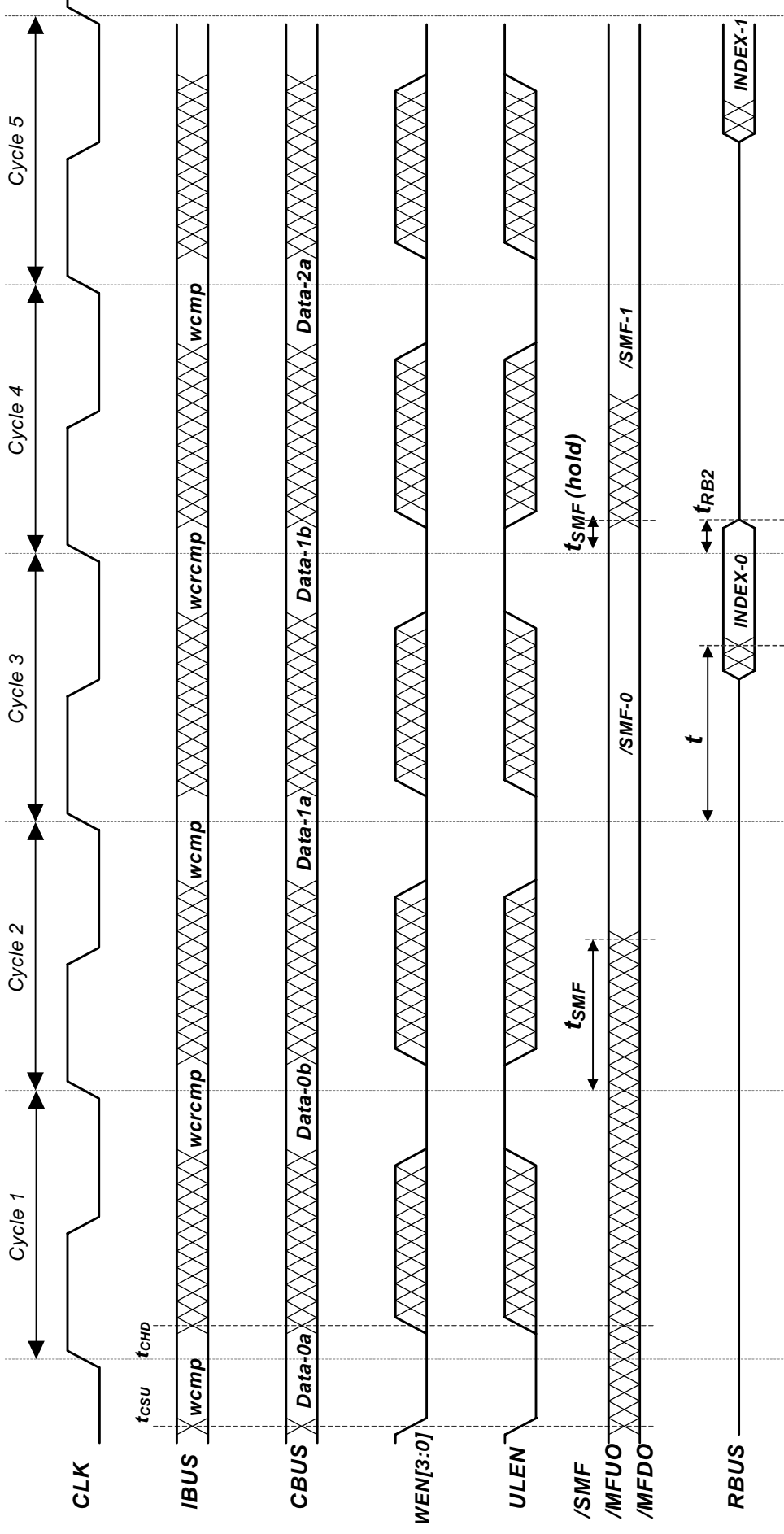
During Reset, CBUS[63:0], IBUS[13:0], WEN[3:0] and ULEN inputs are 'don't care'. RBUS is in High-Z. Reset must be followed by at least one "NOP" cycle.

64-bit Word Compare (64-bit interface, Pipelined Mode)



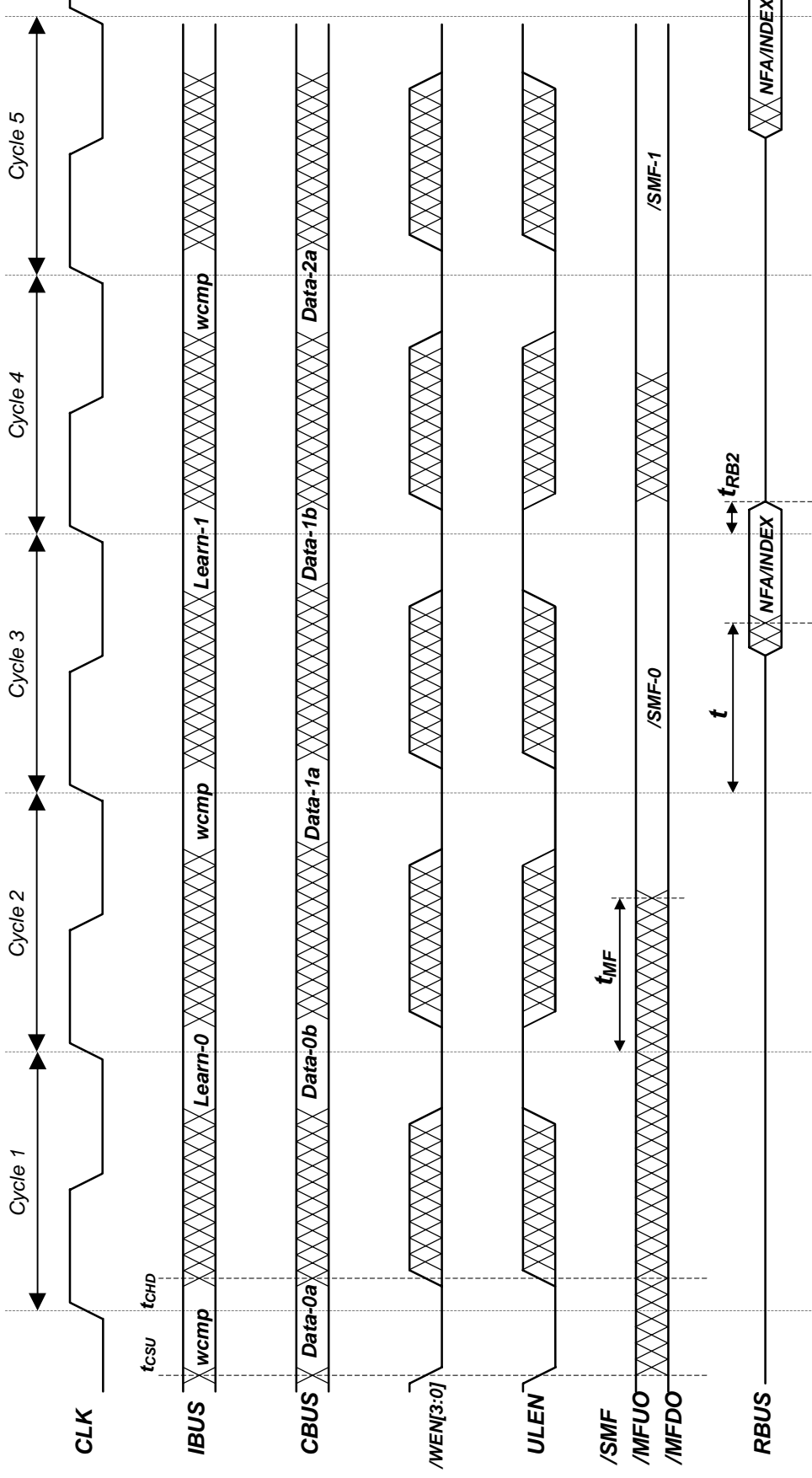
The Compare instruction is issued in the 1st cycle. The corresponding match flag is output in the 1st cycle and the RBUS output in the 2nd cycle. If a compare indicates no match ($\text{SMF}=1$), the corresponding RBUS output is High-Z. For "Flow Through" mode operation, the RBUS data is output in the same cycle as the Compare. The instruction "Write to Comparand register and Compare" is denoted as "wcrcmp" /CE = '0' during these cycles.

128-bit Word Compare (64-bit interface, Pipelined Mode)



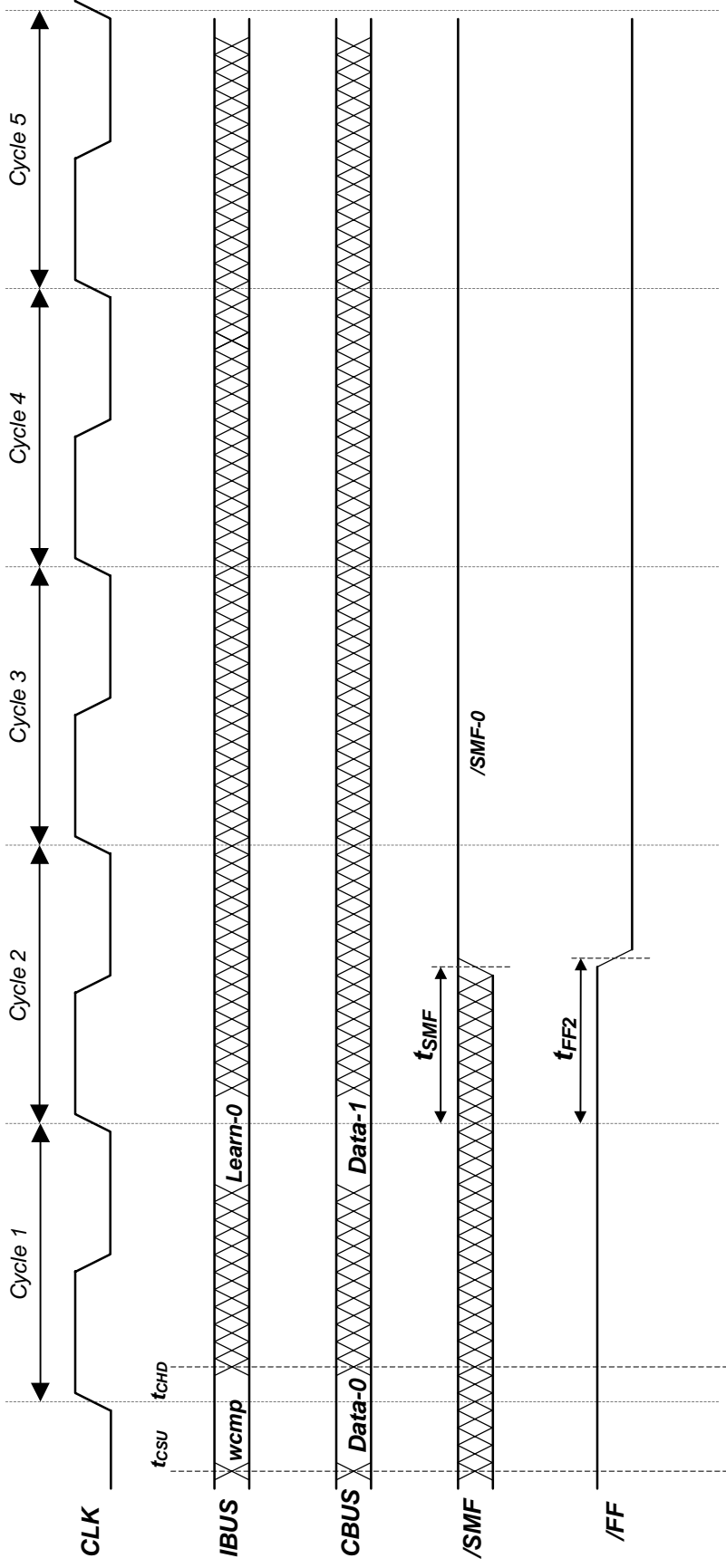
The Compare instruction is issued in the 2nd cycle. The corresponding match flag is output in the 2nd cycle and the RBUS in the 3rd cycle. If the compare instruction indicates no match (/SMF='1') the corresponding RBUS output is High-Z. In "Flow Through" mode of operation, the RBUS data is output in the same cycle as Compare instruction. The instruction "Write to Comparand" is denoted as "wcmp" and "Write to Comparand and Compare" as "wrcmp". /CE = '0' during these cycles.

128-bit Word “Learn” (64-bit interface, Pipelined Mode)



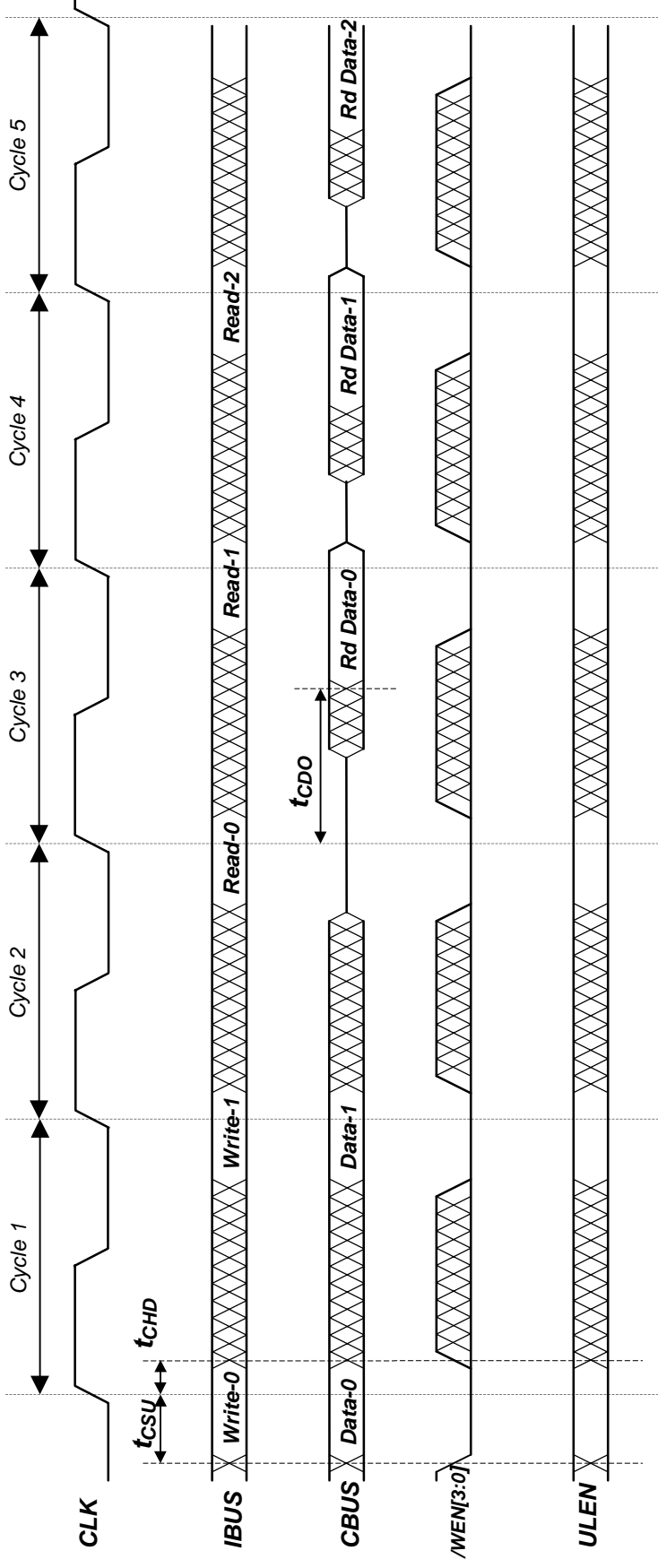
The Learn instruction is issued in the 2nd cycle. The corresponding match flag is output in the 2nd cycle and the RBUS in the 3rd cycle. During “Learn” instruction, if there is a match, Learn operates as a Compare instruction. If there is no match, the comparand data is copied to memory at NFA and this NFA is output on the RBUS. In “Flow Through” mode of operation, the RBUS data is output in the same cycle as the “Learn” instruction. “wcmp” indicates “Write to Comparand” instruction. /CE = ‘0’ during these cycles.

Learn Instruction and the Full Flag (Pipelined Mode)



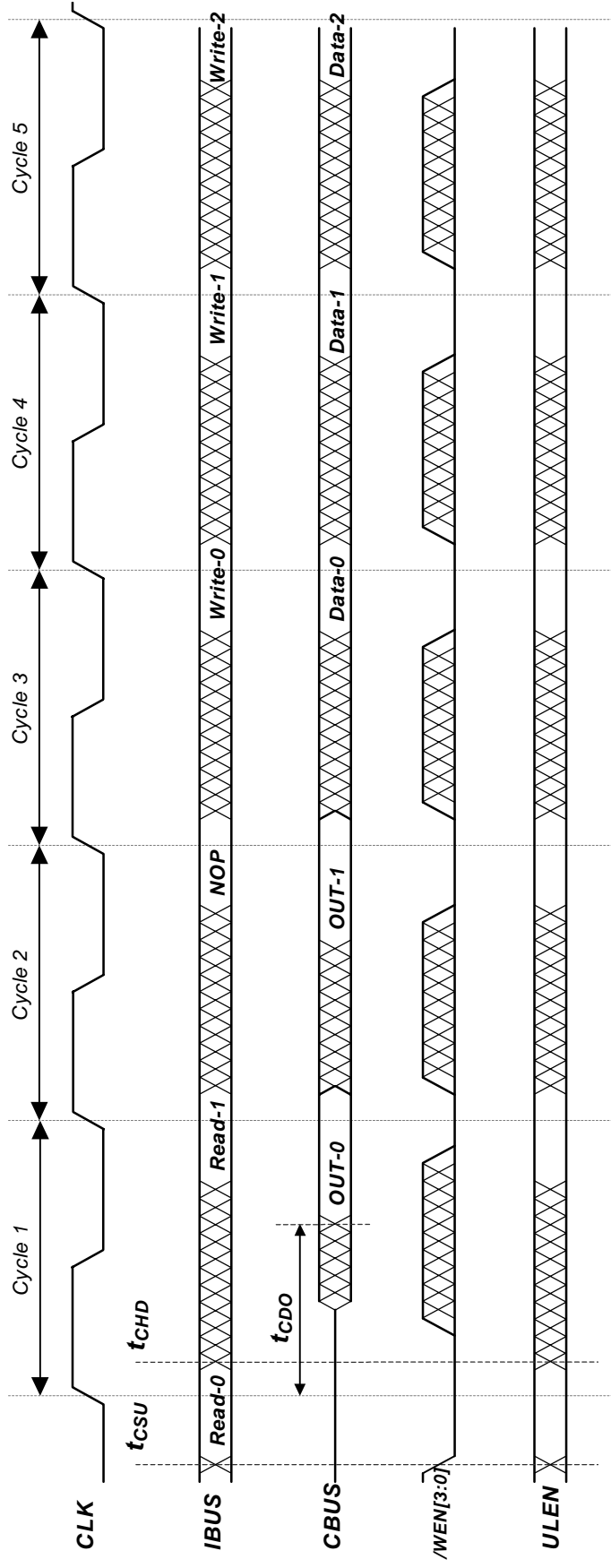
The Learn instruction is issued in the 2nd cycle. The corresponding match flag is output in the 2nd cycle and the RBUS in the 3rd cycle. If during this instruction, the last free location is written into, the full flag is asserted in the same cycle indicating that the device is full and further "Learn" instructions would not be executed. In "Flow Through" mode, the RBUS data is output in the same cycle as the "Learn" instruction. "wcmp" indicates "Write to Comparand" instruction. /CE = '0' during these cycles.

Memory Write-Memory Read Cycles (64-bit interface)



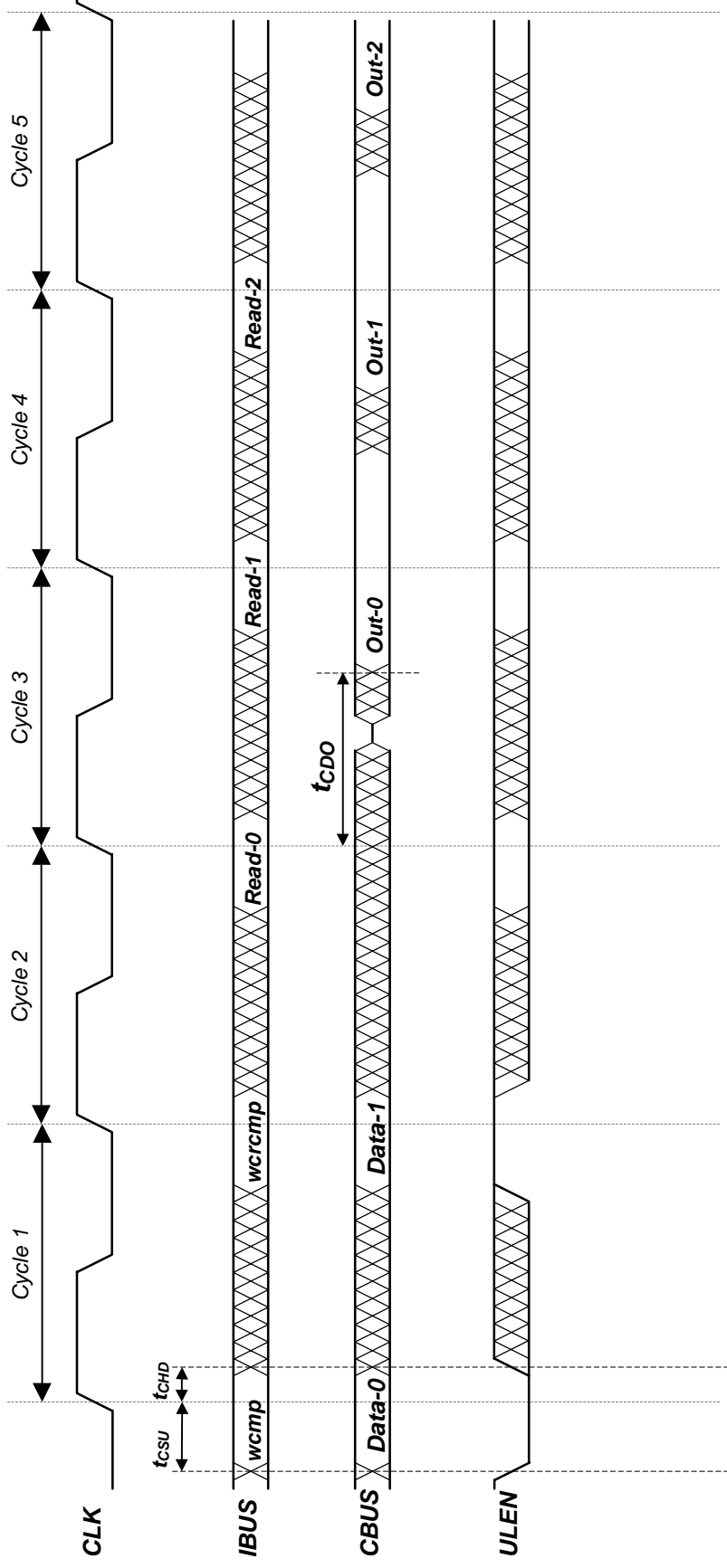
/CE = '0' during these cycles.

Memory Read-Memory Write Cycles (64-bit interface)



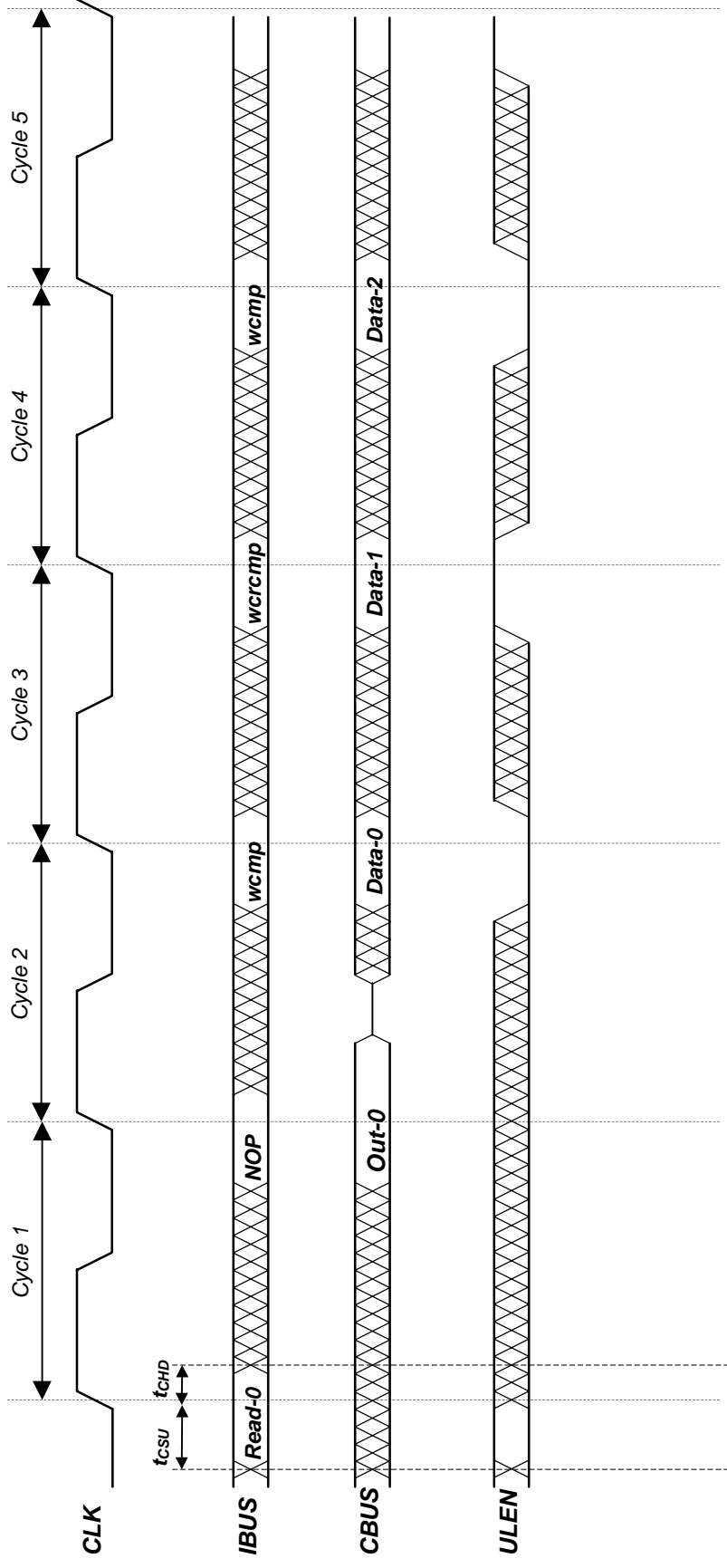
/CE = '0' during these cycles.

Compare/Memory Read Sequence



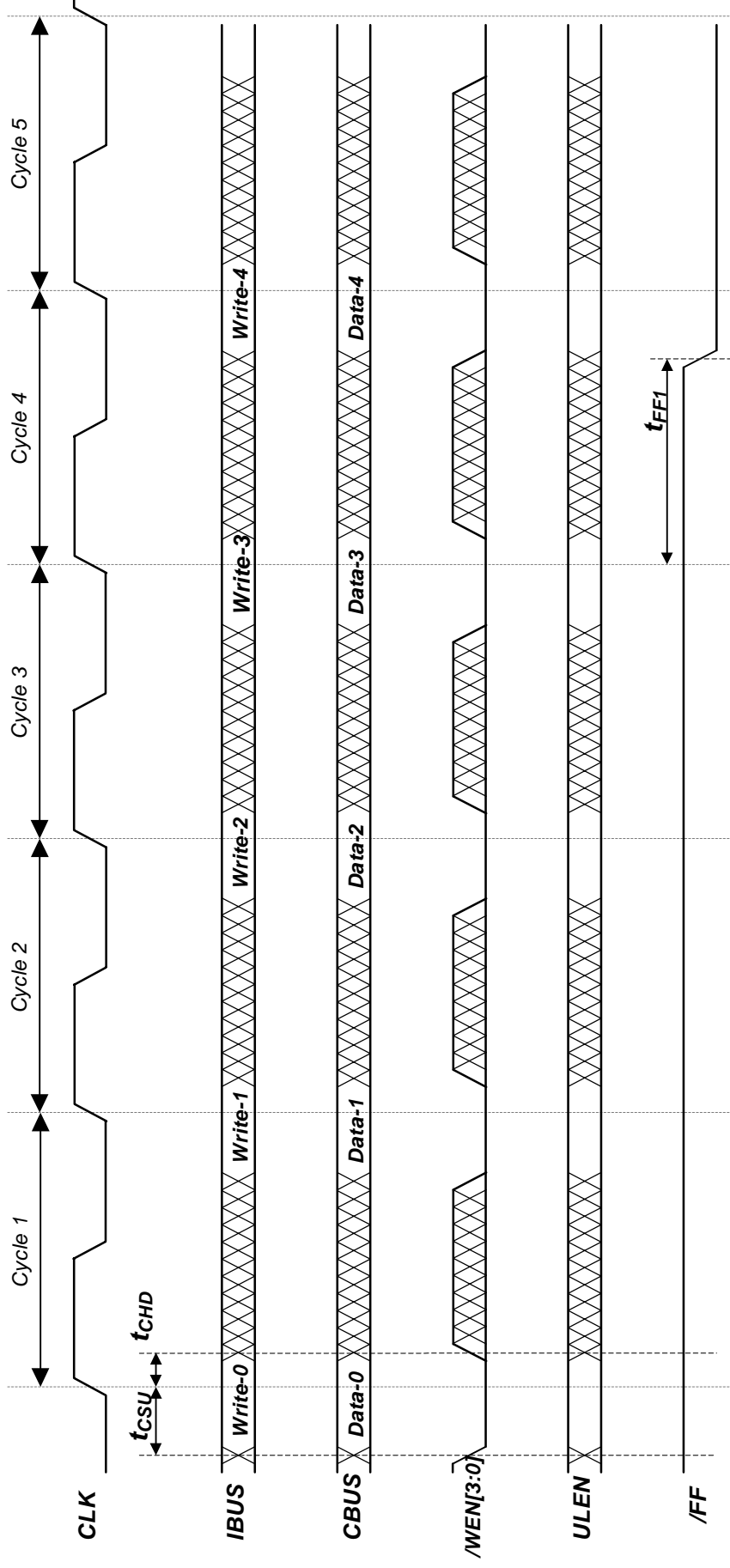
The compare instruction is issued in the 2nd cycle. The instruction "Write to Comparand" is denoted as "wcmp" and "Write to Comparand and Compare" as "wrcmp". /CE = '0' during these cycles.

Memory Read/Compare Sequence (128-bit)



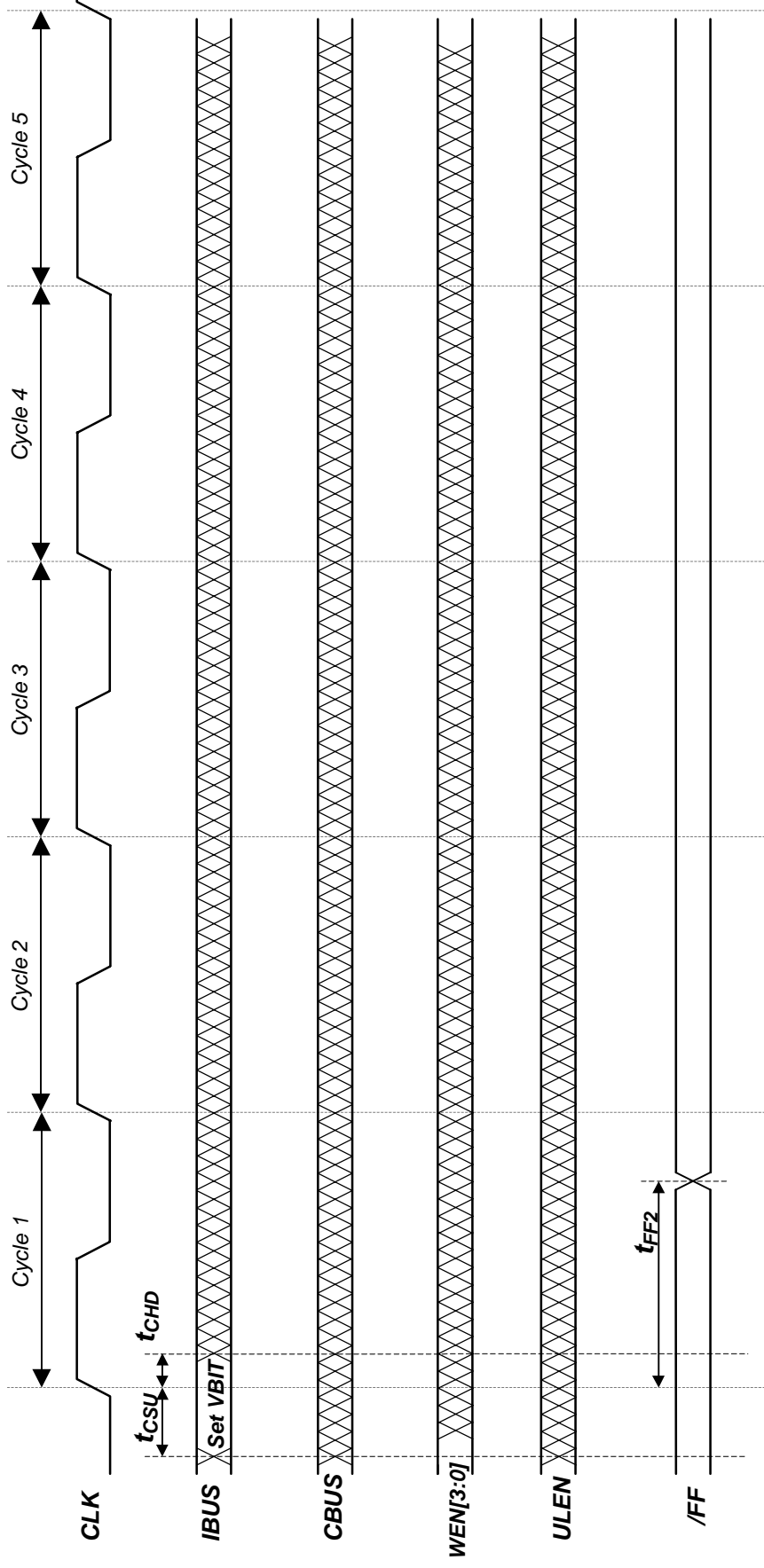
The instruction "Write to Comparand" is denoted as "wcmp" and "Write to Comparand and Compare" as "wrcmp". The /WEN[3:0] inputs are all '0'. /CE = '0' during these cycles.

Memory Write Operation and the Full Flag



The device becomes full after write-3 operation is completed. The Full Flag is asserted in the same cycle as shown. /CE = '0' during these cycles.

Validity Bit Operation and the Full Flag



If the device becomes full after the instruction is executed, the Full Flag is asserted; if the device was originally full and the instruction sets a location to empty, the Full Flag is de-asserted. The Full Flag assertion/Deassertion happens in the same cycle as the instruction. /CE = '0' during these cycles.

16.0 Ordering Information

Part Number	Cycle Time	Package	Comments
NL82721-33	33MHz	292 PBGA	
NL82721-40	40MHz	292 PBGA	Contact Factory

How to reach us:

Worldwide Headquarters:

465 Fairchild Drive, #101
Mountain View, CA 94043
1.650.961.6676
1.877.796.2226 (SyncCAM)

www.netlogicmicro.com

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