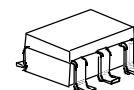


# DRIVER-AMPLIFIER GaAs MMIC

## ■GENERAL DESCRIPTION

NJG1308F is a GaAs MMIC Driver-Amplifier for 800MHz-1.9 GHz band of Cellular phone System.  
It features a low current consumption and a high gain.  
Small MTP6 package is adopted.

## ■PACKAGE OUTLINE

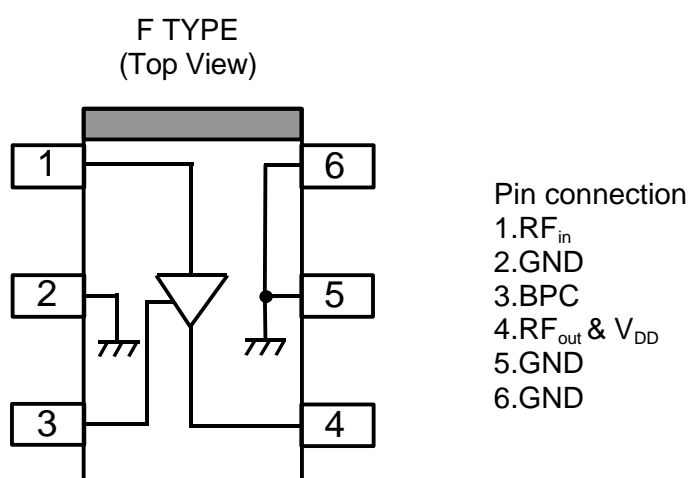


NJG1308F

## ■FEATURES

- Low supply voltage operation +3.0V typ.
- Low current consumption 15mA typ. @ $P_{out}=+8\text{dBm}$
- High gain 18dB typ. @ $f=938\text{MHz}$   
16dB @ $f=1441\text{MHz}$   
14dB @ $f=1900\text{MHz}$
- $P_{out}$  at 1dB Gain Compression point +12dBm typ. @ $f=938\text{MHz}$   
+11dBm typ. @ $f=1441/1900\text{MHz}$
- package MTP6

## ■PIN CONFIGURATION



Note: is a package orientation mark.

# NJG1308F

## ■ABSOLUTE MAXIMUM RATINGS

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Drain Voltage	$V_{DD}$		6	V
Input Power	$P_{in}$	$V_{DD}=3\text{V}$	15	dBm
Power Dissipation	$P_D$		300	mW
Operating Temperature	$T_{opr}$		-40~+85	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$		-55~+150	$^{\circ}\text{C}$

## ■ELECTRICAL CHARACTERISTICS 1(Application circuit 1)

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	Freq	$V_{DD}=3.0\text{V}$	915	938	960	MHz
Drain Voltage	$V_{DD}$		2.7	3.0	5.0	V
Operating Current	$I_{DD}$	$V_{DD}=3.0\text{V}$ , $P_{out}=+8\text{dBm}$	-	15	21	mA
Small Signal Gain	Gain	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	15	18	21	dB
Gain Flatness	$G_{flat}$	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	-	0.5	-	dB
Pout at 1dB Gain Compression point	$P_{-1\text{dB}}$	$V_{DD}=3.0\text{V}$	-	+12	-	dBm
Adjacent Channel Leakage Power (PDC Regulation)	$P_{acp}$	$V_{DD}=3.0\text{V}$ , $P_{out}=+8\text{dBm}$ offset=50kHz $P_{in}; \pi/4$ DQPSK	-	-60	-	dBc
Input VSWR	$VSWR_i$	$V_{DD}=3.0\text{V}$	-	1.5	-	
Output VSWR	$VSWR_o$	$V_{DD}=3.0\text{V}$	-	1.5	-	

## ■ELECTRICAL CHARACTERISTICS 2 (Application circuit 2)

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	freq	$V_{DD}=3.0\text{V}$	1429	1441	1453	MHz
Drain Voltage	$V_{DD}$		2.7	3.0	5.0	V
Operating Current	$I_{DD}$	$V_{DD}=3.0\text{V}$ , $P_{out}=+8\text{dBm}$	-	15	21	mA
Small Signal Gain	Gain	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	13	16	19	dB
Gain Flatness	$G_{flat}$	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	-	0.5	-	dB
Pout at 1dB Gain Compression point	$P_{-1\text{dB}}$	$V_{DD}=3.0\text{V}$	-	+11	-	dBm
Adjacent Channel Leakage Power (PDC Regulation)	$P_{acp}$	$V_{DD}=3.0\text{V}$ , $P_{out}=+8\text{dBm}$ offset=50kHz $P_{in}; \pi/4$ DQPSK	-	-60	-	dBc
Input VSWR	$VSWR_i$	$V_{DD}=3.0\text{V}$	-	1.5	-	
Output VSWR	$VSWR_o$	$V_{DD}=3.0\text{V}$	-	1.5	-	

## ■ELECTRICAL CHARACTERISTICS 3 (Application circuit 3)

( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

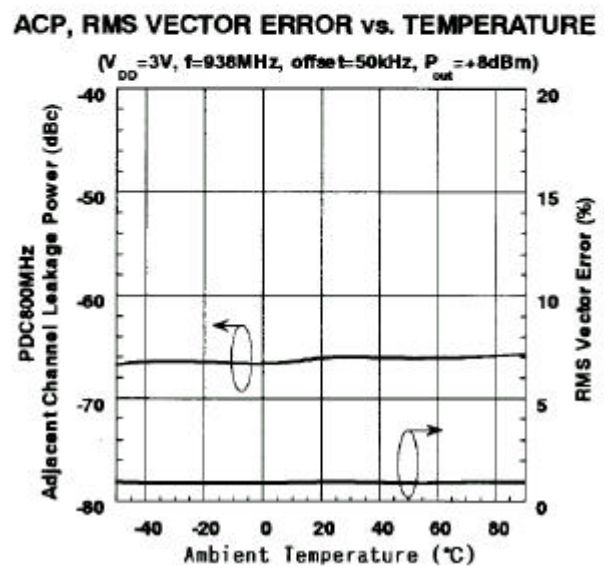
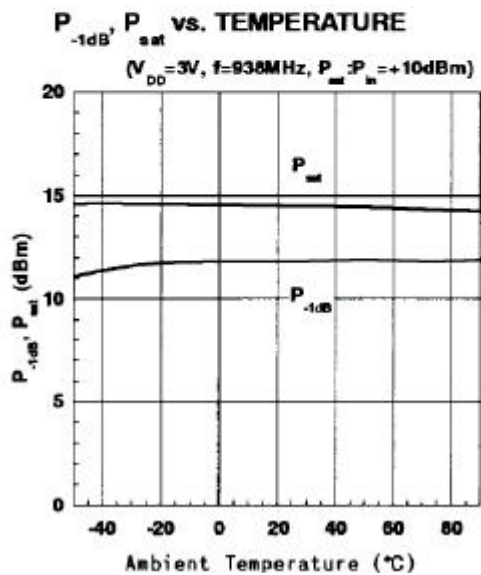
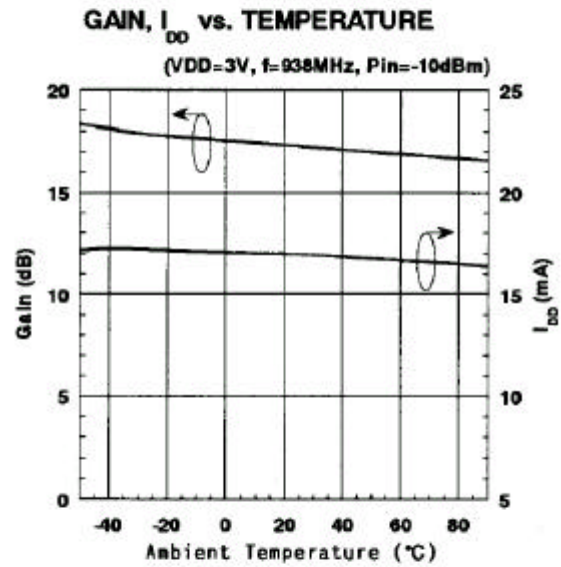
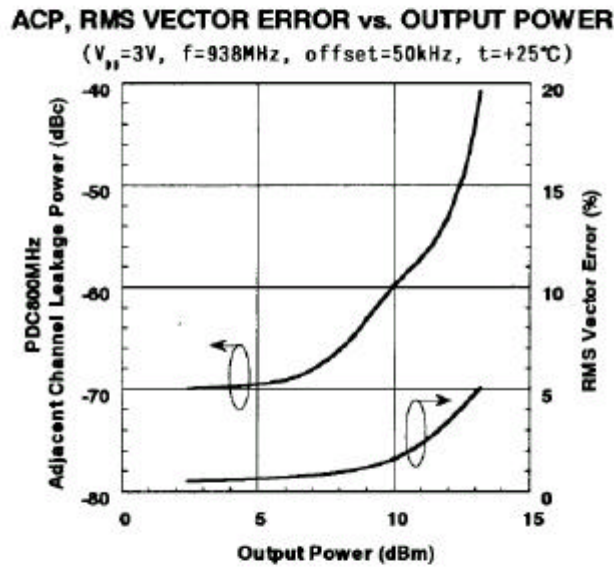
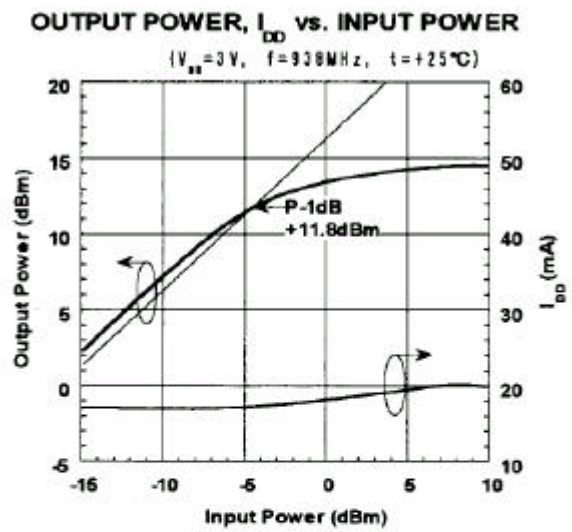
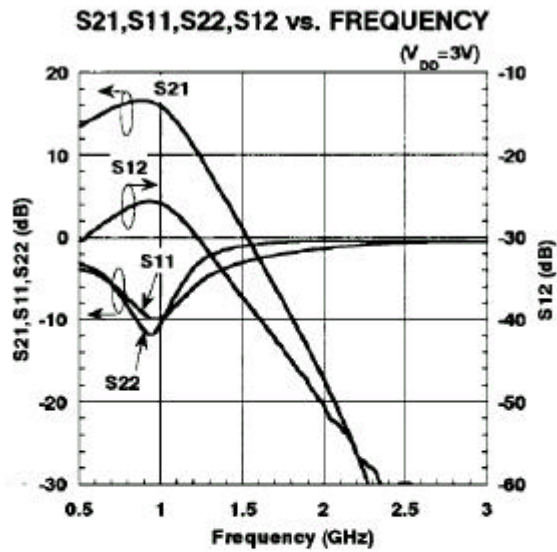
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	freq	$V_{DD}=3.0\text{V}$	1890	1900	1920	MHz
Drain Voltage	$V_{DD}$		2.7	3.0	5.0	V
Operating Current	$I_{DD}$	$V_{DD}=3.0\text{V}$ , $P_{out}=+8\text{dBm}$	-	15	21	mA
Small Signal Gain	Gain	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	11	14	17	dB
Gain Flatness	$G_{flat}$	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	-	0.5	-	dB
Pout at 1dB Gain Compression point	$P_{-1\text{dB}}$	$V_{DD}=3.0\text{V}$	-	+11	-	dBm
Adjacent Channel Leakage Power (PHS Regulation)	$P_{acp}$	$V_{DD}=3.0\text{V}$ , $P_{out}=+8\text{dBm}$ offset=600kHz $P_{in}$ ; $\pi/4$ DQPSK	-	-60	-	dBc
Input VSWR	$VSWR_i$	$V_{DD}=3.0\text{V}$	-	1.5	-	
Output VSWR	$VSWR_o$	$V_{DD}=3.0\text{V}$	-	1.5	-	

## ■ELECTRICAL CHARACTERISTICS 4 (Application Circuit 4)

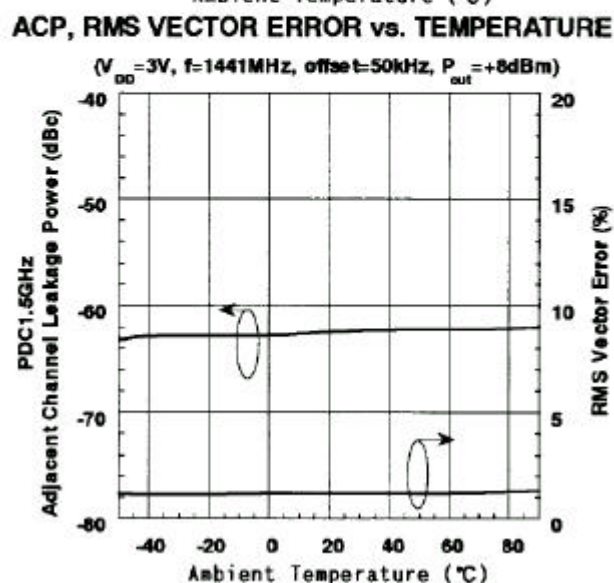
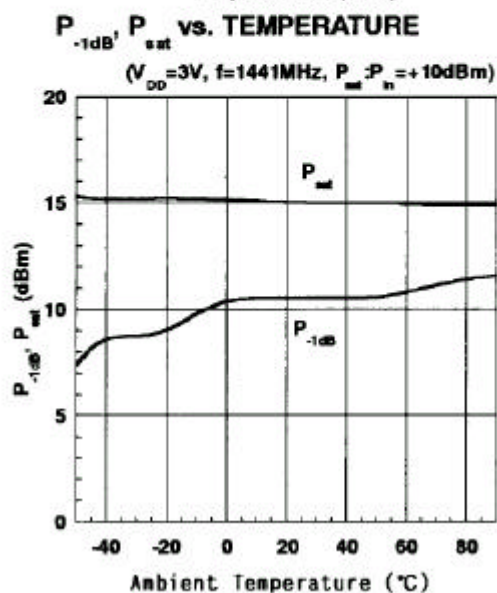
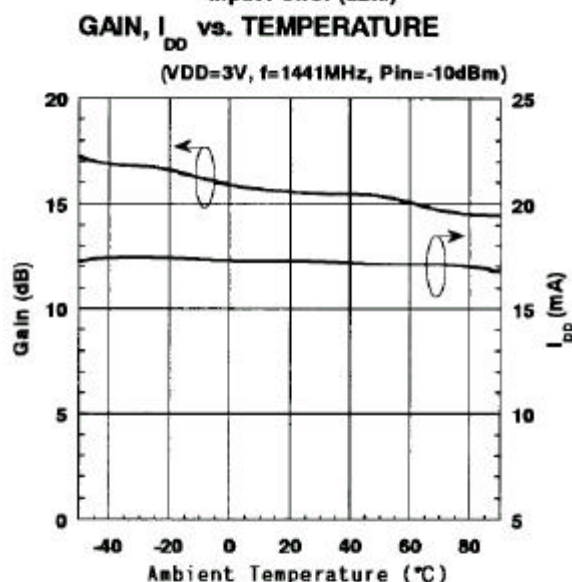
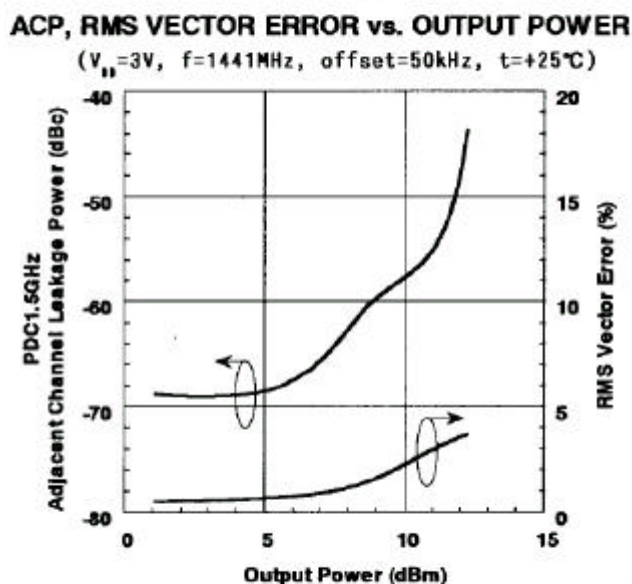
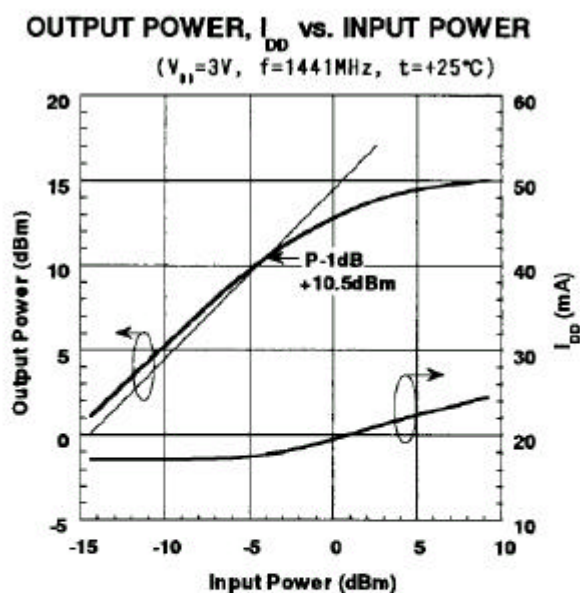
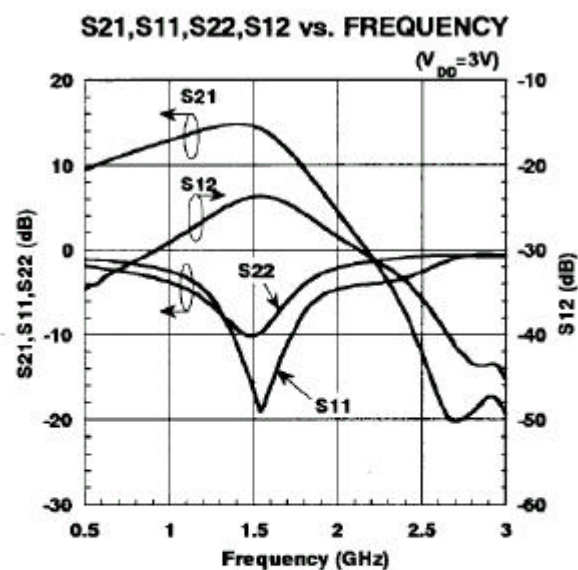
( $T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$ )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	freq	$V_{DD}=3.0\text{V}$	1750	1765	1780	MHz
Supply Voltage	$V_{DD}$		2.7	3.0	5.0	V
Operating Current	$I_{DD}$	$V_{DD}=3.0\text{V}$ , $P_{out}=+8\text{dBm}$	-	15	-	mA
Power Gain	Gain	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	-	14	-	dB
Gain Flatness	$G_{flat}$	$V_{DD}=3.0\text{V}$ , $P_{in}=-10\text{dBm}$	-	0.5	-	dB
Pout at 1dB Compression point	$P_{-1\text{Db}}$	$V_{DD}=3.0\text{V}$	-	+11	-	dBm
Input VSWR	$VSWR_i$	$V_{DD}=3.0\text{V}$	-	1.5	-	
Output VSWR	$VSWR_o$	$V_{DD}=3.0\text{V}$	-	1.5	-	

## ■ TYPICAL CHARACTERISTICS 1 (Application Circuit 1)

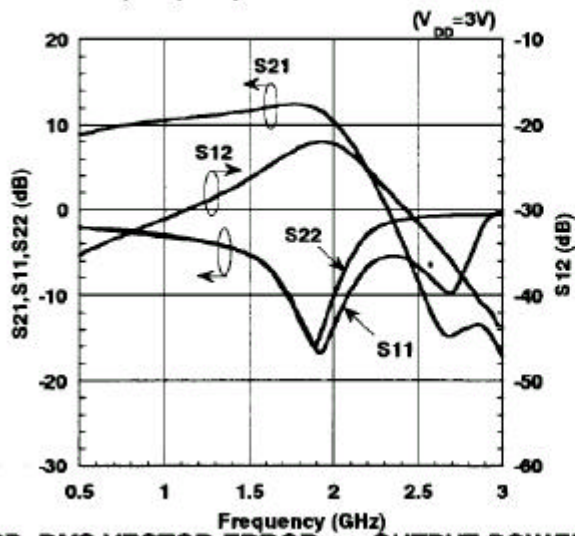


## ■ TYPICAL CHARACTERISTICS 2 (Application Circuit 2)

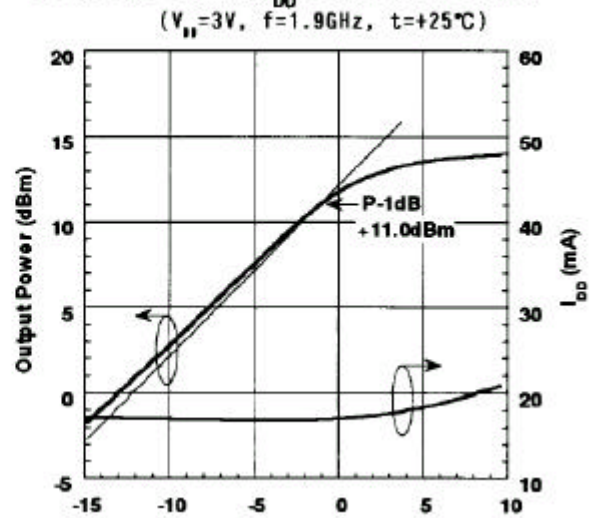


## ■ TYPICAL CHARACTERISTICS 3 (Application Circuit 3)

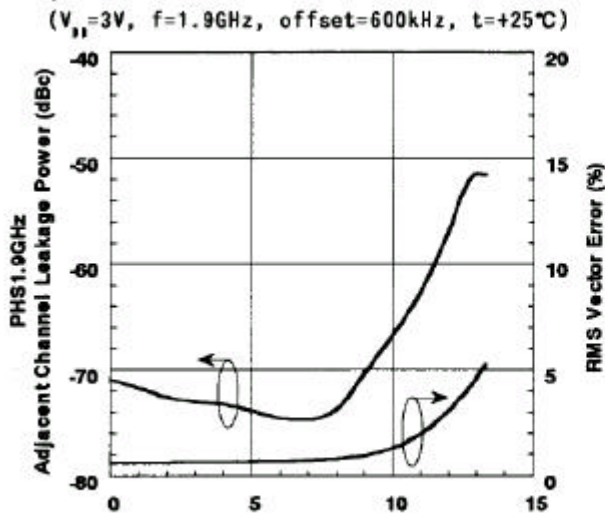
S21, S11, S22, S12 vs. FREQUENCY



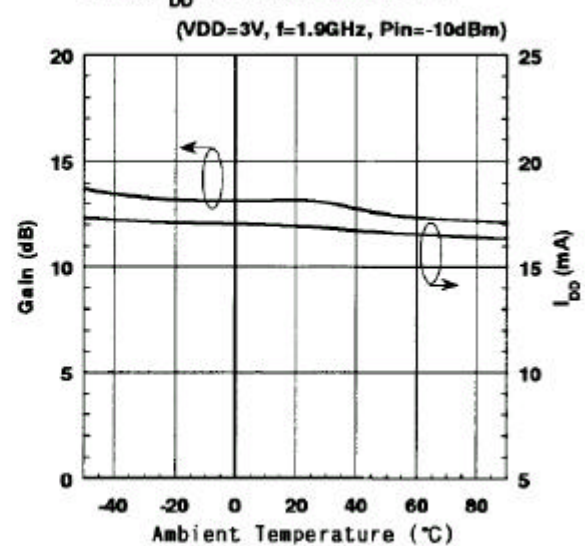
OUTPUT POWER,  $I_{DD}$  vs. INPUT POWER



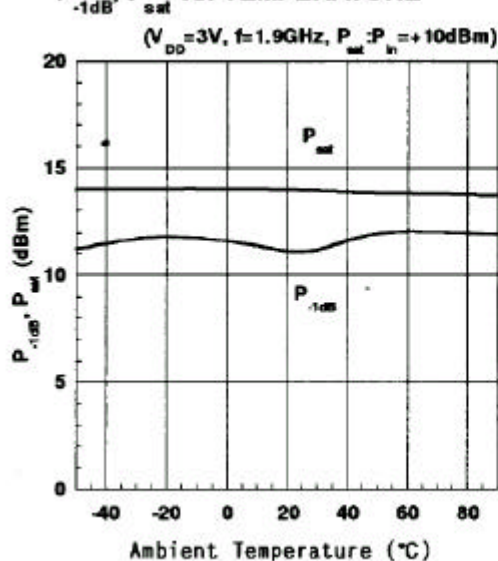
ACP, RMS VECTOR ERROR vs. OUTPUT POWER



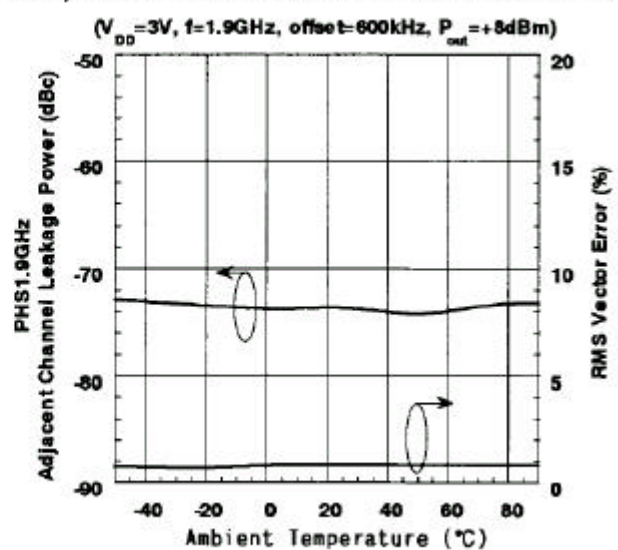
GAIN,  $I_{DD}$  vs. TEMPERATURE



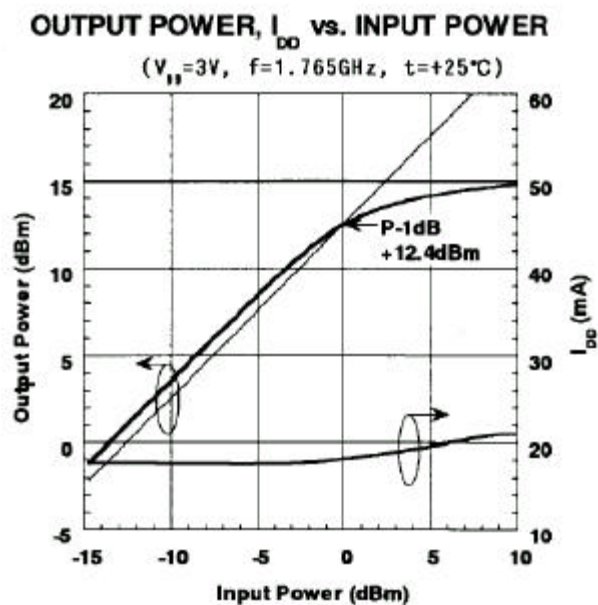
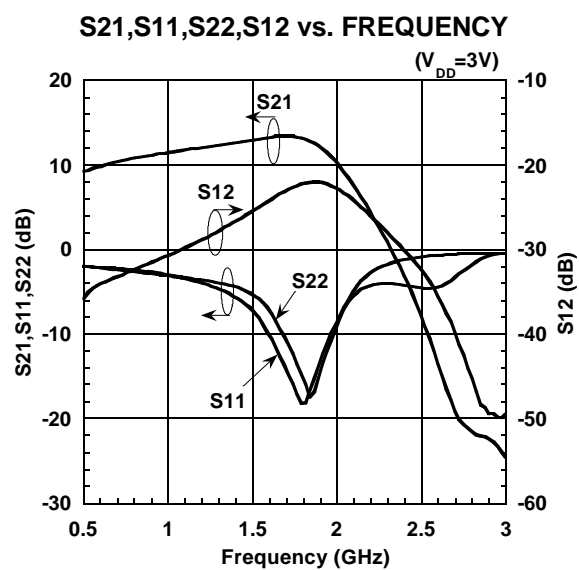
$P_{-1dB}$ ,  $P_{sat}$  vs. TEMPERATURE



ACP, RMS VECTOR ERROR vs. TEMPERATURE



## ■TYPICAL CHARACTERISTICS 4 (Application Circuit 4)

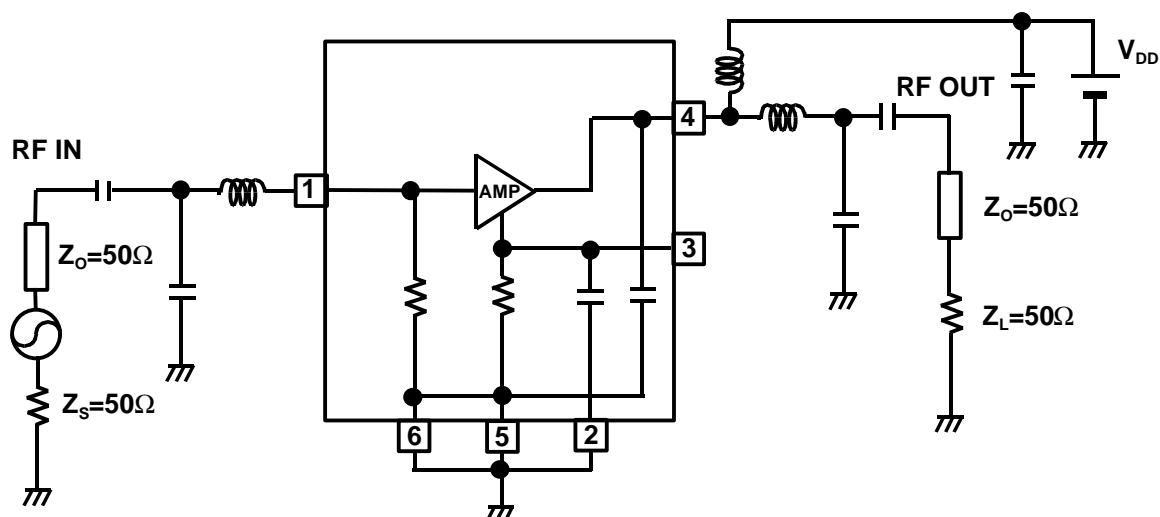


## ■TYPICAL CHARACTERISTICS

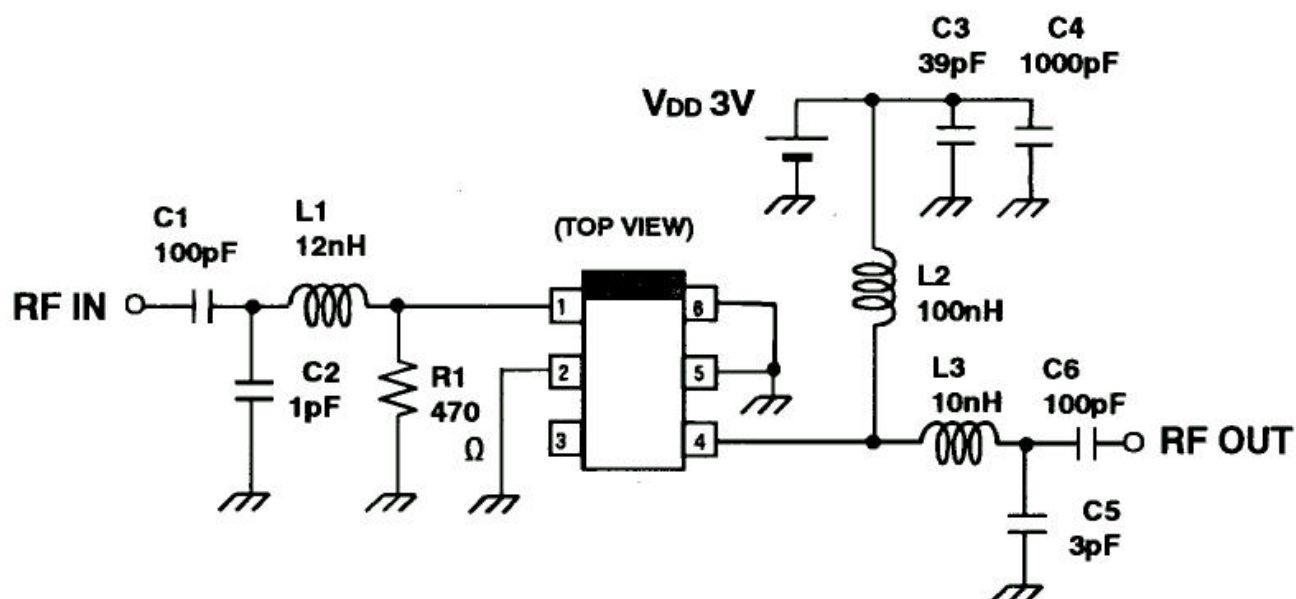
Scattering Parameters ( $V_{DD}=3V$ )

Freq. (GHz)	S 11		S 21		S 12		S 22	
	mag (U)	ang (deg)	mag (U)	ang (deg)	mag (U)	ang (deg)	mag (U)	ang (deg)
0.50	0.865	-26.1	4.892	174.0	0.029	52.0	0.718	-56.5
0.60	0.853	-32.2	5.060	163.2	0.030	48.7	0.681	-63.4
0.70	0.834	-38.2	5.093	152.9	0.033	46.2	0.648	-69.6
0.80	0.810	-43.7	5.046	143.5	0.035	46.4	0.626	-74.9
0.90	0.788	-48.5	4.974	134.5	0.036	44.5	0.603	-78.8
1.00	0.757	-52.8	4.801	126.4	0.038	43.5	0.590	-82.4
1.10	0.729	-56.7	4.650	118.6	0.039	42.7	0.580	-85.6
1.20	0.700	-60.3	4.457	111.5	0.041	44.0	0.579	-88.8
1.30	0.672	-63.1	4.271	104.6	0.043	43.3	0.577	-90.9
1.40	0.645	-65.6	4.083	98.0	0.045	44.6	0.581	-93.6
1.50	0.618	-67.7	3.893	91.3	0.046	44.0	0.588	-96.0
1.60	0.589	-69.0	3.687	85.2	0.049	43.8	0.597	-98.5
1.70	0.563	-69.7	3.509	79.3	0.051	42.4	0.612	-100.8
1.80	0.541	-69.8	3.317	72.9	0.055	40.3	0.630	-103.7
1.90	0.519	-69.6	3.122	66.5	0.058	38.3	0.650	-106.9
2.00	0.502	-67.9	2.904	60.0	0.060	35.8	0.671	-110.2
2.10	0.489	-65.9	2.696	53.6	0.063	31.4	0.700	-114.5
2.20	0.490	-62.3	2.432	46.6	0.065	25.7	0.728	-119.5
2.30	0.502	-58.9	2.150	39.1	0.065	17.4	0.764	-125.8
2.40	0.536	-55.6	1.814	31.9	0.066	8.5	0.795	-132.8
2.50	0.592	-53.5	1.409	24.6	0.062	-5.9	0.828	-142.1
2.60	0.669	-53.8	0.933	21.3	0.056	-24.0	0.846	-153.2
2.70	0.760	-56.9	0.461	41.1	0.050	-54.3	0.842	-166.5
2.80	0.851	-62.8	0.575	106.1	0.048	-96.7	0.800	178.6
2.90	0.920	-70.6	1.154	113.3	0.060	-140.4	0.731	161.6
3.00	0.951	-79.2	1.703	105.2	0.081	-172.8	0.624	144.2

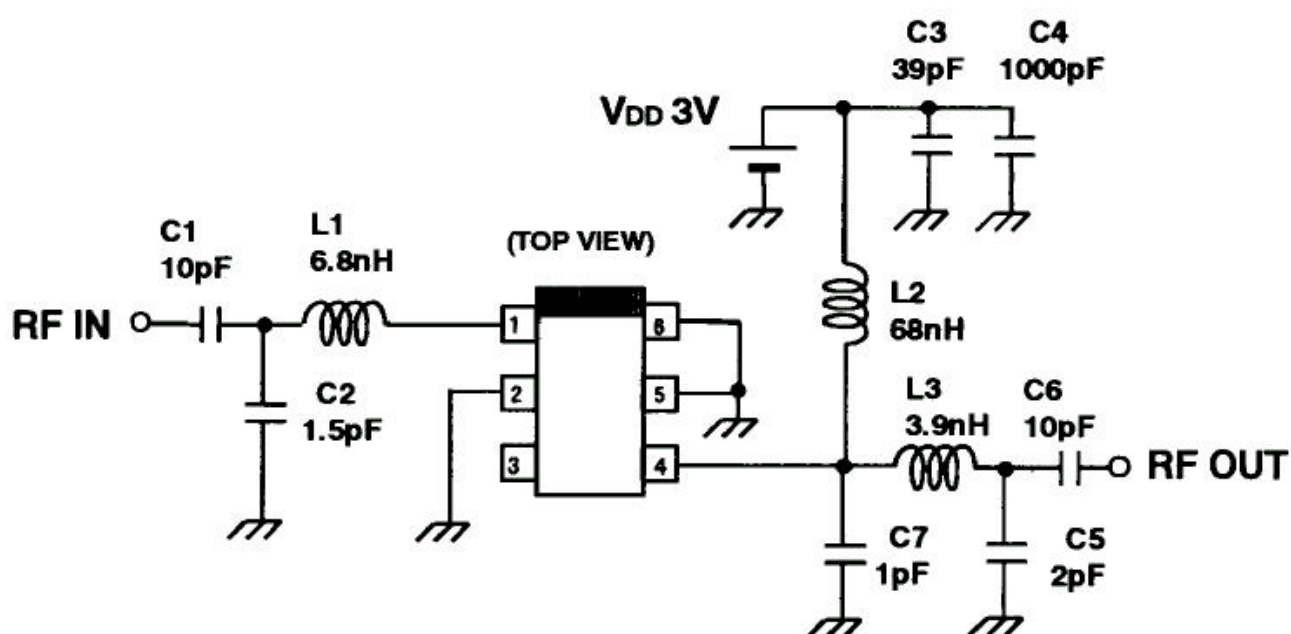
## ■PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



## APPLICATION CIRCUIT 1

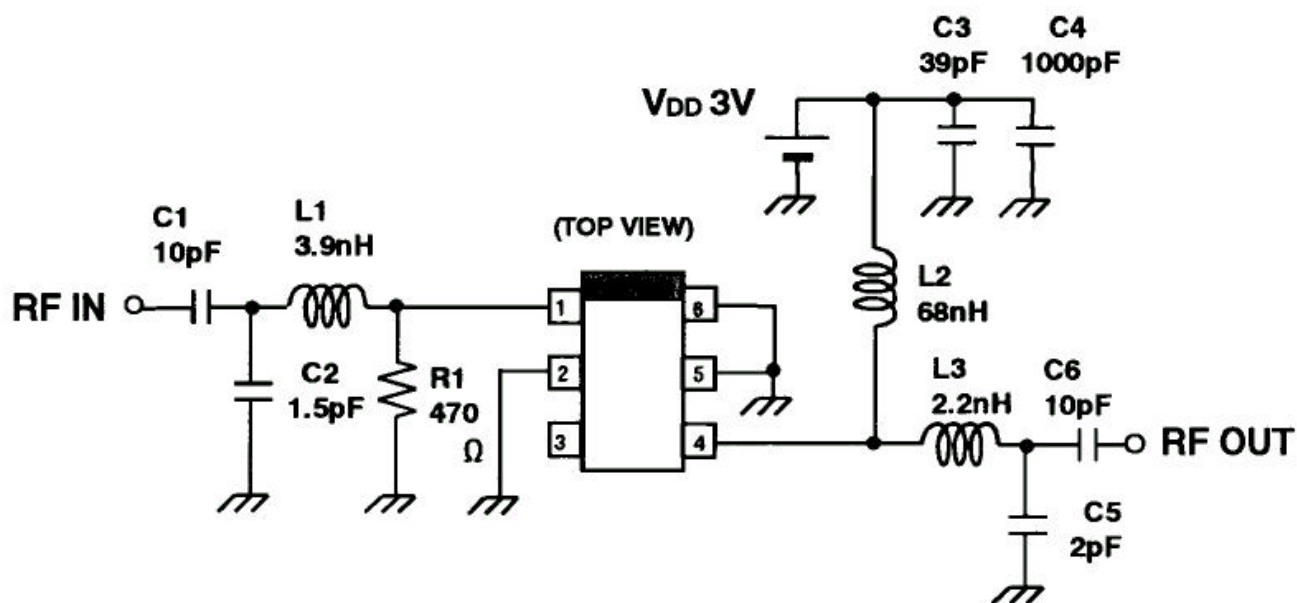


## APPLICATION CIRCUIT 2

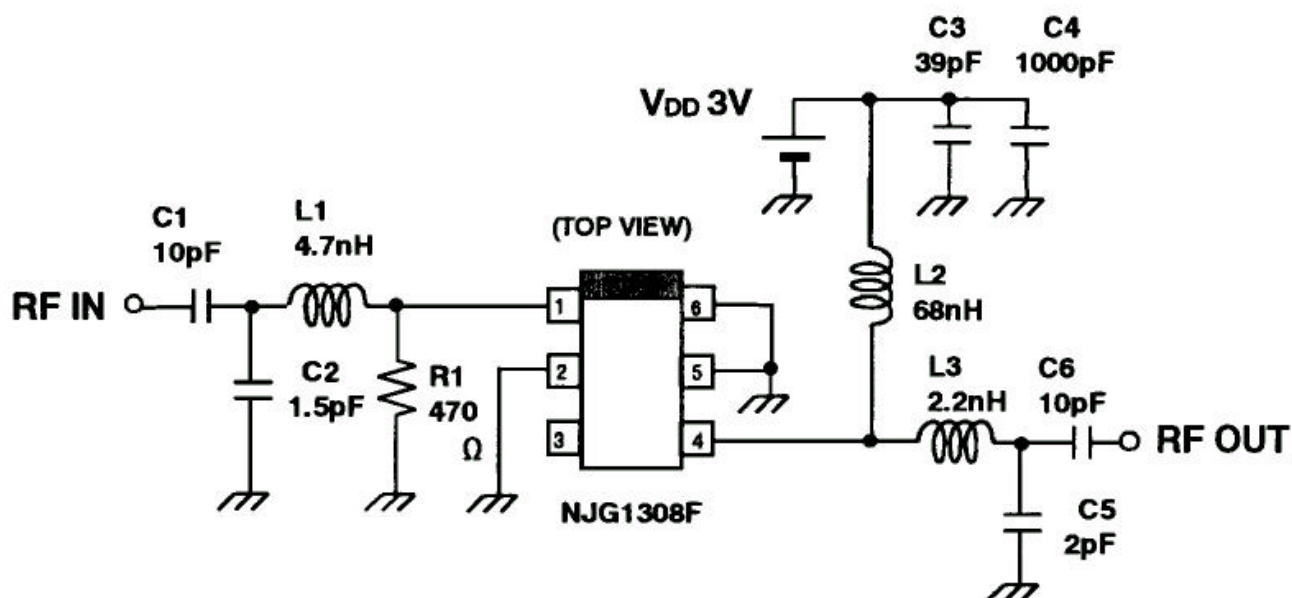


# NJG1308F

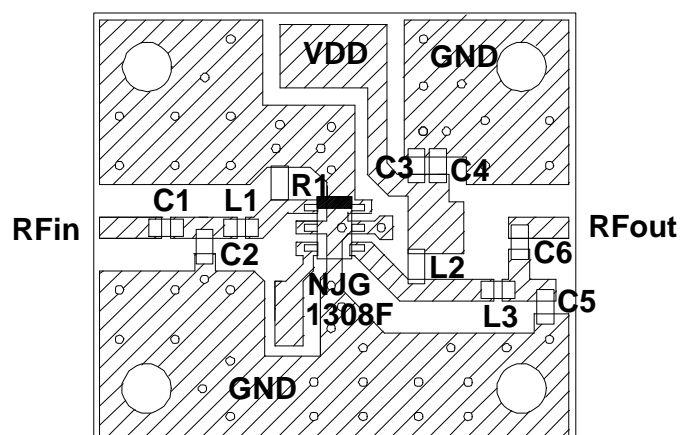
## APPLICATION CIRCUIT 3



## APPLICATION CIRCUIT 4



## RECOMMENDED PCB DESIGN



PCB:FR-4 22.5x20.0mm, t=0.5mm  
 MICROSTRIP LINE WIDTH=1.0mm ( $Z_0=50\Omega$ )  
 CHIP SIZE:1608

### Notes:

[1] Following chip capacitor should be connected near to each terminal as bypass capacitor.

- (1) C3
- (2) C4

[2] Following chip capacitors are necessary to block DC bias.

- (3) C1
- (4) C6

[3] Chip parts list.

Parts ID	Comment
C1~C6	MURATA GRM39 Series
L1~L3	TAIYO-YUDEN HK1608 Series

