



NJU6575A

PRELIMINARY

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6575A is a bit map LCD driver to display graphics or characters.

It contains 4,422 bits display data RAM, microprocessor interface circuits, instruction decoder, 134-segment and 33-common (1 out of 33-driver is prepared for icon display) drivers.

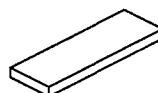
The bit image display data is transfer d to the display data RAM by serial or 8-bit parallel interface.

33 x 134 dots graphics or 8-character 2-line by 16 x 16 dot character with icon are displayed by NJU6575A itself.

The wide operating voltage from 2.4V to 5.5V and low operating current are useful for small size battery operating items.

The build-in Electrical Variable Resistance is very precision, furthermore the rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE OUTLINE



NJU6575ACH

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 4,422 bits
- 167 LCD Drivers - 33- common and 134-segment
- Direct micro processor Interface for both of 68 and 80 type MPU
- Serial Interface
- Programmable Duty Ratio ; 1/32 or 1/33 Duty
- Useful Instruction Set
 - Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
 - Step up Circuits, Regulator, Voltage Follower x 4
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.4V to 5.5V
- LCD Driving Voltage --- 6.0V to 13.5V
- Package Outline --- TCP/Bumped Chip
- C-MOS Technology



NJU6575A

■ PAD COORDINATES

Chip Size 11.49mm x 2.44mm (Chip Center X=0um, Y=0um)

N.O.	Termi.	X= μ m	Y= μ m
1	V _{DD}	5472	1054
2	V _{DD}	5392	1054
3	V _{DD}	5312	1054
4	P/S	5232	1054
5	C86	5152	1054
6	V _{SS}	5072	1054
7	V _{SS}	4992	1054
8	V _{SS}	4912	1054
9	T ₂	4832	1054
10	T ₁	4752	1054
11	OSC ₁	4672	1054
12	SCL	4592	1054
13	SI	4192	1054
14	CS	3792	1054
15	A0	3392	1054
16	WR	2992	1054
17	RD	2592	1054
18	D ₀	2192	1054
19	D ₁	1792	1054
20	D ₂	1392	1054
21	D ₃	992	1054
22	D ₄	592	1054
23	D ₅	192	1054
24	D ₆	-208	1054
25	D ₇	-608	1054
26	V _{SS}	-928	1054
27	V _{SS}	-1008	1054
28	V _{SS}	-1088	1054
29	C1 ⁺	-1328	1054
30	C1 ⁺	-1408	1054
31	C1 ⁺	-1488	1054
32	C1 ⁻	-1728	1054
33	C1 ⁻	-1808	1054
34	C1 ⁻	-1888	1054
35	C2 ⁺	-2128	1054
36	C2 ⁺	-2208	1054
37	C2 ⁺	-2288	1054
38	C2 ⁻	-2528	1054
39	C2 ⁻	-2608	1054
40	C2 ⁻	-2688	1054
41	V _{OUT}	-2928	1054
42	V _{OUT}	-3008	1054
43	V _{OUT}	-3088	1054
44	V _{DD}	-3328	1054
45	V _{DD}	-3408	1054
46	V _{DD}	-3488	1054
47	VR	-3728	1054
48	VR	-3808	1054
49	VR	-3888	1054
50	V _S	-4128	1054

N.O.	Termi.	X= μ m	Y= μ m
51	V _S	-4208	1054
52	V _S	-4288	1054
53	V ₄	-4528	1054
54	V ₄	-4608	1054
55	V ₄	-4688	1054
56	V ₃	-4928	1054
57	V ₃	-5008	1054
58	V ₃	-5088	1054
59	V ₂	-5328	1054
60	V ₂	-5408	1054
61	V ₂	-5488	1054
62	V ₁	-5584	862
63	V ₁	-5584	782
64	C ₀	-5584	702
65	C ₁	-5584	622
66	C ₂	-5584	542
67	C ₃	-5584	462
68	C ₄	-5584	382
69	C ₅	-5584	302
70	C ₆	-5584	222
71	C ₇	-5584	142
72	C ₈	-5584	62
73	C ₉	-5584	-18
74	C ₁₀	-5584	-98
75	C ₁₁	-5584	-178
76	C ₁₂	-5584	-258
77	C ₁₃	-5584	-338
78	C ₁₄	-5584	-418
79	C ₁₅	-5584	-498
80	NC	-5584	-634
81	NC	-5584	-770
82	NC	-5584	-906
83	NC	-5434	-1055
84	SEG ₀	-5306	-1055
85	SEG ₁	-5226	-1055
86	SEG ₂	-5146	-1055
87	SEG ₃	-5066	-1055
88	SEG ₄	-4986	-1055
89	SEG ₅	-4906	-1055
90	SEG ₆	-4826	-1055
91	SEG ₇	-4746	-1055
92	SEG ₈	-4666	-1055
93	SEG ₉	-4586	-1055
94	SEG ₁₀	-4506	-1055
95	SEG ₁₁	-4426	-1055
96	SEG ₁₂	-4346	-1055
97	SEG ₁₃	-4266	-1055
98	SEG ₁₄	-4186	-1055
99	SEG ₁₅	-4106	-1055
100	SEG ₁₆	-4026	-1055

N.O.	Termi.	X= μ m	Y= μ m
101	SEG ₁₇	-3946	-1055
102	SEG ₁₈	-3866	-1055
103	SEG ₁₉	-3786	-1055
104	SEG ₂₀	-3706	-1055
105	SEG ₂₁	-3626	-1055
106	SEG ₂₂	-3546	-1055
107	SEG ₂₃	-3466	-1055
108	SEG ₂₄	-3386	-1055
109	SEG ₂₅	-3306	-1055
110	SEG ₂₆	-3226	-1055
111	SEG ₂₇	-3146	-1055
112	SEG ₂₈	-3066	-1055
113	SEG ₂₉	-2986	-1055
114	SEG ₃₀	-2906	-1055
115	SEG ₃₁	-2826	-1055
116	SEG ₃₂	-2746	-1055
117	SEG ₃₃	-2666	-1055
118	SEG ₃₄	-2586	-1055
119	SEG ₃₅	-2506	-1055
120	SEG ₃₆	-2426	-1055
121	SEG ₃₇	-2346	-1055
122	SEG ₃₈	-2266	-1055
123	SEG ₃₉	-2186	-1055
124	SEG ₄₀	-2106	-1055
125	SEG ₄₁	-2026	-1055
126	SEG ₄₂	-1946	-1055
127	SEG ₄₃	-1866	-1055
128	SEG ₄₄	-1786	-1055
129	SEG ₄₅	-1706	-1055
130	SEG ₄₆	-1626	-1055
131	SEG ₄₇	-1546	-1055
132	SEG ₄₈	-1466	-1055
133	SEG ₄₉	-1386	-1055
134	SEG ₅₀	-1306	-1055
135	SEG ₅₁	-1226	-1055
136	SEG ₅₂	-1146	-1055
137	SEG ₅₃	-1066	-1055
138	SEG ₅₄	-986	-1055
139	SEG ₅₅	-906	-1055
140	SEG ₅₆	-826	-1055
141	SEG ₅₇	-746	-1055
142	SEG ₅₈	-666	-1055
143	SEG ₅₉	-586	-1055
144	SEG ₆₀	-506	-1055
145	SEG ₆₁	-426	-1055
146	SEG ₆₂	-346	-1055
147	SEG ₆₃	-266	-1055
148	SEG ₆₄	-186	-1055
149	SEG ₆₅	-106	-1055
150	SEG ₆₆	-26	-1055

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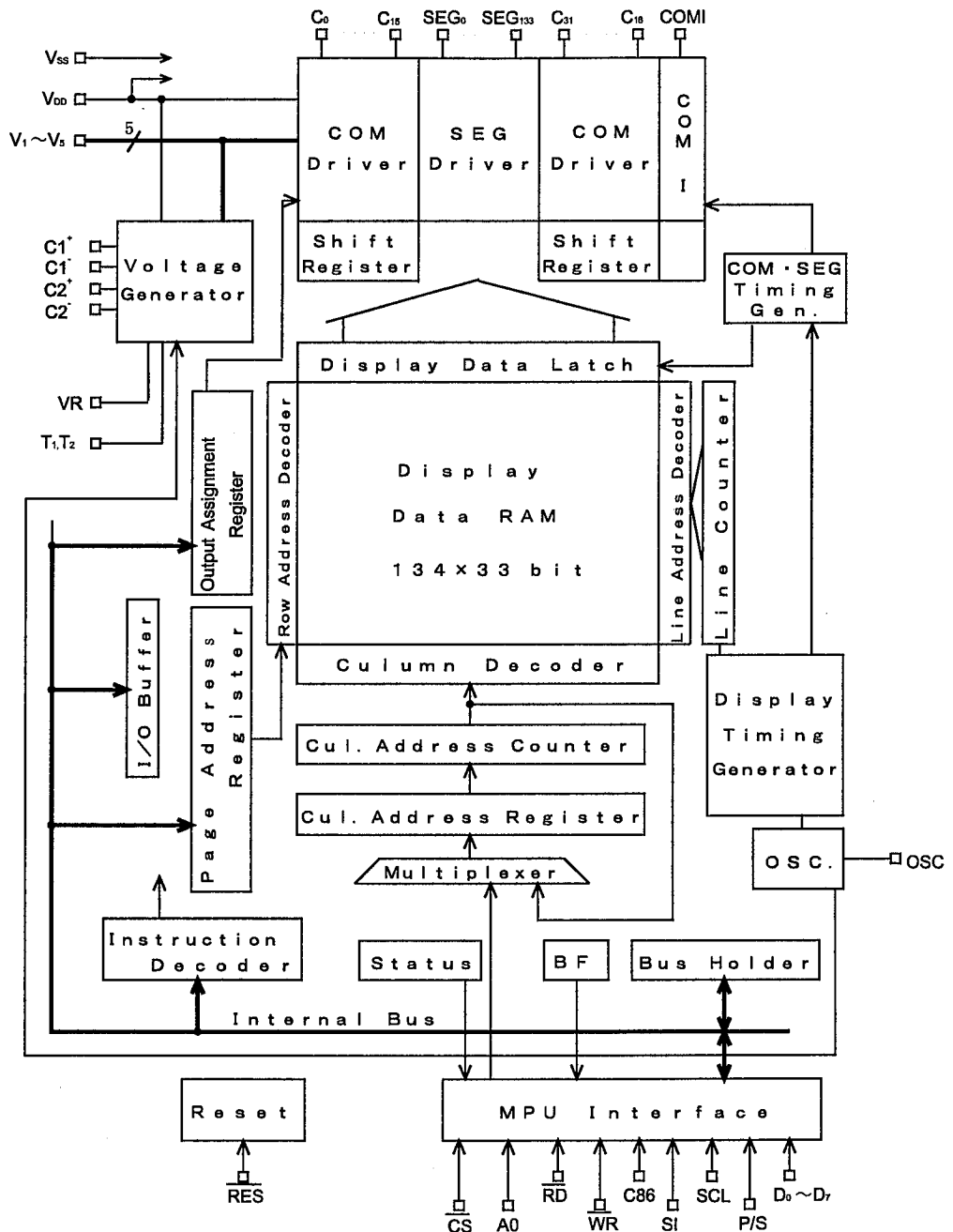


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No.	Terminal	X= μ m	Y= μ m
151	SEG ₆₇	54	-1055
152	SEG ₆₈	134	-1055
153	SEG ₆₉	214	-1055
154	SEG ₇₀	294	-1055
155	SEG ₇₁	374	-1055
156	SEG ₇₂	454	-1055
157	SEG ₇₃	534	-1055
158	SEG ₇₄	614	-1055
159	SEG ₇₅	694	-1055
160	SEG ₇₆	774	-1055
161	SEG ₇₇	854	-1055
162	SEG ₇₈	934	-1055
163	SEG ₇₉	1014	-1055
164	SEG ₈₀	1094	-1055
165	SEG ₈₁	1174	-1055
166	SEG ₈₂	1254	-1055
167	SEG ₈₃	1334	-1055
168	SEG ₈₄	1414	-1055
169	SEG ₈₅	1494	-1055
170	SEG ₈₆	1574	-1055
171	SEG ₈₇	1654	-1055
172	SEG ₈₈	1734	-1055
173	SEG ₈₉	1814	-1055
174	SEG ₉₀	1894	-1055
175	SEG ₉₁	1974	-1055
176	SEG ₉₂	2054	-1055
177	SEG ₉₃	2134	-1055
178	SEG ₉₄	2214	-1055
179	SEG ₉₅	2294	-1055
180	SEG ₉₆	2374	-1055
181	SEG ₉₇	2454	-1055
182	SEG ₉₈	2534	-1055
183	SEG ₉₉	2614	-1055
184	SEG ₁₀₀	2694	-1055
185	SEG ₁₀₁	2774	-1055
186	SEG ₁₀₂	2854	-1055
187	SEG ₁₀₃	2934	-1055
188	SEG ₁₀₄	3014	-1055
189	SEG ₁₀₅	3094	-1055
190	SEG ₁₀₆	3174	-1055
191	SEG ₁₀₇	3254	-1055
192	SEG ₁₀₈	3334	-1055
193	SEG ₁₀₉	3414	-1055
194	SEG ₁₁₀	3494	-1055
195	SEG ₁₁₁	3574	-1055
196	SEG ₁₁₂	3654	-1055
197	SEG ₁₁₃	3734	-1055
198	SEG ₁₁₄	3814	-1055
199	SEG ₁₁₅	3894	-1055

No.	Terminal	X= μ m	Y= μ m
200	SEG ₁₁₆	3974	-1055
201	SEG ₁₁₇	4054	-1055
202	SEG ₁₁₈	4134	-1055
203	SEG ₁₁₉	4214	-1055
204	SEG ₁₂₀	4294	-1055
205	SEG ₁₂₁	4374	-1055
206	SEG ₁₂₂	4454	-1055
207	SEG ₁₂₃	4534	-1055
208	SEG ₁₂₄	4614	-1055
209	SEG ₁₂₅	4694	-1055
210	SEG ₁₂₆	4774	-1055
211	SEG ₁₂₇	4854	-1055
212	SEG ₁₂₈	4934	-1055
213	SEG ₁₂₉	5014	-1055
214	SEG ₁₃₀	5094	-1055
215	SEG ₁₃₁	5174	-1055
216	SEG ₁₃₂	5254	-1055
217	SEG ₁₃₃	5334	-1055
218	NC	5462	-1055
219	NC	5583	-913
220	NC	5583	-777
221	NC	5583	-641
222	C ₃₁	5583	-505
223	C ₃₀	5583	-425
224	C ₂₉	5583	-345
225	C ₂₈	5583	-265
226	C ₂₇	5583	-185
227	C ₂₆	5583	-105
228	C ₂₅	5583	-25
229	C ₂₄	5583	56
230	C ₂₃	5583	136
231	C ₂₂	5583	216
232	C ₂₁	5583	296
233	C ₂₀	5583	376
234	C ₁₉	5583	456
235	C ₁₈	5583	536
236	C ₁₇	5583	616
237	C ₁₆	5583	696
238	COM1	5583	776
239	RES	5583	856
ALIGNMENT	A1	5592	1080
ALIGNMENT	A2	-5593	1080
ALIGNMENT	B1	-5593	-1061
ALIGNMENT	B2	5592	-1061

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■ TERMINAL DESCRIPTION

No.	Symbol	I/O	F u n c t i o n																				
1,2,3,44,45,46	V _{DD}	Power	V _{DD} =+5V. (Less than 4.5V should apply when voltage tripler using.)																				
6,7,8,26,27,28	V _{SS}	GND	V _{SS} =0V																				
62,63 59,60,61 56,57,58 53,54,55 50,51,52	V ₁ V ₂ V ₃ V ₄ V ₅	Power	<p>LCD Driving Voltage Supplying Terminal. When the internal voltage tripler is not used, supply each level of LCD driving voltage from outside with following relation.</p> $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ <p>When the internal power supply is on, the internal circuits generate and supply following LCD bias voltage from V₁ to V₄ terminals.</p> <table><tr><td>Term.</td><td>V₁</td><td>V₂</td><td>V₃</td><td>V₄</td></tr><tr><td>Volt.</td><td>V₅+6/7V_{LCD}</td><td>V₅+5/7V_{LCD}</td><td>V₅+2/7V_{LCD}</td><td>V₅+1/7V_{LCD}</td></tr></table> <p style="text-align: right;">(V_{LCD}=V_{DD}-V₅)</p>	Term.	V ₁	V ₂	V ₃	V ₄	Volt.	V ₅ +6/7V _{LCD}	V ₅ +5/7V _{LCD}	V ₅ +2/7V _{LCD}	V ₅ +1/7V _{LCD}										
Term.	V ₁	V ₂	V ₃	V ₄																			
Volt.	V ₅ +6/7V _{LCD}	V ₅ +5/7V _{LCD}	V ₅ +2/7V _{LCD}	V ₅ +1/7V _{LCD}																			
29,30,31 32,33,34 35,36,37 38,39,40	C1 ⁺ C1 ⁻ C2 ⁺ C2 ⁻	O	<p>Step up capacitor connecting terminals.</p> <p>In case of tripler operation, connect the capacitor between C1⁺ and C1⁻, C2⁺ and C2⁻.</p> <p>In case of doubler operation, connect the capacitor between C2⁺ and C2⁻, connect C2⁺ to C1⁺, and C1⁻ should be open.</p>																				
41,42,43	V _{OUT}	O	Step up voltage output terminal. Connect the set up capacitor between this terminal and V _{SS} .																				
47,48,49	VR	I	Voltage adjust terminal. V ₅ level is adjusted by external bleeder resistance connecting between V _{DD} and V5 terminal.																				
10 9	T ₁ T ₂	I	<p>LCD bias voltage control terminals. ※ Don't Care</p> <table><tr><td>T₁</td><td>T₂</td><td>Step up cir.</td><td>Voltage Adj.</td><td>V/F Cir.</td></tr><tr><td>L</td><td>※</td><td>Available</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr><tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr></table>	T ₁	T ₂	Step up cir.	Voltage Adj.	V/F Cir.	L	※	Available	Available	Available	H	L	Not Avail.	Available	Available	H	H	Not Avail.	Not Avail.	Available
T ₁	T ₂	Step up cir.	Voltage Adj.	V/F Cir.																			
L	※	Available	Available	Available																			
H	L	Not Avail.	Available	Available																			
H	H	Not Avail.	Not Avail.	Available																			
18 to 25	D ₀ to D ₇	I/O	Tri-state bi-directional Data I/O terminal in 8-bit parallel operation.																				
15	A0	I	<p>Connect to the Address bus of MPU. The data on the D₀ to D₇ is distinguished between Display data and Instruction by status of A0.</p> <table><tr><td>A0</td><td>H</td><td>L</td></tr><tr><td>Dist.</td><td>Display Data</td><td>Instruction</td></tr></table>	A0	H	L	Dist.	Display Data	Instruction														
A0	H	L																					
Dist.	Display Data	Instruction																					
239	$\overline{\text{RES}}$	I	Reset terminal. When the $\overline{\text{RES}}$ terminal goes to "L", the initialization is performed. Reset operation is executing during "L" state of RES.																				
14	$\overline{\text{CS}}$	I	Chip select terminal. Data Input/Output are available during $\overline{\text{CS}}$ ="L".																				
17	$\overline{\text{RD}}$ (E)	I	<p><In case of interface with 80 type MPU></p> <p>$\overline{\text{RD}}$ signal of 80 type MPU input terminal. Active "L".</p> <p>During this signal is "L", D₀ to D₇ terminals are output.</p> <p><In case of 68 type MPU></p> <p>Enable signal of 68 type MPU input terminal. Active "H".</p>																				

No.	Symbol	I/O	F u n c t i o n																		
16	\overline{WR} (R/W)	I	<p><In case of with 80 type MPU> Connect to the 80 type MPU \overline{WR} signal. Active "L". The data on the data bus input synchronizing the rise edge of this signal.</p> <p><In case of with 68 type MPU> Read/write control signal of 68 type MPU input terminal.</p> <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Read</td><td>Write</td></tr></table>	R/W	H	L	State	Read	Write												
R/W	H	L																			
State	Read	Write																			
5	C86	I	<p>MPU interface type terminal.</p> <table><tr><td>C86</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>68 Type</td><td>80 Type</td></tr></table>	C86	H	L	Status	68 Type	80 Type												
C86	H	L																			
Status	68 Type	80 Type																			
13	SI	I	Serial data input terminal .																		
12	SCL	I	Serial data clock signal input terminal. SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.																		
4	P/S	I	<p>Serial or parallel interface selection terminal.</p> <table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial CLK</td></tr><tr><td>"H"</td><td>\overline{CS}</td><td>A0</td><td>D₀ to D₇</td><td>\overline{RD} , \overline{WR}</td><td>—</td></tr><tr><td>"L"</td><td>\overline{CS}</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr></table> <p>*RAM data and status read operation do not work in mode of the serial interface.</p> <ul style="list-style-type: none">• In case of the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L".• In case of the serial interface (P/S="L"), \overline{RD} and \overline{WR} must be fixed. "H" or "L", and D₀ to D₇ are high impedance state.	P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK	"H"	\overline{CS}	A0	D ₀ to D ₇	\overline{RD} , \overline{WR}	—	"L"	\overline{CS}	A0	SI	Write only	SCL
P/S	Chip Select	Data/Command	Data	Read/Write	Serial CLK																
"H"	\overline{CS}	A0	D ₀ to D ₇	\overline{RD} , \overline{WR}	—																
"L"	\overline{CS}	A0	SI	Write only	SCL																
11	OSC	I	System clock input terminal for Maker testing. (This terminal should be open.)																		

No.	Symbol	I/O	F u n c t i o n																																	
64 to 79	C ₀ to C ₁₅	O	LCD driving signal output terminals. Segment output terminals : SEG ₀ to SEG ₁₃₃ Common output terminals :C ₀ to C ₃₂ • Segment output terminal The following output voltage are selected by the combination of FR and data in the RAM. <table><tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr><tr><th>Normal</th><th>Reverse</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V₂</td></tr><tr><td>L</td><td>V₅</td><td>V₃</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V₂</td><td>V_{DD}</td></tr><tr><td>L</td><td>V₃</td><td>V₅</td></tr></table> • Common Output Terminal The following output voltage are selected by the combination of FR and status of common. <table><tr><th>Scan data</th><th>FR</th><th>Output Voltage</th></tr><tr><td rowspan="2">H</td><td>H</td><td>V₅</td></tr><tr><td>L</td><td>V_{DD}</td></tr><tr><td rowspan="2">L</td><td>H</td><td>V₁</td></tr><tr><td>L</td><td>V₄</td></tr></table>	RAM Data	FR	Output Voltage		Normal	Reverse	H	H	V _{DD}	V ₂	L	V ₅	V ₃	L	H	V ₂	V _{DD}	L	V ₃	V ₅	Scan data	FR	Output Voltage	H	H	V ₅	L	V _{DD}	L	H	V ₁	L	V ₄
RAM Data	FR					Output Voltage																														
				Normal	Reverse																															
H	H	V _{DD}	V ₂																																	
	L	V ₅	V ₃																																	
L	H	V ₂	V _{DD}																																	
	L	V ₃	V ₅																																	
Scan data	FR	Output Voltage																																		
H	H	V ₅																																		
	L	V _{DD}																																		
L	H	V ₁																																		
	L	V ₄																																		
84 to 217	SEG ₀ to SEG ₁₃₃																																			
222 to 237	C ₃₁ to C ₁₆																																			
238	COMI	O	Icon common output terminal. Icon common output when Icon Display instruction execution. <table><tr><td></td><td>Icon Display ON</td><td>Icon Display OFF</td></tr><tr><td>State</td><td>COM₃₂</td><td>V₁ or V₄</td></tr></table>		Icon Display ON	Icon Display OFF	State	COM ₃₂	V ₁ or V ₄																											
	Icon Display ON	Icon Display OFF																																		
State	COM ₃₂	V ₁ or V ₄																																		

(Terminals 80,81,82,83,218,219,220,221 are NC)

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

While D_6 to D_7 the internal circuits are operating, the busy flag(BF) is "1", and any instruction excepting for the status read are inhibited .

The busy goes to "1" from D_7 terminal when status read instruction is executed.

When enough cycle time over than t_{CYC} indicated in "BUS TIMING CHARACTERISTICS" is ensured, no need to check the busy flag for reduction of the MPU loads.

(1-2) Line Counter

The Line Counter generates the line address of display data RAM by the count up operation synchronizing the common cycle after the reset operation at the status change of internal FR signal.

(1-3) Column Address Counter

The column address counter is 8-bit pre-settable counter addressing the column address of display data RAM as shown in Fig. 1. It is incremented (+1) up to $(A0)_H$ by the Display Data Read/Write instruction execution. It stops the count up operation at $(A0)_H$, and it does not count up non existing address area over than $(A0)_H$ by the count lock function. This count lock is released by new column address set.

The column address counter is independent of the Page Register.

By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM corresponding to the Segment Driver.

(1-4) Page Register

The page register gives a page address of Display Data RAM as shown in Fig. 1. When the MPU accesses the data with the page change, the page address set instruction is required.

Page address "4"(D_2 ="H" and D_1 ="L") is Icon RAM area, the data only for the D_0 is valid.

(1-5) Display Data RAM

Display Data RAM is the bit map RAM consisting of 4,422 bits to memorize the display data corresponding to each pixel of LCD panel. The each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by following bit data.

When Normal Display : On="1" , Off="0"

When Inverse Display : On="0" , Off="1"

The Display Data RAM outputs 134-bit parallel data in the area addressed by the line counter, and these data are set into the Display Data Latch.

The access operation from MPU to the display data RAM and the data output from the display data RAM are so controlled operate independently that the data rewriting does not influence with any malfunctions to the display.

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.

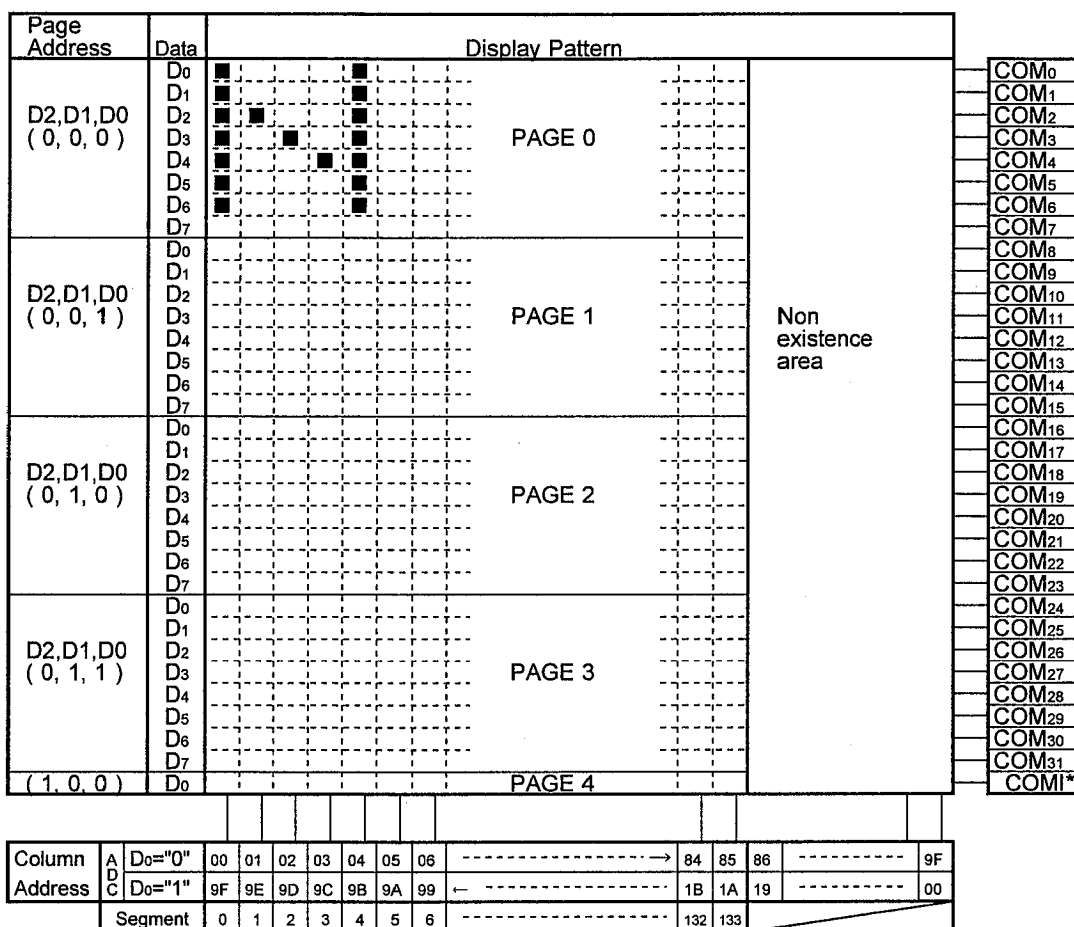


Fig.1 Correspondence with Display Data RAM and Address
(COMI can be used in case of 1/33 duty set.)

* When readout the Display Data RAM address 86H to 9FH in normal ADC or 00H to 19H in inverse ADC the data FFH is output as those address data.

(1-6) Common Driver Assignment

The scanning order can be assigned by setting A₃ of the Output Assignment Register as shown Table 1.

Table 1

Register		COM Output Terminals			
A ₃	PAD No.	64		222	
	Pin name	79		237	
		C ₀	C ₁₅	C ₃₁	C ₄₆
0	→	COM ₁₅	←-----→ COM ₀	COM ₁₆	-----→ COM ₃₁
1	→	COM ₁₆	-----→ COM ₃₁	COM ₁₅	←-----→ COM ₀

The Icon display is regardless with this function, therefore the Icon Display instruction must be executed when the Icon display is needed. In this time, the Icon display driver COM_I is fixed to COM₃₂ timing regardless the other Common Driver assignment.

(1-7) Reset Circuit

Reset circuit operates the following initializations when the condition of $\overline{\text{RES}}$ terminal goes to "L" level.

Initialization

- ① Display Off
- ② Normal Display(Non-inverse display)
- ③ Icon Display Reset
- ④ ADC Select : Normal (ADC Instruction D₀="0")
- ⑤ Read Modify Write Mode Off
- ⑥ Internal Power supply(Step up) circuits Off
- ⑦ Clear the serial interface register
- ⑧ Set the address (00)_H to the Column Address Counter
- ⑨ Set the page "0" to the Page Address Register
- ⑩ Select the D₃ of the Output Assignment Register to "0"
- ⑪ Set the EVR register to (00)_H

The $\overline{\text{RES}}$ terminal should be connected to the Reset terminal of MPU for the initialization at the mean time with MPU as shown "MPU Interface Example". The period of reset signal requires over than 10us RES="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{\text{RES}}$ signal, the operation goes to normal.

When the internal LCD power supply is not used, the external LCD power supply into the NJU6575A must be turned on during $\overline{\text{RES}}$ ="L". Although the condition of $\overline{\text{RES}}$ ="L" clear each registers and initialize as above, the oscillation circuit and the output terminal conditions (D₀ to D₇) are not influenced. The initialization must be performed using $\overline{\text{RES}}$ terminal at the power on, to prevent hung up or any incorrect operations. The reset Instruction performs the initialization procedures from No.8 to No.11 as shown in above.

NOTE) The noise into the $\overline{\text{RES}}$ terminal should be eliminated to avoid the error on the application with the careful design.

(1-8) LCD Driving

(a) LCD Driving Circuits

LCD driving circuits are consisted of 167 multiplexers which operate as 134 Segment drivers and 32 Common drivers and 1 Icon common driver. 33 Common drivers with the shift register which the common display signal. The combination of the Display data, COM scan signal and FR signal forms the LCD driving output voltage. The output wave form is shown in the Fig. 7.

(b) Display Data Latch Circuits

Display Data Latch stores 134-bit display data temporarily which is output to LCD driver circuits at a common cycle from Display Data RAM addressed by Line Counter. The instructions of Display On/Off, Display inverse ON/OFF and static Drive On/Off control only the data in Display Data Latch, therefore the data in the Display Data RAM is not changed.

(c) Line Counter and Latch signal of Latch Circuits

The clock to Line Counter and latch signal to the Latch Circuits are generated from the internal display clock(CL). The line address of Display Data RAM is renewed synchronizing with display clock(CL). 134 bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator

Display timing Generator generates the timing signal for the display system by combination of the master clock CL and Driving Signal FR (refer to Fig.2). The Frame Signal FR and LCD alternative signal generate LCD driving waveform of the two frame alternative driving method.

(e) Common Timing Generation

The common timing is generated by display clock CL (refer to Fig.2).

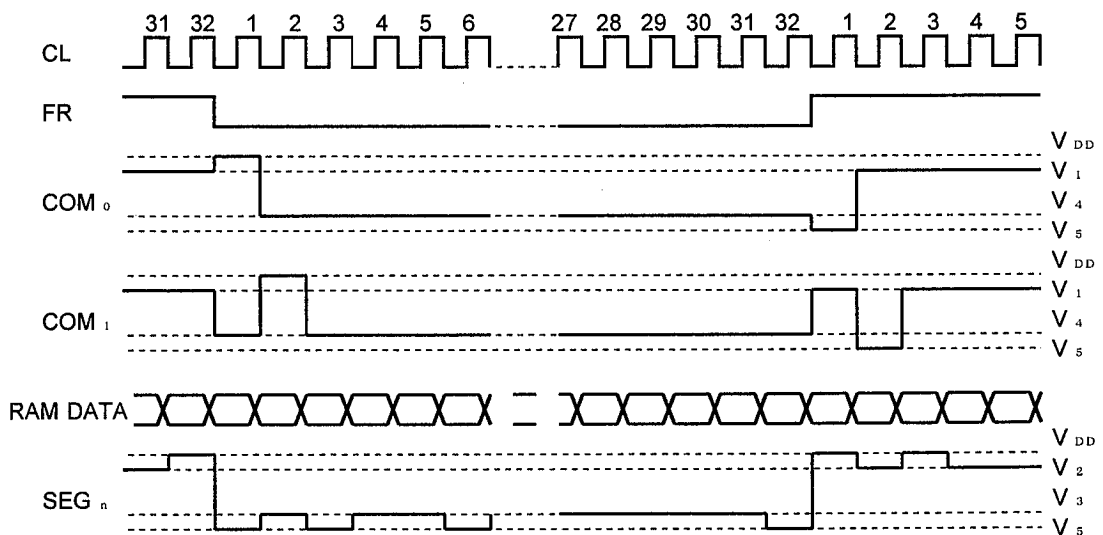


Fig. 2 Waveform of Display Timing

(f) Oscillation Circuit

The Oscillation Circuit is a low power CR oscillator incorporating with a Resistor and a Capacitor. It generates clocks for display timing signal source and voltage Step up circuits for LCD driving. The oscillation circuit output frequency is divided by 4 which is used as display clock CL.

(g) Power Supply Circuit

Internal Power Supply Circuit generate the High voltage and Bias voltage for the LCD. The power Supply Circuit consists of Step up(Tripler or Doubler) Circuits, Regulator Circuits, and Voltage Followers. The internal Power Supply is designed for small size LCD panel, therefore it is not suitable for the large size LCD panel application. If the contrast is not good in the large size LCD panel application, please supply the external.

The suitable values of the capacitors connecting to the V1 to V5 terminals and the step up circuit. And the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption with the LCD panel is depending on the display pattern. Please evaluate with actual LCD module.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1 , V_2 , V_3 , V_4 , and V_5 for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminal. Furthermore The external power supply operates with some of internal power supply function.

Table 3.

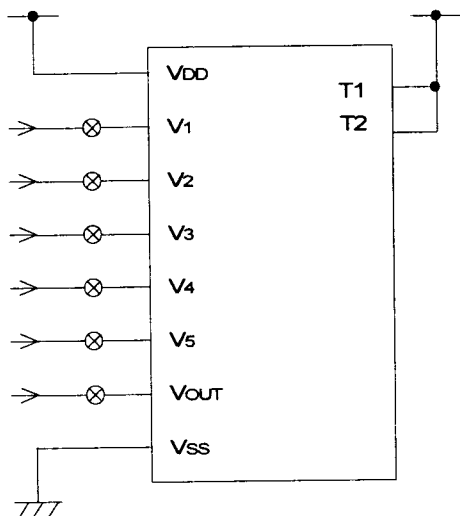
(*:Don't Care)

T_1	T_2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	$C1^+$, $C1^-$, $C2^+$, $C2^-$	VR Term.
L	*	○	○	○	-		
H	L	x	○	○	V_{OUT}	OPEN	
H	H	x	x	○	V_S , V_{OUT}	OPEN	OPEN

When (T_1 , T_2)=(H, L), $C1^+$, $C1^-$, $C2^+$, $C2^-$ terminals for step up circuits are open because the step up circuits doesn't operate. Therefore LCD driving voltage to the V_{OUT} terminal should be supplied from outside. When (T_1 , T_2)=(H, H), terminals for step up circuits and VR are open, because the step up circuits and Voltage adjust circuits do not operate.

○ Power Supply applications

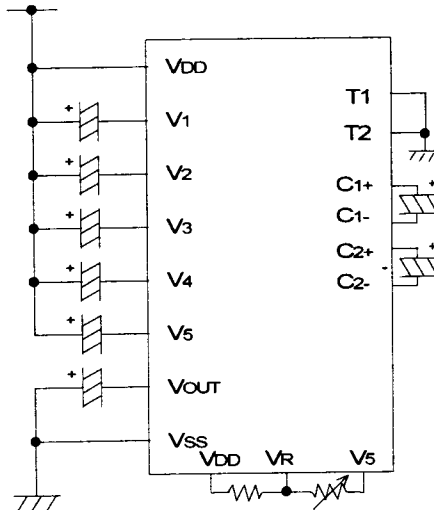
(1) External power supply operation.



(2) Internal power supply operation.

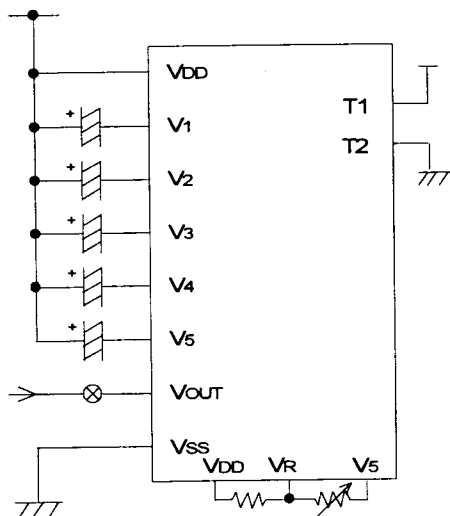
(Voltage Booster, Voltage Adj., Buffer(V/F))

Internal power supply ON (instruction) (T1,T2)=(L,L)



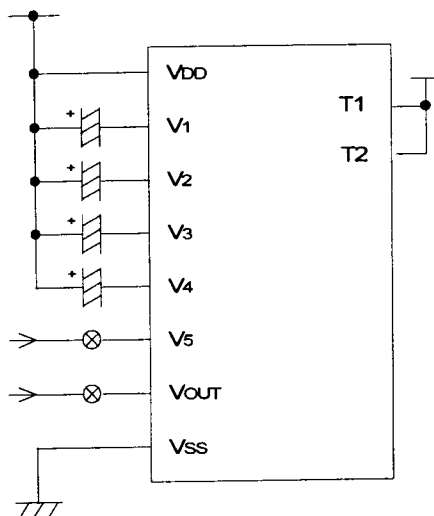
(3) External power supply operation with Voltage Adjustment, Buffer(V/F)

Internal power supply ON (Instruction) (T1,T2) = (H,L)



(4) External power supply operation adjusted Voltage to V5.

Internal power supply ON (Instruction) (T1,T2) =(H,H)



* ⊗ : These switches should be open during the power save mode.

(2) Instruction

The NJU6575A distinguishes the signal on the data bus by combination of $A0$, \overline{RD} and \overline{WR} . The decode of the instruction and execution performs only depend on the internal timing only neither the external clock. In case of serial interface, the data input as MSB first serially.

The Table. 4 shows the instruction codes of the NJU6575A.

Table 4. Instruction Code

Instruction		Code											Description
		A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0	LCD Display ON/OFF 0:OFF 1:ON
(2)	Page Address Set	0	1	0	1	0	1	1	*	Page Address			Set the page of DD RAM to the Page Add. Register
(3)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
(4)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(5)	Status Read	0	0	1	Status			0	0	0	0	0	Read out the internal Status
(6)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(7)	Read Display Data	1	0	1	Read Data								Read the Data from the Display Data RAM
(8)	ADC Select	0	1	0	1	0	1	0	0	0	0	0	Set the DD RAM vs Segment 0:Normal 1:Inverse
(9)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0	Inverse the On and Off Display 0:Normal 1:Inverse
(10)	Whole Display On /Normal Display	0	1	0	1	0	1	0	0	1	0	0	Whole Display Turns On 0:Normal 1:Whole Disp. On
(11)	Icon Display	0	1	0	1	0	1	0	1	0	1	0	Set the Duty Ratio 0:No Icon 1:With Icon
(12)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(15)	Output Assignment Register Set	0	1	0	1	1	0	0	A ₃	*	*	*	Set the scanning order of common drivers to the Register
(16)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0	0:Int. Power Supply Off 1:Int. Power Supply On
(17)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal(external) power supply is turned on
(18)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V _s output level to the EVR register
(19)	Power Save (Dual Command)	0	1	0	1	0	1	0	1	1	1	0	Set the Power save Mode
		0	1	0	1	0	1	0	0	1	0	1	

(*:Don't Care)

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

A0	\overline{RD}	\overline{WR}	D ₇ _____							D ₀
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off

1: Display On

(b) Page Address Set

When MPU accesses the Display Data RAM, the page address must be selected before the data writing. The access to the Display Data RAM is available by the page and column address set(Refer the Fig. 1.). The page address change does not influence with the display. Page 4 is a Icon display data area which available only for the D₀.

A0	\overline{RD}	\overline{WR}	D ₇ _____							D ₀
0	1	0	1	0	1	1	*	A ₂	A ₁	A ₀

(*:Don't Care)

A ₂	A ₁	A ₀	Page
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

(c) Column Address

When MPU accesses the Display Data RAM, the page address (refer(b)) and column address set are required before the data writing. The column address set requires twice address set which are higher order 4 bits address set and lower-order 4 bits. When the MPU accesses the Display Data RAM sequentially, the column address is increase one by one automatically, therefore, the MPU can access only the data sequentially without address set.

After writing 1page data ,page address setting is required due to page address doesn't increase automatically the increment of the column address is stopped at the address of (A0)_H automatically, and the page address is not changed even if the column address increase to (A0)_H and stop. In this time the page address is not changed.

	A0	\overline{RD}	R/W WR	D ₇				D ₀			
Higher Order	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower Order	0	1	0	0	0	0	0	A3	A2	A1	A0
	A7	A6	A5	A4	A3	A2	A1	A0	Column Address		
	0	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	1	1		
		
	1	0	1	0	0	0	0	0	A0		

(d) Status Read

This instruction reads out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	\overline{RD}	R/W WR	D ₇				D ₀			
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.

The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.

0 : Counterclockwise Output(Inverse) Column Address 133-n \longleftrightarrow Segment Driver n

1 : Clockwise Output (Normal) Column Address n \longleftrightarrow Segment Driver n

(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.

0 : Whole Display "On"

1 : Whole Display "Off"

(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initializing by \overline{RES} signal or reset instruction.

0 : —

1 : Initialization Period

(e) Write Display Data

This instruction writes the 8-bit data on the data bus into the Display Data RAM. The column address increases "1" automatically after data writing, therefore, the MPU can write the 8-bit data into the Display Data RAM continuously without any address setting after the start address setting.

		R/W		D ₇ _____ D ₀							
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$									
1	1	0		WRITE DATA							

(f) Read Display Data

This instruction reads out the 8-bit data from Display Data RAM addressed by the column and page address. The column address increase "1" automatically after data reading out, therefore, the MPU can read out the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy read must operate after column address set as the explanation in "(5-5) Access to the Display Data RAM and Internal Register". In the serial interface mode, the display data is not read out.

		R/W		D ₇ _____ D ₀							
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$									
1	0	1		READ DATA							

(g) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

		R/W		D ₇ _____ D ₀							
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$									
0	1	0		1	0	1	0	0	0	0	D

D 0: Clockwise Output (Normal)

1: Counterclockwise Output (Inverse)

(h) Normal or Inverse On/Off Set

This instruction changes the condition of display turn on and off as normal or inverse. The contents of Display Data RAM is not changed by this instruction execution.

		R/W		D ₇ _____ D ₀							
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$									
0	1	0		1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"

1: Inverse RAM data "0" correspond to "On"

(i) Whole Display On

This instruction turns on the all pixels independent of the contents of the Display Data RAM. In this time, the contents of Display Data RAM is not changed and kept. This instruction takes precedence over the "Normal or Inverse On/Off Set Instruction".

		R/W		D ₇ _____ D ₀							
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$									
0	1	0		1	0	1	0	0	1	0	D

D 0: Normal Display

1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits go to the power save mode(refer to the (s) Power Save) .

(j) Icon Display

This instruction set the 1/33 duty for the Icon Display. The COM1 terminal operate as COM₃₂ and output the icon display data stored in D₀ of Display Data RAM page 4 (refer to the Fig. 1).

A0	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	1	0	1	D

D 0: 1/32 Duty
1: 1/33 Duty

(k) Read Modify Write

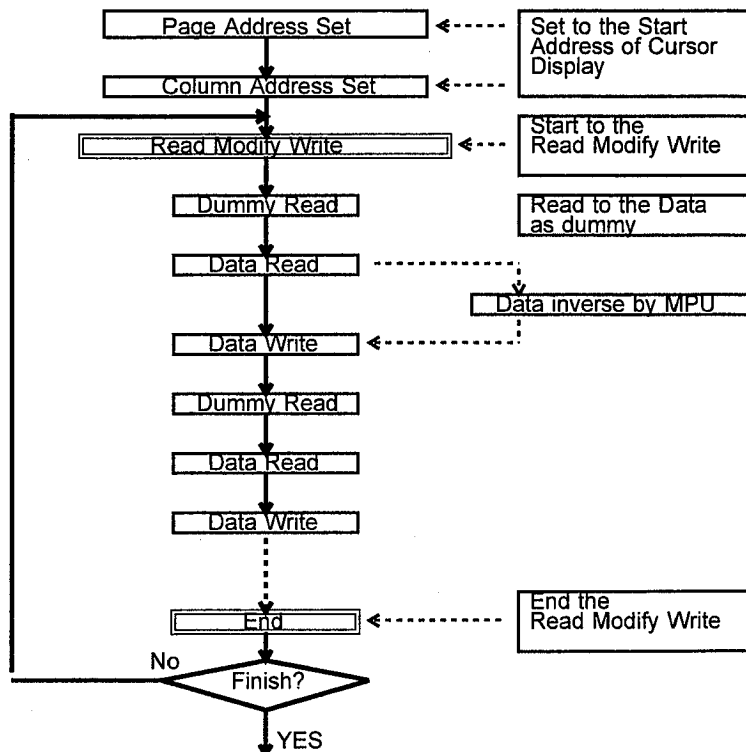
This instruction sets the Read Modify Write Mode for the column address increment control. In mode of the Read Modify, Write the column address increases "1" automatically when the Display Data Write Instruction is executed, but the address does not change when the Display Data Read Instruction is executed. This status is continued until End instruction execution. When the End instruction is input, the column address goes back to the start address before the Read Modify Write instruction input. This function reduces the load of MPU for repeating the display data change in the fixed area(ex. cursor blink).

the read modify write mode setting.

A0	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	0	0	0	0

Note) In mode of the Read Modify Write mode, any instructions except for Column Address Set can be execute.

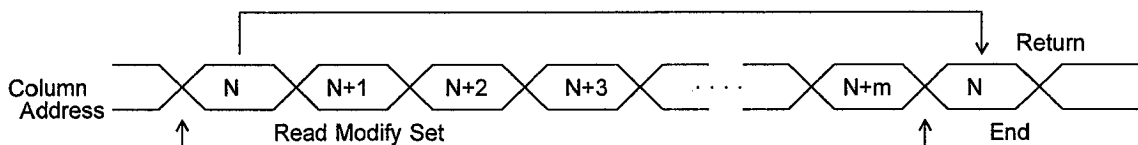
(l) Sequence of cursor blink display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

A0	\overline{RD}	R/W WR	D ₇					D ₀
0	1	0	1	1	1	0	1	1



(n) Reset

This instruction executes the following initialization.

Initialization

- ① Set the Address (00)_H into the Column Address Counter.
- ② Set the page "0" into the Page Address Register.
- ③ Select the D3 of the Output Assignment Register to "0".
- ④ Set 0 to the EVR Register to (00)_H.

In this time, the Display Data RAM is not influenced.

A0	\overline{RD}	R/W WR	D ₇					D ₀
0	1	0	1	1	1	0	0	0

The reset signal input to the \overline{RES} terminal (hardware reset) must be input for the power on initialization. Reset instruction does not perform completely in stead of hardware reset using the \overline{RES} terminal.

(o) Output Assignment Register

This instruction sets the common driver scanning order .

A0	\overline{RD}	R/W WR	D ₇					D ₀
0	1	0	1	1	0	0	A3	*

(*:Don't Care)

A3: Set the scanning order .(Refer to 1-6)

(p) Internal Power Supply

This instruction set the condition Of internal Power Supply On/Off. Voltage Booster circuits, Voltage Regulator and Voltage Follower operate at On. To operate the voltage booster circuits, the oscillation circuits must be operating.

A0	\overline{RD}	R/W WR	D ₇					D ₀
0	1	0	0	0	1	0	0	D

D 0: Internal Power Supply Off

1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

(q) LCD Driving Voltage Set

This instruction controls LCD driving waveform output through the COM/SEG terminals.

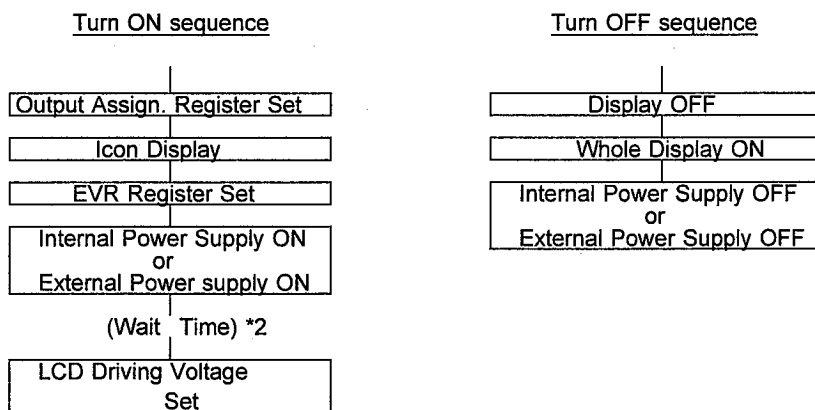
A0	$\overline{\text{RD}}$	$\overline{\text{WR}}$	D ₇ _____ D ₀							
0	1	0	1	1	1	0	1	1	0	1

NJU6575A contains low power LCD driving voltage generator circuit reducing own operation current. Therefore, it requires the following sequence procedures at power on for the power source stabilized operation.

● LCD driving power supply ON/OFF sequences

The following sequences are required when the power supply is tuned on/of.

When the power supply is tuned on again after the turn off (by the power save instruction), the power save release sequence (s) ((3-21)Power Save) is required.

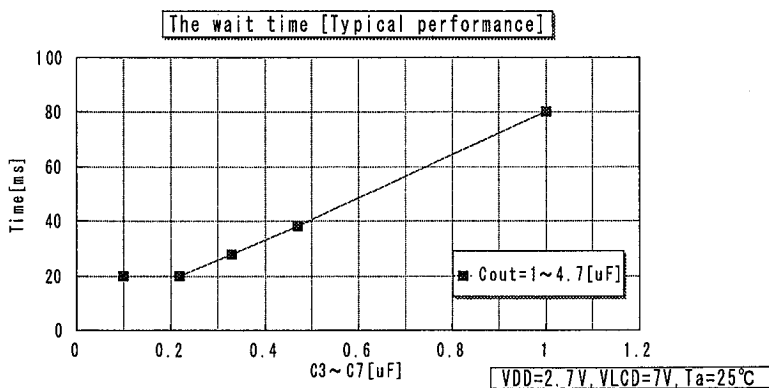


*1 This instruction is required in both cases of the internal and external power supply.

Until "LCD driving voltage Set" execution, NJU6575A operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously.

*2 The wait time depends on the C_3 to C_7 , C_{OUT} capacitors(refer(4) (d)Fig.4), V_{DD} and V_{LCD} voltage.

Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the following graph.)



(r) EVR Register Set

This instruction controls voltage adjustment circuits of internal LCD power supply and changes LCD driving voltage "V_s". Finally, it adjusts the contrast of LCD display. By setting a data into EVR register. V5 output voltage selects one condition out of 16-voltage conditions. The range of V_s voltage is adjusted by setting external resistors as mentioned in "(4) (b) Voltage Adjust Circuits".

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	0	0	A3	A2	A1	A0

A3	A2	A1	A0	V _{LCD}
0	0	0	0	Low
		:		:
		:		:
1	1	1	1	High

$$V_{LCD} = V_{DD} - V_s$$

When EVR doesn't use, set the EVR register to (0,0,0,0).

(s) Power Save(Dual Command)

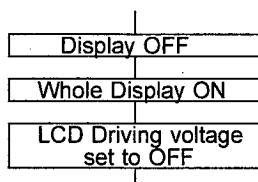
When both of Display Off and Whole Display On are executed, the internal circuits go to the power save mode and the operating current is reduced as same as the stand by current.

The internal status in the Power Save Mode is shown in follows;

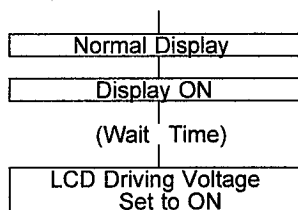
- ① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
- ② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
- ③ Keep the display data and operating mode just before the power save mode.
- ④ All of LCD driving bias voltage fix to the V_{DD} level.

The power save and its release perform according to the following sequences.

Power Save Sequence



Power Save Release Sequence

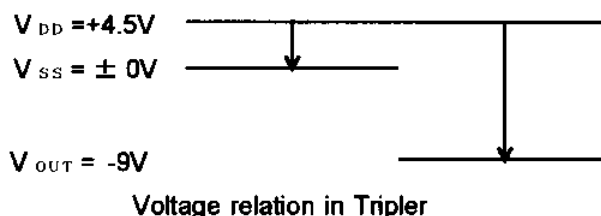
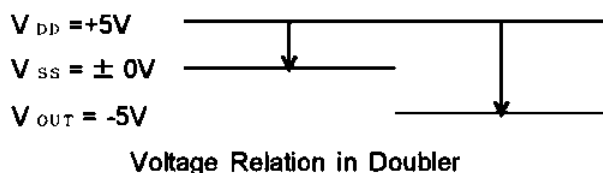


- *1 In the power save sequence, the power save mode is started after the second instruction "whole Display ON".
- *2 In the power save release sequence, the power save mode is released after the Normal Display instruction (Whole display OFF).
The instruction of display ON is input at any timing after the instruction of normal display in power save release sequence.
- *3 Until "LCD driving voltage set to ON" execution, NJU6575A operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously.
- *4 In case of external power supply for LCD driving, it should be turned off and made condition like as disconnection or connected to V_{DD} before the power save mode or at the same time. In this time, V_{OUT} terminal should be made condition like as disconnection or connect to the lowest voltage of the system(V_s level from the external power supply).

(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage (V_{DD} common) of the voltage $V_{DD} - V_{SS}$ is output from V_{OUT} terminal when connecting three capacitor between $C1^+$ and $C1^-$, $C2^+$ and $C2^-$, V_{SS} and V_{OUT} . In case of the voltage doubler operation, connecting the two capacitors between $C2^+$ and $C2^-$, V_{SS} and V_{OUT} , then connect the $C1^+$ and $C2^+$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 4.5V.



(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_S through the voltage adjust circuits for LCD driving. The output voltage of V_S is adjusted by changing the R_a and R_b within the range of $|V_S| < |V_{OUT}|$. The output voltage is calculated by the following formula.

$$V_{LCD} = V_{DD} - V_S = (1 + R_b/R_a) \cdot V_{REG} \dots\dots ①$$

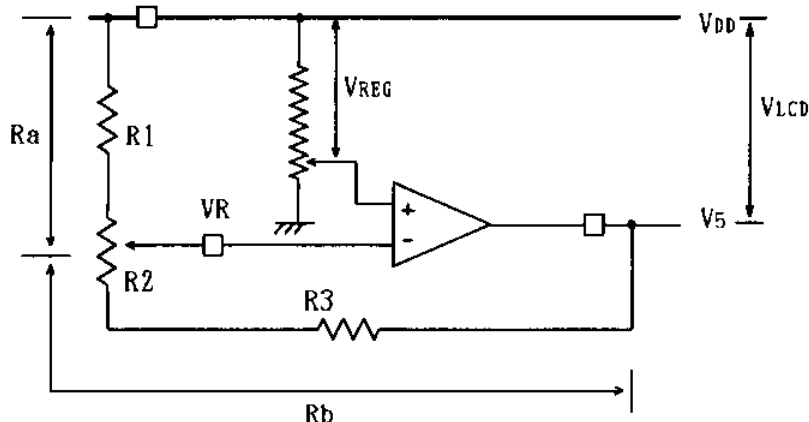


Fig. 3

The voltage of V_{REG} is a standard voltage produced from built-in bleeder resistance. And V_{REG} is possible to be fine-adjusted by EVR functions mentioned in (c).

For fine-adjustment of V_S , R_2 as variable resistor, R_1 and R_3 as fixed constant should be connected to V_{DD} terminal, VR and V_S as shown in Fig. 3.

[Design example for R_1 , R_2 and R_3 / Reference]

- $R_1 + R_2 + R_3 = 5M \Omega$ (Determined by the current flown between $V_{DD} - V_S$)
- Variable voltage range by the R_2 . $-3V \sim -4.5V$ ($V_{LCD} = V_{DD} - V_S \rightarrow 6.0V \sim 7.5V$)
 (Determined by the LCD electrical characteristics)
- $V_{REG} = 3V$ (In case of $EVR = (0F)_H$)
- R_1 , R_2 and R_3 are calculated by above conditions and the formula of ① to mentioned below;
 $R_1 = 2.0M \Omega$, $R_2 = 0.5M \Omega$, $R_3 = 2.5M \Omega$

* If the power supply voltage between V_{DD} and V_{SS} changes, V_5 changes too. Therefore the power supply voltage should be stabilized for V_5 stable operation.

(c) Contrast Adjustment by using the EVR function

The EVR controls voltage of V_{REG} by instruction and changes voltage of V_S .

As result, LCD display contrast is adjusted by V_S . The EVR selects a voltage of V_{REG} in the following 16 conditions by setting 4bits data in to the EVR register.

In case of EVR operation, T_1 terminal and T_2 require to set couples of value as (L,L),(L,H) and (H,L) excepting for (H,H) and the internal power supply must turn on by instruction.

EVR register		$V_{REG}[V]$	V_{LCD}
(00) _H	(0, 0, 0, 0)	(135/150)·($V_{DD}-V_{SS}$)	Low
(01) _H	(0, 0, 0, 1)	(136/150)·($V_{DD}-V_{SS}$)	
(02) _H	(0, 0, 1, 0)	(137/150)·($V_{DD}-V_{SS}$)	
⋮	⋮	⋮	
(0D) _H	(1, 1, 0, 1)	(148/150)·($V_{DD}-V_{SS}$)	High
(0E) _H	(1, 1, 1, 0)	(149/150)·($V_{DD}-V_{SS}$)	
(0F) _H	(1, 1, 1, 1)	(150/150)·($V_{DD}-V_{SS}$)	

● Adjustable range of the LCD driving voltage by EVR function using

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors R_a and R_b .

[Design example for the adjustable range / Reference]

- Condition $V_{DD} = 3.0V$, $V_{SS} = 0V$
 $R_a = 1M\Omega$, $R_b = 1M\Omega$ ($R_a : R_b = 1 : 1$)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting (00)_H in the EVR register,

$$\begin{aligned}
 V_{LCD} &= ((R_a + R_b) / R_a) \cdot V_{REG} \\
 &= (2/1) \cdot [(135/150) \cdot 3.0] \\
 &= 5.4V
 \end{aligned}$$

In case of setting (0F)_H in the EVR register,

$$\begin{aligned}
 V_{LCD} &= ((R_a + R_b) / R_a) \cdot V_{REG} \\
 &= (2/1) \cdot [(150/150) \cdot 3.0] \\
 &= 6.0V
 \end{aligned}$$

	Min. (00) _H	Max. (0F) _H
Adjustable Range	5.4	6.0 [V]
Step Voltage	40	[mV]

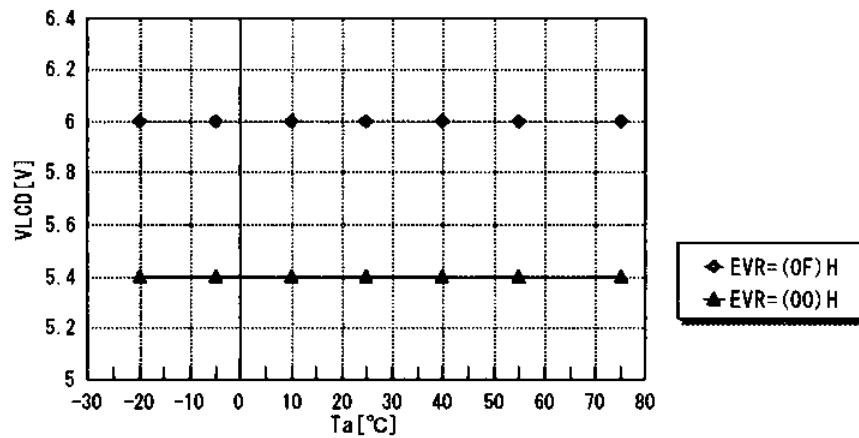
*) The V_{LCD} operating temperature. Please refer to the following graphs.

(condition) $V_{DD} = 3V$

$R_a = 1M\ \Omega$, $R_b = 1M\ \Omega$ ($R_a : R_b = 1 : 1$)

Voltage tripler

VLCD vs. Temperature (Typical performance)

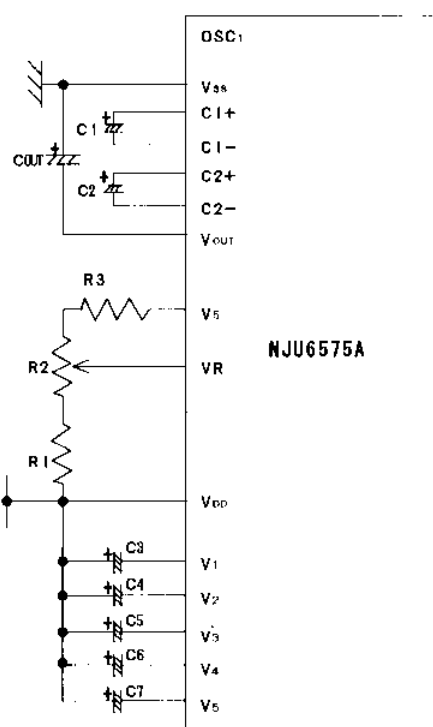


(d) LCD Driving Voltage Generation Circuits

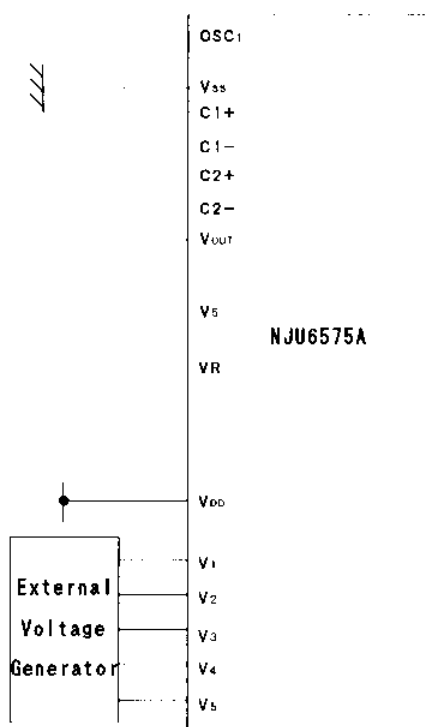
The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally by dividing the V_5 voltage with the internal bleeder resistance. And it is supplied to the LCD driving circuits after the impedance conversion with voltage follower circuit.

As shown in Fig. 4, Five capacitors are required to connect to each LCD driving voltage terminal for voltage stabilizing. And the value of capacitors C3, C4, C5, C6 and C7 determined depending on the actual LCD panel display evaluation.

Using the internal Power Supply



Using the external Power Supply



Reference set up value
VLCD = VDD-V5 \approx 6 ~ 7.5V

Item	Value
C _{OUT}	4.7 ~ 10 μ F
C1, C2	4.7 ~ 10 μ F
C3 to C7	0.1 ~ 0.47 μ F
R1	2.0M Ω
R2	0.5M Ω
R3	2.5M Ω

Fig. 4

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

*2 Following connection of VOUT is required when external power supply using.

When $V_{SS} > V_5$ -- $V_{OUT} = V_5$

When $V_{SS} \leq V_5$ -- $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6575A interfaces with MPU by 8-bit bi-directional data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined by a condition of the P/S terminal connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out operation is impossible.

Table 5

P/S	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	\overline{CS}	A0	\overline{RD}	\overline{WR}	C86	-	-	$D_0 \sim D_7$
L	Serial	\overline{CS}	A0	-	-	-	SI	SCL	OPEN

(5-2) Parallel Interface

The NJU6575A interfaces to 68 or 80 type MPU directly when the parallel interface (P/S="H") is selected. 68 type MPU or 80 is determined by the condition of C86 terminal connecting to "H" or "L" as shown in table 6.

Table 6

C86	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	$D_0 \sim D_7$
H	68 type MPU	\overline{CS}	A0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	\overline{CS}	A0	\overline{RD}	\overline{WR}	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6575A discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and (\overline{RD} , \overline{WR}) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	\overline{RD}	\overline{WR}	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminal \overline{CS} set to "L" and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition when chip is not selected. The data input from SI terminal is MSB first like as the order of D_7, D_6, \dots, D_0 , and the data are entered into the shift register synchronizing with the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction of the serial input data is executed by the condition of A0 at the 8th serial clock rise edge. A0="H" is display data and A0="L" is instruction. When RES terminal becomes "L" or \overline{CS} terminal becomes "H" before 8th serial clock rise edge, NJU6575A recognizes them as a instruction data incorrectly. Therefore a unit of serial data must be structured by 8-bits. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface.

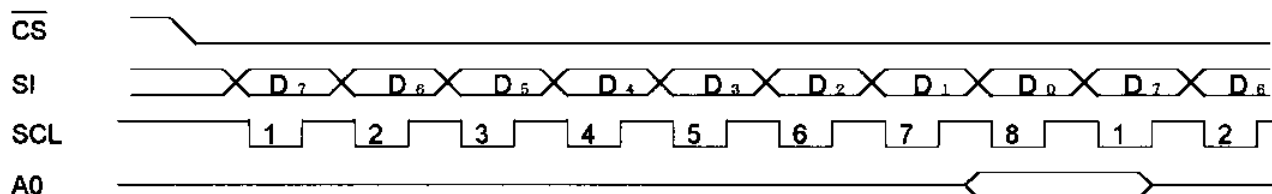


Fig. 5

(5-5) Access to the Display Data RAM and Internal Register.

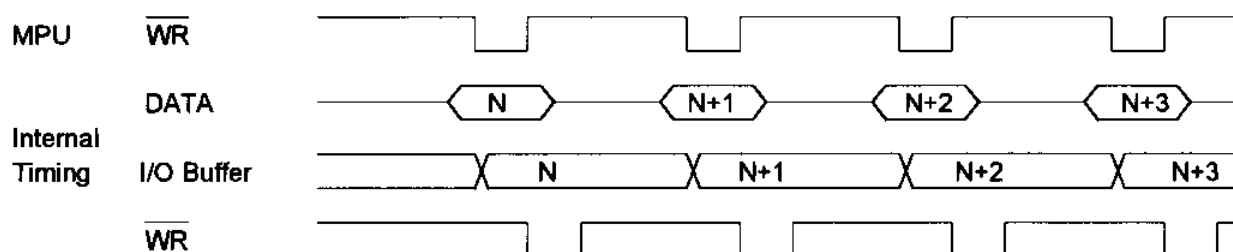
The NJU6575A is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register. For example, when the MPU reads out the data from the Display Data RAM, the read out data in the data read cycle(dummy read) is held in the bus-holder, then it is read out from the bus-holder to the system bus at the next data read cycle. When writes the data into the Display Data RAM, the data is held in the bus-holder, then it is written into the Display Data RAM by the next data write cycle.

Therefore high speed data transmission between MPU and NJU6575A is available because of it is not limited by the t_{ACC} and t_{DS} as display data RAM access time and limited by the system cycle time (R) or (W). If the cycle time is not be kept in the MPU operation, NOP should be inserted to the system instead of the waiting operation.

The read out operation does not read the data in the pointed address just after the address set operation, and second read out operation can read out the data correctly from the pointed address.

Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

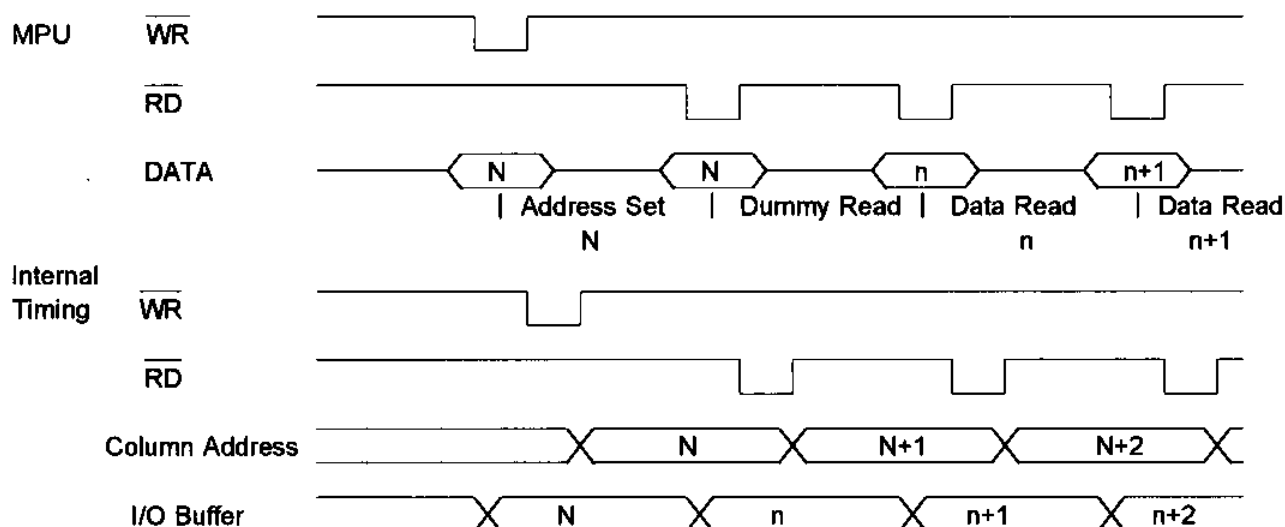


Fig.6

(5-6) Chip Select

\overline{CS} is Chip Select terminal. In case of \overline{CS} ="L", the interface with MPU is available. In case of \overline{CS} ="H", the D_0 to D_7 are high impedance and A_0 , \overline{RD} , \overline{WR} , \overline{SI} and \overline{SCL} inputs are ignored. If the serial interface is selected when \overline{CS} ="H", the shift register and counter are reset. However, the reset is always operated in any conditions of \overline{CS} .

ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V _{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 4.5 (used Tripler)	V
Supply Voltage (2)	V _S	V _{DD} -13.5 ~ V _{DD} +0.3	V
Supply Voltage (3)	V ₁ ~V ₄	V _S ~ V _{DD} +0.3	V
Input Voltage	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Operating Temperature	T _{opr}	- 30 ~ + 80	°C
Storage Temperature	T _{stg}	- 55 ~ + 125 (Chip) - 55 ~ + 100 (TCP)	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V_S ; V_{DD} > V_{SS} ≥ V_{OUT} must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

ELECTRICAL CHARACTERISTICS (1)

(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~+75°C)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage (1)	Recommend	V _{DD}			4.5	5.0	5.5	V	5
	Available				2.4		5.5		
Operating Voltage (2)	Recommend	V _S			V _{DD} -13.5		V _{DD} -3.5	V	
	Available				V _{DD} -13.5				
	Available	V ₁ , V ₂	V _{LCD} =V _{DD} -V _S	V _{DD} -0.6xV _{LCD}		V _{DD}			
	Available	V ₃ , V ₄		V _S	V _{DD} -0.4xV _{LCD}				
Input Voltage	1	V _{IHC1}	D0, D1... D7,	V _{DD} =2.7V	0.7xV _{DD}		V _{DD}	V	
		V _{IHC2}	A0, CS, RES,		0.8xV _{DD}		V _{DD}		
	2	V _{ILC1}	RD, WR, C86, S1, SCL, P/L Terminals	V _{DD} =2.7V	V _{SS}		0.3xV _{DD}		
		V _{ILC2}			V _{SS}		0.2xV _{DD}		
Output Voltage	1	V _{OHC11}	D0, D1... D7,	I _{OH} =-1mA I _{OH} =-0.5mA V _{DD} =2.7V	0.8xV _{DD}		V _{DD}	V	
		V _{OHC12}	Terminals		0.8xV _{DD}		V _{DD}		
	2	V _{OLC11}	D0, D1... D7,	I _{OL} =1mA I _{OL} =0.5mA V _{DD} =2.7V	V _{SS}		0.2xV _{DD}		
		V _{OLC12}	Terminals		V _{SS}		0.2xV _{DD}		
Input Leakage Current		I _{L1}	All input terminals		-1.0		1.0	uA	6
		I _{L0}	All I/O term. (D0... D7)		-3.0		3.0		
Driver On-resistance		R _{ON1}	Ta=25°C	V _{LCD} =13.5V		2.0	3.0	kΩ	7
		R _{ON2}		V _{LCD} =8.0V		3.0	4.5		
Stand-by Current		I _{DD0}	during Power save Mode			0.05	5.0	uA	8
Operating Current		I _{DD12}	Display			28	45	uA	
		I _{DD14}	V _{LCD} =8.0V	V _{DD} =2.7V		16	25		
		I _{DD21}	Accessing			350	500	uA	
		I _{DD22}	fcyc=200kHz	V _{DD} =2.7V		170	240		

ELECTRICAL CHARACTERISTICS (2)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Input Terminal Capacitance		C_{IN}	A0, CS, RES, RD, WR, C86, S1, SCL, P/S, T1, T2, D0...D7 $T_a=25^{\circ}\text{C}$		10		pF	
Oscillation Frequency		fosc	$T_a=25^{\circ}\text{C}$ $V_{DD}=5.0\text{V}$ $V_{DD}=2.7\text{V}$	9 8	11 9.75	13 11.5	kHz	
Voltage Tripler	Input Voltage	V_{DD1}	$V_{DD}-V_{SS}$	2.4		5.5	V	
		V_{DD2}	$V_{DD}-V_{SS}$, used Tripler	2.4		4.5	V	10
	Output Volt.	V_{OUT}	$V_{SS}-V_{LCD}$, used Tripler	-9.0			V	
	On-resistance	R_{TR1}	$V_{DD}=3\text{V}$; $C=4.7\mu\text{F}$ used Tripler		600	1000	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Tripler Circuit "OFF"	$V_{DD}-13.5$		$V_{DD}-5.0$	V	11
	Voltage Follower	V_S	Voltage Adjustment Circuit "OFF"	$V_{DD}-13.5$		$V_{DD}-5.0$	V	
	Operating Current	I_{OUT1}	$V_{DD}=4.5\text{V}$, $V_{LCD}=8\text{V}$ COM/SEG Terminals Open		58	120	μA	12
		I_{OUT2}	No Access		22	45		
		I_{OUT3}	Display Checkered pattern		21	43		
	Voltage Reg.	V_{REG}	$V_{DD}=3.0\text{V}$, $T_a=25^{\circ}\text{C}$			3	%	13

Note 5) NJU6575A can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of the D₀ to D₇ terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V₁, V₂, V₃, V₄) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,12) Apply to current after "LCD Driving Voltage Set".

Note 8) Apply to the external display clock operation in no access from the MPU and no use internal power supply circuits.

Note 9) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 10) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 11) LCD driving voltage V_S can be adjusted within the voltage follower operating range.

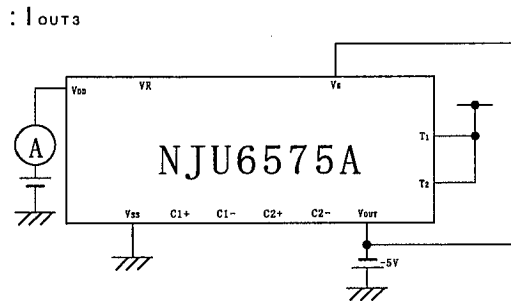
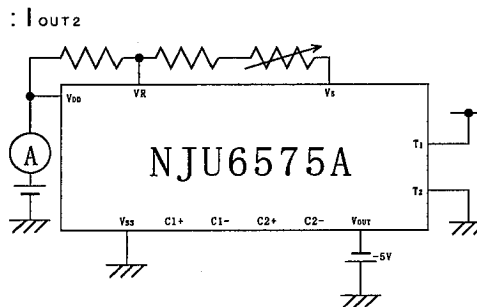
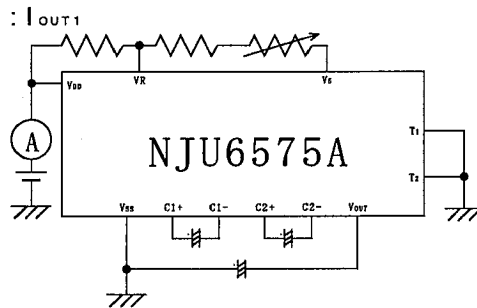
Note 12) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T ₁	T ₂	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I _{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I _{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use (V _{OUT})
I _{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use (V _{OUT} , V _S)

* = Don't Care

Note 13) Apply to the precision of the voltage between V_{DD} and V_S with EVR function.

MEASUREMENT BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS (3)

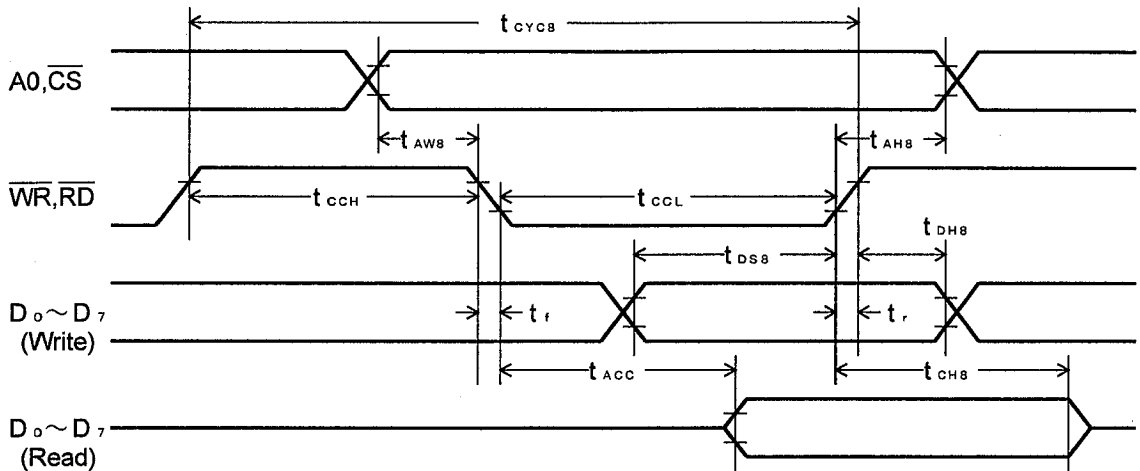
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	\overline{RES} Terminal	1.0			us	14
Reset "L" Level Pulse Width	t_{RW}	\overline{RES} Terminal	10			us	15

Note 14) Specified from the rising edge of \overline{RES} to finish the internal circuit reset.

Note 15) Specified minimum pulse width of RES signal. Over than t_{RW} "L" input should be required for correct reset operation.

BUS TIMING CHARACTERISTICS

• Read/Write operation sequence (80 Type MPU)



($V_{DD}=5.0V \pm 10\%$, $T_a=-20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		AO, \overline{CS}	t_{AH8}	10		ns
Address Set Up Time		Terminals	t_{AW8}	10		
System Cycle Time			t_{CYCS}	180		
Control Pulse Width	\overline{WR} , "L"	\overline{WR} , \overline{RD} Terminals	$t_{CCL}(W)$	25		
	\overline{RD} , "L"		$t_{CCL}(R)$	80		
	"H"		t_{CCH}	70		
Data Set Up Time		$D_0 \sim D_7$ Terminals	t_{DS8}	60		
Data Hold Time			t_{DH8}	10		
RD Access Time			t_{ACC8}		70	
Output Disable Time			t_{OH8}	0	30	
					CL=100pF	
Rise Time, Fall Time		\overline{CS} , \overline{WR} , \overline{RD} , AO, $D_0 \sim D_7$ Terminals	t_r, t_f		15	

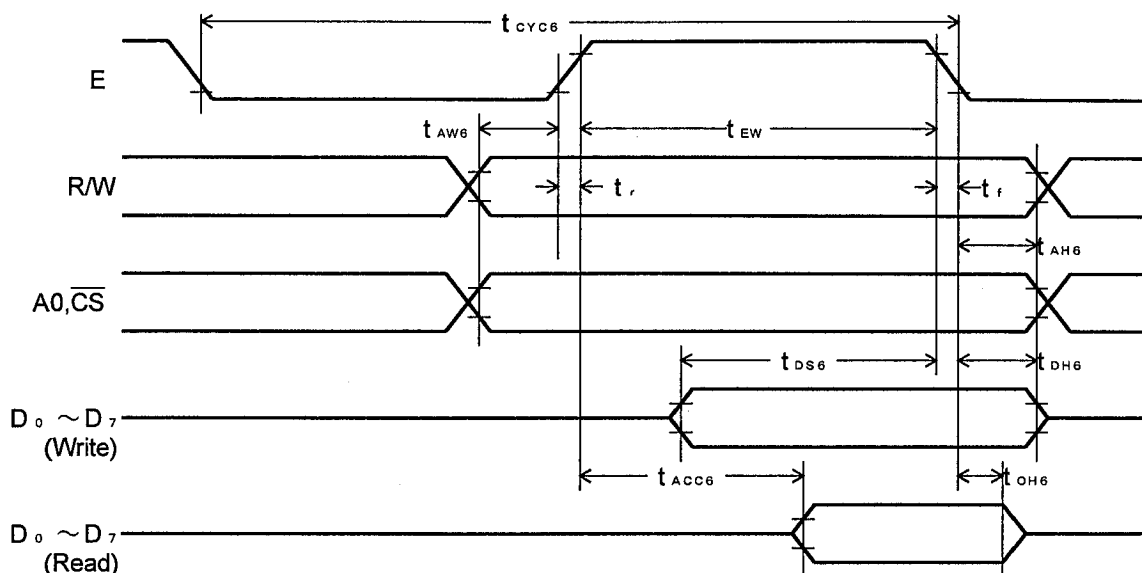
($V_{DD}=2.7V \sim 4.5V$, $T_a=-20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, \overline{CS}	t_{AH8}	25		ns
Address Set Up Time		Terminals	t_{AW8}	25		
System Cycle Time			t_{CYCS}	450		
Control Pulse Width	\overline{WR} , "L"	WR, \overline{RD} Terminals	$t_{CCL}(W)$	50		
	\overline{RD} , "L"		$t_{CCL}(R)$	200		
	"H"		t_{CCH}	220		
Data Set Up Time		$D_0 \sim D_7$ Terminals	t_{DS8}	120		
Data Hold Time			t_{DH8}	35		
RD Access Time			t_{ACC8}		140	
Output Disable Time			t_{OH8}	0	35	
Rise Time, Fall Time		\overline{CS} , \overline{WR} , \overline{RD} , A0, $D_0 \sim D_7$ Terminals	t_r, t_f		15	

Note 16) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 17) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

• Read/Write operation sequence (68 Type MPU)


 $(V_{DD}=5.0V\pm10\%, T_a=-20\sim75^{\circ}C)$

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, \overline{CS} , R/W Terminals	t_{AH6}	10			ns
Address Set Up Time		t_{AW6}	10			
System Cycle Time		t_{CYC6}	180			
Enable	E Terminal	t_{EW}	100			
Pulse Width			25			
Data Set Up Time	D ₀ ~D ₇ Terminals	t_{DS6}	60			
Data Hold Time		t_{DH6}	20			
Access Time		t_{ACC6}		70		
Output Disable Time	A0, \overline{CS} , R/W, E, D ₀ ~D ₇ Terminals	t_{OH6}	0	25		
Rise Time, Fall Time		t_r, t_f		15		

 $(V_{DD}=2.7V\sim4.5V, T_a=-20\sim75^{\circ}C)$

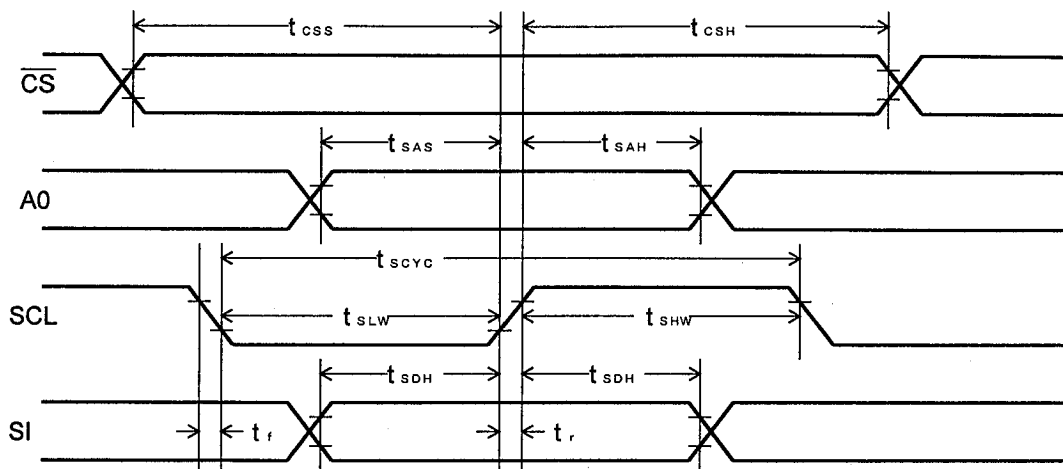
PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, \overline{CS} , R/W Terminals	t_{AH6}	25			ns
Address Set Up Time		t_{AW6}	25			
System Cycle Time		t_{CYC6}	450			
Enable	E Terminal	t_{EW}	200			
Pulse Width			50			
Data Set Up Time	D ₀ ~D ₇ Terminals	t_{DS6}	120			
Data Hold Time		t_{DH6}	40			
Access Time		t_{ACC6}		140		
Output Disable Time	A0, \overline{CS} , R/W, E, D ₀ ~D ₇ Terminals	t_{OH6}	0	45		
Rise Time, Fall Time		t_r, t_f		15		

Note 18) t_{CYC6} indicates the E signal cycle during the \overline{CS} activation period. The System Cycle Time must be required after \overline{CS} becomes active.

Note 19) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 20) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

• Write operation sequence (Serial Interface)



($V_{DD}=5.0V \pm 10\%$, $T_a=-20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	500			ns
SCL "H" pulse width		t_{SHW}	150			
SCL "L" pulse width		t_{SLW}	150			
Address Set Up Time	AO Terminal	t_{SAS}	120			
Address Hold Time		t_{SAH}	200			
Data Set Up Time	SI Terminal	t_{SDS}	120			
Data hold Time		t_{SDH}	50			
\overline{CS} -SCL Time	\overline{CS} Terminal	t_{CSS}	30			
		t_{CSH}	400			
Rise Time, Fall Time	SCL, AO, \overline{CS} , SI Terminals	t_r, t_f		15		

($V_{DD}=2.7V \sim 4.5V$, $T_a=-20 \sim 75^\circ C$)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	1000			ns
SCL "H" pulse width		t_{SHW}	300			
SCL "L" pulse width		t_{SLW}	300			
Address Set Up Time	AO Terminal	t_{SAS}	250			
Address Hold Time		t_{SAH}	400			
Data Set Up Time	SI Terminal	t_{SDS}	250			
Data hold Time		t_{SDH}	100			
\overline{CS} -SCL Time	\overline{CS} Terminal	t_{CSS}	60			
		t_{CSH}	800			
Rise Time, Fall Time	SCL, AO, \overline{CS} , SI Terminals	t_r, t_f		15		

Note 21) Rise time(t_r) and fall time(t_f) of input signal should be less than 15ns.

Note 22) Each timing is specified based on $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$.

LCD DRIVING WAVEFORM

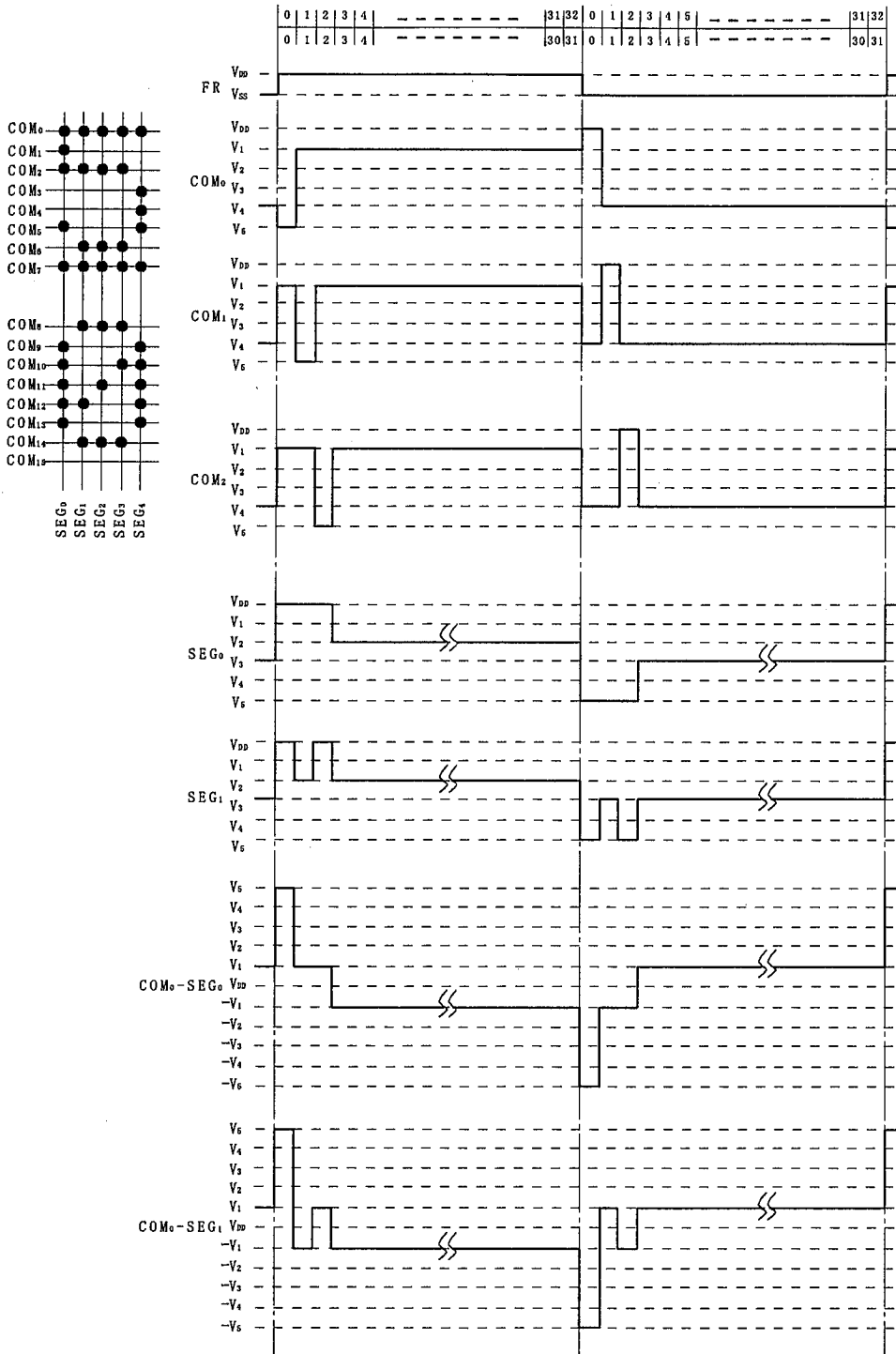


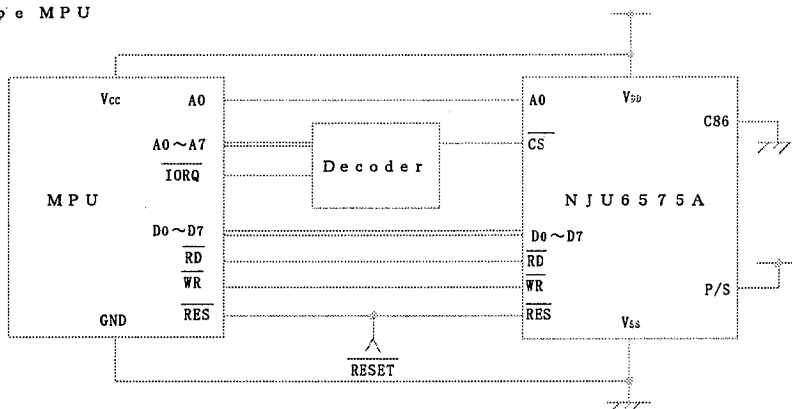
Fig. 7

■ APPLICATION CIRCUIT

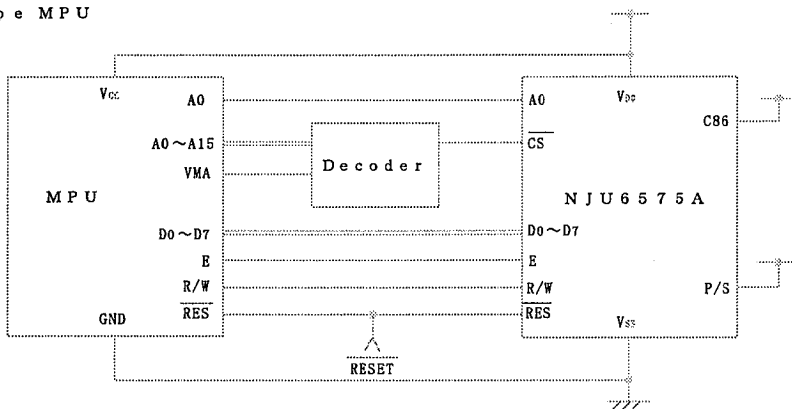
Microprocessor Interface Example

The NJU6575A interfaces to 80 type or 68 type MPU directly.
And the serial interface also communicate with MPU.

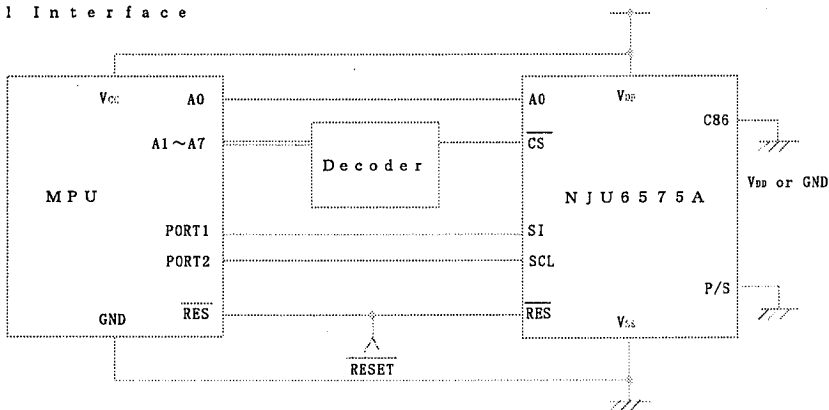
● 80 Type MPU



● 68 Type MPU



● Serial Interface



MEMO

[CAUTION]

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